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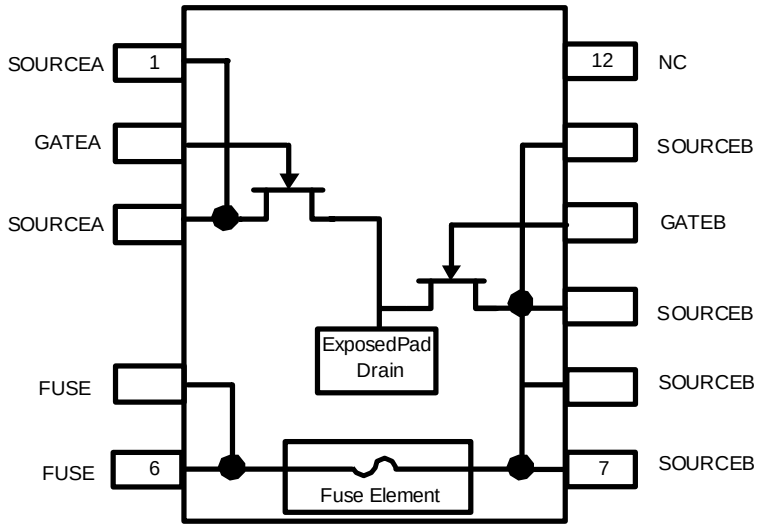
DEI1604
SURGE BLOCKING MODULE (SBM)

1. FEATURES

- Bidirectional surge protection
- Protection for Airbus A350 XWB Aircraft Lightning Induced Transients (Also as part of DO160E, Sect 22E)
  - o Waveform 5A: Pin Injection, 1500V/15A, 500V/500A, 300V/300A, 200V/200A and 100V/100A
  - o Waveform 3: Pin Injection, 100V/4A, 250V/10A, 600V/24A, 1500V/60A 1MHZ
  - o Waveform 2: Pin Injection, 100V/4A, 250V/10A, 750V/50A and 1600V/107A
- Low overall resistance: 1.7Ω
- Operating currents: ±0.45A
- Limits surge current
- 115VAC Fuse for fail safe protection
- Package: 12L DFN 6x7.7

2. PIN ASSIGNMENTS



Note: The exposed pad is electrically connected to the internal node shown.
It should be soldered to an electrically isolated PCB land to provide thermal heat sinking.

Figure 1 12L DFN Pinout

3. GENERAL DESCRIPTION

3.1. OVERVIEW

The DEI1604 Surge Blocking Module (SBM) is a high voltage, bidirectional current limiting element implemented with normally ON N-Channel Silicon Carbide JFET technology. The device is intended to be used in conjunction with a Transient Voltage Suppressor (TVS) diode to implement a current limiting / voltage clamping protection network.

In normal operation, the SBM acts as a low value series resistor (< 1.7Ω including JFETs and integrated fuse) and is designed to operate at currents up to ±0.45A. In surge stress operation, the TVS device conducts surge current when the surge voltage exceeds the TVS standoff voltage. The series SBM limits the surge current to few Amps, thus allowing use of small, low power, low capacitance TVS diodes to provide the voltage clamp protection.

A fuse element is provided to implement a "Fail Safe" interface. The integrated fuse is designed to fail OPEN when the surge current exceeds time duration much greater than a normal lightning induced transient, such as a short to 115VAC aircraft power bus. Figure 2 shows the integrated fuse connections. Fuse is connected to External IO Pin. Since the bi-directional capability of the SBM, fuses can also be connected to TVS.

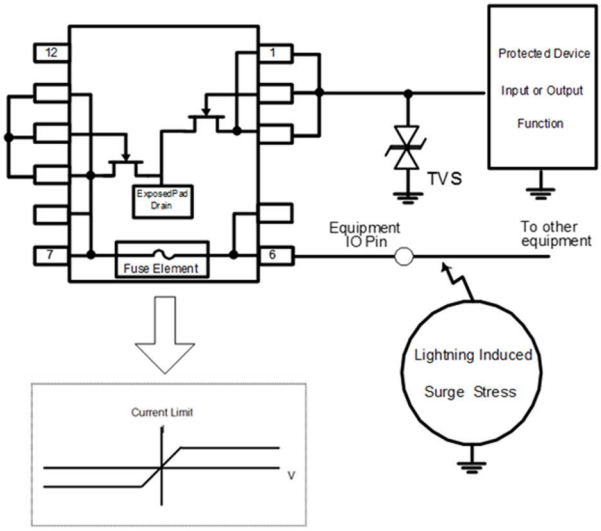


Figure 2 Application Circuit with Integrated Fuse

3.2. CURRENT LIMITING

The JFET current limiting function is illustrated for several surge and fault scenarios. These waveforms result with the indicated stress voltage waveform is applied directly across the JFET limiter.

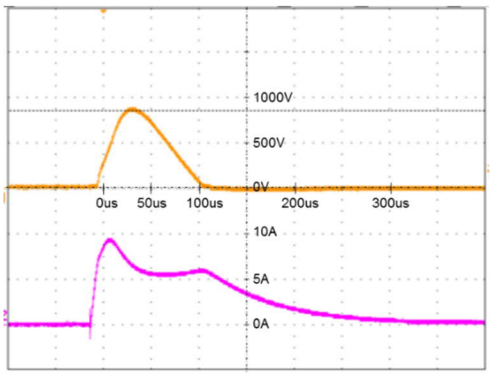


Figure 3 SBM Limit Current – DO160 WF5A 1500V/15A

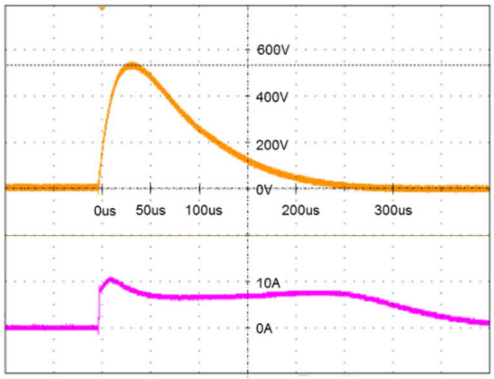


Figure 4 SBM Limit Current – DO160 WF5A 500V/500A

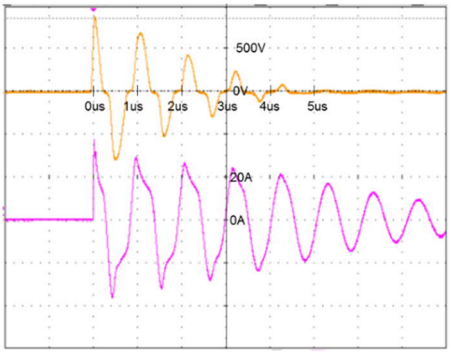


Figure 5 SBM Limit Current - DO160 WF3 1MHz 1500V/60

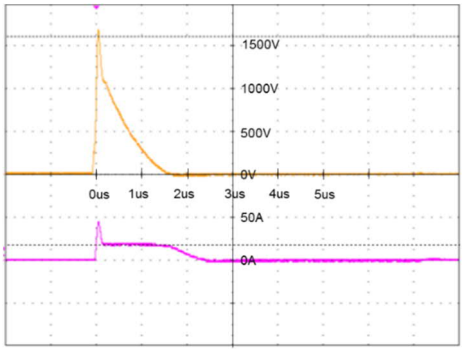


Figure 6 SBM Limit Current - DO160 WF2 1600V/107A

3.3. INTEGRATED 115VAC FUSE

Figure 7 shows the joule integral relationship between the integrated fuse and surge currents. The y-axis unit is ms*amp^2, and therefore proportional to the resistive heating of the fuse element. The "DEI1604 Fuse" curve denotes the i^{2}t & time that will cause the fuse element to arc (open). The "Fuse Trigger" window demonstrate the variation of current-time integral that will cause the fuse element to arc (open) due to 350Hz 115VAC short. The "Transient WFM Envelope" denotes the JFET limited current that will flow during WF5A lightning transients. The "115VAC Fuse Envelope" denotes the JFET limited current that will flow during inadvertent application of 115VAC. When the 115VAC envelope rises above the DEI1604 fuse curve, the fuse element is activated to arc (open). There are wide margin exist between the energy generated by the transient lightning wavform and DEI1604 Fuse trigger energy.

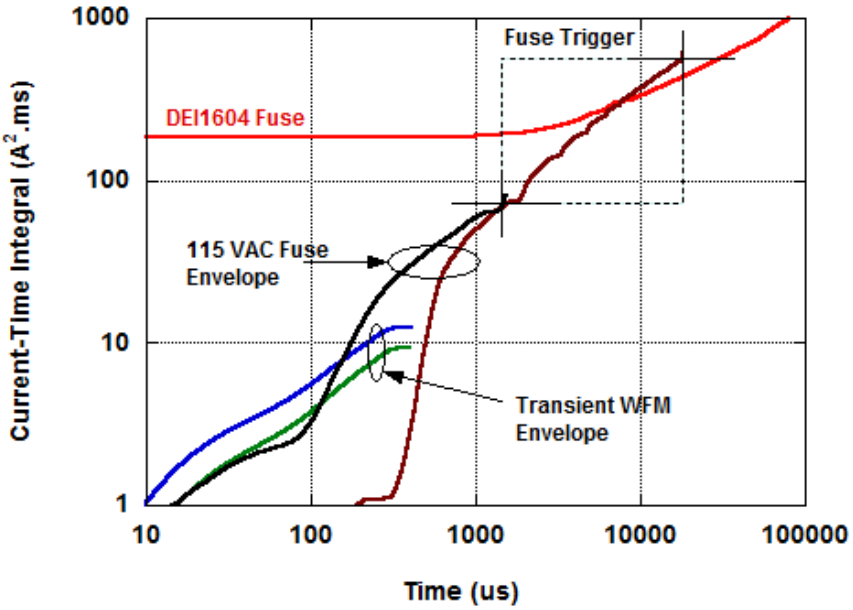


Figure 7 Joule Integral of Integrated 115VAC Fuse Relative to Surge Currents

4. ELECTRICAL CHARACTERISTICS

4.1. ABSOLUTE MAXIMUM RATINGS

Table 1 Absolute Maximum Ratings

PARAMETER	SYMBOL	MIN	MAX	UNITS
Storage Temperature	$T_{STORE-MAX}$	-55	+150	°C
Junction Temperature, Continuous Operation	T_{OP-MAX}	-55	+125	°C
V(GATEA)–V(SOURCEA), V(GATEB) – V(SOURCEB)	V_{MAX}	-20	+3	V
V(SOURCEA) –V(SOURCEB) Surge Voltage WF5A (with 100Ω Rs) WF5A (with 1Ω Rs) WF3 (1 MHz) WF2	V_{MAX}	 -1500 -500 -1600 -1500	 +1500 +500 +1600 +1500	V

4.2. RECOMMENDED OPERATING CONDITIONS

Table 2 Recommended Operating Conditions

PARAMETER	SYMBOL	MIN	MAX	UNITS
Ambient Operating Temperature - MIS	T_{OP}	-40	+85	°C
Operating Voltage, V(SOURCEA) – V(SOURCEB)	V_{DIF}	-0.77	+0.77	V
Gate Voltage, V(GATEA) – V(SOURCEA), V(GATEB) – V(SOURCEB)	V_{GS}	0	0	V
Operating Current	I_{OP}	-0.45	+0.45	A

4.3. DC CHARACTERISTICS

Table 3 DC Characteristics

Conditions: T_A = -40 to +85 ºC						
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
SBM CHARACTERISTICS						
Series Resistance SOURCEA to SOURCEB SOURCEB to SOURCEA	R_{ON}	I_{SS} = -0.45A to +0.45A (1) $V_{GSA} = V_{GSB}$ = 0V T_A = -40°C (MIS) T_A = 25°C T_A = 85°C	 - - -	 - - -	 1.7 1.4 1.7	Ω
Saturation current SOURCEA to SOURCEB SOURCEB to SOURCEA	I_{ON}	Pulsed V_{GS} = 0V Vds = 20V T_A = 25°C	 ±6.0	 -	 ±8.5	A
Blocking Voltage DRAIN to SOURCEA DRAIN to SOURCEB	BV_{DS}	I_{Ds} = 600µA, 8ms pulse V_{GS} = -20V T_A = 25°C	1700	-	-	V
FUSE CHARACTERISTICS						
Fuse Resistance, SOURCEB to FUSE	R_{FUSE}	I_{FUSE} = 0.45A applied to Fuse and measure V_{FUSE}	-	50	-	mΩ
Rated Current	I_rated	Max Rated Current, Continuous Operation	-	1.2	-	A
Rated Voltage	V_rated	Max Rate RMS Voltage, Continuous Operation	-	-	115	V
Notes: (1) Ron = V_{SS} / I_{SS} = Voltage/Current from SOURCEA to SOURCEB or SOURCEB to SOURCEA.						

5. CHARACTERIZATION DATA

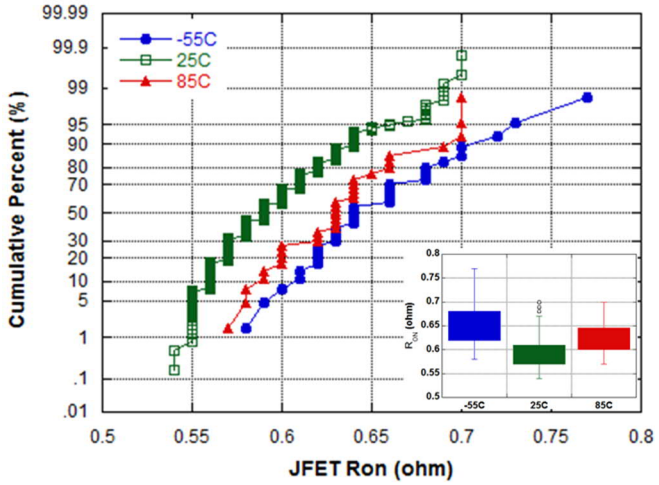


Figure 8 The statistical distribution of JFET $R_{DS,ON}$ at three different temperatures (Enclosed is box-chart)

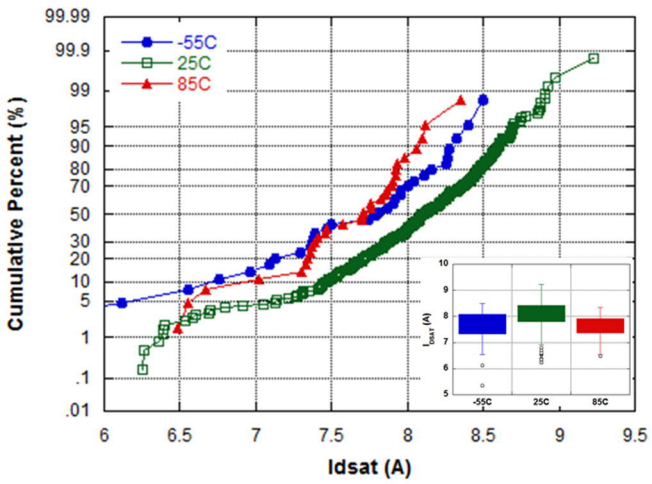


Figure 9 The statistical distribution of JFET I_{DSAT} at three different temperatures (Enclosed is box-chart)

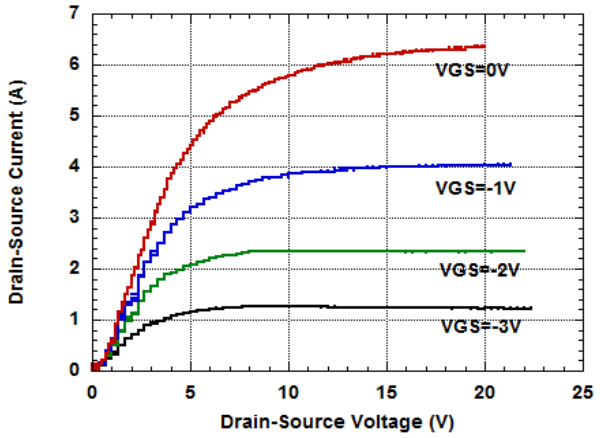


Figure 10 JFET IDSAT vs VDS Over VGS at 25°C

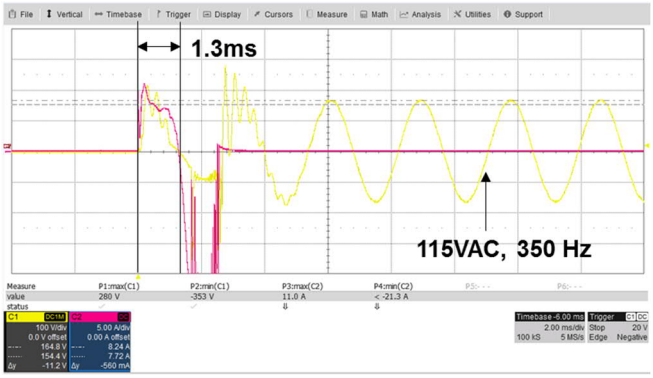


Figure 11 115V 350Hz AC applied to activate the fuse integrated in DEI1604. It was arced to open at 1.3ms

6. APPLICATION INFORMATION

6.1. TVS SELECTION

The selection of TVS type based on the TVS clamping voltage is shown in Figure . The most challenging waveform with respect to TVS thermal stress is WF5A as it has the longest pulse width (tw). The technique to select a TVS is to convert the power waveform of the lightning transient that the TVS will see to the equivalent 10x1000us of the TVS specification. The power waveform of TVS with the SBM current limiter was modeled as a square wave for WF5A transient and the current limit was determined at breaking point of the trailing edge of SBM current waveform as shown in Figure 13. The Figure 12 displays the Transient Voltage Suppressor (TVS) diodes rated 400W (SMA) with 48V clamp voltage is adequate for DEI1604 at room temperature. When the TVS clamping voltage requires higher than 48V, the TVS type needs to switch from SMA to SMB (600W), and even to SMC (1500W) for the 77.4V clamping voltage case. It is appropriate to select a TVS with a power rating that can withstand the current limited surge to minimize the possibility of a TVS failure during lightning transient.

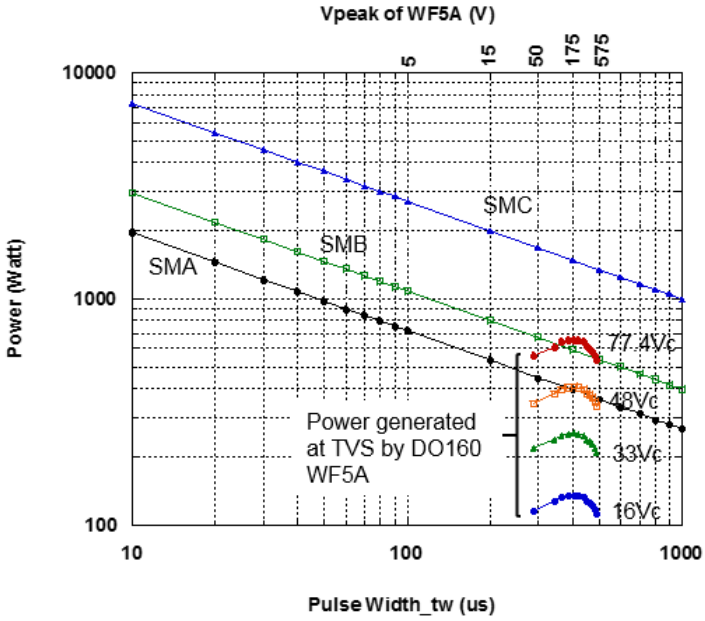


Figure 12 TVS selection based on the WF5A Vpeak and TVS clamping voltage (Temperature= 25 ºC). The peak power of TVS was rated based on the 10/1000 us waveform and the K factor 1.5 was used for the square wave shape.

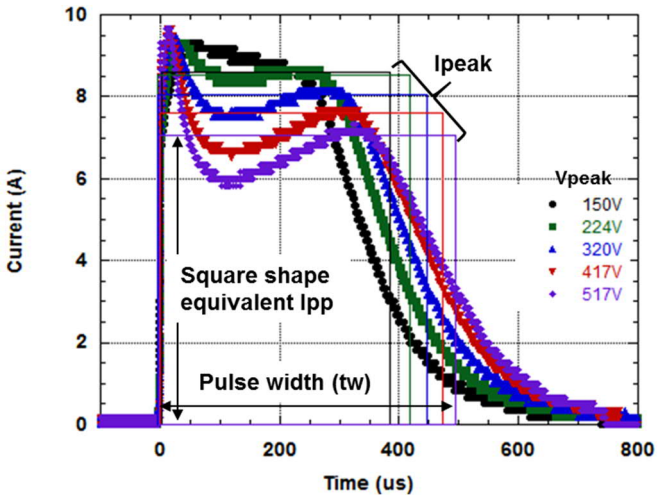


Figure 13 The Ipeak and pulse width (tw) of each waveform was extracted from the current and time integration. Once the Ipeak of square waveform is determined at the breaking point of trailing edge, the tw can be extracted from the integrated I*t dividing by Ipeak

6.2. PCB DESIGN RECOMMENDATIONS

The 12DFN package incorporates a bottom thermal contact (BTC) and two smaller dummy contacts. The dummy contacts exist to balance the solder density to center the part during soldering. The thermal contact exists to conduct heat from the JFET to a heat spreader land on the PCB. The BTC is electrically connected to the JFET drains; thus the PCB heat spreader land must be electrically isolated. This node is not fully protected and must maintain surge voltage design rules. It should also minimize capacitive coupling to internal ground and power planes to minimize BCI resonance.

To maximize the heat spreader performance, it is recommended the PCB design include thermal vias to heat spreader lands on the back side of the PCB and internal planes if possible. Vias should be plugged or tented to prevent solder wicking.

However, the thermal optimization does not affect lightning surge performance since the transient is too fast, but is important to limit Tj in applications with IR heating from high operating current.

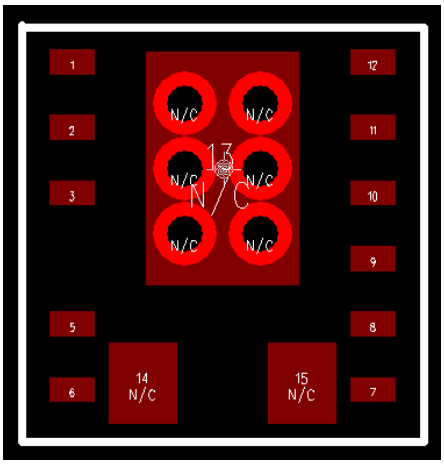


Figure 14 Example PCB footprint with thermal vias

7. ORDERING INFORMATION

Table 4 Ordering Information

Part Number	Marking	Package	Temperature
DEI1604-MIS-G	DEI1604-MIS	12DFN6x7.7	-40 ºC to +85 ºC

8. PACKAGE DESCRIPTION

Table 5 Package Characteristics

PACKAGE TYPE	PACKAGE REF	THERMAL RESIST. (ºC/W)	JEDEC MOISTURE SENSITIVITY LEVEL & PEAK BODY TEMP	LEAD FINISH / JEDEC Pb-Free DESIGNATION	Pb Free Type
12L DFN 6x7.7	12DFN 6x7.7	θJC ~3 θJA ~ 40 /[1]	MSL 3 260ºC	NiPdAu e3	RoHS

Notes:

1. Double sided PCB thermal land with thermal vias. (To be characterized)

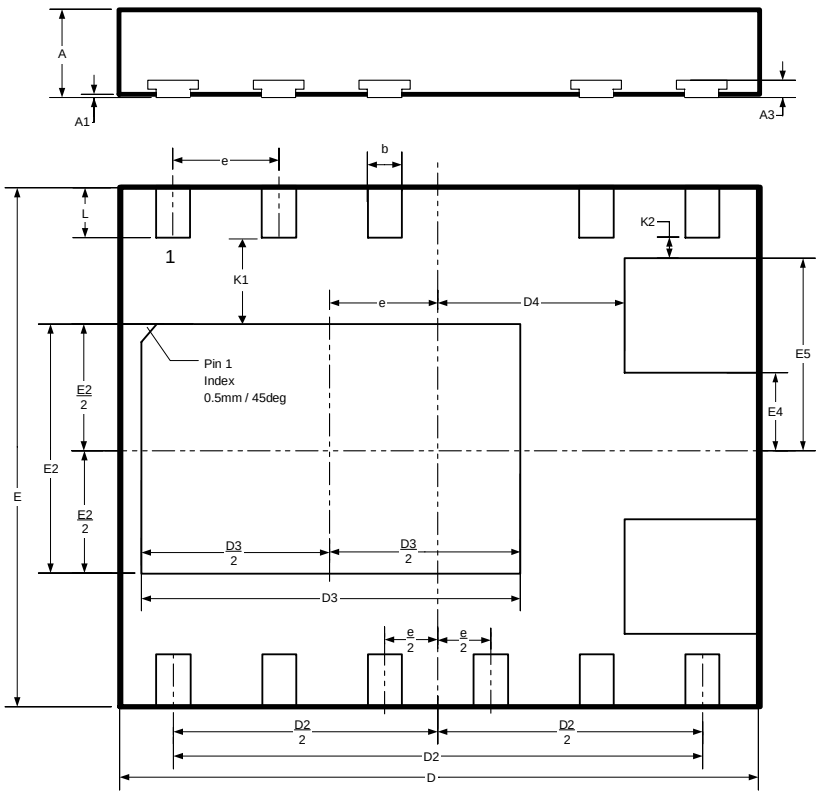


Figure 15 12DFN 6x7.7 Mechanical Outline

SYMBOL	MIN	NOM	MAX	NOTES
A	1.30	1.40	1.50	
A1	0.00	0.02	0.05	
A3		0.20		Ref
b	0.33	0.42	0.51	
D		7.69		BSC
D2		6.35		BSC
D3		4.55		BSC
D4	2.20	2.25	2.30	
E		6.15		BSC
e		1.270		BSC
E2	2.90	2.95	3.00	
E4	0.82	0.87	0.92	
E5	2.18	2.23	2.28	
K1	0.95	1.00	1.05	
K2	0.20	0.25	0.30	
L	0.51	0.61	0.71	
Dimensions in mm				