SB-3642 SYNCHRO/RESOLVER-TO-DIGITAL PMC INTERFACE CARD HARDWARE MANUAL

MN-3642XX-001

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Revision	Date	Pages	Description
Pre A	12/2016	All	Preliminary Release
Pre B	2/2017	All	Updated Preliminary Release
Pre C	4/2017	All	Updated Preliminary Release
Pre D	6/2017	All	Updated Preliminary Release
Rev A	10/2017	All	Initial Release
Rev B	2/2018	22 – 24	Updated software support information
Rev C	2/2019	All	Added additional ordering options, aligned channel enumeration to match software
Rev D	4/2019	9-12	Spec table description updated

1 PREFACE

This manual uses typographical conventions to assist the reader in understanding the content. This section will define the text formatting used in the rest of the manual.

1.1 Text Usage

- **BOLD** – indicates important information and table, figure, and chapter references.
- `Courier New –` indicates code examples.
- <…> - indicates user - entered text or commands.

1.2 Standard Definitions

PCI Peripheral Component Interconnect
PMC PCI Mezzanine Card

1.3 Special Handling and Cautions

The ***SB-3642*** series uses state-of-the-art components, and proper care should be used to ensure that the device will not be damaged by Electrical Static Discharge (ESD), physical shock, or improper power surges and that precautions are taken to avoid electrocution.

Warnings: Turn off power to the computer hardware and unplug from wall.

NEVER insert or remove card with power turned on.

Ensure that standard ESD precautions are followed. As a minimum, one hand should be grounded to the power supply in order to equalize the static potential.

Do not store disks in environments exposed to excessive heat, magnetic fields or radiation.

1.4 Trademarks

All trademarks are the property of their respective owners.

1.5 What is included in this manual?

This manual contains a complete description of hardware installation and use.

1.6 Technical Support

In the event that problems arise beyond the scope of this manual, you can contact DDC by the following:

US Toll Free Technical Support:
1-800-DDC-5757, ext. 7771

Outside of the US Technical Support:
1-631-567-5600, ext. 7771

Fax:
1-631-567-5758 to the attention of Motion Feedback Technologies Applications

DDC Website:
www.ddc-web.com/ContactUs/TechSupport.aspx

Please note that the latest revisions of Software and Documentation are available for download at DDC's Web Site, www.ddc-web.com.

2 OVERVIEW

The SB-3642 is a Front-I/O PCI Mezzanine Card (PMC) with up to eight channels of Synchro or Resolver conversion. The SB-3642 utilizes a PCI interface (*Revision 3.0 Compliant 32-bit, 33/66 MHz*). It is available in the industrial and commercial operating temperature ranges.

The conversion in each channel utilizes DDC's RD-19230 converter, which has a long history of proven performance. For complete converter specifications, the RD-19230 Datasheet can be downloaded from the DDC website.

2.1 Features

Resolver Conversion

- Four or Eight Independent Resolver-to-Digital Channels
  - 2V, 11.8Vrms, and 90Vrms Synchro and Resolver Ordering Options
- Utilizes High Accuracy RD-19230 Converters
- Software Programmable Resolution (10,12,14, or 16 bits)
- Software Programmable Bandwidth (Low or High Bandwidth)
- Self-Test, Built-in-Test, and Velocity Outputs
- Incremental Encoder Emulation (A quad B outputs) with Independent Resolution Control (4-channel ordering option only)
- Configurable Two-Speed Conversion
- Synthesized Reference and Independent Reference Inputs for Each Channel

General

- VITA-47 Shock and Vibration Tested
- RoHS Compliant (Lead-free and hazardous substance-free)
- -40º to +85ºC Temperature Range
- 32-bit/66 MHz PCI Rev. 3.0 Compliant Interface
- Operates in 3.3V or 5V PCI Signaling Environments
- Front Panel I/O (68-Pin) Air-Cooled Design
- Only 5V & 3.3V Supply Required (+/- 12V not needed)
- Four Opto-Isolated Discrete Input and Four Discrete Outputs for External Control Functions (4-channel ordering option only)

The card includes **SB-36030Sx Motion Feedback Library** along with code samples and detailed documentation. To install the latest official software from DDC, download via DDC's website at www.ddc-web.com/.

2.2 System Requirements

- PCI-PMC connector supporting 3.3 or 5V PCI signaling
- PCI-PMC connector with +5V and +3.3V supply voltage available
- A supported operating system

2.3 Configuration Options

Table 1. Input Signal Options

Ordering Option (x)	SB-3642x	
	Signal Input	Bandwidth
0	2V Single-Ended	80 Hz / 300 Hz
1	11.8Vrms Synchro	80 Hz / 300 Hz
2	11.8 Vrms Resolver	80 Hz / 300 Hz
3	90Vrms Synchro	80 Hz / 300 Hz
4	90Vrms Synchro	15 Hz / 45 Hz

2.4 Applications

The SB-3642 PMC card's rugged construction and ability to operate over the industrial temperature range makes it ideal for use in mission computers and other embedded systems. This device can be combined with carrier cards for use in VME or cPCI control systems employing 33/66MHz bus. The card also provides an ideal solution for encoder-based systems that will mate with Resolver inputs. The card is a valuable addition to design and test teams involved with resolver simulation and positioning.

Resolvers are used in applications that include modern high performance industrial and military position feedback and control systems. Typical motion feedback applications include motor control, machine tool control, antenna control, robotics, and process control systems.

2.5 Mechanical Design

The SB-3642 is a Front-I/O air-cooled PCI Mezzanine Card (PMC) designed to meet or exceed vibration requirements specified in VITA-47 for a class V2 in air-cooled applications. The SB-3642 card also features CCPMC (Conduction Cooled PMC) thermal rails and connector “anti-fretting” mounting holes per VITA-20-2005.

The front panel I/O connector layout uses a 68-pin front panel connection. The board has conduction rails that do not interfere with the front panel connector. The front panel connector includes a metal backshell with fastening thumbscrews.

The SB-3642 is designed to meet or exceed the humidity requirements of ANSI/VITA 47, and has been tested to withstand 95% humidity.

To operate within the specified -40 to +85°C operating temperature, supplemental air cooling of 300 LFM (Linear Feet per Minute) in the system is required. The SB-3642 utilizes a custom heat sink design using the conduction cooled rails to efficiently operate within the temperature range.

MTBF (Mean Time Between Failure) report is available upon factory request.

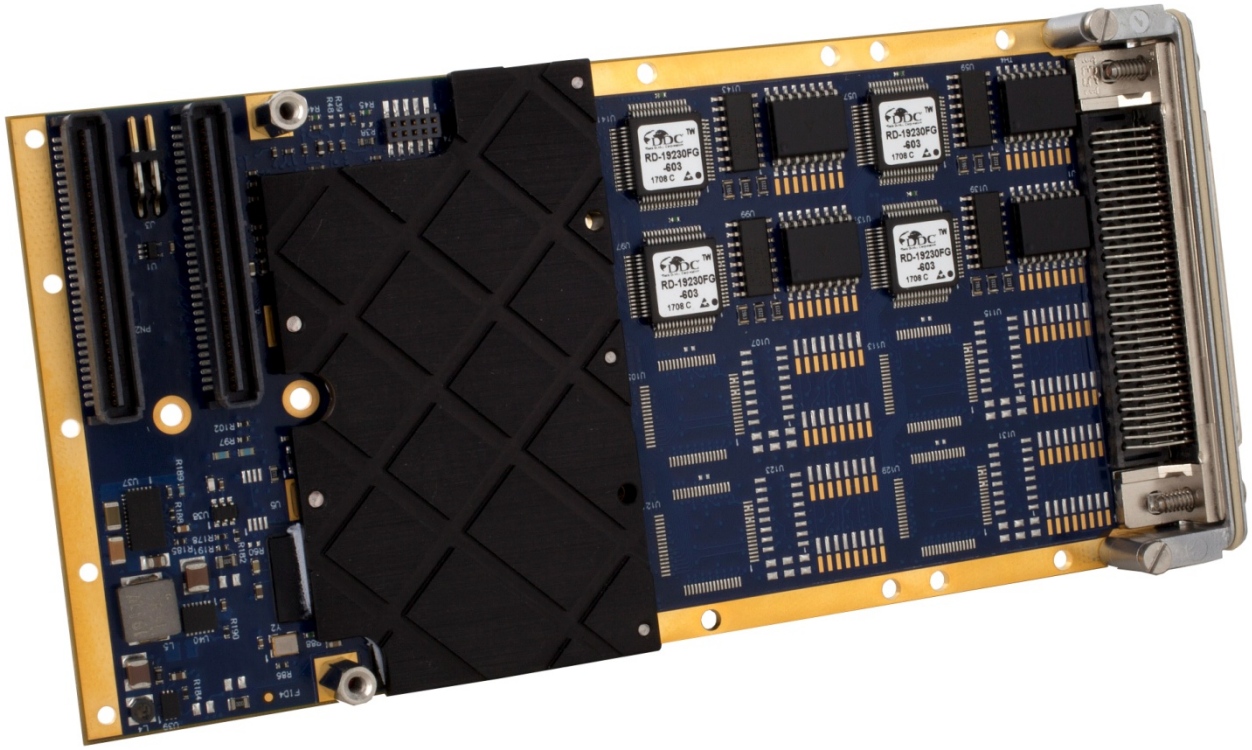

Figure 1. SB-3642 Resolver-to-Digital PMC Card (4-channel card shown)

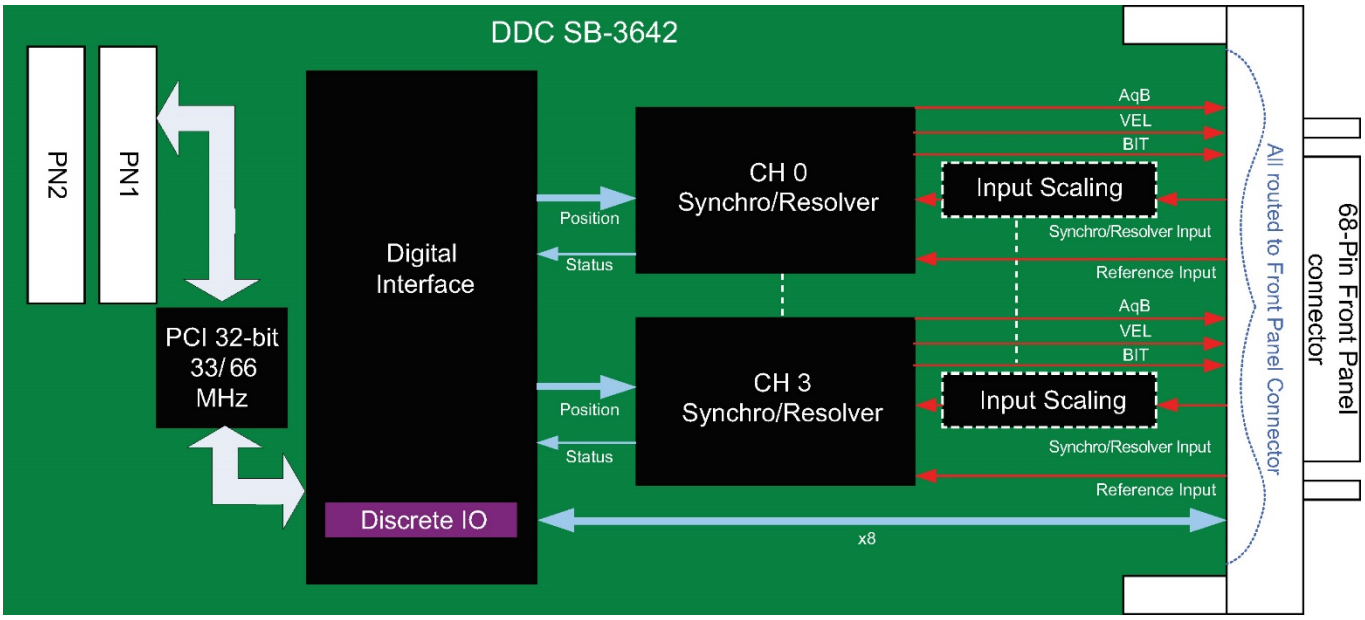

Figure 2. SB-3642 Architecture (8-channel card removes AqB, BIT, and Discrete IO from front panel connector to accommodate additional 4 channels)

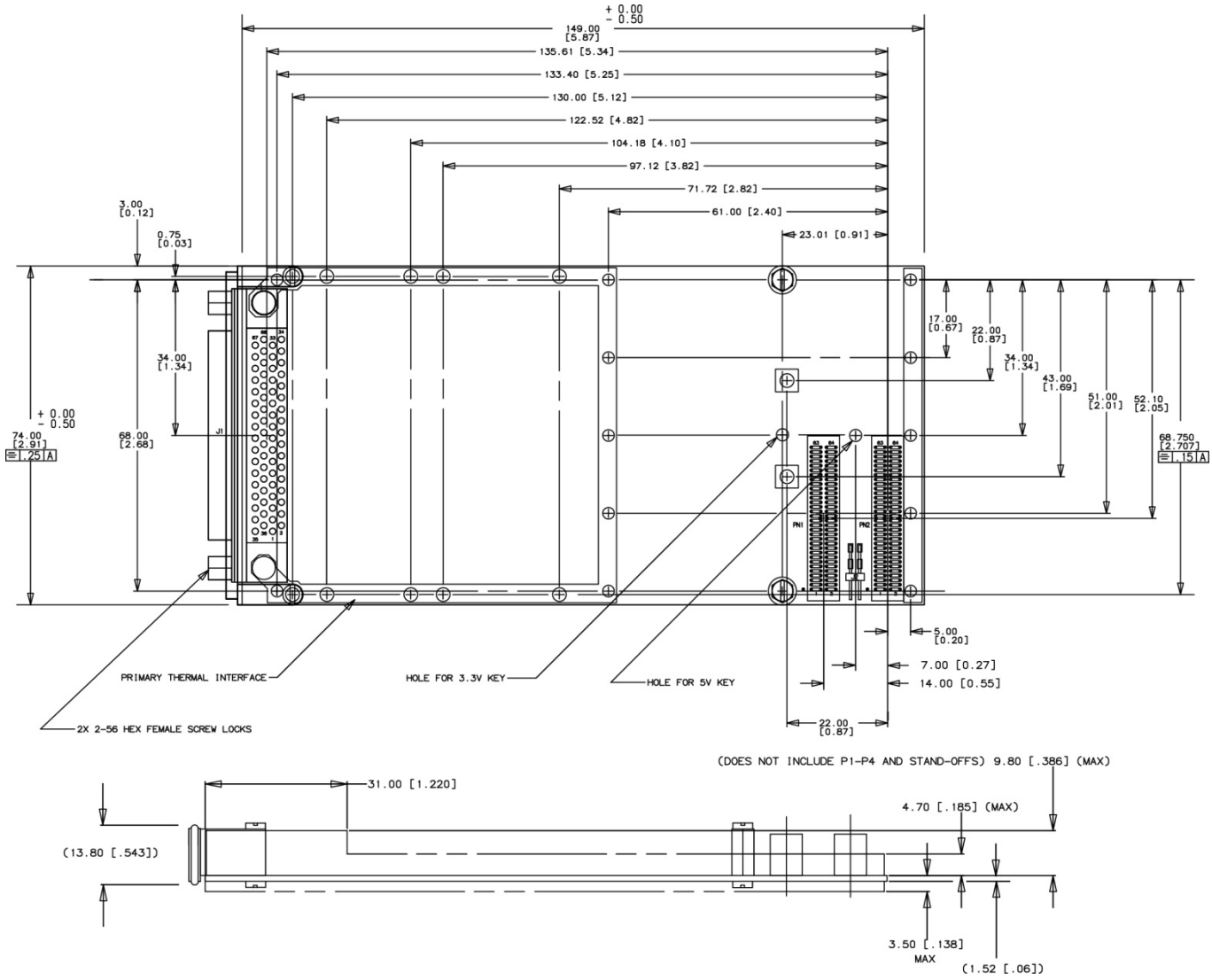

Figure 3. SB-3642 Mechanical Outline

2.6 Specifications

Table 2. SB-3642 Specification Table (Note 1)

These specs apply over the rated power supply, temperature, and reference frequency ranges: 10% signal amplitude variation, and 10% harmonic distortion (for values without a tolerance already specified).

PARAMETER	MIN	TYP	MAX	UNITS
ANGLE POSITION INDICATION CHANNELS				
Channel Count:				
• SB-3642xF4		4		Channels
• SB-3642xF8		8		Channels
Resolution (Programmable)		10, 12, 14, or 16		Bits
Accuracy + Repeatability (Note 2)	**@ 47 Hz to 1kHz**	**@ 400 Hz to 4kHz**	**@ 4001 Hz to 7kHz**	
• SB-36420 (2Vrms Single Ended)	–	1 + 1 LSB	5 + 1 LSB	Arc-Minutes
• SB-36421 (11.8Vrms Synchro)	–	1 + 1 LSB	5 + 1 LSB	Arc-Minutes
• SB-36422 (11.8Vrms Resolver)	–	1 + 1 LSB	5 + 1 LSB	Arc-Minutes
• SB-36423 (90Vrms Synchro)	–	2 + 1 LSB	5 + 1 LSB	Arc-Minutes
• SB-36424 (90Vrms Synchro)	2 + 1 LSB	–	–	Arc-Minutes
Signal Input Voltage and Impedance	**Dependent on Card Ordering Option**			
	SB-36420 (Note 3)	**SB-36421 SB-36422**	**SB-36423 SB-36424**	
• Synchro	–	11.8	90	Vrms L-L
- Zin line-to-line	–	52k	195k	Ohms
- Zin each line-to-ground	–	35k	130k	Ohms
• Resolver	2	11.8	–	Vrms L-L
- Zin single-ended **(Note 4)**	10M min || 20F	70k	–	Ohms
- Zin Differential	–	140k	–	Ohms
• Common-mode Range	–	30	–	V max

Reference Input Parameters	**Dependent on Card Ordering Option**				
	SB-36420	**SB-36421 SB-36422**	**SB-36423**	**SB-36424**	
• Carrier Frequency	360 to 7k	360 to 7k	360 to 1k	47 to 400	Hz
• Type	Differential or Single-ended				
• Voltage Range	2 to 130				Vrms
• Input Impedance **(Note 5)**					
- Z_{in} Single-Ended	400				kΩ
- Z_{in} Differential	800				kΩ

Table 2. SB-3642 Specification Table (Note 1)

These specs apply over the rated power supply, temperature, and reference frequency ranges: 10% signal amplitude variation, and 10% harmonic distortion (for values without a tolerance already specified).

PARAMETER		MIN	TYP		MAX	UNITS
DYNAMIC CHARACTERISTICS		**AT 400 HZ NOMINAL CARRIER F.**				
At Resolution		10	12	14	16	Bits
At Bandwidth	Low	**Note 6**	**Note 6**	80	80	Hz
	High	300	300	**Note 7**	**Note 7**	Hz
• Max. Tracking Rate		320	80	20	5	RPS
• Velocity Scale Factor		0.0125	0.05	0.2	0.8	Volts / RPS
DYNAMIC CHARACTERISTICS		**AT 60 HZ NOMINAL CARRIER F.**				
At Resolution		10	12	14	16	Bits
At Bandwidth	Low	**Note 6**	**Note 6**	15	15	Hz
	High	45	45	**Note 7**	**Note 7**	Hz
• Max. Tracking Rate		32	8	2	0.5	RPS
• Velocity Scale Factor		0.125	0.5	2	8	Volts / RPS
VELOCITY OUTPUT CHARACTERISTICS						
Voltage Range		-4.0			4.0	V
Scale Factor Error			10		20	%
Scale Factor TC			100		200	PPM / ºC
Reversal Error			1		2	%
Linearity			0.5		1	% output
Zero Offset			5		15	mV
Zero Offset TC			15		30	µV / ºC
Load		10				kΩ
BIT FAULT CONDITIONS (Note 8)		**Dependent on Card Ordering Option**				
(hardware pin available on 4-channel board only)		**SB-36420**	**SB-36421 SB-36422**		**SB-36423 SB-36424**	
Loss of Signal (LOS) when SIN & COS is below…		0.5 Vrms	3 VLL		22.5 VLL	
Loss of Reference (LOR) when reference is below…		1.0				Vrms
Loss of Tracking (LOT) when difference between digital output and analog input exceeds…		100 LSBs in the positive direction, or 250 LSBs in the negative direction				LSBs
180º Phase Error when input signal to reference input gives false null		180º Out of Phase				Degrees
DIGITAL OUTPUTS DRIVE CAPABILITY (A, B, ZIP, BIT signals)						
Logic 0, 1 TTL load at 0.4V max.		1.6				mA
Logic 1, 10 TTL loads at 2.8V min.		0.4				mA

Table 2. SB-3642 Specification Table (Note 1)

These specs apply over the rated power supply, temperature, and reference frequency ranges: 10% signal amplitude variation, and 10% harmonic distortion (for values without a tolerance already specified).

PARAMETER	MIN	TYP	MAX	UNITS
DISCRETE DIGITAL I/O (4-channel board only), see Para. 4.3.3				
V_{IL}			3	V
V_{IH}			30	V
V_{OL}			1.5	V
V_{OH}			30	V
POWER SUPPLY REQUIREMENTS (Note 9)				
Voltages/Tolerances				
+5 V	4.75	5	5.25	V
+3.3 V	3.0	3.3	3.6	V
Current Drain (+5V)			0.20	A
Current Drain (+3.3V)			0.60	A
PCI INTERFACE				
Bit Size			32	bits
Clock Speed			66	MHz
Bus Signaling (Universal Bus Voltage)		3.3 / 5		V
COOLING METHOD				
Air-cooled (Required for industrial temp. range)	300			LFM
THERMAL				
Card Operating Temperature Range (2A0)				
with 300 LFM air-flow	-40		+85	°C
Storage Temperature	-65		+150	°C
MECHANICAL DESIGN				
Shock	Vita-47 / MIL-STD-810, TM516, Class S1 for CC (50 g, 11ms, half-sine, 18 shocks total)			
Vibration	Vita-47 / MIL-STD-810, TM514, “V2” (AC)			
Humidity	Vita-47 / MIL-STD-810, TM507, Procedure II			
PHYSICAL CHARACTERISTICS				
Size	2.91 x 5.87 x 0.39 (74.0 x 149.0 x 10.0)			in. (mm.)
Weight	4.16 (118)			oz. (g)

Table 2. SB-3642 Specification Table (Note 1)

These specs apply over the rated power supply, temperature, and reference frequency ranges: 10% signal amplitude variation, and 10% harmonic distortion (for values without a tolerance already specified).

PARAMETER	MIN	TYP	MAX	UNITS

Notes:

1. The specifications apply over the rated power supply, temperature, and reference frequency ranges.
2. Accuracy is tested in 16 bit resolution. Expect ± 1 LSB of jitter for frequencies less than or equal to 1 kHz.
3. Direct input requires SIN input, COS input, and a common ground.
4. || = “in parallel with”
5. Minimum impedance is guaranteed over the operating range, but is not tested.
6. Exceeds Tracking Rate / Bandwidth Ratio, See Table 4. An instantaneous large step angle increment can cause spin-around condition. To avoid spin-around at power up, the default condition is 16 Bit resolution and Low Bandwidth.
7. Carrier Frequency / Bandwidth Ratio of 5X is recommended to maintain jitter < 1 LSB
8. For more information, see section on Built-In-Test (BIT) Output
9. All power measurements were taken with a 66-MHz PCI bus.

3 HARDWARE INSTALLATION

The SB-3642 card is a 32-bit, 33/66 MHz PCI Local Bus Rev. 3.0 compliant interface target device that may be inserted into any compatible slot. Note that this card is capable of universal PCI signal and automatically defaults to 3.3V or 5V depending on the host bus.

When installing the card, the following should be observed:

- **NEVER** insert or remove the card with the power turned on.
- **ALWAYS** take proper precautions to guard against static damage.
- Use a wrist strap if available, or ensure proper static grounding by touching the power supply cover **WITH POWER OFF**.
- Insert the card at a slight angle so that the connectors first protrude from the rear opening and then gently press the card into the motherboard connector. Secure with proper hardware.
- Make sure that adjacent cabling and wiring do not hinder the airflow around the card.

This card is designed as a Plug-and-Play device and as such, there are no jumpers or switches to be set for address and interrupt selection.

3.1 Hardware Configuration and Operation

The SB-3642 card utilizes the PCI interface, and the configuration for Plug-and-Play PCI is performed by the operating system. During the initial power on boot process, the system performs an enumeration of the PCI bus and allocates a resource configuration that satisfies the card requirements. The system will save the configuration information in the SB-3642's PCI configuration space registers. These registers are configured at the factory to contain information that identifies the card type, vendor, required memory sizes, and interrupt resources. When the driver loads, it will access the configuration registers and identify how the system has configured the card. After identifying each of the installed cards, the device driver will enumerate each of the channels on the card and create a configuration structure that defines the allocated address and interrupt. The end user does not need to know this information if using one of the supplied C API libraries to operate the card.

4 DETAILED ARCHITECTURE

4.1 PCI Interface

The card provides a target 32-bit PCI interface, as defined in the PCI Local Bus Specification, Rev 3.0, which operates at clock speeds of up to 66 MHz for applications where a higher bus speed is desired. If a 33 MHz device was placed on a 66 MHz bus, the bus speed would be forced to slow down to 33 MHz. Although resolver simulation may not require the additional bandwidth of a 66 MHz bus, the SB-3642 66 MHz device allows the base CPU PCI bus to run at 66 MHz, enabling other high-speed devices on the bus to take advantage of the higher bandwidth.

When using the card with the supplied Motion Feedback C SDK (SB-36030Sx) and drivers there is no need to reference the PCI configuration registers.

Connection to the host is established through the card's Pn1 and Pn2 connectors. PCI 64 bit extension is not supported, the PMC Pn3 for PCI 64 bit extension and Pn4 for user I/O connectors are not populated on the card.

4.1.1 Use with 5V PCI Signaling

The PCI interface signals on the SB-3642 support +3.3V or +5V signaling. The device incorporates both 3.3V and 5V signal keying holes.

4.1.2 Register & Memory Addressing

The SB-3642 PCI interface contains a set of "Type 00h" PCI configuration registers that are used to map the device into the host system. The configuration register space is mapped in accordance with PCI Revision 3.0 specifications. These registers are arranged such that all memory and register space may be addressed through a single PCI function.

Configuration registers implement the Subsystem Vendor and Device ID, and control the Fail-Safe operation of the device. There is one Base Address Registers (BAR) used on the design of this card. All BAR mapping is located in PCI configuration register space.

When using this card with DDC's driver and the API library software, the details of these registers and memory addresses are abstracted from the user to provide an easy-to-use High Level "C" programming environment.

4.2 Synchro/Resolver to Digital Channels

4.2.1 Signal Interface

The front panel connector provides signal connections for all channels. These signals include S1, S2, S3, S4 inputs and differential reference inputs RH and RL. See below to identify which inputs are applicable to the selected model number.

Configuration for the resolver inputs is accomplished by the use of specific thin film resistor networks installed on the card. These networks scale the input voltage to the converter for a 2V, 11.8V, or 90V resolver or synchro full scale input signal.

Below are the input signal designations for synchro, resolver, and single-ended mode:

- Synchro Mode Connect (SB-36421, SB-36423, SB-36424)
  - S1
  - S2
  - S3
  - S4 is not used
- Resolver Mode Connect (SB-36422)
  - S3 = +SIN
  - S1 = -SIN
  - S2 = +COS
  - S4 = -COS
- Single-ended Mode Connect (SB-36420)
  - S2 = +COS
  - S3 = +SIN

When using single ended configuration, S1 and S4 need to be returned to the analog ground using the associated analog ground pin, see pinout in **Error! Reference source not found.**.

4.2.1 Bandwidth

The user can program each channel independently for one of two bandwidth settings through software. The bandwidth selection is programmable for either 80 or 300 Hz.

The bandwidth selection configures the converters' bandwidth setting in order to optimize signal noise rejection and dynamic response. For best dynamics, the rule of thumb is bandwidth should be less than or equal to ¼ of the Resolver carrier frequency, F_c.

For instance, a 400 Hz Resolver (F_c = 400Hz) should nominally have a converter bandwidth set at 400 Hz / 4 = 100 Hz or less. In the case of SB-3642, the low bandwidth is set to 80 Hz. This bandwidth setting would be an appropriate selection for 400Hz carrier frequency.

If operating at a carrier frequency 1200 Hz or above, the 300Hz bandwidth setting would be an appropriate selection, as follows: 300 x 4 = 1200Hz (Fc). The greater bandwidth setting allows for increased dynamic performance, but the tradeoff is less noise immunity than the 80 Hz bandwidth setting.

For optimal performance at high bandwidth and high resolution (14 or 16 bits), it is recommended to use a carrier frequency above 1.5 kHz. Refer to Table 3 for Dynamic Characteristics depending on device selection.

Note: *Use caution when operating in 10 bit and 12 bit modes. Large input steps can induce a high acceleration into the converter that may cause the maximum velocity to be exceeded. If this occurs, the converter can enter a spin-around condition where it may never settle to an angle because of the low bandwidths at these resolutions.*

Table 3. Dynamic Characteristics

Type		400 Hz Nominal Carrier Freq.			
Resolution (bits)		10	12	14	16
Bandwidth (Hz)	Low	*	*	80	
	High	300		**	**
Tracking Rate (RPS)		320	80	20	5
Scale Factor (Volts / RPS)		0.0125	0.05	0.2	0.8

* Exceeds tracking Rate/Bandwidth Ratio, See Table 4. An instantaneous large step angle increment can cause spin-around condition. To avoid spin-around at power up, the default condition is 16 Bit resolution and Low Bandwidth.
** Carrier Frequency/Bandwidth ratio of 5X is recommended to maintain jitter < 1 LSB.

Table 4. Tracking to Bandwidth Relationship

Rev per Second (Max) / BW	Resolution
1	10
0.50	12
0.25	14
0.125	16

4.2.1 Velocity Output

Each channel has an analog velocity output. The voltage range is ± 4V. The polarity indicates the direction of rotation where a positive voltage is for increasing angle. See Table 5 below for Analog Velocity Characteristics.

Table 5. Velocity Characteristics			
PARAMETER	**UNITS**	**TYPICAL**	**MAX./MIN.**
POLARITY			
Voltage Range	V	4.0	
VOLTAGE SCALING			
(resolution dependent)	RPS/V	Typical TR (See Table 3)	
SCALE FACTOR			
Error	%	10	20 (max.)
Scale Factor TC	PPM/ deg C	100	200 (max.)
Reversal Error	%	1	2 (max.)
Linearity	% output	0.5	1 (max.)
Zero Offset	mV	5	15 (max.)
Zero Offset TC	uV/ deg C	15	30 (max.)
Load	k Ohms		10 (min.)

4.2.2 Built-In-Test (BIT) Output

The Built-In-Test (BIT) will flag Loss-of-Signal (LOS), Loss-of-Reference (LOR), Loss-of-Tracking (LOT), and 180° phase error fault conditions. The BIT output is active low and a logical OR of these four conditions. Any one or combination of these conditions will assert the BIT output. These fault conditions are described in Table 6 below. Also, excessive error is detected when the difference between the analog input and the digital output exceeds approximately 100 LSBs of positive or 250 LSBs of negative error (in the selected resolution), the BIT will be asserted.

Table 6. BIT Fault Conditions	
Fault Condition	**Description**
LOS	Both SIN and COS inputs (S1-S3, S2-S4) must fall below 0.5 Vrms.
LOR	The reference input (RH-RL) must fall below 0.5 Vrms.
LOT	This condition occurs when the difference between the analog input and digital output exceeds 100 LSBs in the positive direction or 250 LSBs in the negative direction. This typically occurs when exceeding the maximum tracking rate or during power up.
180° Phase Error	180° phase error input signal to reference input (false null) causes a BIT plus kickstarts the converter counter to correct the error.

4.2.3 Synthesized Reference

The synthesized reference eliminates errors due to phase shift within the resolver sensor of up to 45° between the reference and the signal inputs. This feature is built into all input channels of this device.

4.2.1 Sample Read Sequence

Write to inhibit channels, read position for that channel, and write to un-inhibit channels. This process will prevent reading data in transition. See the SB-36030Sx Software Manual for specific commands and explanations.

4.3 Additional Functionality

4.3.1 Self-Test

The device has a built-in self-test capability which can run a simulated test angle of 0, 45, or 90 degrees on each channel. Any channel not reporting back an answer within ±1° will fail.

4.3.2 Two-Speed Mode

Two-speed mode allows resolutions greater than 16 bits to be achieved. Two-speed mode may be implemented for both static angles and rotations. The procedure to use two-speed mode is described in Software Manual SB-36030Sx. For more information on two-speed mode, refer to the Two-Speed Application Note (AN/MFT-10), the RD/RDC Applications Manual (MN-19220XX-001) and the Synchro/Resolver Conversion Handbook. These documents are available at www.ddc-web.com.

4.3.3 Discrete Digital I/O

Note: This feature is only available on the 4-channel board, SB-3624xF4.

The SB-3642 has 4 discrete inputs and 4 discrete outputs. Outputs are physically driven by the output of the Darlington open-collector drivers. Output pins are opto-isolated by opto-couplers whose output current sinking capability has been increased using a discrete transistor connected in a Darlington configuration. The emitters of all the output transistors are the pins labeled "DIO_Ext_GND" on the connector. The Inputs are also referenced to these same pins. The opto-isolators provide up to 1500 Vac isolation for the discrete I/O on the card.

The discrete digital I/O can be used for a variety of applications including triggering events, indicating status, or general purpose use.

Refer to SB-36030Sx Software Manual for Discrete I/O operation and control.

4.3.3.1 I/O Characteristics

- Discrete Outputs:
  - Max Output Voltage = 30 V
  - Any single output can drive 100 mA at 25° C
- Discrete Inputs:
  - Input pins are directly connected to inputs of the opto-couplers.
  - Max Input voltage = 30 V
  - Input impedance is approximately 2.7 kΩ with input turned on and high impedance with input approximately less than 3 V

4.3.4 Incremental Encoder Emulation (A Quad B)

Note: This feature is only available on the 4-channel board, SB-3624xF4.

The SB-3642 can also be used for incremental encoder emulation. The following outputs are readily available on the front I/O connector: A, B, and ZIP (Zero Index Pulse). The timing of the A & B outputs are dependent on the rate of change of the resolver position (rps or degrees per second) and the encoder resolution latched into the converter (refer to Figure 5). The calculations for the timing are:

n = resolution of parallel data

t = 1 / (2n * Velocity(RPS))

T = 1 / (Velocity(RPS))

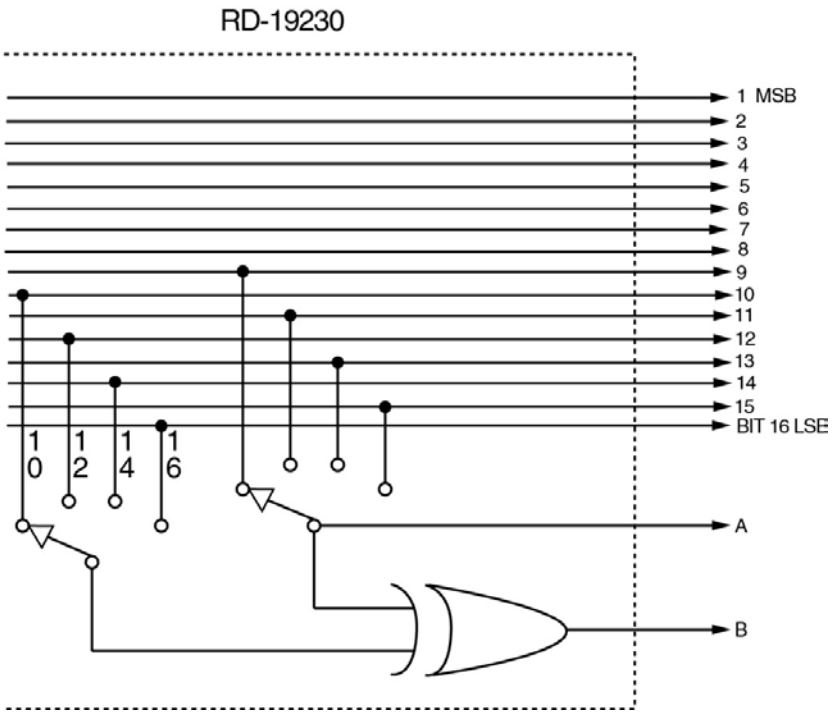

Figure 4. Incremental Encoder Emulation Resolution Control

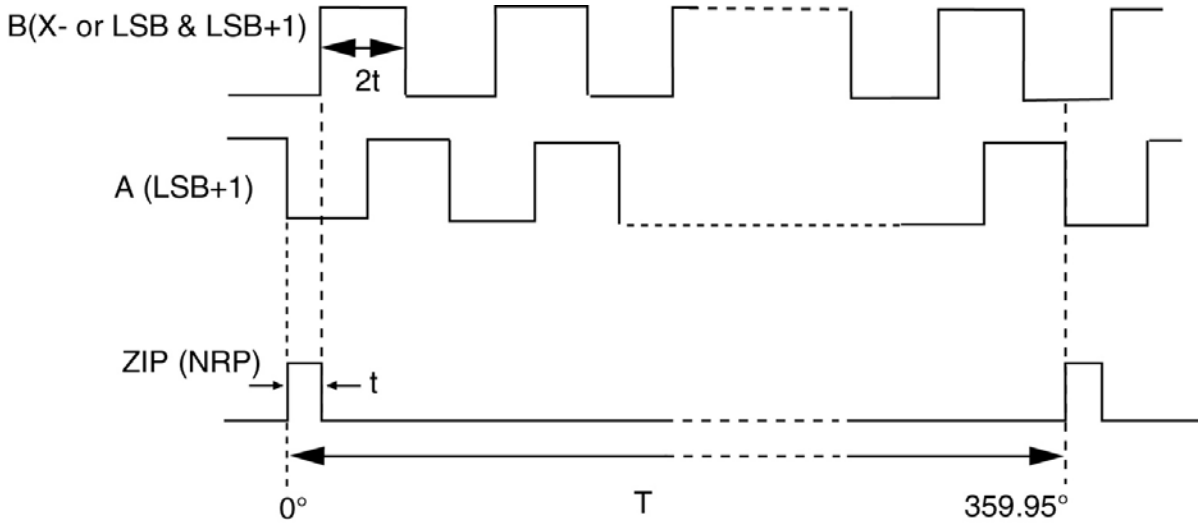

Figure 5. Incremental Encoder Emulation Timing

4.4 Card Pinouts

This section delineates the pinouts for the card. The front-panel configuration allows all signals to pass through a 68-pin I/O connector. Note that PCI signal inputs are via Pn1 & Pn2 ports on the PMC connector.

The front panel connector described here contains each channel's Interface Signals, Reference Inputs, Velocity Output, BIT Output, Encoder Emulation Outputs, and Programmable Digital I/O signals.

Table 7. Signal List

SIGNAL NAME	Direction	Description
CHx_RH	Input	Channel Reference High
CHx_RL	Input	Channel Reference Low
CHx_S1	Input	Channel S1 Signal
CHx_S2	Input	Channel S2 Signal
CHx_S3	Input	Channel S3 Signal
CHx_S4	Input	Channel S4 Signal
CHx_AGND	Ground	Channel Analog Ground
CHx_BIT_L	Output	Channel Built-In-Test Signal
CHx_VEL	Output	Channel Velocity Signal
CHx_A	Output	Channel Encoder Emulation Signal A
CHx_U/B	Output	Channel Encoder Emulation Signal B
CHx_CB/Zi	Output	Channel Encoder Emulation Signal Zi
DGND	Ground	Digital ground reference connection
DIO_Input_x	Input	Discrete Input
DIO_Output_x	Output	Discrete Output
DIO_Ext_GND	Ground	Discrete ground reference connection
EXT_FLASH_WRITE_EN_L	Flashing	For new firmware flashes only. No Connect during normal use
BOOT_SELECT	Flashing	For new firmware flashes only. No Connect during normal use

Note: Within each Signal Name, "x" designates a particular value from 0 to 7.

Table 8. Front Panel Connector Pinout							
SB-3642xF4 (4-Channel Board)				SB-3642xF8 (8-Channel Board)			
PIN	NAME	PIN	NAME	PIN	NAME	PIN	NAME
1	DGND	35	DGND	1	DGND	35	DGND
2	CH1_RH	36	CH1_S4	2	CH1_RH	36	CH1_S4
3	CH1_AGND	37	CH1_S3	3	CH1_AGND	37	CH1_S3
4	CH1_RL	38	CH1_S2	4	CH1_RL	38	CH1_S2
5	CH1_VEL	39	CH1_S1	5	CH1_VEL	39	CH1_S1
6	CH0_RH	40	CH0_S4	6	CH0_RH	40	CH0_S4
7	CH0_AGND	41	CH0_S3	7	CH0_AGND	41	CH0_S3
8	CH0_RL	42	CH0_S2	8	CH0_RL	42	CH0_S2
9	CH0_VEL	43	CH0_S1	9	CH0_VEL	43	CH0_S1
10	CH2_RH	44	CH2_S4	10	CH2_RH	44	CH2_S4
11	CH2_AGND	45	CH2_S3	11	CH2_AGND	45	CH2_S3
12	CH2_RL	46	CH2_S2	12	CH2_RL	46	CH2_S2
13	CH2_VEL	47	CH2_S1	13	CH2_VEL	47	CH2_S1
14	CH3_RH	48	CH3_S4	14	CH3_RH	48	CH3_S4
15	CH3_AGND	49	CH3_S3	15	CH3_AGND	49	CH3_S3
16	CH3_RL	50	CH3_S2	16	CH3_RL	50	CH3_S2
17	CH3_VEL	51	CH3_S1	17	CH3_VEL	51	CH3_S1
18	CH3_CB_Zi	52	DIO_Ext_GND	18	CH5_RH	52	CH5_S4
19	DGND	53	DIO_Output_3	19	CH5_AGND	53	CH5_S3
20	CH0_A	54	DIO_Output_2	20	CH5_RL	54	CH5_S2
21	CH0_U/B	55	CH0_BIT_L	21	CH5_VEL	55	CH5_S1
22	CH0_CB/Zi	56	DIO_Ext_GND	22	CH4_RH	56	CH4_S4
23	DGND	57	DIO_Output_1	23	CH4_AGND	57	CH4_S3
24	CH1_A	58	DIO_Output_0	24	CH4_RL	58	CH4_S2
25	CH1_U/B	59	CH1_BIT_L	25	CH4_VEL	59	CH4_S1
26	CH1_CB/Zi	60	DIO_Ext_GND	26	CH6_RH	60	CH6_S4
27	DGND	61	DIO_Input_1	27	CH6_AGND	61	CH6_S3
28	CH2_A	62	DIO_Input_0	28	CH6_RL	62	CH6_S2
29	CH2_U/B	63	CH2_BIT_L	29	CH6_VEL	63	CH6_S1
30	CH2_CB/Zi	64	DIO_Ext_GND	30	CH7_RH	64	CH7_S4
31	DGND	65	DIO_Input_3	31	CH7_AGND	65	CH7_S3
32	CH3_A	66	DIO_Input_2	32	CH7_RL	66	CH7_S2
33	CH3_U/B	67	CH4_BIT_L	33	CH7_VEL	67	CH7_S1
34	BOOT_SELECT	68	EXT_FLASH_ WRITE_EN_L	34	BOOT_SELECT	68	EXT_FLASH_ WRITE_EN_L

Notes:
1. All AGND and DGND pins are internally common
2. EXT_FLASH_WRITE_EN_L and BOOT_SELECT are for flashing new firmware. No Connect if not flashing

4.4.1 Front Panel I/O Connector

The connector (soldered on the board) used for the front-panel I/O connection is a 68-pin. Pin numbering designations for the connector are as shown in Figure 7.

Figure 6. 68-Pin I/O Connector Photograph

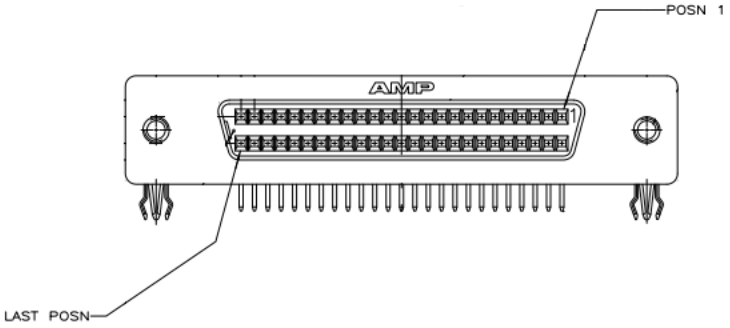

Figure 7. 68-Pin I/O Connector Pin Locations
(viewed from front panel of card, 1 to 34 top row, 35 to 68 bottom row)

4.4.2 Supplied I/O Mating Connector Components

The ***SB-3642*** is supplied with the I/O mating connector components as listed in Table 9. These components may be used to construct a cable to interface to the I/O on the card. **Error! Reference source not found.** lists the Front Panel Connector Pinout.

Table 9. Supplied I/O Mating Connector Components

Connector Description	Part Number (Pickering)	Part Number (DDC)
Pickering SCSI style Micro-D Solder Bucket Connector and Backshell	40-962A-068-SB-M	5301-0987-0101

5 SOFTWARE

Numerous software packages are available for the SB-3642. The DDC software packages are developed to allow shorter design cycles while allowing all SB-3642 functionality to be accessed by user level code.

The available software packages include:

- Motion Feedback C SDK (SB-36030Sx)
- Motion Feedback Application (SB-36000S0)
- Motion Feedback LabVIEW SDK (SB-36030SL)

5.1 Software Overview

5.1.1 Motion Feedback C SDK (SB-36030Sx)

The card is supplied with the SB-36030Sx Motion Feedback C SDK. This software development kit includes a runtime library that provides the user with a hardware abstraction layer for the DDC Motion Feedback hardware. This software layer includes the routines that dramatically reduce software development time by providing high-level C functions for the application programmer to interface to the SB-3642 card. C samples are included with the library to demonstrate how the API works with the hardware. Table 10 shows a summary of the supported operating systems.

The ***SB-36030Sx Software Manual*** can be downloaded from the DDC web site at *www.ddc-web.com*.

Table 10. Motion Feedback Library C SDK Part Number Descriptions

Part Number	Operating System
SB-36030S0	Windows
SB-36030S1	Linux

5.1.2 Motion Feedback Application (SB-36000S0)

The card is supplied with the SB-36000S0 Motion Feedback Application. This is a graphical software which runs on Windows.

The ***SB-36000S0 Manual*** can be downloaded from the DDC web site at www.ddc-web.com.

5.1.3 Motion Feedback LabVIEW SDK (SB-36030SL)

The card is supplied with the SB-36030SL Motion Feedback LabVIEW support package. This software development kit includes a set of VIs that provides the user with a hardware abstraction layer for the DDC Motion Feedback hardware in a LabVIEW environment. The Package includes 3 layers of VIs which enable easy application development. Functional user samples are included for common functions.

5.1.4 Troubleshooting the Installation

Usually the installation will be successful, and the self-test within the sample programs will pass. There are, however, some situations that can cause problems during the installation. The most common are detailed below.

An error is returned when an attempt is made to run any of the samples. This fault is almost always related to an incorrectly assigned device number. Be sure that a device number was correctly assigned through the DDC Card Manager.

If an error is encountered and the device number appears to be correctly assigned, check the operating system. The BIOS setting for a PnP operating system is sometimes set to YES, which can cause a problem. This BIOS option must be set for NO. The operating system, as well as all hardware on your system, will still maintain PnP compatibility; it will not be necessary to manually configure resources for PnP cards.

6 ORDERING INFORMATION

SB-3642 x F x–2A0 N

Supplemental Process Requirements:
N = Acrylic Conformal Coating

Operational Temperature:
2A0 = -40°C to +85°C Rugged Air Cooled Card

Channel Count:
4 = 4 Channels
8 = 8 Channels

I/O Connection:
F = PMC Front Connector I/O
T = PMC on cPCI carrier card

Signal Input Options:

Ordering Option #	Input Mode	Programmable Bandwidths
0	2V Single Ended	80 Hz and 300 Hz
1	11.8Vrms Synchro	80 Hz and 300 Hz
2	11.8Vrms Resolver	80 Hz and 300 Hz
3	90Vrms Synchro	80 Hz and 300 Hz
4	90Vrms Synchro	15 Hz and 45 Hz

Notes:
1) Bandwidth is related to the operating frequency; see **Bandwidth Section** for more information.

INCLUDED ACCESSORIES

- Product DVD with ***SB-3642*** manual
- 1 mating connector and backshell

INCLUDED SOFTWARE (Available on ***SB-3642*** Product Page at www.ddc-web.com)

SB-36030SX- Motion Feedback C Software Development Kit (SDK)

Operation System:
0 = Windows
1 = Linux
L = LabVIEW (Windows)

SB-36000S0- Motion Feedback Application

STANDARD DDC PROCESSING FOR DISCRETE MODULES/PC BOARD ASSEMBLIES		
TEST	**METHOD(S)**	**CONDITION(S)**
INSPECTION/WORKMANSHIP	IPC-A-610	Class 3
ELECTRICAL TEST	DDC ATP	—