NANO-ACE® MIL-STD-1553 TERMINAL WITH SPI INTERFACE

BU-67743L, BU-67753L, BU-67833L DATA SHEET

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Revision	Date	Pages	Description
A	8/2015	All	Initial Release
B	7/2017	All	Added lead finish information to outline drawing pg. 63. Changed “package style” description. Removed all references to self-test and BC mode. Updates to tables 2, 6, 17, 19, 21, 22, 28 and 43. Updated text in sections 4.3, 4.13, 5.7, 5.8, 7.3, 7.4. Deleted Table 20, section 4.13 and section 7.5.
C	8/30/2018	All	Add section 5 and 6 (Monitor and Bus Controller modes). In section 8.7 define A2/E2 as always set to ‘0’ and flag Errata for reading/writing from Host to I2C EEPROM

1 PREFACE

This data sheet uses typographical conventions to assist the reader in understanding the content. This section will define the text formatting used in the rest of the data sheet.

1.1 Text Usage

- BOLD–indicates important information and table, figure, and chapter references.
- Courier New–indicates code examples.
- <…> - indicates user-entered text or commands.

1.2 Special Handling and Cautions

Warnings: Turn off power to the computer hardware and unplug from wall.

Ensure that standard ESD precautions are followed. As a minimum, one hand should be grounded to the power supply in order to equalize the static potential.

Do not store disks in environments exposed to excessive heat, magnetic fields or radiation.

1.3 Trademarks

All trademarks are the property of their respective owners.

1.4 What is included in this data sheet?

This data sheet contains a complete description of component.

1.5 Technical Support

In the event that problems arise beyond the scope of this data sheet, you can contact DDC by the following:

US Toll Free Technical Support:
1-800-DDC-5757, ext. 7771

Outside of the US Technical Support:
1-631-567-5600, ext. 7771

Fax:
1-631-567-5758 to the attention of DATA BUS Applications

DDC Website:
www.ddc-web.com/ContactUs/TechSupport.aspx

Please note that the latest revisions of Software and Documentation are available for download at DDC's Web Site, www.ddc-web.com.

2 OVERVIEW

The Nano-ACE® is a complete and compact solution to MIL-STD-1553 applications. With a footprint of just 7mm by 7mm, it is the world's smallest MIL-STD-1553 terminal. The device is powered entirely by +3.3 volts.

Ideal for extended temperature range applications where PC board space is at a premium, the Nano-ACE is available in a 48-pad QFN package, and is rated for -55°C to +125°C operation at base.

The Nano-ACE is software and architecturally compatible with DDC's Enhanced Mini-ACE series of devices. It integrates dual transceivers, protocol engine and 4K or 32K words of internal RAM. The Nano-ACE's Serial Peripheral Interface (SPI) allows direct connection with little or no glue logic and minimal pin usage to a variety of Microcontrollers, DSPs, and FPGAs.

The advanced architecture is key to the Nano-ACE series' high performance. The advanced bus controller architecture gives the Nano-ACE a high degree of flexibility and autonomy. This creates advantages in a number of areas: improving message scheduling control, minimizing host overhead for asynchronous message insertion, facilitating bulk data transfers and double buffering, message retry and bus switching strategies, and data logging and fault reporting. In addition, its remote terminal architecture provides flexibility in meeting all common MIL-STD-1553 protocols. RT data buffering and interrupt options offer support for synchronous and asynchronous messaging, ensure data sample consistency, and support bulk data transfers. The Nano-Ace's Monitor mode includes filtering based on RT Address and Subaddress, and provides true message monitoring.

The versions of the Nano-ACE are:

- BU-67833LC: BC/RT/MT with 32K x17 RAM
- BU-67753LC: RT/MT with 4K x 17 RAM
- BU-67743LC: RT only with 4K x 16 RAM

2.1 Features

- World's Smallest MIL-STD-1553 Terminal Solution
- Small Package QFN (7mm x 7mm x 1mm)
- 50MHz 4-wire Serial Peripheral Interface (SPI) to Host
- Fully Compatible with Enhanced Mini-ACE® Software and Architecture
- Minimal Signal Count SPI Processor Interface
- Available in Full Military Temperature Range: -55°C to +125°C

- +3.3 Volt Only
- 4K or 32K words of internal RAM
- 1mm Max Height
- Compliance with MIL-STD-1553A/B Notice 2, STANAG-3838, and MIL-STD-1760
- Highly Autonomous BC Architecture (BU-67883LC)
- Built-In Message Sequence Controller with 20-Instruction Set
- Flexible RT Buffering with Single, Double, and Circular Buffering
- Selective Message Monitor with Filtering
- 50% Rollover Interrupts for Stacks and Circular Buffers
- Software and Register Compatible to ACE and Enhanced Mini-ACE devices
- RT-Only Operation for Safety-Critical Applications
- Auto-Configuration Mode (BU-67833LC and BU-67753LC)

- Applications Include:
- Displays
- Simple Systems
- Radios/Modems
- Stores Management

Figure 1. BU-67XX3 Nano-ACE®

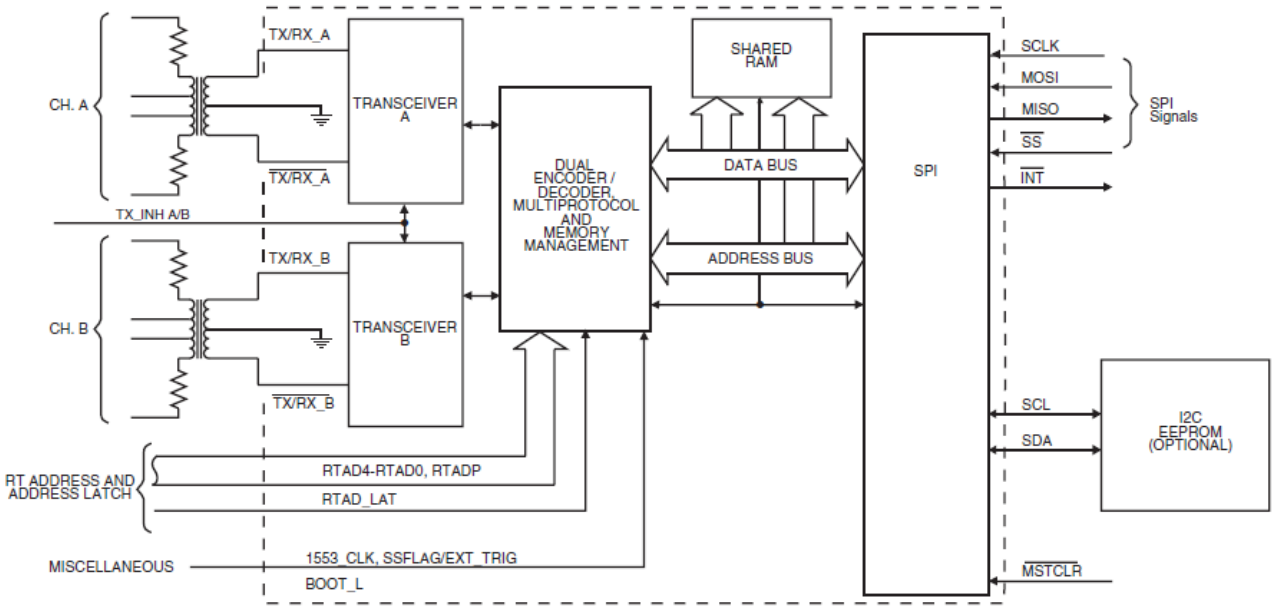


Figure 2. BU- Nano-ACE Architecture (I2C interface not available on BU-67743LC)

Table 1. BU-67833L, BU-67753L, BU-67743L Specification Table				
PARAMETER	**MIN**	**TYP**	**MAX**	**UNITS**
ABSOLUTE MAXIMUM RATING				
Supply Voltage (Note 11)				
• +3.3V (BU-67743LC version only)	-0.3		4.5	V
• +3.3V (BU-67753LC & BU-67833LC)	-0.3		4.0	V
Logic				
+3.3V Logic Input Range	-0.3		Vcc + 0.3	V
POWER SUPPLY REQUIREMENTS				
Voltages/Tolerances (Note 11)				
• +3.3V	3.14	3.3	3.46	V
Current Drain(Total Chip)				
- (BU-67743LC version only)				
• Idle		40	60	mA
• 25% Transmitter Duty Cycle		170	210	mA
• 50% Transmitter Duty Cycle		300	360	mA
• 100% Transmitter Duty Cycle		550	660	mA

Table 1. BU-67833L, BU-67753L, BU-67743L Specification Table				
PARAMETER	**MIN**	**TYP**	**MAX**	**UNITS**
- (BU-67753LC & BU-67833LC)				
• Idle		40	55	mA
• 25% Transmitter Duty Cycle		170	190	mA
• 50% Transmitter Duty Cycle		300	330	mA
• 100% Transmitter Duty Cycle		580	610	mA
POWER DISSIPATION				
TOTAL CHIP(Note 13)				
- (BU-67743LC version only)				
• Idle		0.13	0.21	W
• 25% Transmitter Duty Cycle		0.26	0.38	W
• 50% Transmitter Duty Cycle		0.39	0.55	W
• 100% Transmitter Duty Cycle		0.65	0.90	W
- (BU-67753LC & BU-67833LC)				
• Idle		0.14	0.20	W
• 25% Transmitter Duty Cycle		0.19	0.30	W
• 50% Transmitter Duty Cycle		0.24	0.40	W
• 100% Transmitter Duty Cycle		0.44	0.60	W
RECEIVER				
Differential Input Impedance (Note 1 – 6)	5			k□
Differential Input Capacitance (Note 1 – 6)			10	pF
Threshold Voltage				
• Transformer Coupled, Measured on Stub	0.200	0.600	0.860	Vp-p
• Direct Coupled, Measured on Stub	0.280		1.20	Vp-p
Common-Mode Voltage			±10	Vpeak
TRANSMITTER				
Differential Output Voltage				
• Direct Coupled Across 35□, Measured on Bus	6	7.35	9.0	Vp-p
• Transformer Coupled Across 70□□, Measured on Stub (Note 12)	20	22.0	27	Vp-p
Output Noise, Differential			14	mVRMS
Output Offset Voltage, Transformer Coupled Across 70□□	-250		250	mVp
Rise/Fall Time	100	150	300	nsec

Table 1. BU-67833L, BU-67753L, BU-67743L Specification Table				
PARAMETER	**MIN**	**TYP**	**MAX**	**UNITS**
LOGIC				
VIH	2.1			V
VIL			0.7	V
Schmidt Hysteresis	0.2			V
IIH, IIL				
All signals except CLK_IN, SCLK, MOSI, SS				
IIH (Vcc = 3.6V, VIN = 2.5V)	-100	-40	-10	µA
IIL (Vcc = 3.6V, VIN = 0.0V)	-125	-68	-20	µA
CLK_IN, SCLK, MOSI, SS				
IIH	-10		10	µA
IIL	-10		10	µA
VOH (VCC = 3.0V, VIH = 2.7V, (VIL = 0.2V, IOH = max)	2.4			V
VOL (VCC = 3.0V, VIH = 2.7V, (VIL = 0.2V, IOH = max)			0.4	V
IOL (VCC = 3.0V)	4			mA
IOH (VCC = 3.0V)			-4	mA
CI (Input Capacitance)		6		pF

Table 1. BU-67833L, BU-67753L, BU-67743L Specification Table				
PARAMETER	**MIN**	**TYP**	**MAX**	**UNITS**
CLOCK INPUT				
Frequency				
• Nominal Value		40.0		MHz
Long Term Tolerance				
• 1553A Compliance	-0.01		0.01	%
• 1553B Compliance	-0.10		0.10	%
Short Term Tolerance, 1 second				
• 1553A Compliance	-0.001		0.001	%
• 1553B Compliance	-0.01		0.01	%
Duty Cycle	40		60	%
1553 MESSAGE TIMING				
Completion of CPU Write (BC Start)-to-Start of First Message for Non-enhanced BC Mode	2.5			µs
BC Intermessage Gap (Note 7)				
• Non-enhanced (Mini-ACE compatible) BC mode		9.5		µs
• Enhanced BC mode (Note 8)		10 to 10.5		µs
RT/MT Response Timeout (Note 9)				
• 18.5 nominal	17.5	18.5	19.5	µs
• 22.5 nominal	21.5	22.5	23.5	µs
• 50.5 nominal	49.5	50.5	51.5	µs
• 128.0 nominal	127	129.5	131	µs
RT Response Time (mid-parity to mid-sync) (Note 10)	4		7	µs
Transmitter Watchdog Timeout		668		µs
THERMAL				
NANO-ACE				
48-pad QFN Package				
Thermal Resistance				
• Junction-to-Case (□JC)				
- (BU-67743LC version only)			20	°C/W
- (BU-67753LC & BU-67833LC)			13	°C/W
• Junction-to-Board (□JB) (Note 14)			8	°C/W

Table 1. BU-67833L, BU-67753L, BU-67743L Specification Table				
PARAMETER	**MIN**	**TYP**	**MAX**	**UNITS**
ALL PACKAGES				
Operating Case Temperature				
- 1XX	-55		+125	°C
- 2XX	-40		+80	°C
Operating Junction Temperature				
- (BU-67743LC version only)	-55		+150	°C
- (BU-67753LC & BU-67833LC)	-55		+135	°C
Storage Temperature	-		+150	°C
Pad Temperature (soldering, 10 sec.)	65		+300	°C
SOLDERING/MOUNTING 48-PAD QFN PACKAGE Maximum Peak Body Temperature The reflow profile detailed in IPC/JEDEC J-STD-020 is applicable for both leaded and lead-free products (Refer to DDC's Application Note #AN/B-54 "Design Guide for BU-67401L LPCC Packaged Transceivers" for additional important mounting information.)			+260	°C
PHYSICAL CHARACTERISTICS				
• Moisture Sensitivity Level	MSL-2			
• Electrostatic Discharge Sensitivity	ESD Class 0			
• Package Body Size (48-pad QFN)	0.280 x 0.280 x 0.040			in.
	(7.1x 7.1 x 1.0)			(mm)
• Weight	.0054			oz.
	(.15)			(g)

Table 1. BU-67833L, BU-67753L, BU-67743L Specification Table				
PARAMETER	**MIN**	**TYP**	**MAX**	**UNITS**

Table 1 Notes:

(Notes 1 through 6 are applicable to the Receiver Differential Input Impedance and Differential Capacitance specifications)

1. Specifications include both the transmitter, and receiver (assumed to be tied together without a transformer).
2. Impedance parameters are specified directly between pads TX_A(B)/RX_A(B) and TX_A(B)_L/RX_A(B)_L of the package.
3. It is assumed that all power and ground inputs to the chip are connected.
4. The specifications are applicable for both unpowered and powered conditions.
5. The specifications assume a 2 volt rms balanced, differential, sinusoidal input. The applicable frequency range is 75 kHz to 1 MHz.
6. Minimum resistance and maximum capacitance parameters are guaranteed over the operating range, but are not tested.
7. Typical value for minimum intermessage gap time. Under software control, this may be lengthened (to 65.535 ms – message time) in increments of 1 µs. If ENHANCED CPU ACCESS, bit 14 of Configuration Register #6, is set to logic "1", then host accesses during BC Start-of-Message (SOM) and End-of-Message (EOM) transfer sequences could have effect of lengthening the intermessage gap time. For each host access during an SOM or EOM sequence, the intermessage gap time will be lengthened by 6 clock cycles. Since there are 7 internal transfers during SOM and 5 during EOM, this could theoretically lengthen the intermessage gap by up to 72 clock cycles; i.e., up to 7.2 ms with a 10 MHz clock, 6.0 µs with a 12 MHz clock, 4.5 µs with a 16 MHz clock, or 3.6 µs with a 20 MHz clock.
8. For Enhanced BC mode, the typical value for intermessage gap time is approximately 10 clock cycles longer that for the non-enhanced BC mode. That is, an addition of 1.0 µsat 10 MHz, 833 ns at 12 MHz, 625 ns at 16 MHz, or 500 ns at 20 MHz.
9. Software programmable (4 options). Includes RT-to-RT Timeout (measured mid-parity of transmit Command Word to mid-sync of transmitting RT Status Word).
10. Measured from mid-parity crossing of Command Word to mid-sync crossing of RT's Status Word.
11. External 10 µF tantalum and 0.1 µF capacitors should be located as close as possible to the voltage input balls.
12. MIL-STD-1760 requires a 20 Vp-p minimum output on the transformer-coupled stub connection.
13. Power Dissipation is the input power minus the power delivered to the 1553 fault isolation resistors, the power delivered to the bus termination resistors, and the copper losses in the bus coupling transformer. The external power dissipation for the transformer-coupled configuration (while transmitting) is assumed to be as follows: 0.057 watts for the active bus coupling transformer, 0.422 watts for each of the two bus isolation resistors and 0.141 watts for each of the two bus termination resistors.
14. Junction-to-board thermal resistance is measured in accordance with JEDEC standard JESD51-8. The 16 thermal vias connecting the LPCC heat sink to PCB internal plane are in accordance with JEDEC JESD51-5 (2s2p). Each via is 0.3 mm diameter with 0.035 mm plating. Please refer to JEDEC standard JESD51-5 for detailed PCB construction.

3 INTRODUCTION

The Nano-ACE® is the industry's smallest integrated MIL-STD-1553 terminal solution, enabling its use in applications where PC board space is at a premium. The BU-67XX3LC Nano-ACE requires only the addition of an isolation transformer to provide a complete interface between a host processor and a MIL-STD-1553 bus. The Nano-ACE is available in a 7mm x 7mm plastic QFN package. The Nano-ACE's architecture is identical to that of the Enhanced Mini-ACE family, and most features are both functionally compatible and software compatible with the previous Mini-ACE (Plus) and ACE generations.

The Nano-ACE provides complete multiprotocol support of MIL-STD-1553A/B/McAir, STANAG 3838, and MIL-STD-1760. The Nano-ACE integrates dual +3.3V transceivers, protocol logic, and 4K or 32K words of internal RAM.

The Nano-ACE includes dual +3.3 volt, MIL-STD-1760 trimmed voltage source transceivers for improved line driving capability. The Nano-ACE operates from a 40 MHz clock input.

One of the new salient features of the Nano-ACE (BU-67833LC only) is its Enhanced bus controller architecture. The Enhanced BC's highly autonomous message sequence control engine provides a means for offloading the host processor for implementing multiframe message scheduling, message retry schemes, data double buffering, and asynchronous message insertion. For the purpose of performing messaging to the host processor, the Enhanced BC mode includes a General Purpose Queue, along with user-defined interrupts.

A second major new feature of the Nano-ACE is the incorporation of a fully autonomous built-in self-test (BU-67753LC and BU67833 only). This test provides comprehensive testing of the internal protocol logic. A separate test verifies the operation of the internal RAM. Since the self-tests are fully autonomous, they eliminate the need for the host to write and read stimulus and response vectors.

The Nano-ACE in RT mode offers the same choices of single, double, and circular buffering for individual subaddresses as the ACE, Mini-ACE (Plus), Enhanced Mini-ACE, and Mini-ACE Mark3 terminals. New enhancements to the RT architecture include a global circular buffering option for multiple (or all) receive subaddresses, a 50% rollover interrupt for circular buffers, an interrupt status queue for logging up to 32 interrupt events, and an option to automatically initialize to RT mode with the Busy bit set. The interrupt status queue and 50% rollover interrupt features are also included as improvements to the Monitor architecture.

To minimize board space and "glue" logic, the Nano-ACE terminal provides a 4-wire Serial Peripheral Interconnect (SPI) interface to the host processor. This greatly

simplifies routing and eliminates the need to tie up FPGA or Microcontroller resources providing a wide parallel bus to the 1553 terminal.

The Nano-ACE terminal operates over the standard military temperature range of -55 to +125°C (case) and is ideal for small processor-to-1553 RT applications powered by 3.3 volts only.

3.1 Supporting Documentation

Enhanced Miniature Advanced Communications Engine
(Enhanced Mini-ACE® Series) Users Guide MN-6186X-001
Volume 1 – Architectural Reference

Enhanced Miniature Advanced Communications Engine
(Enhanced Mini-ACE® Series) User's Guide MN-6186X-002
Volume 2 – Hardware Reference

3.2 Transceivers

The transceivers in Nano-ACE® series terminals are fully monolithic, requiring only +3.3 power input. Nano-ACE transmitters inherently satisfy the MIL-STD-1760 requirement for a minimum of 20 volts peak-to-peak, transformer-coupled output.

Besides eliminating the demand for an additional power supply, the use of +3.3 volt only transceivers requires the use of a built-in step-up, rather than a step-down, isolation transformer. This provides the advantage of a higher terminal input impedance than is possible for a 15V, 12V or 5V transceiver. As a result, there is a greater margin for the input impedance test, mandated for the 1553 validation test. This allows for longer cable lengths between a system connector and the isolation transformers of an embedded 1553 terminal.

The receiver sections of the Nano-ACE are fully compliant with MIL-STD-1553B Notice 2 in terms of front-end overvoltage protection, threshold, common-mode rejection, and word error rate.

3.3 Register and Memory Addressing

The software interface of the Nano-ACE to the host processor consists of 24 internal operational registers for normal operation, an additional 24 test registers, plus 64K words of shared memory address space. The Nano-ACE's 4K x 16, 4K X 17 or 32K x 17 of internal RAM resides within this address space.

For normal operation, the host processor only needs to access the lower 32 register address locations (00-1F). The next 32 locations (20-3F) are accessible by setting bit 2 to a '1' in Configuration Register #6 (address 18 H).

3.4 Internal Registers

The address mapping for the Nano-ACE® registers is illustrated in Table 2.

Table 2. Address Mapping

Address	Address Bits						Register Description/Accessibility
HEX	A5	A4	A3	A2	A1	A0	
XX00	0	0	0	0	0	0	Interrupt Mask Register #1 (RD/WR)
XX01	0	0	0	0	0	1	Configuration Register #1 (RD/WR)
XX02	0	0	0	0	1	0	Configuration Register #2 (RD/WR)
XX03	0	0	0	0	1	1	Start/Reset Register (WR)
XX03	0	0	0	0	1	1	Non-Enhanced BC/RT Command Stack Pointer Register / Enhanced BC Instruction List Pointer Register (RD)
XX04	0	0	0	1	0	0	BC Control Word / RT Subaddress Control Word Register (RD/WR)
XX05	0	0	0	1	0	1	Time Tag Register (RD/WR)
XX06	0	0	0	1	1	0	Interrupt Status Register #1 (RD)
XX07	0	0	0	1	1	1	Configuration Register #3 (RD/WR)
XX08	0	0	1	0	0	0	Configuration Register #4 (RD/WR)
XX09	0	0	1	0	0	1	Configuration Register #5 (RD/WR)
XX0A	0	0	1	0	1	0	RT/Monitor Data Stack Address Register (RD)
XX0B	0	0	1	0	1	1	BC Frame Time Remaining Register (RD)
XX0C	0	0	1	1	0	0	BC Time Remaining to Next Message Register (RD)
XX0D	0	0	1	1	0	1	Non-Enhanced BC Frame Time / Enhanced BC Initial Instruction Pointer / RT Last Command / MT Trigger Word Register (RD/WR)
XX0E	0	0	1	1	1	0	RT Status Word Register (RD)
XX0F	0	0	1	1	1	1	RT BIT Word Register (RD)
XX10	0	1	0	0	0	0	Test Mode Register 0
XX11	0	1	0	0	0	1	Test Mode Register 1

Table 2. Address Mapping							
Address	**Address Bits**						**Register Description/Accessibility**
HEX	**A5**	**A4**	**A3**	**A2**	**A1**	**A0**	
XX12	0	1	0	0	1	0	Test Mode Register 2
XX13	0	1	0	0	1	1	Test Mode Register 3
XX14	0	1	0	1	0	0	Test Mode Register 4
XX15	0	1	0	1	0	1	Test Mode Register 5
XX16	0	1	0	1	1	0	Test Mode Register 6
XX17	0	1	0	1	1	1	Test Mode Register 7
XX18	0	1	1	0	0	0	Configuration Register #6 (RD/WR)
XX19	0	1	1	0	0	1	Configuration Register #7 (RD/WR)
XX1A	0	1	1	0	1	0	Reserved
XX1B	0	1	1	0	1	1	BC Condition Code Register (RD)
XX1B	0	1	1	0	1	1	BC General Purpose Flag Register(WR)
XX1C	0	1	1	1	0	0	BIT Test Status Register (RD)
XX1D	0	1	1	1	0	1	Interrupt Mask Register #2 (RD/WR)
XX1E	0	1	1	1	1	0	Interrupt Status Register #2 (RD)
XX1F	0	1	1	1	1	1	BC General Purpose Queue Pointer / RT-MT Interrupt Status Queue Pointer Register (RD/WR)
XX20 - XX24							Address 100000 to 100100 are Reserved
XX25	1	0	0	1	0	1	Auto Configuration Control Word (RD)
XX26	1	0	0	1	1	0	Auto Configuration Check Sum Value (RD)
XX27	1	0	0	1	1	1	Auto Configuration I2C EEPROM Pointer (RD)
XX28 - XX2E							Address 101000 to 101110 are Reserved
XX2F	1	0	1	1	1	1	I2C EEPROM Write Data (RD/WR)
XX30	1	1	0	0	0	0	I2C EEPROM Address (RD/WR)
XX31	1	1	0	0	0	1	I2C EEPROM Control/Status (RD/WR)
XX32	1	1	0	0	1	0	I2C EEPROM Read Data (RD)
XX33 - XXFF							Address 110011 to 111111 are Reserved

Table 3. Interrupt Mask Register #1 (Read/Write 00H)	
BIT	**Description**
15 (MSB)	RESERVED
14	RAM Parity Error
13	BC/RT Transmitter Timeout
12	BC/RT Command Stack Rollover
11	MT Command Stack Rollover
10	MT Data Stack Rollover
9	Handshake Fail
8	BC Retry (Note 1)
7	RT Address Parity Error
6	Time Tag Rollover
5	RT Circular Buffer Rollover
4	BC Control Word/RT Subaddress Control Word EOM
3	BC End of Frame (Note 1)
2	Format Error
1	BC Status Set/RT Mode Code/MT Pattern Trigger
0 (LSB)	End of Message

Note 1: This bit is not applicable for the BU-67753LC and BU-67743LC

Table 4. Configuration Register #1 (Read/Write 01H)				
BIT	**BC Function (Bits 11-0 Enhanced Mode Only)**	**RT Without Alternate Status**	**RT With Alternate Status (Enhanced Only)**	**Monitor Function (Enhanced Mode Only BITS 12-0)**
15 (MSB)	RT/ $\overline{\text{BC-MT}}$ (logic 0)	(logic 1)	(logic 1)	(logic 0)
14	MT/ $\overline{\text{BC-RT}}$ (logic 0)	(logic 0)	(logic 0)	(logic 1)
13	Current Area B/ $\overline{\text{A}}$	Current Area B/ $\overline{\text{A}}$	Current Area B/ $\overline{\text{A}}$	Current Area B/ $\overline{\text{A}}$
12	Message Stop-On-Error	Message Monitor Enabled (MMT)	Message Monitor Enabled	Message Monitor Enabled
11	Frame Stop-On-Error	$\overline{\text{Dynamic Bus Control}}$ $\overline{\text{Acceptance}}$	S10	Trigger Word Enabled
10	Status Set Stop-On-Message	$\overline{\text{BUSY}}$	S09	Start-On-Trigger
9	Status Set Stop-On-Frame	$\overline{\text{SERVICE REQUEST}}$	S08	Stop-On-Trigger
8	Frame Auto-Repeat	$\overline{\text{SSFLAG}}$	S07	Not Used
7	External Trigger Enabled	$\overline{\text{RT FLAG}}$ (Enhanced Mode Only)	S06	External Trigger Enabled
6	Internal Trigger Enabled	Not Used	S05	Not Used
5	Intermessage Gap Timer Enabled	Not Used	S04	Not Used
4	Retry Enabled	Not Used	S03	Not Used
3	Doubled / $\overline{\text{Single}}$ Retry	Note Used	S02	Not Used
2	BC Enabled (Read Only)	Not Used	S01	Monitor Enabled (Read Only)
1	BC Frame In Progress (Read Only)	Not Used	S00	Monitor Triggered (Read Only)
0 (LSB)	BC Message In Progress (Read Only)	RT Message In Progress (Enhanced mode only, Read Only)	RT Message in Progress (Read Only)	Monitor Active (Read Only)

Table 5. Configuration Register #2 (Read/Write 02H)	
BIT	**Description**
15 (MSB)	Enhanced Interrupts
14	RAM Parity Enable (Note 2)
13	Busy Lookup Table Enable
12	RX SA Double Buffer Enable
11	Overwrite Invalid Data
10	256-Word Boundary Disable
9	Time Tag Resolution 2
8	Time Tag Resolution 1
7	Time Tag Resolution 0
6	Clear Time Tag on Synchronize
5	Load Time Tag on Synchronize
4	Interrupt Status Auto Clear
3	Level / $\overline{\text{Pulse}}$ Interrupt Request
2	Clear Service Request
1	Enhanced RT Memory Management
0 (LSB)	Separate Broadcast Data

Note 1: This bit is not applicable for the BU-67753LC and BU-67743LC
Note 2: This bit is not applicable for the BU-67743LCt

Table 6. Start/Reset Register (Write 03H)	
BIT	**Description**
15 (MSB)	Reserved
14	Reserved
13	Reserved
12	Reserved
11	Clear RT Halt (Note 2)
10	Clear Self-Test Register (Note 2)
9	Initiate RAM Self-Test (Note 2)
8	Reserved
7	Initiate Protocol Self-Test (Note 2)
6	BC/MT Stop-On-Message (Note 1)
5	BC Stop-On-Frame (Note 1)
4	Time Tag Test Clock
3	Time Tag Reset
2	Interrupt Reset
1	BC/MT Start (Note 2)
0 (LSB)	Reset

Table 7. BC/RT Command Stack Pointer Reg.(Read 03H)	
BIT	**Description**
15 (MSB)	Command Stack Pointer 15
•	•
•	•
•	•
0 (LSB)	Command Stack Pointer 0

Table 8. BC Control Word Register (Read/Write 04H) (Note 1)	
BIT	**Description**
15 (MSB)	Transmit Time Tag for Synchronize Mode Command
14	Message Error Mask
13	Service Request Bit Mask
12	Busy Bit Mask
11	Subsystem Flag Bit Mask
10	Terminal Flag Bit Mask
9	Reserved Bits Mask
8	Retry Enabled
7	Bus Channel A/ $\overline{B}$
6	Off-Line Self-Test
5	Mask Broadcast Bit
4	EOM Interrupt Enable
3	1553A/B Select
2	Mode Code Format
1	Broadcast Format
0 (LSB)	RT-to-RT Format

Note 1: This Table is not applicable for the BU-67753LC and BU-67743LC

Table 9. RT Subaddress Control Word (Read/Write 04H)	
BIT	**Description**
5	RX: Memory Management 0 (MM0)
4	BCST: EOM INT
3	BCST: CIRC BUF INT
2	BCST: Memory Management 2 (MM2)
1	BCST: Memory Management 1 (MM1)
0 (LSB)	BCSTL Memory Management 0 (MM0)

Table 10. Time Tag Register. (Read/Write 05H)	
BIT	**Description**
15 (MSB)	Time Tag 15
•	•
•	•
•	•
0 (LSB)	Time Tag 0

Table 9. RT Subaddress Control Word (Read/Write 04H)	
BIT	**Description**
15 (MSB)	RX: Double/Global Buffer Enable
14	TX: EOM INT
13	TX: CIRC BUF INT
12	TX: Memory Management 2 (MM2)
11	TX: Memory Management 1 (MM1)
10	TX: Memory Management 0 (MM0)
9	RX: EOM INT
8	RX: CIRC BUF INT
7	RX: Memory Management 2 (MM2)
6	RX: Memory Management 1 (MM1)

Table 11. Interrupt Status Register #1 (Read 06H)

BIT	Description
15 (MSB)	Master Interrupt
14	RAM Parity Error (Note 2)
13	Transmitter Timeout
12	BC/RT Command Stack Rollover
11	MT Command Stack Rollover (Note 2)
10	MT Data Stack Rollover (Note 2)
9	Reserved
8	BC Retry (Note 1)
7	RT Address Parity Error
6	Time Tag Rollover
5	RT Circular Buffer Rollover
4	BC Control Word / RT Subaddress Control Word EOM
3	BC End of Frame (Note 1)
2	Format Error
1	BC Status Set / RT Mode Code / MT Pattern Trigger
0 (LSB)	End of Message

Table 12. Configuration Register #3 (Read/Write 07H)

BIT	Description
15 (MSB)	Enhanced Mode Enable
14	BC/RT Command Stack Size 1
13	BC/RT Command Stack Size 0
12	MT Command Stack Size 1 (Note 2)
11	MT Command Stack Size 0 (Note 2)
10	MT Data Stack Size 2 (Note 2)
9	MT Data Stack Size 1 (Note 2)
8	MT Data Stack Size 0 (Note 2)
7	Illegalization Disabled
6	Override Mode T/$\overline{R}$ Error
5	Alternate Status Word Enable
4	Illegal Rx Transfer Disable
3	Busy RX Transfer Disable
2	$\overline{\text{RTFAIL}}$ / $\overline{\text{RTFLAG}}$ Wrap Enable
1	1553A Mode Codes Enable
0 (LSB)	Enhanced Mode Code Handling

Note 1: This bit is not applicable for the BU-67753LC and BU-67743LC
Note 2: This bit is not applicable for the BU-67743LC

Table 13. Configuration Register #4 (Read/Write 08H)

BIT	Description
15 (MSB)	External Bit Word Enable
14	Inhibit Bit Word If Busy
13	Mode Command Override Busy
12	Expanded BC Control Word Enable (Note 1)
11	Broadcast Mask ENA/XOR
10	Retry If –A and M.E.
9	Retry if Status Set
8	1st Retry ALT/ $\overline{\text{SAME}}$ Bus
7	2nd Retry ALT/ $\overline{\text{SAME}}$ Bus
6	Valid M.E./No Data
5	Valid Busy/No Data
4	MT Tag Gap Option (Note 2)
3	Latch RT Address with Config #5
2	Test Mode 2
1	Test Mode 1
0 (LSB)	Test Mode 0

Note 1: This bit is not applicable for the BU-67753LC and BU-67743LC

Note 2: This bit is not applicable for the BU-67743LC

Table 14. Configuration Register #5 (Read/Write 09H)

BIT	Description
15 (MSB)	Reserved
14	Reserved
13	External TX Inhibit A
12	External TX Inhibit B
11	Expanded Crossing Enabled
10	Response Timeout Select 1
9	Response Time out Select 0
8	Gap Check Enabled
7	Broadcast Disabled
6	RT Address Latch/ $\overline{\text{Transparent}}$
5	RT Address 4
4	RT Address 3
3	RT Address 2
2	RT Address 1
1	RT Address 0
0 (LSB)	RT Address Parity

Table 15. RT/Monitor Data Stack Address Register (Read/Write 0AH)

BIT	Description
15 (MSB)	RT / Monitor Data Stack Address 15
•	•
•	•
•	•
0 (LSB)	RT / Monitor Data Stack Address 0

Table 16. BC Frame Time Remaining Register (Read/Write 0BH) (Note 1)	
BIT	**Description**
15 (MSB)	BC Frame Time Remaining 15
•	•
•	•
•	•
0 (LSB)	BC Frame Time Remaining 0

Note: resolution = 100 µs per LSB

Table 17. BC Frame Time Remaining Register (Read/Write 0CH) (Note 1)	
BIT	**Description**
15 (MSB)	BC Frame Time Remaining 15
•	•
•	•
•	•
0 (LSB)	BC Frame Time Remaining 0

Note: resolution = 100 µs per LSB

Table 18. BC Frame Time/RT Last Command/MT Trigger Register (Read/Write 0DH)	
BIT	**Description**
15 (MSB)	BIT 15
•	•
•	•
•	•
0 (LSB)	BIT 0

Table 19. RT Status Word Register (Read/Write 0EH)	
BIT	**Description**
15 (MSB)	Logic “0”
14	Logic “0”
13	Logic “0”
12	Logic “0”
11	Logic “0”
10	Message Error
9	Instrumentation
8	Service Request
7	Reserved
6	Reserved
5	Reserved
4	Broadcast Command Received
3	Busy
2	SSFLAG
1	Dynamic Bus Control Accept
0 (LSB)	Terminal Flag

Note 1: This Table is not applicable for the BU-67753LC and BU-67743LC

Table 20. RT BIT Word Register (Read/Write 0FH)	
BIT	**Description**
15 (MSB)	Transmitter Timeout
14	Loop Test Failure B
13	Loop Test Failure A
12	Handshake Failure
11	Transmitter Shutdown B
10	Transmitter Shutdown A
9	Terminal Flag Inhibited
8	Reserved
7	High Word Count
6	Low Word Count
5	Incorrect Sync Received
4	Parity/Manchester Error Received
3	RT-to-RT Gap / Sync / Address Error
2	RT-to-RT No Response Error
1	RT-to-RT 2nd Command Word Error
0 (LSB)	Command Word Contents Error

Table 21. Configuration Register #6 (Read/Write 18H)	
BIT	**Description**
15 (MSB)	Enhanced Bus Controller (Note 1)
14	Reserved
13	Command Stack Pointer Increment on EOM (RT, MT)
12	Global Circular Buffer Enable
11	Global Circular Buffer Size 2
10	Global Circular Buffer Size 1
9	Global Circular Buffer Size 0
8	Disable Invalid Messages to Interrupt Status Queue
7	Disable Valid Messages to Interrupt Status Queue
6	Interrupt Status Queue Enable
5	RT Address Source
4	Enhanced Message Monitor
3	Reserved
2	64-Word Register Space
1	Reserved
0 (LSB)	Reserved

Note 1: This bit is not applicable for the BU-67753LC and BU-67743LC

Table 22. Configuration Register #7 (Read/Write 19H)	
BIT	**Description**
15 (MSB)	Memory Management Base Address 15 (Note 3)
14	Memory Management Base Address 14 (Note 3)
13	Memory Management Base Address 13 (Note 3)
12	Memory Management Base Address 12 (Note 3)
11	Memory Management Base Address 11 (Note 3)
10	Memory Management Base Address 10 (Note 3)
9	Reserved
8	Reserved
7	Reserved
6	Reserved
5	Reserved
4	RT Halt Enable (Note 3)
3	1553B Response Time
2	Enhanced Time Tag Synchronize
1	Enhanced BC Watchdog Timer Enabled (Note 1)
0 (LSB)	Mode Code Reset / INCMD Select

Note 1: This bit is not applicable for the BU-67753LC and BU-67743LC

Table 23. BC Condition Register (Read 1BH) (Note 2)	
BIT	**Description**
15 (MSB)	Logic “1”
14	Retry 1
13	Retry 0
12	Bad Message
11	Message Status Set
10	Good Block Transfer
9	Format Error
8	No Response
7	General Purpose Flag 7
6	General Purpose Flag 6
5	General Purpose Flag 5
4	General Purpose Flag 4
3	General Purpose Flag 3
2	General Purpose Flag 2
1	Equal Flag / General Purpose Flag 1
0 (LSB)	Less Than Flag / General Purpose Flag 1

Note 1: If the Nano-ACE is not online in enhanced BC mode (i.e., processing instructions), the BC condition code register will always return a value of 0000.

Note 2: This Table is not applicable for the BU-67753LC and BU-67743LC

Note 3: This bit is not applicable for the BU-67743LC

Table 24. BC General Purpose Flag Register (Write 1BH) (Note 1)

BIT	Description
15 (MSB)	Clear General Purpose Flag 7
14	Clear General Purpose Flag 6
13	Clear General Purpose Flag 5
12	Clear General Purpose Flag 4
11	Clear General Purpose Flag 3
10	Clear General Purpose Flag 2
9	Clear General Purpose Flag 1
8	Clear General Purpose Flag 0
7	Set General Purpose Flag 7
6	Set General Purpose Flag 6
5	Set General Purpose Flag 5
4	Set General Purpose Flag 4
3	Set General Purpose Flag 3
2	Set General Purpose Flag 2
1	Set General Purpose Flag 1
0 (LSB)	Set General Purpose Flag 0

Note 1: This Table is not applicable for the BU-67753LC and BU-67743LC

Table 25. BIT Test Status Flag Register (Read 1CH) (Note 2)

BIT	Description
15 (MSB)	Protocol Built-In Test Complete
14	Protocol Built-In Test In-Progress
13	Protocol Built-In Test Passed
12	CPU Write Abort
11	Auto-Initialization Complete
10	Auto-Initialization In-Progress
9	Auto-Initialization Passed
8	CPU Write Abort during Auto-Initialization
7	RAM Built-In Test Complete
6	RAM Built-In Test In-Progress
5	RAM Built-In Test In-Passed
4	CPU Write Abort during Built-in RAM Test
3	Model ID bit 3
2	Model ID bit 2
1	Model ID bit 1
0 (LSB)	Model ID bit 0

Note 2: This Table is not applicable for the BU-67743LC

Table 26. Interrupt Mask Register #2 (Read/Write 1DH)	
BIT	**Description**
15 (MSB)	Not Used
14	BC Op Code Parity Error (Note 1)
13	RT Illegal Command/Message MT Message Received
12	General Purpose Queue / Interrupt Status Queue Rollover
11	Call Stack Pointer Register Error
10	BC Trap Op Code (Note 1)
9	RT Command Stack 50% Rollover
8	RT Circular Buffer 50% Rollover
7	Monitor Command Stack 50% Rollover
6	Monitor Data Stack 50% Rollover
5	Enhanced BC IRQ3 (Note 1)
4	Enhanced BC IRQ2 (Note 1)
3	Enhanced BC IRQ1 (Note 1)
2	Enhanced BC IRQ0 (Note 1)
1	Bit Test Complete (Note 2)
0 (LSB)	Not Used

Note 1: This bit is not applicable for the BU-67753LC and BU-67743LC
Note 2: This bit is not applicable for the BU-67743LC

Table 27. Interrupt Status Register #2 (Read 1EH)	
BIT	**Description**
15 (MSB)	Master Interrupt
14	BC Op Code Parity Error (Note 1)
13	General Purpose Queue / RT Illegal Command/Message MT Message Received
12	Interrupt Status Queue Rollover
11	Call Stack Pointer Register Error
10	BC Trap Op Code (Note 1)
9	RT Command Stack 50% Rollover
8	RT Circular Buffer 50% Rollover
7	Monitor Command Stack 50% Rollover (Note 2)
6	Monitor Data Stack 50% Rollover (Note 2)
5	Enhanced BC IRQ3 (Note 1)
4	Enhanced BC IRQ2 (Note 1)
3	Enhanced BC IRQ1 (Note 1)
2	Enhanced BC IRQ0 (Note 1)
1	Bit Test Complete (Note 2)
0 (LSB)	Interrupt Chain Bit

Table 28. RT, MT Interrupt Status Queue Pointer Register (Read/Write 1FH)	
BIT	**Description**
15 (MSB)	Queue Pointer Base Address 15
14	Queue Pointer Base Address 14
13	Queue Pointer Base Address 13
12	Queue Pointer Base Address 12
11	Queue Pointer Base Address 11
10	Queue Pointer Base Address 10
9	Queue Pointer Base Address 9
8	Queue Pointer Base Address 8
7	Queue Pointer Base Address 7
6	Queue Pointer Base Address 6
5	Queue Pointer Address 5
4	Queue Pointer Address 4
3	Queue Pointer Address 3
2	Queue Pointer Address 2
1	Queue Pointer Address 1
0 (LSB)	Queue Pointer Address 0

Note: Table 29 to Table 35 are not Registers, but they are words stored in RAM.

Table 29. BC Mode Block Status Word (Note 1)	
BIT	**Description**
15 (MSB)	EOM
14	SOM
13	Channel B/ $\overline{A}$
12	Error Flag
11	Status Set
10	Format Error
9	No Response Timeout
8	Loop Test Fail
7	Masked Status Set
6	Retry Count 1
5	Retry Count 0
4	Good Data Block Transfer
3	Wrong Status Address / No Gap
2	Word Count Error
1	Incorrect Sync Type
0 (LSB)	Invalid Word

Note 1: This Table is not applicable for the BU-67753LC and BU-67743LC

Table 30. RT Mode Block Status Word	
BIT	**Description**
15 (MSB)	EOM
14	SOM
13	Channel B/ $\overline{A}$
12	Error Flag
11	RT-to-RT Format
10	Format Error
9	No Response Timeout
8	Loop Test Fail
7	Data Stack Rollover
6	Illegal Command Word
5	Word Count Error
4	Incorrect Data Sync
3	Invalid Word
2	RT-to-RT Gap / Sync / Address Error
1	RT-to-RT 2nd Command Error
0 (LSB)	Command Word Contents Error

Table 31. 1553 Command Word	
BIT	**Description**
15 (MSB)	Remote Terminal Address BIT 4
14	Remote Terminal Address BIT 3
13	Remote Terminal Address BIT 2
12	Remote Terminal Address BIT 1
11	Remote Terminal Address BIT 0
10	Transmit / $\overline{\text{Receive}}$
9	Subaddress / Mode Code BIT 4
8	Subaddress / Mode Code BIT 3
7	Subaddress / Mode Code BIT 2
6	Subaddress / Mode Code BIT 1
5	Subaddress / Mode Code BIT 0
4	Data Word Count / Mode Code Bit 4
3	Data Word Count / Mode Code Bit 3
2	Data Word Count / Mode Code Bit 2
1	Data Word Count / Mode Code Bit 1
0 (LSB)	Data Word Count / Mode Code Bit 0

Table 32. Word Monitor Identification Word (Note 1)	
BIT	**Description**
15 (MSB)	Gap Time (MSB)
•	•
•	•
•	•
8	Gap Time (LSB)
7	Word Flag
6	$\overline{\text{This}}$ $\overline{\text{RT}}$
5	$\overline{\text{Broadcast}}$
4	Error
3	Command / $\overline{\text{Data}}$
2	Channel B/ $\overline{\text{A}}$
1	Contiguous Data / $\overline{\text{Gap}}$
0 (LSB)	$\overline{\text{Mode\_Code}}$

Note 1: This Table is not applicable for the BU-67743LC

Table 33. Message Monitor Mode Block Status Word (Note 1)	
BIT	**Description**
15 (MSB)	EOM
14	SOM
13	Channel B/ $\overline{\text{A}}$
12	Error Flag
11	RT-to-RT Transfer
10	Format Error
9	No Response Timeout
8	Good Data Block Transfer
7	Data Stack Rollover
6	Reserved
5	Word Count Error
4	Incorrect Sync
3	Invalid Word
2	RT-to-RT Gap / Sync / Address Error
1	RT-to-RT 2nd Command Error
0 (LSB)	Command Word Contents Error

Table 34. RT/Monitor Interrupt Status Word (For Interrupt Status Queue)

BIT	Definition for Message Interrupt Event	Definition for Non-Message Interrupt Event
15	Transmitter Timeout	Not Used
14	Illegal Command	Not Used
13	Monitor Data Stack 50% Rollover	Not Used
12	Monitor Data Stack Rollover	Not Used
11	RT Circular Buffer 50% Rollover	Not Used
10	RT Circular Buffer Rollover	Not Used
9	Monitor Command (Descriptor) Stack 50% Rollover	Not Used
8	Monitor Command (Descriptor) Stack Rollover	Not Used
7	RT Command (Descriptor) Stack 50% Rollover	Not Used
6	RT Command (Descriptor) Stack Rollover	Not Used
5	Handshake Fail	Not Used
4	Format Error	Time Tag Rollover
3	Mode Code Interrupt	RT Address Parity Error
2	Subaddress Control Word EOM	Reserved
1	End-Of-Message (EOM)	RAM Parity Error
0	“1” For Message Interrupt Event “0” For Non-Message Interrupt Event	

Table 35. 1553B Status Word

BIT	Description
15 (MSB)	Remote Terminal Address BIT 4
14	Remote Terminal Address BIT 3
13	Remote Terminal Address BIT 2
12	Remote Terminal Address BIT 1
11	Remote Terminal Address BIT 0
10	Message Error
9	Instrumentation
8	Service Request
7	Reserved
6	Reserved
5	Reserved
4	Broadcast Command Received
3	Busy
2	SSFLAG
1	Dynamic Bus Control Acceptance
0 (LSB)	Terminal Flag

Table 36. I2C EEPROM Write Data (2FH) (Note 1)	
BIT	**Description**
15 (MSB)	D15
14	D14
13	D13
12	D12
11	D11
10	D10
9	D9
8	D8
7	D7
6	D6
5	D5
4	D4
3	D3
2	D2
1	D1
0 (LSB)	D0

Table 37. I2C EEPROM Address (30H) (Note 1)	
BIT	**Description**
15 (MSB)	Not used
14	A14
13	A13
12	A12
11	A11
10	A10
9	A9
8	A8
7	A7
6	A6
5	A5
4	A4

Table 37. I2C EEPROM Address (30H) (Note 1)	
BIT	**Description**
3	A3
2	A2
1	A1
0 (LSB)	A0

Table 38. I2C EEPROM Status (31H) (Read) (Note 1)	
BIT	**Description**
15 (MSB)	I2C EEPROM Idle
14	I2C EEPROM Code bit 2
13	I2C EEPROM Code bit 1
12	I2C EEPROM Code bit 0
11	I2C EEPROM Operation Complete (Host)
10	I2C EEPROM Operation Active (Host)
9	I2CEEPROM Operation bit 1
8	I2C EEPROM Operation bit 0
7	I2C EEPROM Error 1
6	I2C EEPEOM Error 2
5	Boot Active
4	Boot Code bit 3
3	Boot Code Bit 2
2	Boot Code bit 1
1	Boot Code bit 0
0 (LSB)	I2C EEPROM Address MSB bit

Note 1: This Table is not applicable for the BU-67743LC

Table 39. I2C EEPROM Control (31H) (Write) (Note 1)	
BIT	**Description**
15 (MSB)	Not Used
14	Not Used
13	Not Used
12	Not Used
11	Not Used
10	Not Used
9	Not Used
8	Not Used
7	Not Used
6	Not Used)
5	Not Used
4	I2C EEPROM Address MSB bit
3	Clears I2C EEPROM Status flags
2	Starts a Read from I2C EEPROM
1	Starts a Write to I2C EEPROM
0 (LSB)	I2C EEPROM Soft Reset

Note 1: This Table is not applicable for the BU-67743LC

Table 40. I2C EEPROM Read Data (32H) (Note 1)	
BIT	**Description**
15 (MSB)	D15
14	D14
13	D13
12	D12
11	D11
10	D10
9	D9
8	D8
7	D7
6	D6
5	D5
4	D4
3	D3
2	D2
1	D1
0 (LSB)	D0

4 NON-TEST REGISTER FUNCTION SUMMARY

A summary of the Nano-ACE®'s 24 non-test registers follows.

4.1 Interrupt Mask Registers #1 and #2

Interrupt Mask Registers #1 and #2 are used to enable and disable interrupt requests for various events and conditions.

4.2 Configuration Registers #1 and #2

Configuration Registers #1 and #2 are used to select the Nano-ACE's mode of operation, and for software control of RT Status Word bits, Active Memory Area, BC Stop-On-Error, RT Memory Management mode selection, and control of the Time Tag operation.

4.3 Start/Reset Register

The Start/Reset Register is used for "command" type functions such as software reset, BC/MT Start, Interrupt reset, Time Tag Reset, Time Tag Register Test, Initiate protocol self-test, Initiate RAM self-test, Clear self-test register, and Clear RT Halt. The Start/Reset Register also includes provisions for stopping the BC in its auto-repeat mode, either at the end of the current message or at the end of the current BC frame.

4.4 BC/RT Command Stack Register

The BC/RT Command Stack Register allows the host CPU to determine the pointer location for the current or most recent message.

4.5 BC Instruction List Pointer Register

The BC Instruction List Pointer Register may be read to determine the current location of the Instruction List Pointer for the Enhanced BC mode.

4.6 BC Control Word/RT Subaddress Control Word Register

In BC mode, the BC Control Word/RT Subaddress Control Word Register allows host access to the current word or most recent BC Control Word. The BC Control Word contains bits that select the active bus and message format, enable off-line self-test, masking of Status Word bits, enable retries and interrupts, and specify MIL-STD-1553A or -1553B error handling. In RT mode, this register allows host access to the current or most recent Subaddress Control Word. The Subaddress Control Word is

used to select the memory management scheme and enable interrupts for the current message.

4.7 Time Tag Register

The Time Tag Register maintains the value of a real-time clock. The resolution of this register is programmable from among 2, 4, 8, 16, 32, and 64 µs/LSB. The Start-of-Message (SOM) and End-of-Message (EOM) sequences in RT, and Message Monitor modes cause a write of the current value of the Time Tag Register to the stack area of the RAM.

4.8 Interrupt Status Registers #1 and #2

Interrupt Status Registers #1 and #2 allow the host processor to determine the cause of an interrupt request by means of one or two read accesses. The interrupt events of the two Interrupt Status Registers are mapped to correspond to the respective bit positions in the two Interrupt Mask Registers. Interrupt Status Register #2 contains an INTERRUPT CHAIN bit, used to indicate an interrupt event from Interrupt Status Register #1.

4.9 Configuration Registers #3, #4, and #5

Configuration Registers #3, #4, and #5 are used to enable many of the Nano-ACE®'s advanced features that were not implemented by the prior generation products, the ACE and Mini-ACE (Plus). For BC, RT, and MT modes, use of the Enhanced Mode enables the various read-only bits in Configuration Register #1. For BC mode, Enhanced Mode features include the expanded BC Control Word and BC Block Status Word, additional Stop-On-Error and Stop-On-Status Set functions, frame auto-repeat, programmable intermessage gap times, automatic retries, expanded Status Word Masking, and the capability to generate interrupts following the completion of any selected message. For RT mode, the Enhanced Mode features include the expanded RT Block Status Word, combined RT/Selective Message Monitor mode, automatic setting of the TERMINAL FLAG Status Word bit following a loop test failure; the double buffering scheme for individual receive (broadcast) subaddresses, and the alternate (fully software programmable) RT Status Word. For MT mode, use of the Enhanced Mode enables the Selective Message Monitor, the combined RT/Selective Monitor modes, and the monitor triggering capability.

4.10 RT/Monitor Data Stack Address Register

The RT/Monitor Data Stack Address Register provides a read/writable indication of the last data word stored for RT or Monitor modes.

4.11 BC Frame Time Remaining Register

The BC Frame Time Remaining Register provides a read-only indication of the time remaining in the current BC frame. In the enhanced BC mode, this timer may be used for minor or major frame control, or as a watchdog timer for the BC message sequence control processor. The resolution of this register is 100 μs/LSB.

4.12 BC Time Remaining to Next Message Register

The BC Time Remaining to Next Message Register provides a read-only indication of the time remaining before the start of the next message in a BC frame. In the enhanced BC mode, this timer may also be used for the BC message sequence control processor's Delay (DLY) instruction, or for minor or major frame control. The resolution of this register is 1 μs/LSB.

4.13 BC Frame Time / RT Last Command / MT Trigger Word Register

In BC mode, this register is used to program the BC frame time, for use in the frame auto-repeat mode. The resolution of this register is 100 μs/LSB, with a range up to 6.55 seconds. In RT mode, this register stores the current (or most previous) 1553 Command Word processed by the Nano-ACE RT. In the Word Monitor mode, this register is used to specify a 16-bit Trigger (Command) Word. The Trigger Word may be used to start or stop the monitor, or to generate interrupts.

4.14 BC Initial Instruction List Point Register

The BC Initial Instruction List Pointer Register enables the host to assign the starting address for the enhanced BC Instruction List.

4.15 RT Status Word Register and BIT Word Registers

The RT Status Word Register and BIT Word Registers provide read-only indications of the RT Status and BIT Words.

4.16 Configuration Registers #6 and #7

Configuration Registers #6 and #7 are used to enable the Nano-ACE features that extend beyond the architecture of the ACE/Mini-ACE (Plus). These include the Enhanced BC mode; RT Global Circular Buffer (including buffer size); the RT/MT Interrupt Status Queue, including valid/invalid message filtering; enabling a software-assigned RT address; LSB filtering for the Synchronize (with data) time tag operations; and enabling a watchdog timer for the Enhanced BC message sequence control engine.

4.17 BC Condition Code Register

The BC Condition Code Register is used to enable the host processor to read the current value of the Enhanced BC Message Sequence Control Engine's condition flags.

4.18 BC General Purpose Flag Register

The BC General Purpose Flag Register allows the host processor to be able to set, clear, or toggle any of the Enhanced BC Message Sequence Control Engine's General Purpose condition flags.

4.19 BIT Test Status Register

The BIT Test Status Register is used to provide read-only access to the status of the protocol, RAM built-in self-tests (BIT) and Auto-initialization

4.20 BC General Purpose Queue Pointer

The BC General Purpose Queue Pointer provides a means for initializing the pointer for the General Purpose Queue, for the Enhanced BC mode. In addition, this register enables the host to determine the current location of the General Purpose Queue pointer, which is incremented internally by the Enhanced BC message sequence control engine.

4.21 RT/MT Interrupt Status Queue Pointer

The RT/MT Interrupt Status Queue Pointer provides a means for initializing the pointer for the Interrupt Status Queue, for RT, MT, and RT/MT modes. In addition, this register enables the host to determine the current location of the Interrupt Status Queue pointer, which is incremented by the RT/MT message processor.

4.22 Auto Initialization Debug Registers

The read only, Auto-Initialization debug registers provides the user a way to monitor the last value of the Control Word read from I2C EEPROM; the present value of the Check Sum calculated for the data read from I2C EEPROM to date and the present value of the I2C EEPROM Address Pointer during development of the Auto-Initialization I2C EEPROM code.

4.23 I2C EEPROM Control/Status Register

In read mode, this register contains the status of the Auto-Initialization at boot up and User operations to the I2C EEPROM during development. In write mode, the user can configures the I2C EEPROM during development of I2C EEPROM code.

4.24 I2C EEPROM Write Data Register

The value written to this register (MSB bit 15) is the word that will be written to the I2C EEPROM when the user initiates the transfer.

4.25 I2C EEPROM Address Register

The value written to this register is the location in I2C EEPROM where data will be read or written to when initiated by the user.

4.26 I2C EEPROM Read Data Register

Used to verify a user write operations to I2C EEPROM. After a write to I2C EEPROM, the location written will be automatically read back and stored in this register. In addition, this register will store the data read from the I2C EEPROM after a user issued read operation from I2C EEPROM.

5 BUS CONTROLLER (BC) ARCHITECTURE

The BC functionality for the Nano-ACE includes two separate architectures: (1) the older, non-Enhanced Mode, which provides complete compatibility with the previous ACE and Mini-ACE (Plus) generation products; and (2) the newer, Enhanced BC mode. The Enhanced BC mode offers several new powerful architectural features. These include the incorporation of a highly autonomous BC message sequence control engine, which greatly serves to offload the operation of the host CPU.

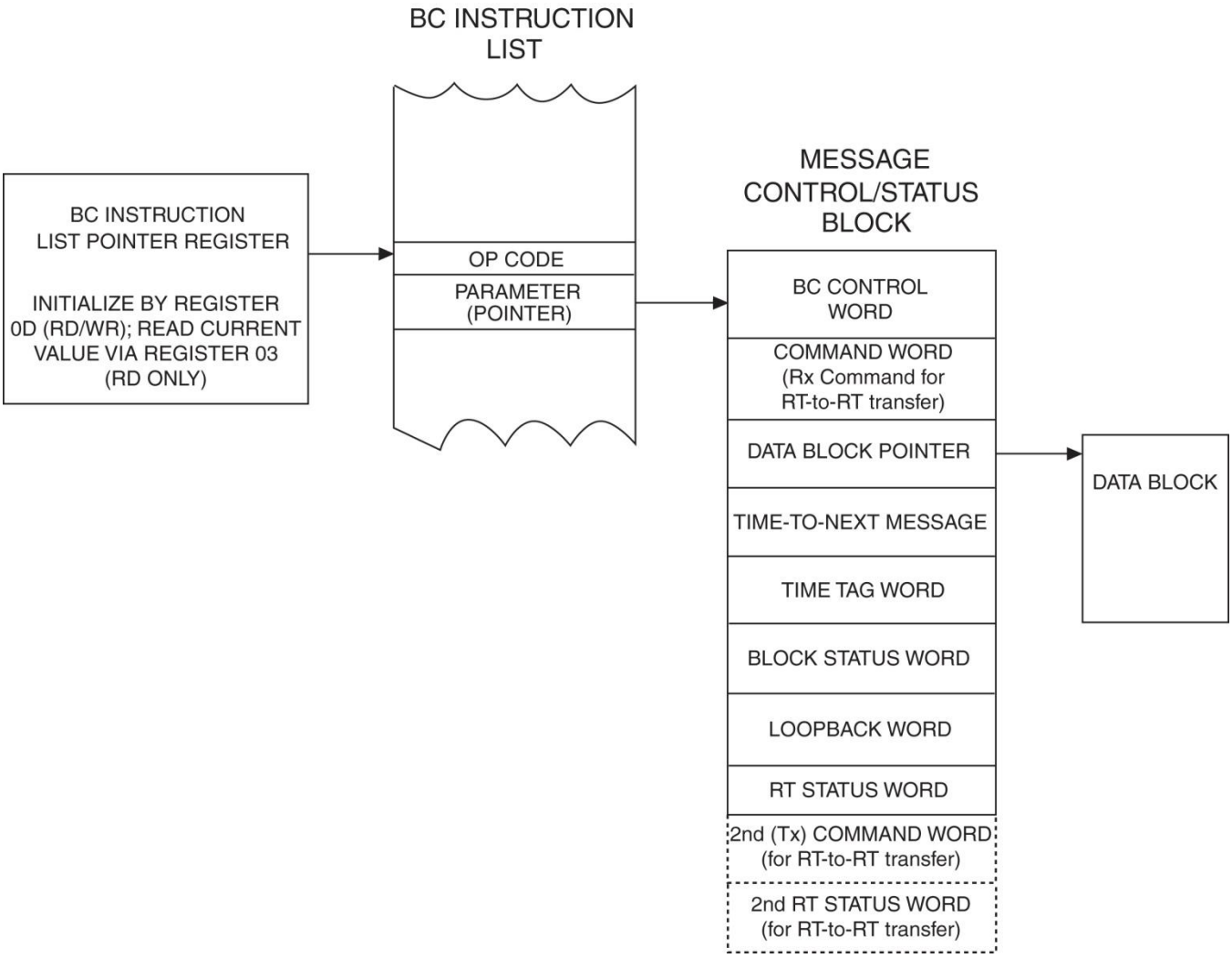


Figure 3. BC Message Sequence Control

The Enhanced BC's message sequence control engine provides a high degree of flexibility for implementing major and minor frame scheduling; capabilities for inserting asynchronous messages in the middle of a frame; to separate 1553 message data from control/status data for the purpose of implementing double buffering and performing bulk data transfers; for implementing message retry

schemes, including the capability for automatic bus channel switchover for failed messages; and for reporting various conditions to the host processor by means of four user defined interrupts and a general purpose queue.

In both the non-Enhanced and Enhanced BC modes, the Nano-ACE BC implements all MIL-STD-1553B message formats. Message format is programmable on a message-by-message basis by means of the BC Control Word and the T/R bit of the Command Word for the respective message. The BC Control Word allows 1553 message format, 1553A/B type RT, bus channel, self-test, and Status Word masking to be specified on an individual message basis. In addition, automatic retries and/or interrupt requests may be enabled or disabled for individual messages. The BC performs all error checking required by MILSTD- 1553B. This includes validation of response time, sync type and sync encoding, Manchester II encoding, parity, bit count, word count, Status Word RT Address field, and various RT-to-RT transfer errors. The Nano-ACE BC response timeout value is programmable with choices of 18, 22, 50, and 130 μs. The longer response timeout values allow for operation over long buses and/ or the use of repeaters.

In its non-Enhanced Mode, the Nano-ACE may be programmed to process BC frames of up to 512 messages with no processor intervention. In the Enhanced BC mode, there is no explicit limit to the number of messages that may be processed in a frame. In both modes, it is possible to program for either single frame or frame auto-repeat operation. In the auto-repeat mode, the frame repetition rate may be controlled either internally, using a programmable BC frame timer, or from an external trigger input.

5.1 Enhanced BC Mode: Message Sequence Control

One of the major new architectural features of the Nano-ACE series is its advanced capability for BC message sequence control. The Nano-ACE supports highly autonomous BC operation, which greatly offloads the operation of the host processor.

The operation of the Nano-ACE's message sequence control engine is illustrated in Figure 3. The BC message sequence control involves an instruction list pointer register; an instruction list, which contains multiple 2-word entries; a message control/status stack, which contains multiple 8-word or 10-word descriptors; and data blocks for individual messages.

The initial value of the instruction list pointer register is initialized by the host processor (via Register 0D), and is incremented by the BC message sequence processor (host readable via Register 03). During operation, the message sequence control processor fetches the operation referenced by the instruction list pointer register from the instruction list.

Note that the pointer parameter referencing the first word of a message's control/status block (the BC Control Word) must contain an address value that is modulo 8. Also, note that if the message is an RT-to-RT transfer, the pointer parameter must contain an address value that is modulo 16.

5.2 OP Codes

The instruction list pointer register references a pair of words in the BC instruction list: an op code word, followed by a parameter word. The format of the op code word, which is illustrated in Figure 4, includes a 5-bit op code field and a 5-bit condition code field. The op code identifies the instruction to be executed by the BC message sequence controller.

Most of the operations are conditional, with execution dependent on the contents of the condition code field. Bits 3-0 of the condition code field identifies a particular condition. Bit 4 of the condition code field identifies the logic sense ("1" or "0") of the selected condition code on which the conditional execution is dependent. Table 36 lists all the op codes, along with their respective mnemonic, code value, parameter, and description. Table 37 defines all the condition codes.

Eight of the condition codes (8 through F) are set or cleared as the result of the most recent message. The other eight are defined as "General Purpose" condition codes GP0 through GP7. There are three mechanisms for programming the values of the General Purpose Condition Code bits: (1) They may be set, cleared, or toggled by the host processor, by means of the BC GENERAL PURPOSE FLAG REGISTER; (2) they may be set, cleared, or toggled by the BC message sequence control processor, by means of the GP Flag Bits (FLG) instruction; and (3) GP0 and GP1 only (but none of the others) may be set or cleared by means of the BC message sequence control processor's Compare Frame Timer (CFT) or Compare Message Timer (CMT) instructions.

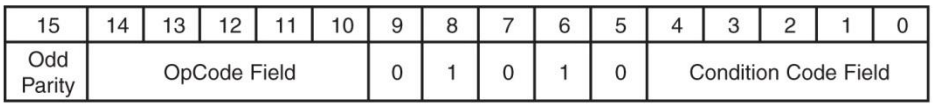


Figure 4. BC OP Code Format

The host processor also has read-only access to the BC condition codes by means of the BC CONDITION CODE REGISTER.

Note that four (4) instructions are unconditional. These are Compare to Frame Timer (CFT), Compare to Message Timer (CMT), GP Flag Bits (FLG), and Execute and Flip

(XQF). For these instructions, the Condition Code Field is "don't care". That is, these instructions are always executed, regardless of the result of the condition code test.

All of the other instructions are conditional. That is, they will only be executed if the condition code specified by the condition code field in the op code word tests true. If the condition code field tests false, the instruction list pointer will skip down to the next instruction.

As shown in Table 36, many of the operations include a single word parameter. For an XEQ (execute message) operation, the parameter is a pointer to the start of the message's Control / Status block. For other operations, the parameter may be an address, a time value, an interrupt pattern, a mechanism to set or clear general purpose flag bits, or an immediate value. For several op codes, the parameter is "don't care" (not used).

As described above, some of the op codes will cause the message sequence control processor to execute messages. In this case, the parameter references the first word of a message Control/Status block. With the exception of RT-to-RT transfer messages, all message status/control blocks are eight words long: a block control word, time-to-next-message parameter, data block pointer, command word, status word, loopback word, block status word, and time tag word.

In the case of an RT-to-RT transfer message, the size of the message control/status block increases to 16 words. However, in this case, the last six words are not used; the ninth and tenth words are for the second command word and second status word.

The third word in the message control/status block is a pointer that references the first word of the message's data word block. Note that the data word block stores only data words, which are to be either transmitted or received by the BC. By segregating data words from command words, status words, and other control and "housekeeping" functions, this architecture enables the use of convenient, usable data structures, such as circular buffers and double buffers.

Other operations support program flow control; i.e., jump and call capability. The call capability includes maintenance of a call stack, which supports a maximum of four (4) entries; there is also a return instruction. In the case of a call stack overrun or under run, the BC will issue a CALL STACK POINTER REGISTER ERROR interrupt, if enabled.

Other op codes may be used to delay for a specified time; start a new BC frame; wait for an external trigger to start a new frame; perform comparisons based on frame time and time-to-next message; load the time tag or frame time registers; halt; and issue host interrupts. In the case of host interrupts, the message control processor

passes a 4-bit user-defined interrupt vector to the host, by means of the Nano-ACE's Interrupt Status Register.

The purpose of the FLG instruction is to enable the message sequence controller to set, clear, or toggle the value(s) of any or all of the eight general purpose condition flags.

The op code parity bit encompasses all sixteen bits of the op code word. This bit must be programmed for odd parity. If the message sequence control processor fetches an undefined op code word, an op code word with even parity, or bits 9-5 of an op code word do not have a binary pattern of 01010, the message sequence control processor will immediately halt the BC's operation. In addition, if enabled, a BC TRAP OP CODE interrupt will be issued. Also, if enabled, a parity error will result in an OP CODE PARITY ERROR interrupt. Table 37 describes the Condition Codes.

Table 36. BC Operations for Message Sequence Control

Instruction	Mnemonic	OP Code (Hex)	Parameter	Conditional or Unconditional	Description
Execute Message	XEQ	0001	Message Control / Status Block Address	Conditional (see Note)	Executes the message at the specified Message Control/Status Block Address if the condition flag tests TRUE, otherwise continue execution at the next OpCode in the instruction list.
Jump	JMP	0002	Instruction List Address	Conditional	Jump to the OpCode specified in the Instruction List if the condition flag test TRUE, otherwise continue execution at the next OpCode in the instruction list.
Subroutine Call	CAL	0003	Instruction List Address	Conditional	Jump to the OpCode specified by the Instruction List Address and push the Address of the Next OpCode on the Call Stack if the condition flag tests TRUE, otherwise continue execution at the next OpCode in the instruction list. Note that the maximum depth of the subroutine call stack is four.
Subroutine Return	RTN	0004	Not Used (Don't Care)	Conditional	Return to the OpCode popped off the Call Stack if the condition flag tests TRUE, otherwise continue execution at the next OpCode in the instruction list.
Interrupt Request	IRQ	0006	Interrupt Bit Pattern in 4 LS bits	Conditional	Generate an interrupt if the condition flag tests TRUE, otherwise continue execution at the next OpCode in the instruction list. The passed parameter (Interrupt Bit Pattern) specifies which of the ENHANCED BC IRQ bit(s) (bits 5-2) will be set in Interrupt Status Register #2. Only the four LSBs of the passed parameter are used. A parameter where the four LSBs are logic "0" will not generate an interrupt.

Table 36. BC Operations for Message Sequence Control					
Instruction	**Mnemonic**	**OP Code (Hex)**	**Parameter**	**Conditional or Unconditional**	**Description**
Halt	HLT	0007	Not Used (Don't Care)	Conditional	Stop execution of the Message Sequence Control Program until a new BC Start is issued by the host if the condition flag tests TRUE, otherwise continue execution at the next OpCode in the instruction list.
Delay	DLY	0008	Delay Time Value (Resolution = 1µs / LSB)	Conditional	Delay the time specified by the Time parameter before executing the next OpCode if the condition flag tests TRUE, otherwise continue execution at the next OpCode without delay. The delay generated will use the Time to Next Message Timer.
Wait Until Frame Timer = 0	WFT	0009	Not Used (Don't Care)	Conditional	Wait until Frame Time counter is equal to Zero before continuing execution of the Message Sequence Control Program if the condition flag tests TRUE, otherwise continue execution at the next OpCode without delay.
Compare to Frame Timer	CFT	000A	Delay Time Value (Resolution = 1µs / LSB)	Unconditional	Compare Time Value to Frame Time Counter. The LT/GP0 and EQ/GP1 flag bits are set or cleared based on the results of the compare. If the value of the CFT's parameter is less than the value of the frame time counter, then the LT/GP0 flag will be set, while the EQ/GP1 flag will be cleared. If the value of the CFT's parameter is equal to the value of the frame time counter, then the EQ/GP1 flag will be set, while the LT/GP0 flag will be cleared. If the value of the CFT's parameter is greater than the current value of the frame time counter, the LT/GP0 and EQ/GP1 flags will be cleared.
Compare to Message Timer	CMT	000B	Delay Time Value (Resolution = 1µs / LSB)	Unconditional	Compare Time Value to Message Time Counter. The LT/GP0 and EQ/GP1 flag bits are set or cleared based on the results of the compare. If the value of the CMT's parameter is less than the value of the message time counter, then the LT/GP0 flag will be set, while the GT-EQ/GP0 and EQ/GP1 flags will be cleared. If the value of the CMT's parameter is equal to the value of the message time counter, then the EQ/GP1 flag will be set, while the LT/GP0 flag will be cleared. If the value of the CMT's parameter is greater than the current value of the message time counter, then the LT/GP0 and EQ/GP1 flags will be cleared.

Table 36. BC Operations for Message Sequence Control

Instruction	Mnemonic	OP Code (Hex)	Parameter	Conditional or Unconditional	Description
GP Flag Bits	FLG	000C	Used to set, clear, or toggle GP (General Purpose) Flag bits (see description)	Unconditional	Used to set, toggle, or clear any or all of the eight general purpose flags. The table below illustrates the use of the GP Flag Bits instruction for the case of GP0 (General Purpose Flag 0). Bits 1 and 9 of the parameter byte affect flag GP1, bits 2 and 10 effect GP2, etc., according to the following rules:

Bit 8	Bit 0	Effect on GP0
0	0	No Change
0	1	Set Flag
1	0	Clear Flag
1	1	Toggle Flag

Load Time Tag Counter	LTT	000D	Time Value Resolution (µs/ LSB) is defined by bits 9, 8, & 7 of Configuration Register #2	Conditional	Load Time Tag Counter with Time Value if the condition flag tests TRUE, otherwise continue execution at the next OpCode in the instruction list.
Load Frame Timer	LFT	000E	Time Value (resolution = 100 µs/LSB)	Conditional	Load Frame Timer Register with the Time Value parameter if the condition flag tests TRUE, otherwise continue execution at the next OpCode in the instruction list.
Start Frame Timer	SFT	000F	Not Used (Don't Care)	Conditional	Start Frame Time Counter with Time Value in Time Frame register if the condition flag tests TRUE, otherwise continue execution at the next OpCode in the instruction list.
Push Time Tag Register	PTT	0010	Not Used (Don't Care)	Conditional	Push the value of the Time Tag Register on the General Purpose Queue if the condition flag tests TRUE, otherwise continue execution at the next OpCode in the instruction list.
Push Block Status Word	PBS	0011	Not Used (Don't Care)	Conditional	Push the Block Status Word for the most recent message on the General Purpose Queue if the condition flag tests TRUE, otherwise continue execution at the next OpCode in the instruction list.
Push Immediate Value	PSI	0012	Immediate Value	Conditional	Push Immediate data on the General Purpose Queue if the condition flag tests TRUE, otherwise continue execution at the next OpCode in the instruction list.
Push Indirect	PSM	0013	Memory Address	Conditional	Push the data stored at the specified memory location on the General Purpose Queue if the condition flag tests TRUE, otherwise continue

Table 36. BC Operations for Message Sequence Control

Instruction	Mnemonic	OP Code (Hex)	Parameter	Conditional or Unconditional	Description
					execution at the next OpCode in the instruction list.
Wait for External Trigger	WTG	0014	Not Used (Don't Care)	Conditional	Wait for a logic "0"-to-logic "1" transition on the EXT_TRIG input signal before proceeding to the next OpCode in the instruction list if the condition flag tests TRUE, otherwise continue execution at the next OpCode without delay.
Execute and Flip	XQF	0015	Message Control / Status Block Address	Unconditional	Execute (unconditionally) the message referenced by the Message Control/Status Block Address. Following the processing of this message, if the condition flag tests TRUE, the BC will toggle bit 4 in the Message Control/Status Block Address, and store the new Message Block Address as the updated value of the parameter following the XQF instruction code. As a result, the next time that this line in the instruction list is executed, the Message Control/Status Block at the updated address (old address XOR 0010h), rather than the old address, will be processed. If the condition flag tests FALSE, the value of the Message Control/Status Block Address parameter will not change.

Note: While the XEQ (Execute Message) instruction is conditional, not all condition codes may be used to enable its use. The ALWAYS and NEVER condition codes may be used. The eight general purpose flag bits, GP0 through GP7, may also be used. However, if GP0 through GP7 are used, it is imperative that the host processor not modify the value of the specific general purpose flag bit that enabled a particular message while that message is being processed. Similarly, the LT, GT-EQ, EQ, and NE flags, which the BC only updates by means of the CFT and CMT instructions, may also be used. However, these two flags are dual use. Therefore, if these are used, it is imperative that the host processor not modify the value of the specific flag (GP0 or GP1) that enabled a particular message while that message is being processed. The NORESP, FMT ERR, GD BLK XFER, MASKED STATUS SET, BAD MESSAGE, RETRY0, and RETRY1 condition codes are not available for use with the XEQ instruction and should not be used to enable its execution

Table 37. BC Condition Codes			
BIT Code	**Name (BIT 4 = 0)**	**Inverse (BIT 4 = 1)**	**Functional Description**
0	LT/GP0	GT-EQ / $\overline{\text{GP0}}$	Less than or GP0 flag. This bit is set or cleared based on the results of the compare. If the value of the CMT's parameter is less than the value of the message time counter, then the LT/GP0 flag will be set. If the value of the CMT's parameter is greater than or equal to the value of the message time counter, then the LT/GP0 flag will be cleared. Also, General Purpose Flag 1 may be set or cleared by a FLG operation.
1	EQ/GP1	NE/ $\overline{\text{GP1}}$	Equal Flag. This bit is set or cleared after CFT or CMT operation. If the value of the CMT's parameter is equal to the value of the message time counter, then the EQ/GP1 flag will be set. If the value of the CMT's parameter is not equal to the value of the message time counter, then the EQ/GP1 flag will be cleared. Also, General Purpose Flag 1 may be set or cleared by a FLG operation.
2	GP2	$\overline{\text{GP2}}$	General Purpose Flags may be set, cleared, or toggled by a FLG operation. The host processor can set, clear, or toggle these flags in the same way as the FLG instruction by means of the BC GENERAL PURPOSE FLAG REGISTER.
3	GP3	$\overline{\text{GP3}}$	
4	GP4	$\overline{\text{GP4}}$	
5	GP5	$\overline{\text{GP5}}$	
6	GP6	$\overline{\text{GP6}}$	
7	GP7	$\overline{\text{GP7}}$	
8	NORESP	$\overline{\text{RESP}}$	NORESP indicates that an RT has either not responded or has responded later than the BC No Response Timeout time. The Nano-ACE's No Response Timeout Time is defined per MIL-STD-1553B as the time from the mid-bit crossing of the parity bit of the last word transmitted by the BC to the mid-sync crossing of the RT Status Word. The value of the No Response Timeout value is programmable from among the nominal values 18.5, 22.5, 50.5, and 130 μs (±1 μs) by means of bits 10 and 9 of Configuration Register #5.
9	FMT ERR	$\overline{\text{FMT ERR}}$	FMT ERR indicates that the received portion of the most recent message contained one or more violations of the 1553 message validation criteria (sync, encoding, parity, bit count, word count, etc.), or the RT's status word received from a responding RT contained an incorrect RT address field.
A	GD BLK XFER	$\overline{\text{GD BLK XFER}}$	For the most recent message, GD BLK XFER will be set to logic "1" following completion of a valid (error-free) RT-to-BC transfer, RT-to-RT transfer, or transmit mode code with data message. This bit is set to logic "0" following an invalid message. GOOD DATA BLOCK TRANSFER is always logic "0" following a BC-to-RT transfer, a mode code with data, or a mode code without data. The Loop Test has no effect on GOOD DATA BLOCK TRANSFER. GOOD DATA BLOCK TRANSFER may be used to determine if the transmitting portion of an RT-to-RT transfer was error free.
B	MASKED STATUS BIT	$\overline{\text{MASKED STATUS}}$	Indicates that one or both of the following conditions have occurred for the most recent message: (1) If one (or more) of the

Table 37. BC Condition Codes

BIT Code	Name (BIT 4 = 0)	Inverse (BIT 4 = 1)	Functional Description
		$\overline{\text{BIT}}$	Status Mask bits (14 through 9) in the BC Control Word is logic "0" and the corresponding bit(s) is (are) set (logic "1") in the received RT Status Word. In the case of the RESERVED BITS MASK (bit 9) set to logic "0," any or all of the 3 Reserved Status Word bits being set will result in a MASKED STATUS SET condition; and/or (2) If BROADCAST MASK ENABLED/ $\overline{\text{XOR}}$ (bit 11 of Configuration Register #4) is logic "1" and the MASK BROADCAST bit of the message's BC Control Word is logic "0" and the BROADCAST COMMAND RECEIVED bit in the received RT Status Word is logic "1."
C	BAD MESSAGE	GOOD MESSAGE	BAD MESSAGE indicates either a format error, loop test fail, or no response error for the most recent message. Note that a "Status Set" condition has no effect on the "BAD MESSAGE/GOOD MESSAGE" condition code.
D	RETRY0	$\overline{\text{RETRY0}}$	These two bits reflect the retry status of the most recent message. The number of times that the message was retried is delineated by these two bits as shown below: Retry Count 1 (bit 14) / Retry Count 2 (bit 13) / Number of Message Retries 0 / 0 / 0 0 / 1 / 1 1 / 0 / N/A 1 / 1 / 2
E	RETRY1	$\overline{\text{RETRY1}}$	
F	ALWAYS	NEVER	The ALWAYS flag should be set (bit 4 = 0) to designate an instruction as unconditional. The NEVER bit (bit 4 = 1) can be used to implement a NOP or "skip" instruction.

5.3 BC Message Sequence Control

The Nano-ACE BC message sequence control capability enables a high degree of offloading of the host processor. This includes using the various timing functions to enable autonomous structuring of major and minor frames. In addition, by implementing conditional jumps and subroutine calls, the message sequence control processor greatly simplifies the insertion of asynchronous, or "out-of-band" messages.

5.4 Execute and Flip Operation

The Nano-ACE BC's XQF, or "Execute and Flip" operation, provides some unique capabilities. Following execution of this unconditional instruction, if the condition code tests TRUE, the BC will modify the value of the current XQF instruction's pointer parameter by toggling bit 4 of the pointer. That is, if the selected condition flag tests true, the value of the parameter will be updated to the value = old address XOR

0010h. As a result, the next time that this line in the instruction list is executed, the Message Control/Status Block at the updated address (old address XOR 0010h) will be processed, rather than the one at the old address. The operation of the XQF instruction is illustrated in Figure 5.

There are multiple ways of utilizing the "execute and flip" instruction. One is to facilitate the implementation of a double buffering data scheme for individual messages. This allows the message sequence control processor to "ping-pong" between a pair of data buffers for a particular message. By doing so, the host processor can access one of the two Data Word blocks, while the BC reads or writes the alternate Data Word block.

A second application of the "execute and flip" capability is in conjunction with message retries. This allows the BC to not only switch buses when retrying a failed message, but to automatically switch buses permanently for all future times that the same message is to be processed. This not only provides a high degree of autonomy from the host CPU, but saves BC bandwidth, by eliminating the need for future attempts to process messages on an RT's failed channel.

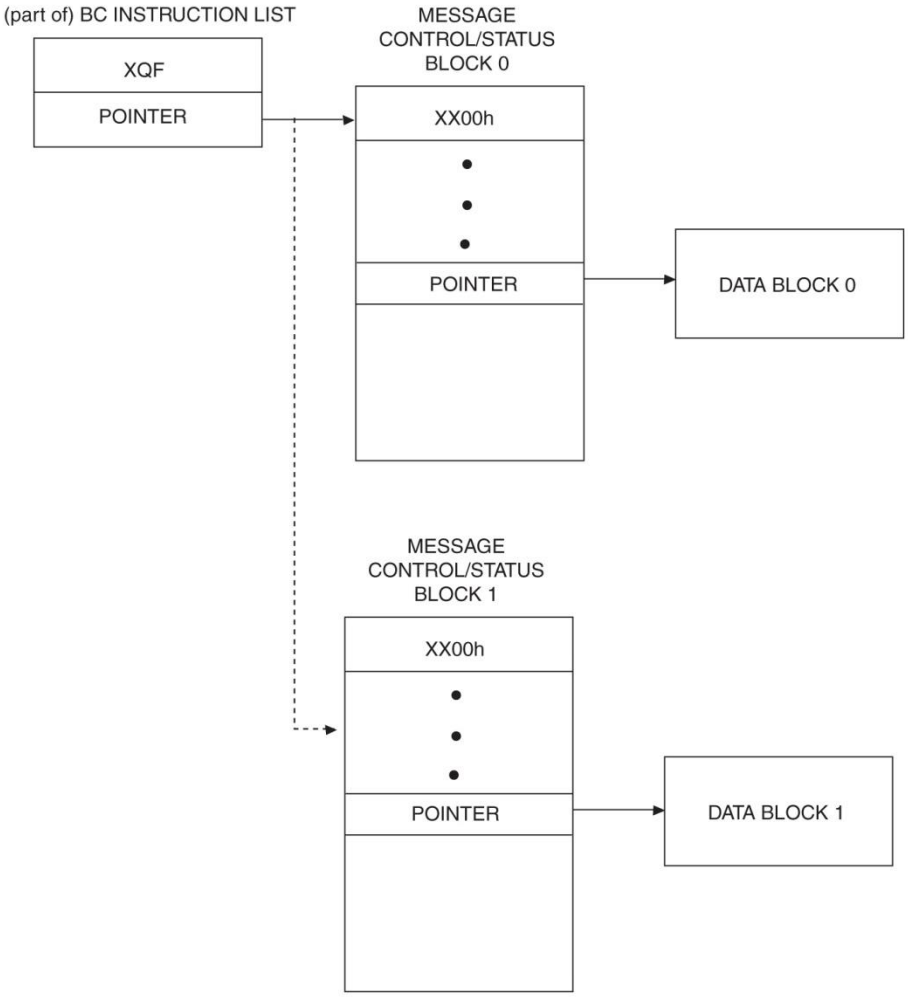


Figure 5. EXECUTE and FLIP (XQF) Operation

5.5 General Purpose Queue

The Nano-ACE BC allows for the creation of a general purpose queue. This data structure provides a means for the message sequence processor to convey information to the BC host. The BC op code repertoire provides mechanisms to push various items on this queue. These include the contents of the Time Tag Register, the Block Status Word for the most recent message, an immediate data value, or the contents of a specified memory address.

Figure 6 illustrates the operation of the BC General Purpose Queue. Note that the BC General Purpose Queue Pointer Register will always point to the next address location (modulo 64); that is, the location following the last location written by the BC message sequence control engine.

If enabled, a BC GENERAL PURPOSE QUEUE ROLLOVER interrupt will be issued when the value of the queue pointer address rolls over at a 64-word boundary. The rollover will always occur at a modulo 64 address.

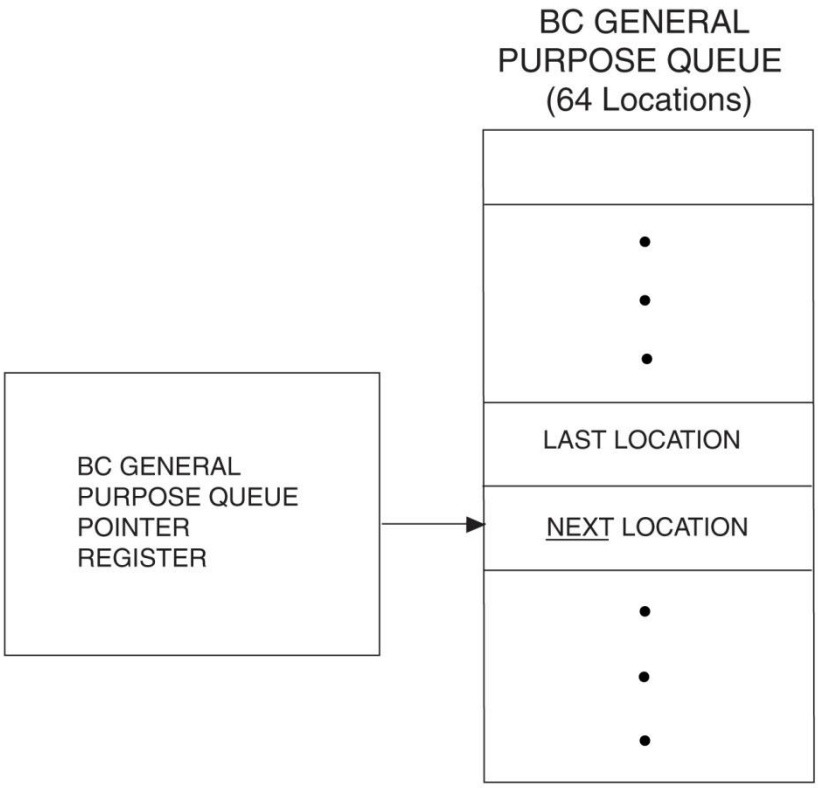


Figure 6. BC General Purpose Queue

6 REMOTE TERMINAL (RT) ARCHITECTURE

The Nano-ACE®'s RT architecture builds upon that of the ACE and Mini-ACE. The Nano-ACE provides multiprotocol support, with full compliance to all of the commonly used data bus standards, including MIL-STD-1553A, MIL-STD-1553B Notice 2, STANAG 3838, General Dynamics 16PP303, and McAir A3818, A5232, and A5690. For the Nano-ACE RT mode, there is programmable flexibility enabling the RT to be configured to fulfill any set of system requirements. This includes the capability to meet the MIL-STD-1553A response time requirement of 2 to 5 μs, and multiple options for mode code subaddresses, mode codes, RT status word, and RT BIT word.

The Nano-ACE RT protocol design implements all of the MIL-STD-1553B message formats and dual redundant mode codes. The design has passed validation testing for MIL-STD-1553B compliance. The Nano-ACE RT performs comprehensive error checking including word and format validation, and checks for various RT-to-RT transfer errors. One of the main features of the Nano-ACE RT is its choice of memory management options. These include single buffering by subaddress, double buffering for individual receive subaddresses, circular buffering by individual subaddresses, and global circular buffering for multiple (or all) subaddresses.

Other features of the Nano-ACE RT include a set of interrupt conditions, a flexible status queue with filtering based on valid and/or invalid messages, flexible command illegalization, programmable busy by subaddress, multiple options on time tagging, and an "auto-boot" feature which allows the RT to initialize as an online RT with the busy bit set following power turn-on.

6.1 RT Memory Organization

Table 38 illustrates a typical memory map for an Nano-ACE RT with 4K RAM. The two Stack Pointers reside in fixed locations in the shared RAM address space: address 0100 (hex) for the Area A Stack Pointer and address 0104 for the Area B Stack Pointer. In addition to the Stack Pointer, there are several other areas of the shared RAM address space that are designated as fixed locations (all shown in bold). These are for the Area A and Area B lookup tables, the illegalization lookup table, the busy lookup table, and the mode code data tables.

The RT lookup tables (see Table 39) provide a mechanism for allocating data blocks for individual transmit, receive, or broadcast subaddresses. The RT lookup tables include subaddress control words as well as the individual data block pointers. If command illegalization is used, address range 0300-03FF is used for command illegalizing. The descriptor stack RAM area, as well as the individual data blocks, may be located in any of the non-fixed areas in the shared RAM address space.

Note that in Table 38, there is no area allocated for "Stack B". This is shown for purpose of simplicity of illustration. Also, note that in Table 38, the allocated area for

the RT command stack is 256 words. However, larger stack sizes are possible. That is, the RT command stack size may be programmed for 256 words (64 messages), 512, 1024, or 2048 words (512 messages) by means of bits 14 and 13 of Configuration Register 3.

Table 38. Typical RT Memory Map (Shown for 4K RAM)

Address (HEX)	Description
0000-00FF	Stack A
0100	Stack Pointer A
0101	Global Circular Buffer A Pointer
0102-0103	RESERVED
0104	Stack Pointer B
0105	Global Circular Buffer B Pointer
0106-0107	RESERVED
0108-010F	Mode Code Selective Interrupt Table
0110-013F	Mode Code Data
0140-01BF	Lookup Table A
01C0-023F	Lookup Table B
0240-0247	Busy Bit Lookup Table
0248-025F	(not used)
0260-027F	Data Block 0
0280-02FF	Data Block 1-4
0300-03FF	Command Illegalization Table
0400-041F	Data Block 5
0420-043F	Data Block 6
•	•
•	•
•	•
0FE0-0FFF	Data Block 100

Table 39. RT Look-up Tables			
Area A	**Area B**	**Description**	**Comment**
0140 • • • 015F	01C0 • • • 01DF	Rx(/Bcst) SA0 • • • Rx(/Bcst) SA31	Receive (/Broadcast) Lookup Pointer Table
0160 • • • 017F	01E0 • • • 01FF	Tx SA0 • • • Tx SA31	Transmit Lookup Pointer Table
0180 • • • 019F	0200 • • • 021F	Bcst SA0 • • • Bcst SA31	Broadcast Lookup Pointer Table (Optional)
01A0 • • • 01BF	0220 • • • 023F	SACW SA0 • • • SACW SA31	Subaddress Control Word Lookup Table (Optional)

6.2 RT Memory Management

The Nano-ACE® provides a variety of RT memory management capabilities. As with the ACE and Mini-ACE, the choice of memory management scheme is fully programmable on a transmit/receive/broadcast subaddress basis.

In compliance with MIL-STD-1553B Notice 2, received data from broadcast messages may be optionally separated from non-broadcast received data. For each transmit, receive or broadcast subaddress, either a single-message data block, a double buffered configuration (two alternating Data Word blocks), or a variable-sized (128 to 8192 words) subaddress circular buffer may be allocated for data storage. The memory management scheme for individual subaddresses is designated by means of the subaddress control word (reference Table 40).

For received data, there is also a global circular buffer mode. In this configuration, the data words received from multiple (or all) subaddresses are stored in a common circular buffer structure. Like the subaddress circular buffer, the size of the global circular buffer is programmable, with a range of 128 to 8192 data words.

The double buffering feature provides a means for the host processor to easily access the most recent, complete received block of valid Data Words for any given subaddress. In addition to helping ensure data sample consistency, the circular buffer

options provide a means for greatly reducing host processor overhead for multi-message bulk data transfer applications.

End-of-message interrupts may be enabled either globally (following all messages), following error messages, on a transmit/receive/broadcast subaddress or mode code basis, or when a circular buffer reaches its midpoint (50% boundary) or lower (100%) boundary. A pair of interrupt status registers allow the host processor to determine the cause of all interrupts by means of a single read operation.

Table 40. RT Subaddress Control Word – Memory Management Options

Double-Buffered or Global circular Buffer (bit 15)	Subaddress Control Word Bits			Memory Management Subaddress Buffer Scheme Description	
	MM2	MM1	MM0		
0	0	0	0	Single Message	
1	0	0	0	For Receive or Broadcast: Double Buffered For Transmit: Single Message	
0	0	0	1	128-Word	Subaddress – specified circular buffer of specified size.
0	0	1	0	256-Word	
0	0	1	1	512-Word	
0	1	0	0	1024-Word	
0	1	0	1	2048-Word	
0	1	1	0	4096-Word	
0	1	1	1	8192-Word	
1	1	1	1	(for receive and/or broadcast subaddress only) Global Circular Buffer: The buffer size is specified by Configuration Register #6, bits 11-9. The pointer to the global circular buffer is stored at address 0101 (for Area A) or address 0105 (for Area B)	

6.3 Single Buffered Mode

The operation of the single buffered RT mode is illustrated in Figure 7. In the single buffered mode, the respective lookup table entry must be written by the host processor. Received data words are written to, or transmitted data words are read from the data word block with starting address referenced by the lookup table pointer. In the single buffered mode, the current lookup table pointer is not updated by the Nano-ACE® memory management logic. Therefore, if a subsequent message is received for the same subaddress, the same Data Word block will be overwritten or overread.

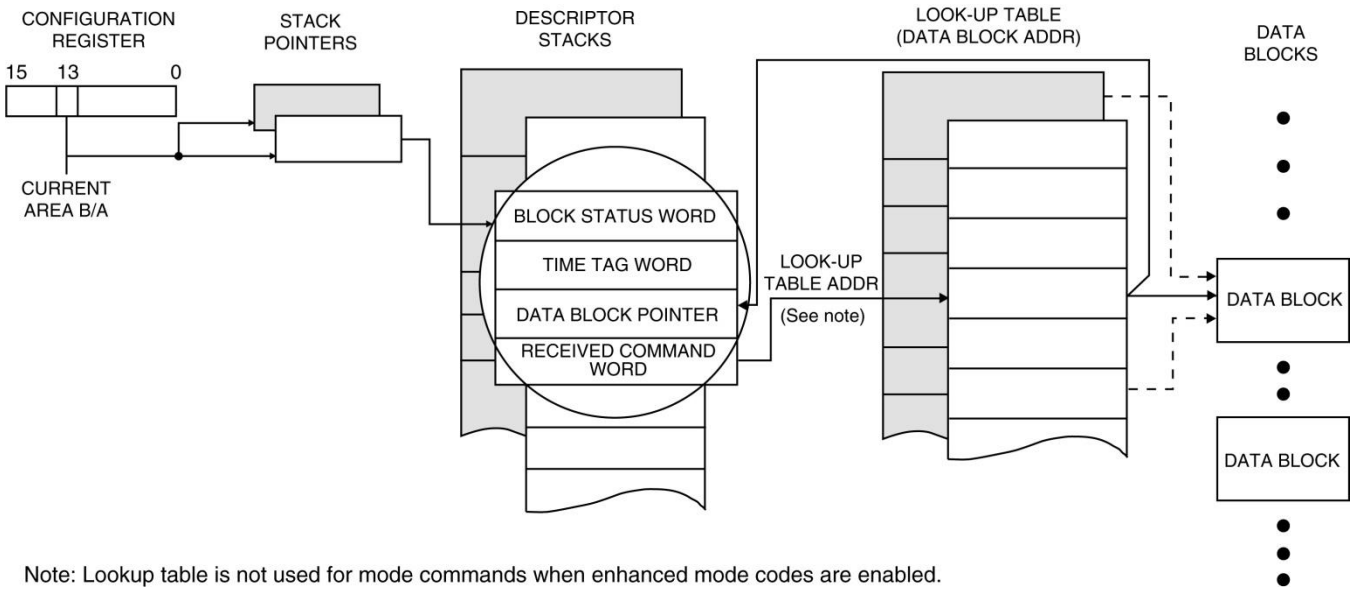


Figure 7. RT Single Buffered Mode

6.4 SUBADDRESS DOUBLE BUFFERING MODE

The Nano-ACE® provides a double buffering mechanism for received data, that may be selected on an individual subaddress basis for any or all receive (and/or broadcast) subaddresses. This is illustrated in Figure 8. It should be noted that the Subaddress Double Buffering mode is applicable for receive data only, not for transmit data. Double buffering of transmit messages may be easily implemented by software techniques.

The purpose of the subaddress double buffering mode is to provide data sample consistency to the host processor. This is accomplished by allocating two 32-word data word blocks for each individual receive (and/or broadcast receive) subaddress. At any given time, one of the blocks will be designated as the "active" 1553 block while the other will be considered as "inactive". The data words for the next receive command to that subaddress will be stored in the active block. Following receipt of a valid message, the Nano-ACE will automatically switch the active and inactive blocks for that subaddress. As a result, the latest, valid, complete data block is always accessible to the host processor.

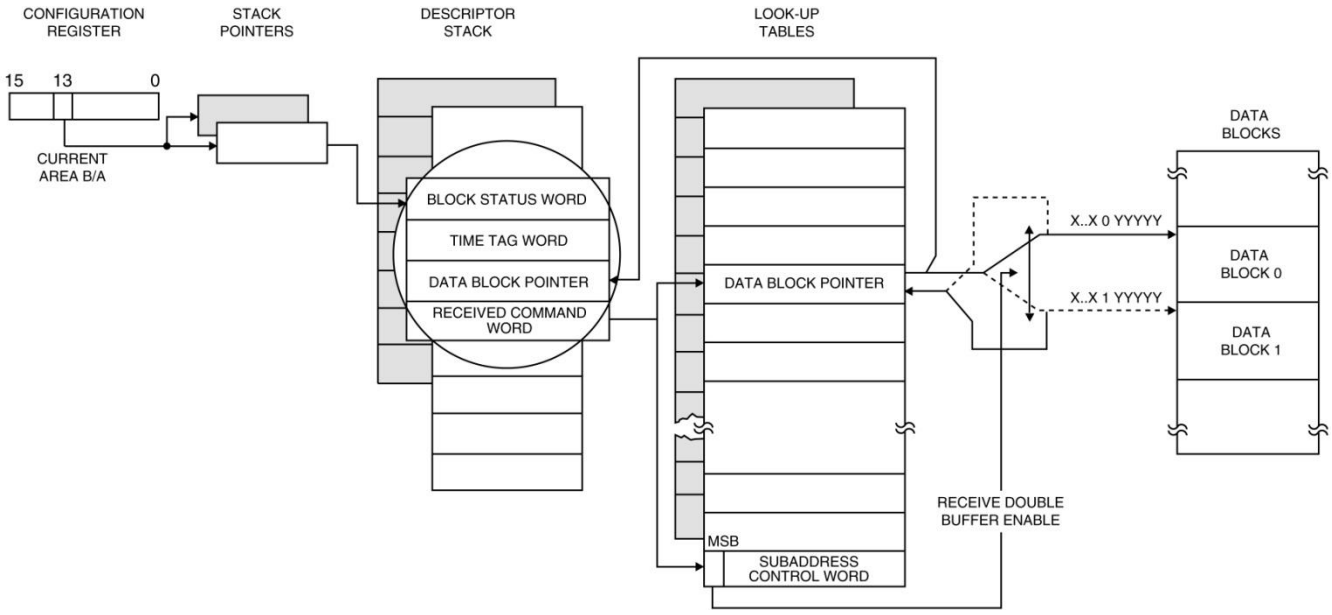


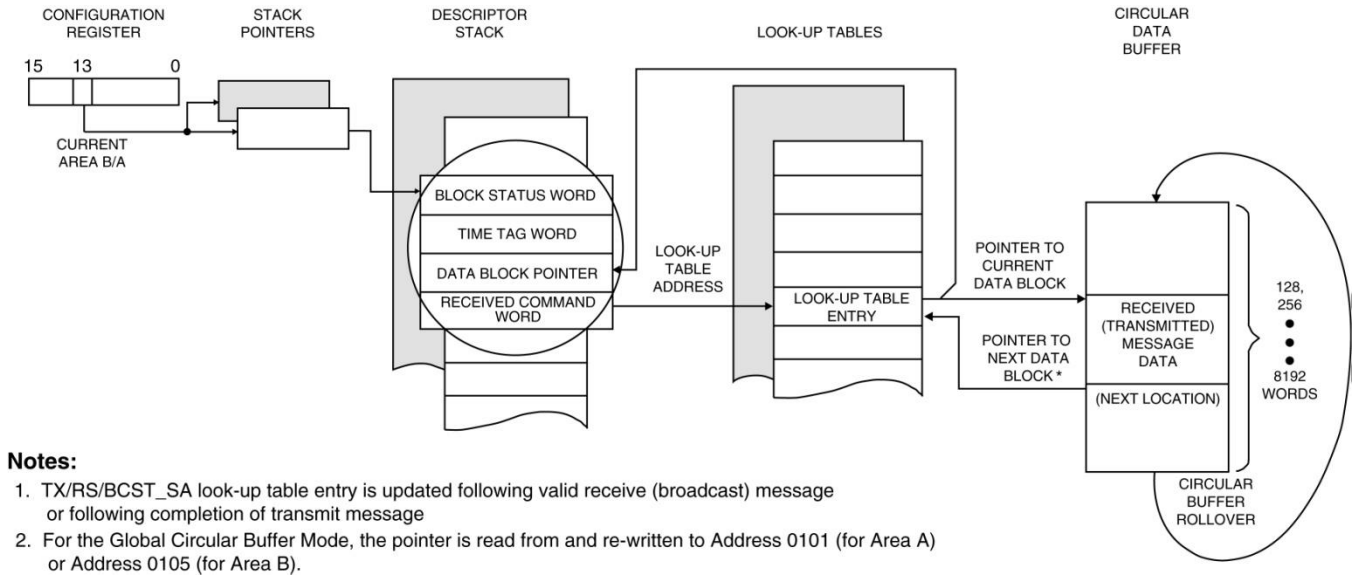
Figure 8. RT Double Buffered Mode

6.5 CIRCULAR BUFFER MODE

The operation of the Nano-ACE®'s circular buffer RT memory management mode is illustrated in Figure 9. As in the single buffered and double buffered modes, the individual lookup table entries are initially loaded by the host processor. At the start of each message, the lookup table entry is stored in the third position of the respective message block descriptor in the descriptor stack area of RAM. Receive or transmit data words are transferred to (from) the circular buffer, starting at the location referenced by the lookup table pointer.

In general, the location after the last data word written or read (modulo the circular buffer size) during the message is written to the respective lookup table location during the end-of-message sequence. By so doing, data for the next message for the respective transmit, receive(/broadcast), or broadcast subaddress will be accessed from the next lower contiguous block of locations in the circular buffer.

For the case of a receive (or broadcast receive) message with a data word error, there is an option such that the lookup table pointer will only be updated following receipt of a valid message. That is, the pointer will not be updated following receipt of a message with an error in a data word. This allows failed messages in a bulk data transfer to be retried without disrupting the circular buffer data structure, and without intervention by the RT's host processor.



Notes:

1. TX/RS/BCST_SA look-up table entry is updated following valid receive (broadcast) message or following completion of transmit message
2. For the Global Circular Buffer Mode, the pointer is read from and re-written to Address 0101 (for Area A) or Address 0105 (for Area B).

Figure 9. RT Circular Buffered Mode

6.6 GLOBAL CIRCULAR BUFFER

Beyond the programmable choice of single buffer mode, double buffer mode, or circular buffer mode, programmable on an individual subaddress basis, the Nano-ACE® RT architecture provides an additional option, a variable sized global circular buffer. The Nano-ACE RT allows for a mix of single buffered, double buffered, and individually circular buffered subaddresses, along with the use of the global double buffer for any arbitrary group of receive(/broadcast) or broadcast subaddresses.

In the global circular buffer mode, the data for multiple receive subaddresses is stored in the same circular buffer data structure. The size of the global circular buffer may be programmed for 128, 256, 512, 1024, 2048, 4096, or 8192 words, by means of bits 11, 10, and 9 of Configuration Register #6. As shown in Table 40, individual subaddresses may be mapped to the global circular buffer by means of their respective subaddress control words.

The pointer to the Global Circular Buffer will be stored in location 0101 (for Area A), or location 0105 (for Area B).

The global circular buffer option provides a highly efficient method for storing received message data. It allows for frequently used subaddresses to be mapped to individual data blocks, while also providing a method for asynchronously received messages to infrequently used subaddresses to be logged to a common area. Alternatively, the global circular buffer provides an efficient means for storing the received data words for all subaddresses. Under this method, all received data words are stored chronologically, regardless of subaddress.

6.7 RT DESCRIPTOR STACK

The descriptor stack provides a chronology of all messages processed by the Nano-ACE® RT. Reference Figure 7, Figure 8, and Figure 9. There is a four-word block descriptor in the Stack for each message processed. The four entries to each block descriptor are the Block Status Word, Time Tag Word, the pointer to the start of the message's data block, and the 16-bit received Command Word.

The RT Block Status Word includes indications of whether a particular message is ongoing or has been completed, what bus channel it was received on, indications of illegal commands, and flags denoting various message error conditions. For the double buffering, subaddress circular buffering, and global circular buffering modes, the data block pointer may be used for locating the data blocks for specific messages. Note that for mode code commands, there is an option to store the transmitted or received data word as the third word of the descriptor, in place of the data block pointer.

The Time Tag Word provides a 16-bit indication of relative time for individual messages. The resolution of the Nano-ACE's time tag is programmable from among 2, 4, 8, 16, 32, or 64 μs/LSB. There is also a provision for using an external clock input for the time tag. If enabled, there is a time tag rollover interrupt, which is issued when the value of the time tag rolls over from FFFF(hex) to 0. Other time tag options include the capabilities to clear the time tag register following receipt of a Synchronize (without data) mode command and/or to set the time tag following receipt of a Synchronize (with data) mode command. For the latter, there is an added option to filter the "set" capability based on the LSB of the received data word being equal to logic "0".

6.8 RT INTERRUPTS

The Nano-ACE offers a great deal of flexibility in terms of RT interrupt processing. By means of the Nano-ACE's two Interrupt Mask Registers, the RT may be programmed to issue interrupt requests for the following events/conditions: End-of-(every) Message, Message Error, Selected (transmit or receive) Subaddress, 100% Circular Buffer Rollover, 50% Circular Buffer Rollover, 100% Descriptor Stack Rollover, 50% Descriptor Stack Rollover, Selected Mode Code, Transmitter Timeout, Illegal Command, and Interrupt Status Queue Rollover.

Interrupts for 50% Rollovers of Stacks and Circular Buffers. The Nano-ACE RT and Monitor are capable of issuing host interrupts when a subaddress circular buffer pointer or stack pointer crosses its mid-point boundary. For RT circular buffers, this is applicable for both transmit and receive subaddresses. Reference Figure 10. There are four interrupt mask and interrupt status register bits associated with the 50% rollover function:

1. RT circular buffer;
2. RT command (descriptor) stack;
3. Monitor command (descriptor) stack; and
4. Monitor data stack.

The 50% rollover interrupt is beneficial for performing bulk data transfers. For example, when using circular buffering for a particular receive subaddress, the 50% rollover interrupt will inform the host processor when the circular buffer is half full. At that time, the host may proceed to read the received data words in the upper half of the buffer, while the Nano-ACE® RT writes received data words to the lower half of the circular buffer. Later, when the RT issues a 100% circular buffer rollover interrupt, the host can proceed to read the received data from the lower half of the buffer, while the Nano-ACE RT continues to write received data words to the upper half of the buffer.

Interrupt status queue. The Nano-ACE RT, Monitor, and combined RT/Monitor modes include the capability for generating an interrupt status queue. As illustrated in Figure 11, this provides a chronological history of interrupt generating events and conditions. In addition to the Interrupt Mask Register, the Interrupt Status Queue provides additional filtering capability, such that only valid messages and/or only invalid messages may result in the creation of an entry to the Interrupt Status Queue. Queue entries for invalid and/or valid messages may be disabled by means of bits 8 and 7 of configuration register #6.

The interrupt status queue is 64 words deep, providing the capability to store entries for up to 32 messages. These events and conditions include both message-related and non-message related events. Note that the Interrupt Vector Queue Pointer Register will always point to the next location (modulo 64) following the last vector/pointer pair written by the Nano-ACE RT.

The pointer to the Interrupt Status Queue is stored in the INTERRUPT VECTOR QUEUE POINTER REGISTER (register address 1F). This register must be initialized by the host, and is subsequently incremented by the RT message processor. The interrupt status queue is 64 words deep, providing the capability to store entries for up to 32 messages.

The queue rolls over at addresses of modulo 64. The events that result in queue entries include both message-related and non-message-related events. Note that the Interrupt Vector Queue Pointer Register will always point to the next location (modulo 64) following the last vector/pointer pair written by the Nano-ACE RT, Monitor, or RT/Monitor.

Each event that causes an interrupt results in a two-word entry to be written to the queue. The first word of the entry is the interrupt vector. The vector indicates which interrupt event(s)/condition(s) caused the interrupt.

The interrupt events are classified into two categories: message interrupt events and non-message interrupt events. Message based interrupt events include End-of-Message, Selected mode code, Format error, Subaddress control word interrupt, RT Circular buffer Rollover, Handshake failure, RT Command stack rollover, transmitter timeout, MT Data Stack rollover, MT Command Stack rollover, RT Command Stack 50% rollover, MT Data Stack 50% rollover, MT Command Stack 50% rollover, and RT Circular buffer 50% rollover. Non-message interrupt events/conditions include time tag rollover, RT address parity error and RAM parity error.

Bit 0 of the interrupt vector (interrupt status) word indicates whether the entry is for a message interrupt event (if bit 0 is logic "1") or a non-message interrupt event (if bit 0 is logic "0"). It is not possible for one entry on the queue to indicate both a message interrupt and a non-message interrupt.

As illustrated in Figure 11, for a message interrupt event, the parameter word is a pointer. The pointer will reference the first word of the RT or MT command stack descriptor (i.e., the Block Status Word).

For a RAM Parity Error non-message interrupt, the parameter will be the RAM address where the parity check failed. For the RT address Parity Error and Time Tag rollover non-message interrupts, the parameter is not used; it will have a value of 0000.

If enabled, an INTERRUPT STATUS QUEUE ROLLOVER interrupt will be issued when the value of the queue pointer address rolls over at a 64-word address boundary.

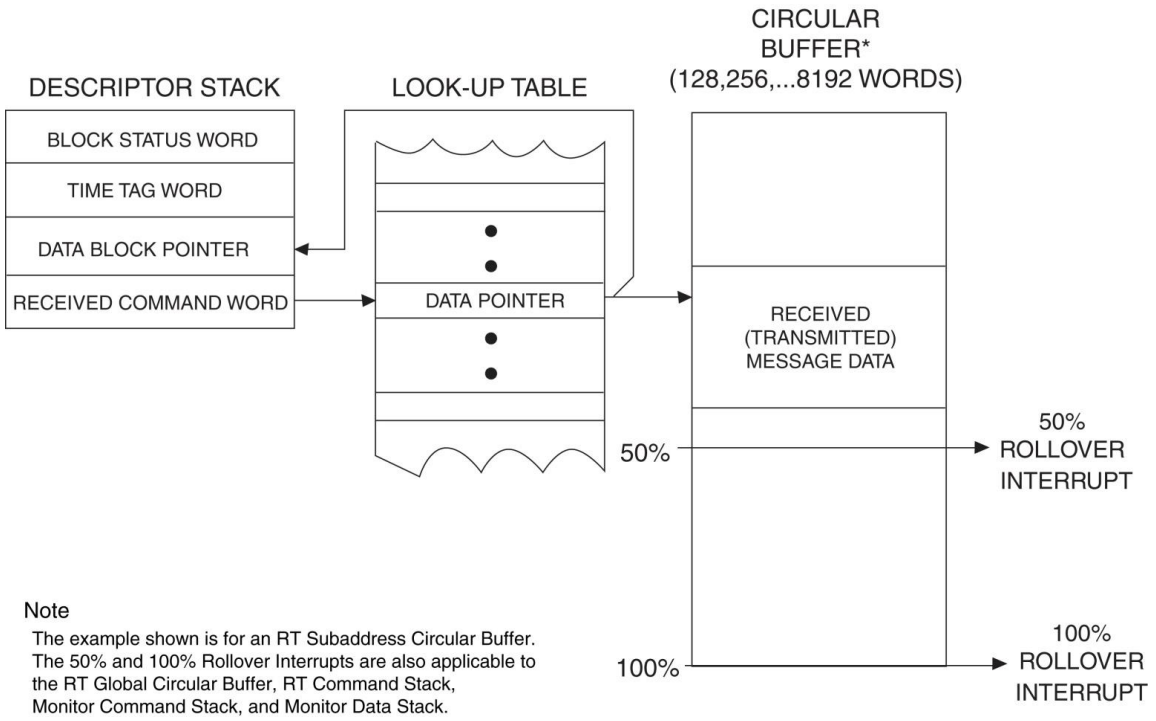


Figure 10. 50% and 100% Rollover Interrupts

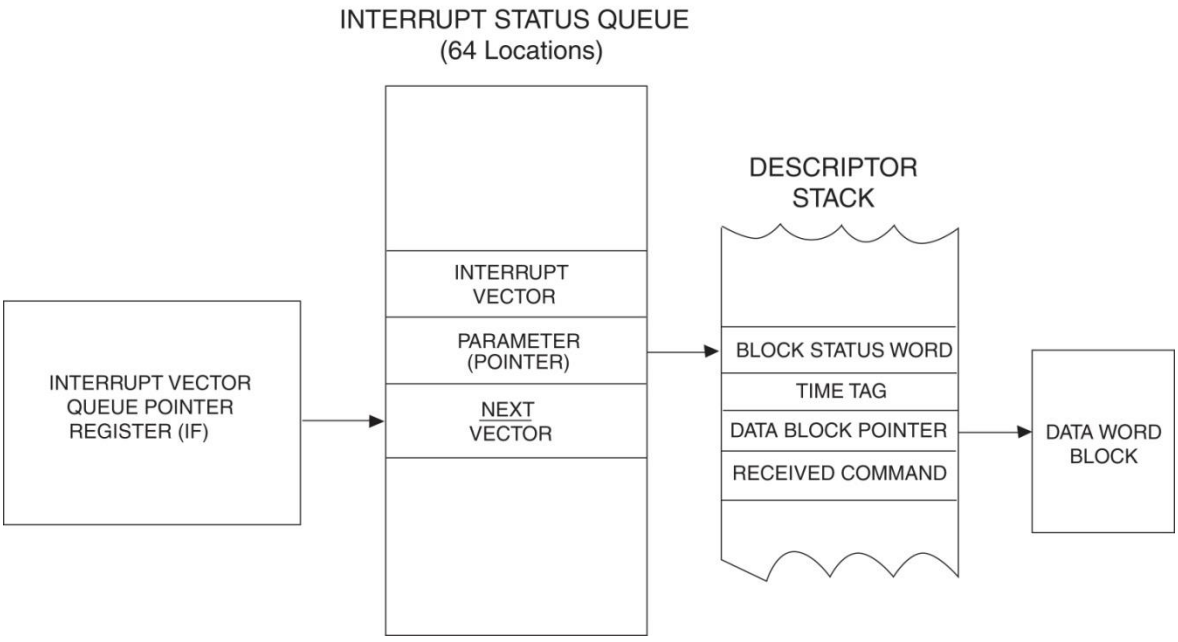


Figure 11. RT (and Monitor) Interrupt Status Queue

(Shown for message interrupt event)

6.9 RT COMMAND ILLEGALIZATION

The Nano-ACE® provides an internal mechanism for RT Command Word illegalizing. By means of a 256-word area in shared RAM, the host processor may designate that any message be illegalized, based on the command word T/R bit, subaddress, and word count/mode code fields. The Nano-ACE illegalization scheme provides the maximum in flexibility, allowing any subset of the 4096 possible combinations of broadcast/own address, T/R bit, subaddress, and word count/mode code to be illegalized.

The address map of the Nano-ACE's illegalizing table is illustrated in Table 41.

Table 41. Illegalization Table Memory Map

Address	Description
300	Brdcst/Rx, SA 0. MC15-0
301	Brdcst/Rx, SA 0. MC31-16
302	Brdcst/Rx, SA 1. WC15-0
303	Brdcst/Rx, SA 1. WC31-16
• • •	• • •
33F	Brdcst/Rx, SA 31. MC31-16
340	Brdcst/Tx, SA 0. MC15-0
341	Brdcst/Tx, SA 0. MC31-16
342	Brdcst/Tx, SA 1. WC15-0
• • •	• • •
37D	Brdcst/Tx, SA 30. WC31-16
37E	Brdcst / Tx, SA 31. MC15-0
37F	Brdcst / Tx, SA 31. MC31-16
380	Own Addr / Rx, SA 0. MC15-0
381	Own Addr / Rx, SA 0. MC31-16
382	Own Addr / Rx, SA 1. WC15-0
383	Own Addr / Rx, SA 1. WC31-16
• • •	• • •
3BE	Own Addr / Rx, SA 31. MC15-0
3BF	Own Addr / Rx, SA 31. MC31-16
3C0	Own Addr / Tx, SA 0. MC15-0
3C1	Own Addr / Tx, SA 0. MC31-16

Table 41. Illegalization Table Memory Map	
Address	**Description**
3C2	Own Addr / Tx, SA 1. WC15-0
3C3	Own Addr / Tx, SA 1. WC31-16
• • •	• • •
3FC	Own Addr / Tx, SA 30. WC15-0
3FD	Own Addr / Tx, SA 30. WC31-16
3FE	Own Addr / Tx, SA 31. MC15-0
3FF	Own Addr / Tx, SA 31. MC31-16

6.10 BUSY BIT

The Nano-ACE® RT provides two different methods for setting the Busy status word bit: (1) globally, by means of Configuration Register #1; or (2) on a T/R-bit/subaddress basis, by means of a RAM lookup table. If the host CPU asserts the BUSY bit to logic “0” in Configuration Register #1, the Nano-ACE RT will respond to all non-broadcast commands with the Busy bit set in its RT Status Word.

Alternatively, there is a Busy lookup table in the Nano-ACE shared RAM. By means of this table, it is possible for the host processor to set the busy bit for any selectable subset of the 128 combinations of broadcast/own address, T/R bit, and subaddress.

If the busy bit is set for a transmit command, the Nano-ACE RT will respond with the busy bit set in the status word, but will not transmit any data words. If the busy bit is set for a receive command, the RT will also respond with the busy status bit set. There are two programmable options regarding the reception of data words for a non-mode code receive command for which the RT is busy: (1) to transfer the received data words to shared RAM; or (2) to not transfer the data words to shared RAM.

6.11 RT ADDRESS

The Nano-ACE® offers several different options for designating the Remote Terminal address. These include the following: (1) hardwired, by means of the 5 RT ADDRESS inputs, and the RT ADDRESS PARITY input; (2) by means of the RT ADDRESS (and PARITY) inputs, but latched via hardware, on the rising edge of the RT_AD_LAT input signal; (3) input by means of the RT ADDRESS (and PARITY) inputs, but latched via host software; and (4) software programmable, by means of an internal register. In all four configurations, the RT address is readable by the host processor.

6.12 RT BUILT-IN-TEST (BIT) WORD

The bit map for the Nano-ACE's internal RT Built-in-Test (BIT) Word is indicated in Table 42.

6.13 RT AUTO-BOOT OPTION

If utilized, the RT pin-programmable auto-boot option allows the Nano-ACE RT to automatically initialize as an active remote terminal with the Busy status word bit set to logic "1" immediately following power turn-on. This is a useful feature for MIL-STD-1760 applications, in which the RT is required to be responding within 150 ms after power-up. This feature is available for versions of the Nano-ACE with 4K words of RAM. When using RT Auto-Boot, the RT ADDRESS must be hardwired in order to respond in 150 ms with no assistance.

6.14 OTHER RT FEATURES

The Nano-ACE includes options for the Terminal flag status word bit to be set either under software control and/or automatically following a failure of the loopback self-test. Other software programmable RT options include software programmable RT status and RT BIT words, automatic clearing of the Service Request bit following receipt of a Transmit vector word mode command, options regarding Data Word transfers for the Busy and Message error (illegal) Status word bits, and options for the handling of 1553A and reserved mode codes.

Table 42. RT BIT Word	
BIT	**Description**
15 (MSB)	Transmitter Timeout
14	Loop Test Failure B
13	Loop Test Failure A
12	Handshake Failure
11	Transmitter Shutdown B
10	Transmitter Shutdown A
9	Terminal Flag Inhibited
8	BIT Test Failure
7	High Word Count
6	Low Word Count
5	Incorrect Sync Received
4	Parity/Manchester error Received
3	RT-to-RT Gap/Sync Address Error
2	RT-to-RT No Response Error
1	RT-to-RT 2nd Command Word Error
0 (LSB)	Command Word Contents Error

7 MONITOR ARCHITECTURE

The Nano-ACE® includes three monitor modes:

1. A Word Monitor mode
2. A selective message monitor mode
3. A combined RT/message monitor mode

For new applications, it is recommended that the selective message monitor mode be used, rather than the word monitor mode. Besides providing monitor filtering based on RT address, T/R bit, and subaddress, the message monitor eliminates the need to determine the start and end of messages by software.

7.1 WORD MONITOR MODE

In the Word Monitor Terminal mode, the Nano-ACE monitors both 1553 buses. After the software initialization and Monitor Start sequences, the Nano-ACE stores all Command, Status, and Data Words received from both buses. For each word received from either bus, a pair of words is stored to the Nano-ACE's shared RAM. The first word is the word received from the 1553 bus. The second word is the Monitor Identification (ID), or "Tag" word. The ID word contains information relating to bus channel, word validity, and inter-word time gaps. The data and ID words are stored in a circular buffer in the shared RAM address space.

7.2 WORD MONITOR MEMORY MAP

A typical word monitor memory map is illustrated in Table 43. Table 43 assumes a 64K address space for the Nano-ACE's monitor. The Active Area Stack pointer provides the address where the first monitored word is stored. In the example, it is assumed that the Active Area Stack Pointer for Area A (location 0100) is initialized to 0000. The first received data word is stored in location 0000, the ID word for the first word is stored in location 0001, etc.

The current Monitor address is maintained by means of a counter register. This value may be read by the CPU by means of the Data Stack Address Register. It is important to note that when the counter reaches the Stack Pointer address of 0100 or 0104, the initial pointer value stored in this shared RAM location will be overwritten by the monitored data and ID Words. When the internal counter reaches an address of FFFF (or 0FFF, for a Nano-ACE with 4K RAM), the counter rolls over to 0000.

7.3 WORD MONITOR TRIGGER

In the Word Monitor mode, there is a pattern recognition trigger and a pattern recognition interrupt. The 16-bit compare word for both the trigger and the interrupt is

stored in the Monitor Trigger Word Register. The pattern recognition interrupt is enabled by setting the MT Pattern Trigger bit in Interrupt Mask Register #1. The pattern recognition trigger is enabled by setting the Trigger Enable bit in Configuration Register #1 and selecting either the Start-on-trigger or the Stop-on-trigger bit in Configuration Register #1.

The Word Monitor may also be started by means of a low-to-high transition on the EXT_TRIG input signal.

7.4 SELECTIVE MESSAGE MONITOR MODE

The Nano-ACE® Selective Message Monitor provides monitoring of 1553 messages with filtering based on RT address, T/R bit, and subaddress with no host processor intervention. By autonomously distinguishing between 1553 command and status words, the Message Monitor determines when messages begin and end, and stores the messages into RAM, based on a programmable filter of RT address, T/R bit, and subaddress.

The selective monitor may be configured as just a monitor, or as a combined RT/Monitor. In the combined RT/Monitor mode, the Nano-ACE functions as an RT for one RT address (including broadcast messages), and as a selective message monitor for the other 30 RT addresses. The Nano-ACE Message Monitor contains two stacks, a command stack and a data stack, that are independent from the RT command stack. The pointers for these stacks are located at fixed locations in RAM.

Table 43. Typical Word Monitor Memory Map

Hex Address	Function
0000	First Received 1553 Word
0001	First Identification Word
0002	Second Received 1553 Word
0003	Second Identification 1553 Word
0004	Third Received 1553 Word
0005	Third Identification Word
• • •	• • •
0100	Stack Pointer (Fixed Location – gets overwritten)
• • •	• • •
FFFF	Received 1553 Words and Identification Word

7.5 MONITOR SELECTION FUNCTION

Following receipt of a valid command word in Selective Monitor mode, the Nano-ACE® will reference the selective monitor lookup table to determine if the particular command is enabled. The address for this location in the table is determined by means of an offset based on the RT Address, T/R bit, and Subaddress bit 4 of the current command word, and concatenating it to the monitor lookup table base address of 0280 (hex). The bit location within this word is determined by subaddress bits 3-0 of the current command word.

If the specified bit in the lookup table is logic "0", the command is not enabled, and the Nano-ACE will ignore this command. If this bit is logic "1", the command is enabled and the Nano-ACE will create an entry in the monitor command descriptor stack (based on the monitor command stack pointer), and store the data and status words associated with the command into sequential locations in the monitor data stack. In addition, for an RT-to-RT transfer in which the receive command is selected, the second command word (the transmit command) is stored in the monitor data stack.

The address definition for the Selective Monitor Lookup Table is illustrated in Table 44.

Table 44. RT BIT Word

BIT	Description
15 (MSB)	Logic “0”
14	Logic “0”
13	Logic “0”
12	Logic “0”
11	Logic “0”
10	Logic “0”
9	Logic “1”
8	Logic “0”
7	Logic “1”
6	RTAD_4
5	RTAD_3
4	RTAD_2
3	RTAD_1
2	RTAD_0
1	TRANSMIT/ $\overline{\text{RECEIVE}}$
0 (LSB)	Subaddress 4

7.6 SELECTIVE MESSAGE MONITOR MEMORY ORGANIZATION

A typical memory map for the Nano-ACE® in the Selective Message Monitor mode, assuming a 4K RAM space, is illustrated in Table 45. This mode of operation defines several fixed locations in the RAM. These locations are allocated in a way in which none of them overlap with the fixed RT locations. This allows for the combined RT/Selective Message Monitor mode.

The fixed memory map consists of two Monitor Command Stack Pointers (locations 102 and 106 hex), two Monitor Data Stack Pointers (locations 103 and 107 hex), and a Selective Message Monitor Lookup Table (locations 0280 through 02FF hex). For this example, the Monitor Command Stack size is assumed to be 1K words, and the Monitor Data Stack size is assumed to be 2K words.

Figure 12 illustrates the Selective Message Monitor operation. Upon receipt of a valid Command Word, the Nano-ACE will reference the Selective Monitor Lookup Table to determine if the current command is enabled. If the current command is disabled, the Nano-ACE monitor will ignore (and not store) the current message. If the command is enabled, the monitor will create an entry in the Monitor Command Stack at the address location referenced by the Monitor Command Stack Pointer, and an entry in the monitor data stack starting at the location referenced by the Monitor Data Stack Pointer.

The format of the information in the data stack depends on the format of the message that was processed. For example, for a BC-to-RT transfer (receive command), the monitor will store the command word in the monitor command descriptor stack, with the data words and the receiving RT's status word stored in the monitor data stack.

The size of the monitor command stack is programmable, with choices of 256, 1K, 4K, or 16K words. The monitor data stack size is programmable with choices of 512, 1K, 2K, 4K, 8K, 16K, 32K or 64K words.

7.7 MONITOR INTERRUPTS

Selective monitor interrupts may be issued for End-of-message and for conditions relating to the monitor command stack pointer and monitor data stack pointer. The latter, as shown in Figure 10, include Command Stack 50% Rollover, Command Stack 100% Rollover, Data Stack 50% Rollover, and Data Stack 100% Rollover.

The 50% rollover interrupts may be used to inform the host processor when the command stack or data stack is half full. At that time, the host may proceed to read the received messages in the upper half of the respective stack, while the Nano-

ACE® monitor writes messages to the lower half of the stack. Later, when the monitor issues a 100% stack rollover interrupt, the host can proceed to read the received data from the lower half of the stack, while the Nano-ACE monitor continues to write received data words to the upper half of the stack.

Table 45. Typical Selective Message Monitor Memory Map (shown for 4K RAM for "Monitor only" mode)

Address (Hex)	Function
0000-0101	Not Used
0102	Monitor Command Stack Pointer A (fixed location)
0103	Monitor Data Stack Pointer A (fixed location)
0104-0105	Not Used
0106	Monitor Command Stack Pointer B (fixed location)
0107	Monitor Data Stack Pointer B (fixed location)
0108-027F	Not Used
0280-02FF	Selective Monitor Lookup Table (fixed location)
0300-03FF	Not Used
0400-07FF	Monitor Command Stack A
0800-0FFF	Monitor Data Stack A

7.8 INTERRUPT STATUS QUEUE

Like the Nano-ACE RT, the Selective Monitor mode includes the capability for generating an interrupt status queue. As illustrated in Figure 11, this provides a chronological history of interrupt generating events. Besides the two Interrupt Mask Registers, the Interrupt Status Queue provides additional filtering capability, such that only valid messages and/or only invalid messages may result in entries to the Interrupt Status Queue. The interrupt status queue is 64 words deep, providing the capability to store entries for up to 32 monitored messages.

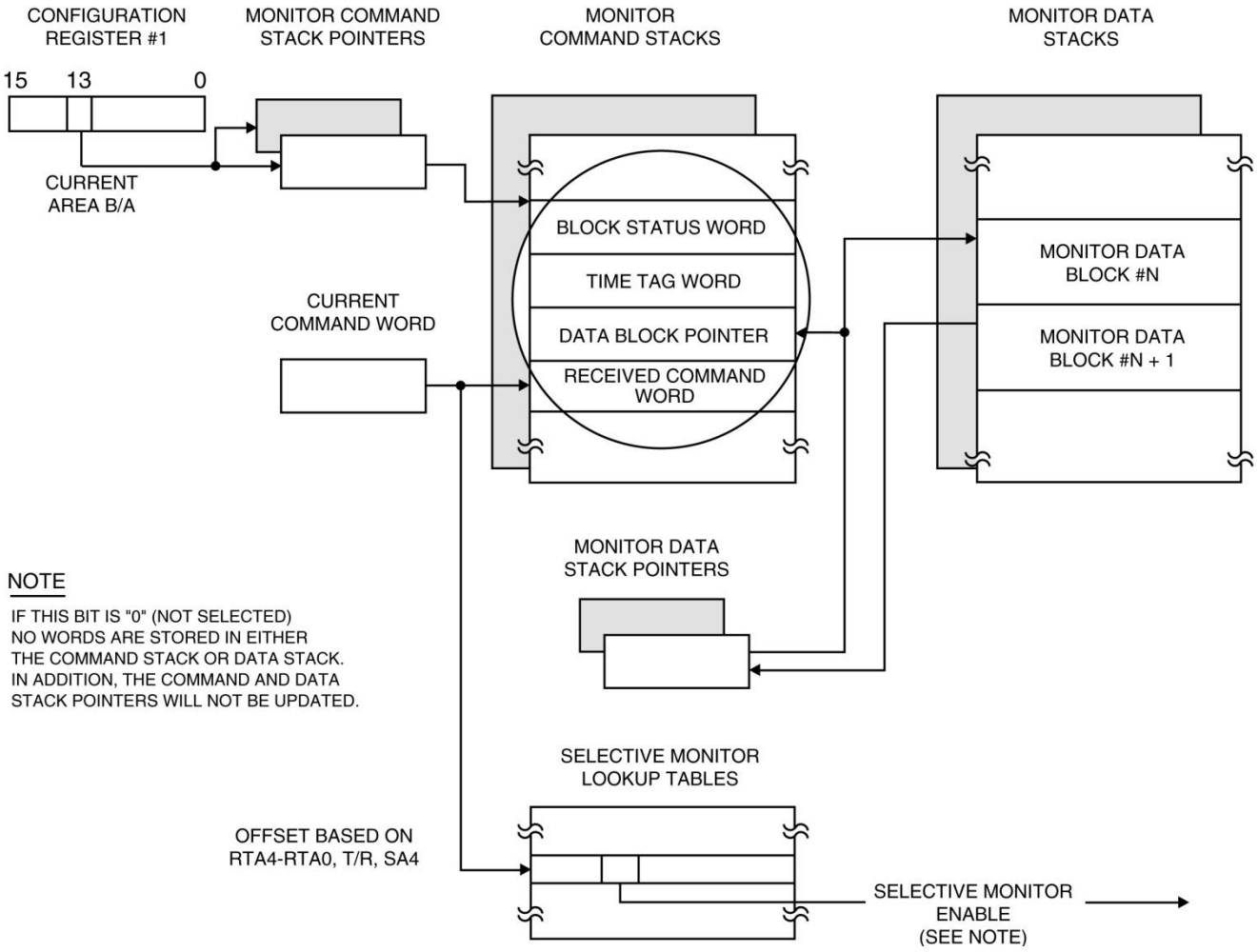


Figure 12. Selective Message Monitor Memory Management

8 MISCELLANEOUS

8.1 CLOCK INPUT

The Nano-ACE® requires a 40 MHz clock input.

8.2 ENCODER/DECODERS

There is internal logic to derive the necessary clocks for the Manchester encoder and decoders from the 40 MHz input clock. The decoders sample the receiver outputs on the rising edge of the input clock. Using a high frequency clock for sampling frequency serves to widen the tolerance to zero-crossing distortion, and reduce the bit error rate.

8.3 TIME TAG

The Nano-ACE includes an internal read/writable Time Tag Register. This register is a CPU read/writable 16-bit counter with a programmable resolution of either 2, 4, 8, 16, 32, or 64 μs per LSB. Another option allows software controlled incrementing of the Time Tag Register. This supports self-test for the Time Tag Register. For each message processed, the value of the Time Tag Register is loaded into the second location of the respective descriptor stack entry ("TIME TAG WORD") for the RT mode.

The functionality involving the Time Tag Register that's compatible with ACE/Mini-ACE (Plus) includes: the capability to issue an interrupt request and set a bit in the Interrupt Status Register when the Time Tag Register rolls over FFFF to 0000; for RT mode, the capability to automatically clear the Time Tag Register following reception of a Synchronize (without data) mode command, or to load the Time Tag Register following a Synchronize (with data) mode command.

The Nano-ACE also includes the capability for the RT to "filter" the data word for the Synchronize with data mode command, by only loading the Time Tag Register if the LSB of the received data word is "0";

8.4 INTERRUPTS

The Nano-ACE series terminals provide many programmable options for interrupt generation and handling. The interrupt output pin (INT) has three software programmable modes of operation: a pulse, a level output cleared under software control, or a level output automatically cleared following a read of the Interrupt Status Register (#1 or #2).

Individual interrupts are enabled by the two Interrupt Mask Registers. The host processor may determine the cause of the interrupt by reading the two Interrupt Status

Registers, which provide the current state of interrupt events and conditions. The Interrupt Status Registers may be updated in two ways. In one interrupt handling mode, a particular bit in Interrupt Status Register #1 or #2 will be updated only if the event occurs and the corresponding bit in Interrupt Mask Register #1 or #2 is enabled. In the enhanced interrupt handling mode, a particular bit in one of the Interrupt Status Registers will be updated if the event/condition occurs regardless of the value of the corresponding Interrupt Mask Register bit. In either case, the respective Interrupt Mask Register (#1 or #2) bit is used to enable an interrupt for a particular event/condition.

The Nano-ACE® supports all the interrupt events from ACE/Mini-ACE (Plus), including RAM Parity Error Transmitter Timeout, BC/RT Command Stack Rollover, MT Command Stack and Data Stack Rollover, Handshake Error, BC Retry, RT Address Parity Error, Time Tag Rollover, RT Circular Buffer Rollover, BC Message, RT Subaddress, BC End-of-Frame, Format Error, BC Status Set, RT Mode Code, MT Trigger, and End-of-Message.

For the Nano-ACE's Enhanced BC mode, there are four user defined interrupt bits. The BC Message Sequence Control Engine includes an instruction enabling it to issue these interrupts at any time.

For RT and Monitor modes, the Nano-ACE architecture includes an Interrupt Status Queue. This provides a mechanism for logging messages that result in interrupt requests. Entries to the Interrupt Status Queue may be filtered such that only valid and/or invalid messages will result in entries on the queue.

The Nano-ACE incorporates additional interrupt conditions beyond the ACE/Mini-ACE (Plus), based on the addition of Interrupt Mask Register #2 and Interrupt Status Register #2. This is accomplished by chaining the two Interrupt Status Registers using the INTERRUPT CHAIN BIT (bit 0) in Interrupt Status Register #2 to indicate that an interrupt has occurred in Interrupt Status Register #1. Additional interrupts include, "Self-Test Completed", masking bits for the Enhanced BC Control Interrupts, 0% Rollover interrupts for RT Command Stack, RT Circular Buffers, MT Command Stack, and MT Data Stack; BC Op Code Parity Error, (RT) Illegal Command, (BC) General Purpose Queue or (RT/MT) Interrupt Status Queue Rollover, Call Stack Pointer Register Error, BC Trap Op Code, and the four User-Defined interrupts for the Enhanced BC mode.

8.5 BUILT-IN TEST

A salient feature of the Nano-ACE (BU-67753LC and BU-67833LC only) is its highly autonomous self-test capability. This includes both protocol and RAM self-tests. Either or both of these self-tests may be initiated by command(s) from the host processor.

The protocol test consists of a comprehensive toggle test of the terminal's logic. The test includes testing of all registers, Manchester decoders, protocol logic, and memory management logs. The protocol test will complete in 130 us with a 40 MHz clock.

There is also a separate built-in self-test (BIST) for the Nano-ACE's 4K x 17 or 32K x 17 shared RAM. This test consists of writing and then reading/verifying the two walking patterns "data = address" and "data = address inverted". For a Nano-ACE with 4K words of RAM, the RAM BIST takes 0.81ms with a 40 MHz clock. For a Nano-ACE with 32K words of RAM, the RAM BIST takes 6.5 ms with a 40 MHz clock.

The Nano-ACE built-in protocol and RAM test is performed automatically at power-up. In addition, the protocol or RAM self-tests may be initiated by a command from the host processor, via the START/RESET REGISTER. For RT mode, the terminal must be offline before self-test can be initiated. When RT HALT is enabled in configuration register #7, and a mode code command to initiate self-test is received, the RT will automatically go offline. It is then the responsibility of the host processor to invoke self-test. When using the BU-67833LC, there is a way for the host processor to also take the RT offline before initiating a self-test. This is done by setting the mode of operation in configuration register #1 from RT to BC. The results of the self-test are host accessible by means of the BIT status register. For RT mode, the result of the self-test may be communicated to the bus controller via bit 8 of the RT BIT word ("0" = pass, "1" = fail).

Assuming that the protocol self-test passes, all of the register and shared RAM locations will be restored to their state prior to the self-test, with the exception of the 60 RAM address locations 0342-037D and the TIME TAG REGISTER. Note that for RT mode, these locations map to the illegalization lookup table for "broadcast transmit subaddresses 1 through 30" (non-mode code subaddresses). Since MIL-STD-1553 does not define these as valid command words, this section of the illegalization lookup table is normally not used during RT operation. The TIME TAG REGISTER will continue to increment during the self-test.

If there is a failure of the protocol self-test, it is possible to access information about the first failed vector. This may be done by means of the Nano-ACE's upper registers (register addresses 32 through 63) which are defined in the EMACE User Guide.. Through these registers, it is possible to determine the self-test ROM address of the first failed vector, the expected response data pattern (from the ROM), the register or memory address, and the actual (incorrect) data value read from register or memory. The on-chip self-test ROM is 4K X 24.

Note that the RAM self-test is destructive. That is, following the RAM self-test, regardless of whether the test passes or fails, the shared RAM is not restored to its state prior to this test. Following a failed RAM self-test, the host may read the internal RAM to determine which location(s) failed the walking pattern test.

The definition of the bits in the BIT Test Status Flag register is as follows:

Table 46. BIT Test Status Flag Register (Read 1CH)

BIT	Description
15 (MSB)	Protocol Built-In Test Complete
14	Protocol Built-In Test In-Progress
13	Protocol Built-In Test Passed
12	CPU Write Abort
11	Auto-Initialization Complete (Note 1)
10	Auto-Initialization In-Progress (Note 1)
9	Auto-Initialization Passed (Note 1)
8	CPU Write Abort during Auto-Initialization (Note 1)
7	RAM Built-In Test Complete
6	RAM Built-In Test In-Progress
5	RAM Built-In Test In-Passed
4	CPU Write Abort during Built-in RAM Test (Note 1)
3	Model ID (Note 1)
2	Model ID (Note 1)
1	Model ID (Note 1)
0 (LSB)	Model ID (Note 1)

Note 1: Differs from EMACE User Guide

PROTOCOL BUILT-IN TEST COMPLETE: When set to a '1' indicates that the Protocol Built-in test has completed. Used in conjunction with bit 13 to flag the host that the Protocol Built-in Test passed or failed.

PROTOCOL BUILT-IN TEST IN-PROGRESS: When set to a '1' indicates that the Protocol Built-in test is running and that no SPI-writes should be attempted.

PROTOCOL BUILT-IN TEST PASSED: When set to a '1' and Protocol Built-in Test Complete bit is also a '1', indicates that the Protocol Built-in Test passed. If set to a '0'

and Protocol Built-in Test Complete bit is set to a '1' indicates the Protocol Built-in Test has failed.

CPU WRITE ABORT: When set to a '1', indicates that a SPI-write was attempted when the Protocol Built-in Test was in progress, thus aborting the Protocol Built -in Test.

AUTO-INITIALIZATION COMPLETE: When set to a '1' indicates that the Auto-Initialization has completed. Used in conjunction with bit 9 to flag the host that Auto-Initialization was successful or failed.

AUTO-INITIALIZATION IN-PROGRESS: When set to a '1' indicates that Auto-Initialization is in progress and that no SPI-writes should be attempted.

AUTO-INITIALIZATION PASSED: When set to a '1' and Auto-Initialization Complete bit is also a '1', indicates that Auto-Initialization completed successfully. If set to a '0' and the Auto-Config Complete bit is set to a '1' indicates that Auto-Initialization has failed.

CPU WRITE ABORT DURING AUTO-INITIALIZATION: When set to a '1', indicates that SPI-write was attempted when the Auto-Initialization was in progress, thus aborting Auto-Initialization. When Auto-Initialization is aborted, all registers are rest to their default values.

MODEL ID: Bits 4, 3, 2 and 1 used to identify the NANO-ACE models as a BU-67753LC, BU-67833LC or a BU-67743LC. These bits can be used to verify the SPI interface can access registers. The Model IDs are defined below:

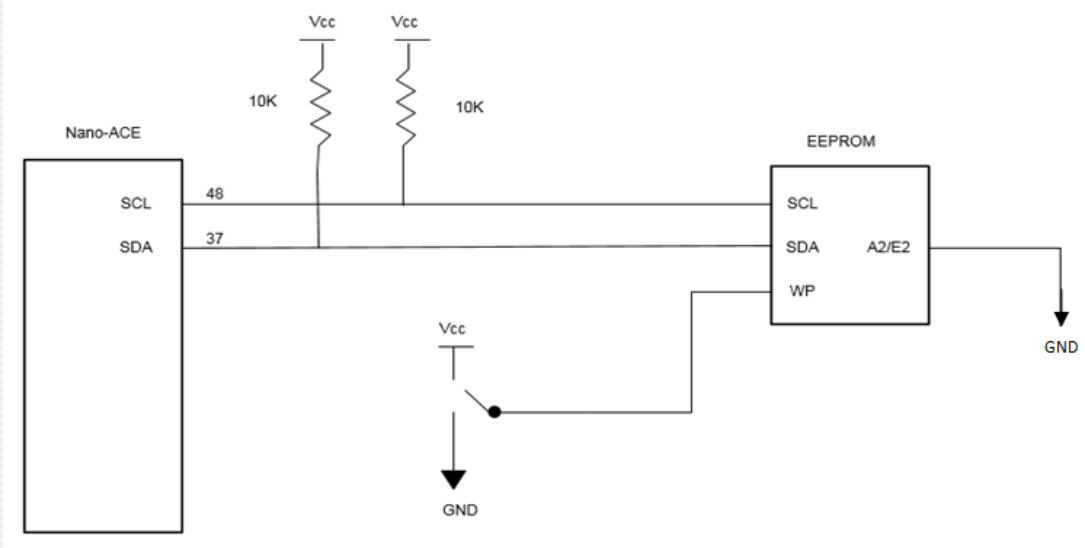
"0000" - BU-67743LC
"1001" - BU-67753LC
"1111" - BU-67833LC

8.6 AUTO-INITIALIZATION OPTION

The BU-67753L and BU-67833L implement an auto-initialization feature that utilizes an I2C interface to read device configuration information from a non-volatile memory and autonomously initialize the Nano-ACE's configuration registers and selected memory locations. The traditional method for initializing a MIL-STD-1553 controller is for host processor software to perform the necessary write operations to the Nano-ACE's registers and memory. Some systems have requirements for an LRU to begin responding to commands on the 1553 bus within a specified period of time following application of power. There are situations where the power-up timeline creates challenges due to the amount of time required to boot the processor and supporting subsystem. The Auto-Initialization feature allows a user to configure the Nano-ACE for

communication without intervention by the host processor, thus alleviating power-on timing constraints.

For Auto-Initialization, an EEPROM is recommend for use as the non-volatile memory as shown in Figure 13. In this figure, the EEPROM pin WP (Write Protect) must be set to a '0' when the host is writing configuration data. Otherwise, the WP may be set to a '1' to disable write operations. The pin A2/E2 on the EEPROM must be grounded.



Note: the Pull-up Resistors are 10K maximum

Figure 13. Nano-ACE Interface to EEPROM

Immediately following the release of the hardware reset input on power up, the Nano-ACE will execute an autonomous built-in self-test (BIST) of both Protocol and RAM. While the BIST is being executed, the Nano-ACE will interrogate the I2C interface as follows:

- Sense the level on Pin 48 (SDA). If '0', no I2C EEPROM is preset, skip Auto-Config. If ‘1’, then go to the next step.
- Issue a soft reset to I2C EEPROM to initialize I2C EEPROM state machine (see Figure 14).

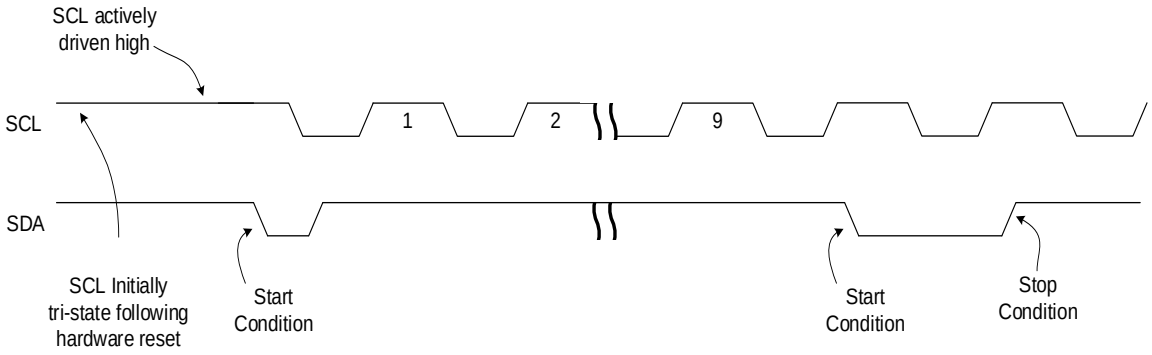


Figure 14. Soft Reset Timing

- Sense the level on Pin 37 (SDA). If '0', no I2C EEPROM is present, skip Auto-Initiation. If ‘1’, then go to the next step.

- Read I2C EEPROM word 0 and 1 starting at location 0000. Expect ID words:
  - 4DDC Hex
  - EACE Hex

  If ID words are not correct, skip Auto-Initialization. If the expected ID words are read, then go to the next step.

- Wait for BIST to Complete. If either Protocol or RAM self-test fails, the Nano-ACE will generate a reset (which will clear all internal registers to their default values) and skip Auto-Initialization. If BIST passes, then go the next step.

- After successful completion of BIST, the Auto-Initialization will commence. The Nano-ACE will read successive locations in the I2C EEPROM and load memory and/or registers as specified by “load records”. Each load record consists of a Control Word, a destination address word, and N number of data words (see section 8.7.1 for a detailed description of the load records including the Control Word).

- If an error occurs when reading I2C EEPROM, the Nano-ACE will end Auto-Initialization and issue a reset and the registers will be set to their default initial values.

- Reading of the I2C EEPROM and storing the data in the appropriate locations in the Nano-ACE will continue until the value "C0DE" Hex is read. "C0DE" Hex identifies the end of file (EOF) in the I2C EEPROM.

- After "C0DE" Hex is read, the Nano-ACE will read a CHECKSUM immediately following “CODE” in the I2C EEPROM. The CHECKSUM read from the I2C EEPROM must equal the CHECKSUM calculated by the Nano-ACE during the sequential read. If a CHECKSUM error occurs, the Nano-ACE will issue a reset and the registers will be set to their default initial values.

The power-up timeline of the Nano-ACE is illustrated in Figure 15

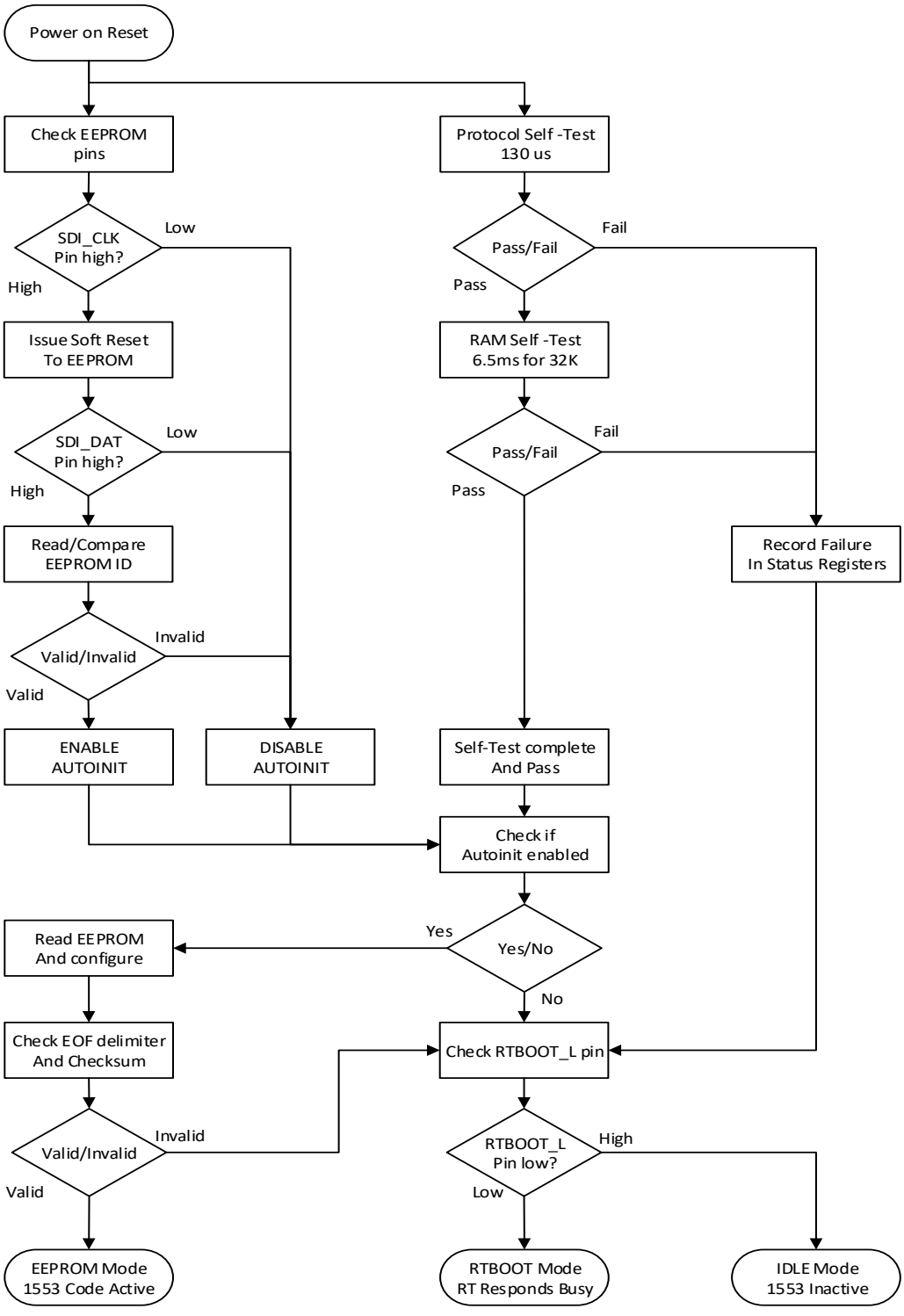


Figure 15. Power up initialization flow chart

Note: Timing specification to transfer 256 words from I2C EEPROM to Nano-ACE is 4.644 us

The Nano-ACE flags errors and gives status of on the progress of the BIST and Auto-Initialization through two registers (BIT Test Status and I2C EEPROM Control/Status registers). Status and progress information can be gained by reading these registers.

Note, that a write by the Host to memory or registers during BIST or Auto-Initialization will abort their process and cause a reset of all registers to their default value. Reading memory or registers during BIST or Auto-Initialization will have no effect on the Nano-ACE's execution of these functions.

Note: I2C EEPROM Control/Status register has a different definition when written.

When reading the Control/Status register, the bit definition is defined as:

Table 47. I2C EEPROM Status (31H) (Read)

BIT	Description
15 (MSB)	I2C EEPROM Idle
14	I2C EEPROM Code bit 2
13	I2C EEPROM Code bit 1
12	I2C EEPROM Code bit 0
11	I2C EEPROM Operation Complete (Host)
10	I2C EEPROM Operation Active (Host)
9	I2CEEPROM Operation bit 1
8	I2C EEPROM Operation bit 0
7	I2C EEPROM Error 1
6	I2C EEPEOM Error 2
5	Boot Active
4	Boot Code bit 3
3	Boot Code Bit 2
2	Boot Code bit 1
1	Boot Code bit 0
0 (LSB)	I2C EEPROM Address MSB bit

I2C EEPROM IDLE: This bit identifies if a transaction to/from the external I2C EEPROM is in process. This bit being set to a '1' indicates EEPROM is being access, while a '0' indicates the EEPROM is not being accessed.

I2C EEPROM CODES: Bits 14, 13 and 12, gives the Host information on I2C interface to the external EEPROM that is useful for debugging. Where a code of:

"000" - Indicates that the I2C EEPROM interface is operating without and issues.
"001" - Indicates that during Auto-Initialization the SCL pin to the external EEPROM is grounded and therefore an external EEPROM is not present.
"010" - Indicates that during Auto-Initialization the SDA pin to the external EEPROM is grounded and therefore an external EEPROM is not present.
"011" - Indicates a fault in the transaction to/from the EEPROM. For this code the device address byte (write) was not ACK by the I2C EEPROM during transfer (SDA bit 9 is not '0'.)
"100" - Indicates a fault in the transaction to/from EEPROM. For this code the MSB Address was not ACK by the EEPROM during transfer (SDA bit after A8 is not '0')
"101" - Indicates a fault in the transaction to/from EEPROM. For this code the LSB Address was not ACK by the EEPROM during transfer (SDA bit after A0 is not '0')
"110" - Indicates a fault in the transaction to/from EEPROM. For this code the device address byte (read) was not ACK by the EEPROM during transfer (SDA bit 9 is not '0')
"111" - Indicates a fault in the transaction to/from EEPROM. For this code, the Device ID was not 4DDC Hex as expected

I2C EEPROM OPERATION COMPLETE: During EEPROM code development, this bit indicates if a read or write operation to the EEPROM by the User has completed. When a User initiates a transfer to/from EEPROM, this bit must be polled to verify it is set to a '1' before another transfer to EEPROM is initiated.

I2C EEPROM OPERATION ACTIVE: During EEPROM code development, this bit indicates if a read or write operation to the EEPROM by the User is in progress. This bit if set to a '1' indicates transfer is still in progress.

I2C EEPROM OPERATION: Bits 9 and 8, gives the Host/User information on what the last transfer to/from EEPROM. Where a code of:

"00" - Indicates that there was no previous transfer and the I2C. Expected state after reset
"01" - Indicates that the last transfer was a command to reset the EEPROM.
"10" - Indicates that the last transfer was a read from the EEPROM.
"11" - Indicates that the last transfer was a write to the EEPROM.

I2C EEPROM ERROR 1: This bit being set to a '1' indicates that the EEPROM did not respond with an ACK to a transfer as expected.

I2C EEPROM ERROR 2: This bit being set to a '1' indicates that the data written by the User to the EEPROM did not match the data that was read back by the Nano-ACE as part of its write verification.

BOOT ACTIVE: This bit being set to a '1' indicates that Self-Test or Auto-Initialization is in process. If there is an SPI write to the Nano-ACE with this bit is '1', the Auto-Initialization and/or Self-Test will not complete properly.

BOOT CODE: Bits 4, 3, 2 and 1, gives the Host information on Self-Test and Auto-Initialization that are useful for debugging. Where a code of:

"0000" - Indicates that Self-Test and Auto-Initialization are operating properly
"0001" - Indicates that Protocol Self-Test aborted due to SPI write access
"0010" - Indicates that the Internal RAM Test aborted due to SPI write access
"0011" - Indicates that Auto-Initialization aborted due to SPI write access
"0100" - Indicates the external EEPROM is not programmed or present
"0101" - Indicates a EEPROM read error (error in transfer)
"0110" - Indicates that ID word 1 read from the EEPROM does not equal to "4DDC" Hex
"0111" - Indicates that ID word 2 read from EEPROM does not equal to "EACE" Hex
"1000" - Indicates the Control word read from EEPROM was in error (incorrect format)
"1001" - Indicated the EEPROM checksum calculated by the Nano-ACE does not equal the checksum read from EEPROM
"1010" - Indicates a Protocol or internal RAM self-test failed
"1011" - Reserved
"1100" - Reserved
"1101" - Reserved
"1110" - Reserved
"1111" - Reserved

I2C EEPROM ADDRESS MSB BIT: Indicates the value set for the MSB bit of the EEPROM Address. When set to '1' Nano-ACE can access the upper 1Mbit of a 2Mbit EEPROM.

When writing the Control/Status register, the bit definition is defined as:

Table 48. I2C EEPROM Control (31H) (Write)

BIT	Description
15 (MSB)	Not Used
14	Not Used
13	Not Used
12	Not Used
11	Not Used
10	Not Used
9	Not Used
8	Not Used
7	Not Used
6	Not Used)
5	Not Used
4	I2C EEPROM Address MSB bit
3	Clears I2C EEPROM Status flags
2	Starts a Read from I2C EEPROM
1	Starts a Write to I2C EEPROM
0 (LSB)	I2C EEPROM Soft Reset

I2C EEPROM ADDRESS MSB BIT: Setting this to a '1' will allow access to upper 1Mbit of a 2Mbit external EEPROM. Setting bit to a '0' only allows access to the lower 1M bit of external EEPROM.

CLEARS I2C EEPROM STATUS FLAG: Setting this bit to a '1' will clears the values set in the I2C EEPROM STATUS register. Bit is self-clearing

STARTS A READ FROM I2C EEPROM. During EEPROM code development, setting this bit to a '1' will read the data stored in the EEPROM at the location set by the I2C EEPROM ADDRESS register. Bit is self-clearing.

STARTS A WRITE TO I2C EEPROM. During EEPROM code development, setting this bit to a '1' will write the I2C EEPROM DATA register to the EEPROM at the location set by the I2C EEPROM ADDRESS register. Bit is self-clearing.

I2C EEPROM SOFT RESET. During EEPROM code development, setting this bit to a '1' will issue a Soft Reset Command to the EEPROM. The Soft Reset re-initiates the I2C EEPROM's state machine. This bit is self-clearing.

8.7 I2C EEPROM

A 256K x 8 I2C EEPROM, that supports a data rate of 1MHz, is required for Auto-Initialization (such as the Atmel AT24CM02, or the ST STI_M24M02).

Errata

Details

Auto-Initialization of the Nano-ACE from an external I2C EEPROM preforms as designed, but reading and writing from the Host SPI to/from the I2C EEPROM to load the I2C EEPROM does not. Due to a timing issue, the reading and writing of the I2C EEPROM locations from the SPI Host will only be successful 98% of the time. The failure to successfully transfer EEPROM data to/from the SPI Host will be flagged in the I2C EEPROM Control/Status Register (31H) by bit 7. Bit 7 being set to a '1' in the I2C EEPROM Control/Status Register is defined as the I2C EEPROM did not respond with an ACK to a transfer. This errata, does not affect functionality of BC, RT or MT modes.

Workaround

It is recommended on all words read or written to the I2C EEPROM by the SPI Host that the I2C EEPROM Control/Status Register (31H) be read by the Host to verify if the operation was successfully. In the event the operation was unsuccessfully, the Host will need to retry the transfer. Since, Host access to the I2C EEPROM is only needed during development, performance of the device in BC, RT and MT modes will not be effected.

8.7.1 I2C EEPROM - Auto-Initialization: Reading Configuration Data

During Auto-Initialization, the Nano-ACE will read sequential locations from the EEPROM starting at location zero within the EEPROM. The Nano-ACE expects the EEPROM to contain the defined ID words, followed by N number of load records, followed by an End of File (EOF) delimiter and a checksum. The Nano-ACE's initial read from the EEPROM begins with a dummy write to the EEPROM to set the starting location (initially 0000h) for the subsequent read transactions. As bytes are read from the EEPROM, the EEPROM's internal address will automatically increment.

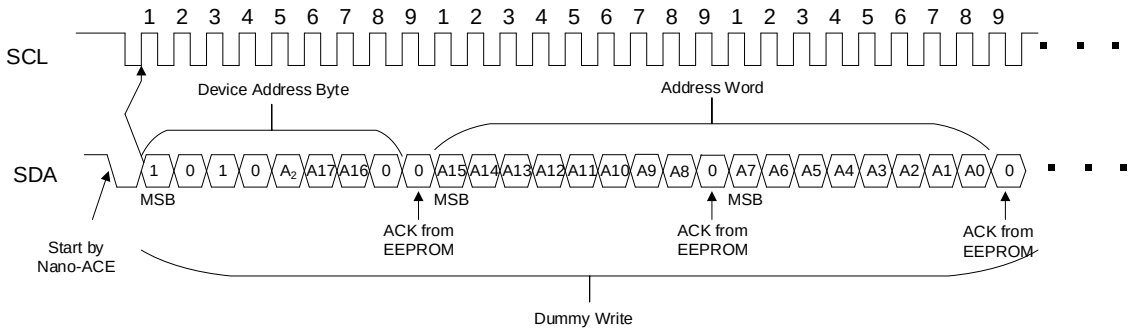


Figure 16. Dummy Write

Note that the A2(E2) input to the EEPROM must be set to a logic '0'.

The eighth bit in the Device Address Byte is the RD/WR bit, which is set to a '0' for a write and '1' for read. RD/WR bit will be set to logic ‘0’ for the dummy write transaction.

The EEPROM State Machine in the Nano-ACE starts at location zero, so A17:A0 in the dummy write will be "00000"Hex .

After the Dummy Write, a device address with the eighth bit set to '1' will be sent to the EEPROM to initiate a read operation. The Nano-ACE interprets data in the EEPROM as 16-bit words; therefore, an even number of 8-bit data bytes will be read. The Nano-ACE will also keep track of the EEPROM addresses, as the Nano-ACE will start its reads beginning at EPPROM address 00000H and will conclude reading when the end of file (EOF) delimiter is reached and the checksum word is read.

The first two words in the EEPROM must be the Nano-ACE’s ID words (as defined in section 8.6). After reading the ID words, the Nano-ACE will begin reading “load records” until an EOF delimiter is read. A load record begins with a control word followed by a destination address and a variable number of words. The control word contains a fixed signature that differentiates it from an EOF delimiter. The EEPROM image may contain multiple load records.

The load records allow the user to initialize selected locations in the Nano-ACE’s memory and register address space (rather than having to initialize every location), which can significantly reduce the initialize time. Refer to Figure 17 for an example of the Nano-ACE reading a load record containing one data word.

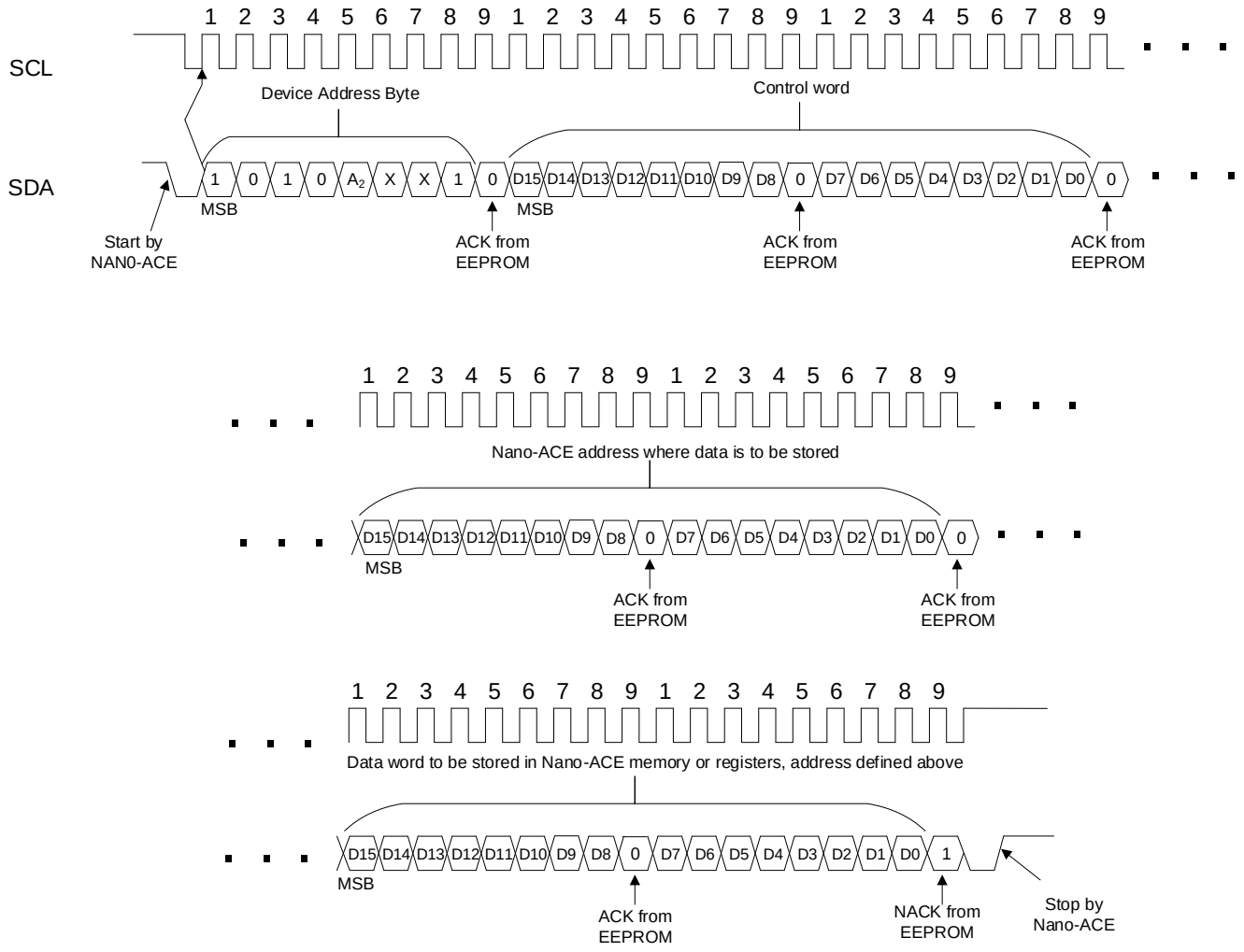


Figure 17. Read of a Load Record with one word

Where the Control Word is defined as:

D15							D8	D7	D0
1	0	0	0	0	0	0	Mem/Reg_L	Burst Count (words)	

Bits 15 to 9 are a set bit pattern to identify the word as a control word (as opposed to an ID word or end of file delimiter).

Bit 8 (Mem/Reg_L) defines whether the data read from the I2C EEPROM will be written to the Nano-ACE's Memory or Register space.

The Burst Count Field defines the number of Data Words that will be read from the I2C EEPROM as part of this load record, where maximum is 256 words (512 bytes). When multiple data words are read from the EEPROM they will be stored in sequential locations in the Nano-ACE memory or register space. The Nano-ACE will continue reading load records until an End of File Delimiter is read out of EEPROM

Example where Burst Count = 1 on each load record

Dummy Write (sets location in EEPROM to read to 00000H)
Read ID words (2 words or 4 bytes)
Read Control Word (defines if write to Nano-ACE is to Memory or Register)
Read address of where to store data in Memory or Register
Read 1 data word and store in location defined above
Read Control Word (defines if write to Nano-ACE is to Memory or Register)
Read address of where to store data in Memory or Register
Read 1 data word and store in location defined above

-
-
-
-

Read last Control Word
Read address of data to be stored
Read data word to be stored
Read End Delimiter "C0DE" Hex
Read Check Sum

Example of a Burst Count > 1

Dummy Write (sets location in EEPROM to read to 00000H)
Read ID words (2 16-bit words as 4 bytes)
Read Control Word (defines if write to Nano-ACE is to Memory or Register), decode Burst Count to identify how many data words to read
Read address of where to store first word of data in Memory or Register
Read 1 data word and store in location defined above (Nano-ACE destination address)
Read next data word, increment Nano-ACE destination address and write word to Memory or Register
Read next data word, increment Nano-ACE destination address and write word to Memory or Register

-
-
-

Read last data word of burst (current load record), increment Nano-ACE destination address and write word to Memory or Register
Read next Control Word (defines if write to Nano-ACE is to Memory or Register), decode Burst Count to identify how many data words to read in this load record
Read address of where to store first word of data in Memory or Register
Read 1 data word and store in location defined above (Nano-ACE destination address)
Read next data word, increment Nano-ACE destination address and write word to Memory or Register

-
-
-

Read next last data word of burst (current load record), increment Nano-ACE destination address and write word to Memory or Register

-
-
-

Read last Control Word (defines if write to Nano-ACE is to Memory or Register), decode Burst Count to identify how many data words to read
Read address of where to store first word of data in Memory or Register (Nano-ACE destination address)
Read 1 data word and store in Nano-ACE destination address
Read next data word, increment Nano-ACE destination address and write word to Memory or Register

-
-

Read next last data word of burst (current load record), increment Nano-ACE destination address and write word to Memory or Register
Read End Delimiter "C0DE" Hex
Read Check Sum

The User has the ability to read data from I2C EEPROM when Auto-Initiation is not active to verify the data loaded. (Note: Errata is applicable). A host initiated read of the EEPROM begins with a write to the I2C EEPROM Address register with the address of the location within EEPROM that the User wants to read followed by a write of a value 0004 to the I2C EEPROM Control/Status register. The write to the I2C EEPROM control/status register will command the Nano-ACE to read the requested location from the EEPROM and place the data is the I2C EEPROM Read Data register. After writing the I2C EEPORM control/status register the host may read the I2C EEPROM Read Data register to fetch the data from the requested location.

8.7.2 I2C EEPROM - Writing Configuration Data

The Nano-ACE provides the ability to write to the I2C EEPROM using the Nano-ACE's SPI interface through the use of three I2C registers within the Nano-ACE's register space. A host initiated EEPROM write transaction utilizes the I2C EEPROM Data Register, the I2C EEPROM Address Register, and the I2C EEPROM Control/Status Register. The host processor writes to the I2C EEPROM Data Register with the 16-bit data value to be written to the EEPROM. The host processor must also write EEPROM destination address into the I2C EEPROM Address Register. The host processor commands the Nano-ACE to write the data to the specified address by writing a value of 0001 to the I2C EEPROM Control/Status Register. (Note: Errata is applicable)

The following is an example of the steps required to write data to the I2C EEPROM:

1. Write "0001" Hex to I2C EEPROM Control/Status register to Reset the I2C EEPROM. Bit 0 in I2C EEPROM Control/Status register is self-clearing.

2. Write the data to be written to I2C EEPROM in the I2C Data register

3. Write address where the data is to be written to in I2C EEPROM in the I2C EEPROM Address register

4. Write "0002" Hex to Control/Status register to initiate the write to EEPROM for this one location. Note that bit 1 in I2C EEPROM Control/Status register is self-clearing so it is not necessary to write 0000 to the I2C EEPROM Control/Status register.

5. Read I2C EEPROM Control/Status register until a bit is set in bits 11, 7 or 6 (i.e. poll the register). If bit 11 is set to '1', the write to I2C EEPROM has been completed. If bits 7 and/or bit 6 are set to '1', an error has occurred when the Nano-ACE was writing to the I2C EEPROM.

6. If write is completed with no errors, the User has the option to verify data was written correctly to I2C EEPROM by reading the I2C EEPROM Write Data register to see if it matched the value of the data written.

7. Repeat from step 3 until I2C EEPROM is configured for Auto-Initialization (including end of file delimiter, "C0DE" Hex, and Check Sum).

Note: Writing "0008" Hex to I2C EEPROM Control/Status register clears error flags in said register. Bit 3 in I2C EEPROM Control/Status register is self-clearing

8.8 I2C EEPROM - Bus Signaling

I2C uses two open-drain signals with weak pull-ups to transfer data between a Master (Nano-ACE) and a Slave (EEPROM): SCL and SDA. SCL is the clock signal and SDA is the data signal. Both the SDA and SCL lines must have pull-up resistors (10K ohms maximum) to pull the signal high when not driven. In this application, SCL will be driven by the Nano-ACE, while both the EEPROM and the Nano-ACE will drive SDA at separate times. The SDA signal is synchronized to the SCL edges. Where SDA is sampled by the EEPROM and Nano-ACE on the rising edge of SCL and driven on the falling edge of SCL.

I2C Bus timing for EEPROM is defined as follows:

Table 49 for Figure 18 and Figure 19 I2C Bus Timing

REF	Description	Notes	3.3V Logic			Units
			MIN	TYP	MAX	
tclk	Clock Frequency, SCL		0.999950	1	1.000050	MHz
tlow	SCL pulse width low		450		550	ns
thigh	SCL pulse width high		450		550	ns
tAA	Clock low to data from Nano-ACE valid				75	ns
tsu.dat_in	Data out set-up time for Nano-ACE		50			ns

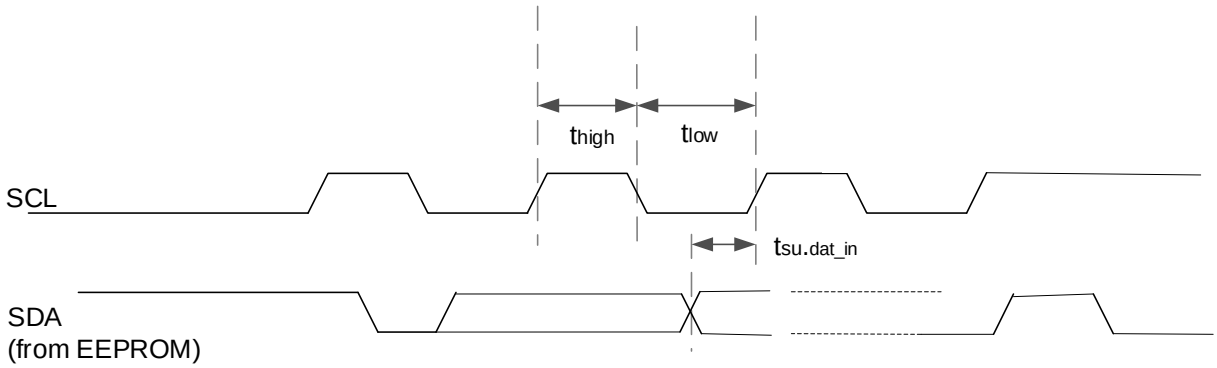


Figure 18. I2C Bus Timing: Transfer from Nano-ACE

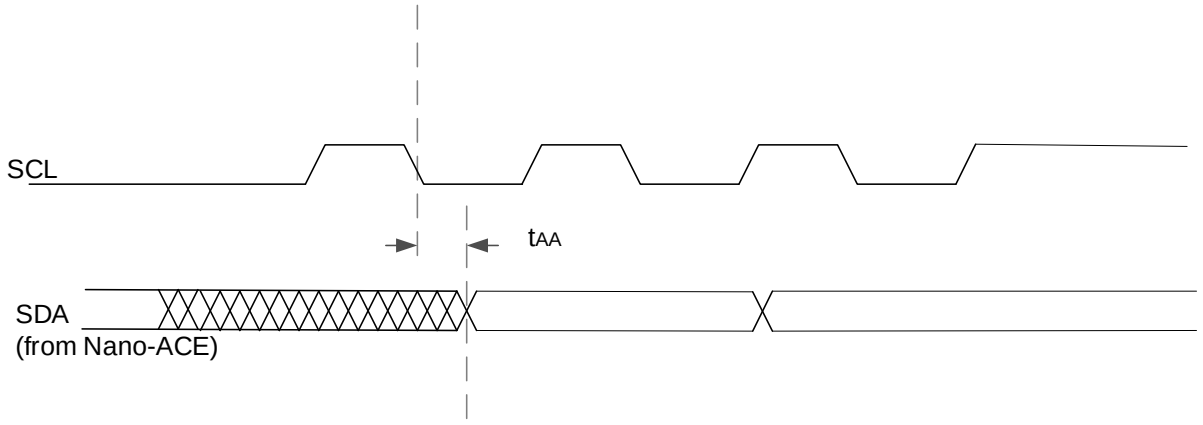


Figure 19. I2C Bus Timing: Transfer to Nano-ACE

8.9 RAM PARITY

The Nano-ACE is available with options for 4K (BU-67753L) or 32K words (BU-67833L) of internal RAM, both of which are 17 bits wide. The internal RAM allows for parity generation for RAM write accesses, and parity checking for RAM read accesses. This includes host RAM accesses, as well as accesses by the Nano-ACE's internal logic. When the Nano-ACE detects a RAM parity error, it reports it to the host processor by means of an interrupt and a register bit. Also, for the RT and Selective Message Monitor modes, the RAM address where a parity error was detected will be stored on the Interrupt Status Queue (if enabled). Note that the BU-67743L implements a 16-bit wide SRAM and as such does not support RAM parity.

8.10 RELOCATABLE MEMORY MANAGEMENT LOCATIONS

In the Nano-ACE's default configuration, there is a fixed area of shared RAM addresses, 0000h-03FF, that is allocated for storage of the BC's or RT's pointers, counters, tables, and other "non-message" data structures. As a means of reducing the overall memory address space for using multiple Nano-ACE's in a given system (e.g., for use with the DMA interface configuration), the Nano-ACE allows this area of RAM to be relocated by means of 6 configuration register bits. To provide backwards compatibility to ACE and Mini-ACE, the default for this RAM area is 0000h-03FFh.

8.11 HOST PROCESSOR INTERFACE

The Nano-ACE® is optimized to require the minimum number of signal pins to communicate with the host processor by using a Synchronous Peripheral Interface (SPI) connection.

The SPI connection consists of 4 wires: a Serial Clock (SCK) supplied by the host, a Slave Select (SS) line supplied by the host, a Master-Out-Slave-In (MOSI) data line supplied by the host, and a Master-In-Slave-Out (MISO) data line supplied by the Nano-Ace. The Nano-Ace supports operation in the CPOL=0, CPHA=0 and CPOL=1, CPHA=1 modes.

Figure 20 illustrates a generic connection diagram between a microprocessor and a Nano-ACE, while Figure 21, Figure 22 and the associated table illustrate the required SPI bus timing.

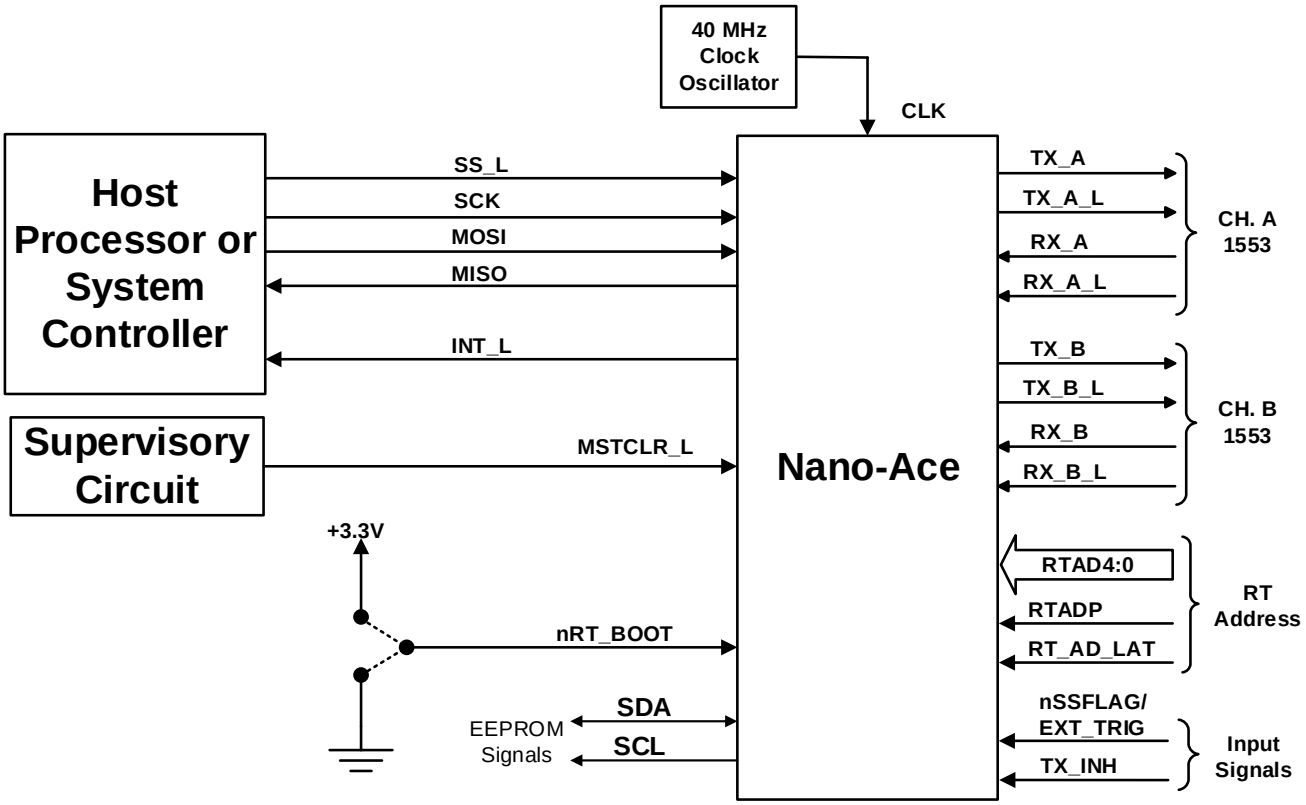


Figure 20. SPI Host Processor Interface

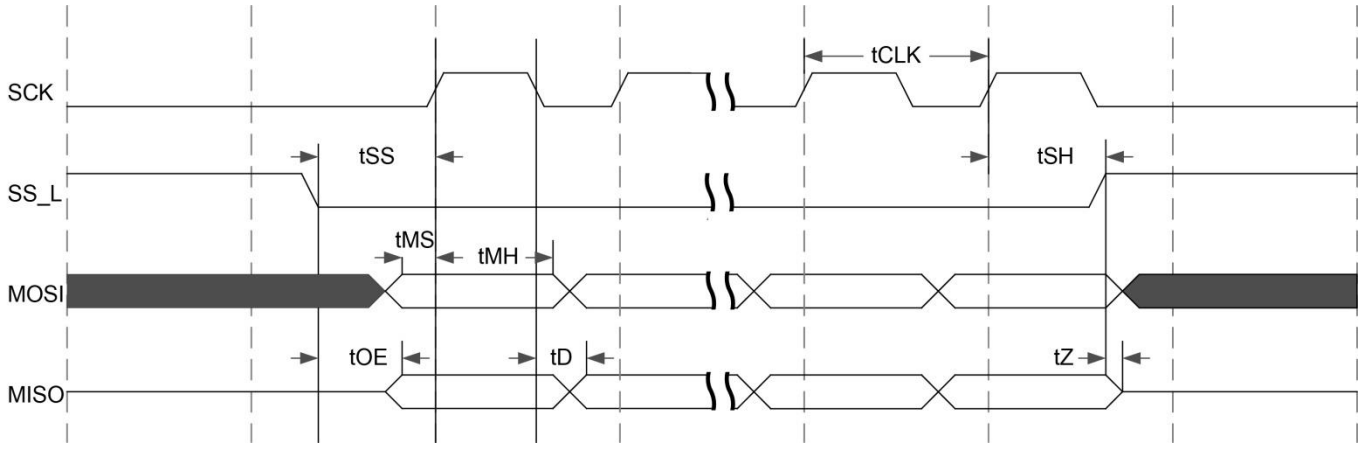


Figure 21. SPI Bus Timing CPOL=0, CPHA=0

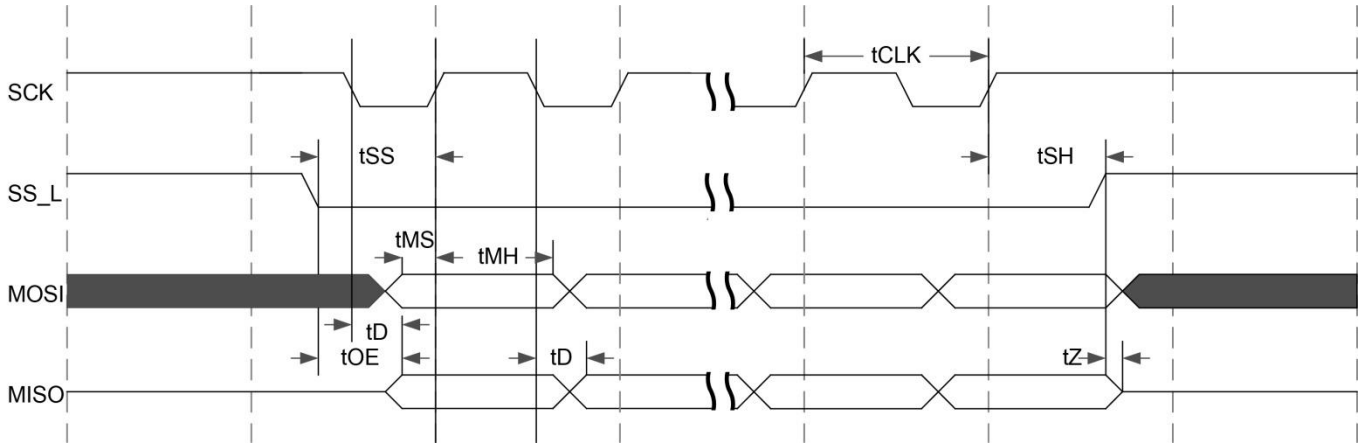


Figure 22. SPI Bus Timing CPOL=1, CPHA=1

Table 50 for Figure 21 and Figure 22 SPI Bus Timing

REF	Description	Notes	3.3V Logic			Units
			MIN	TYP	MAX	
tCLK	SCK period		20			ns
tSS	SS setup time prior to SCK rising edge		9.0			ns
tSH	SS hold time following SCK rising edge		9.0			ns
tMS	MOSI setup time prior to SCK rising edge		2.5			ns
tMH	MOSI hold time following SCK rising edge		0.5			ns
tD	SCK falling edge to MISO stable delay				6.0	ns
tOE	Falling edge of SS_L to MISO stable delay				5.0	ns
tZ	Rising edge of SS_L to MISO high impedance delay				2.0	ns

The Nano-Ace® treats the SPI interface as a multi-drop bus, and will keep the MISO output tri-stated unless the SS line is active (low). It will also ignore any transitions on the SCK line and all data on the MOSI line unless SS is active. Once SS is active, MOSI data is sampled on the rising edge of SCK and MISO data is supplied on the falling edge of SCK. SS must remain active for the full duration of a particular transfer, as the SPI interface is reset by the rising edge of SCK if SS is inactive (high).

The Nano-Ace® supports Simple, Single, and Burst transfers to both Memory and Registers. All transfers begin with a Control byte on the MOSI line that specifies the type and direction of the transfer. The Basic Addressing Control byte defined in Figure 23 is used to address registers and the first 4K of memory. The Basic Addressing Control byte contains the upper 4 bits of address lines used to access up to 4k of internal RAM. Following this control byte will be an additional one byte of address. The Extended Addressing Control byte shown in Figure 24 is used to address memory locations beyond 4K and is identified by bits 7 and 6 being set to "11". The Extended Addressing Control byte is followed by two address bytes.

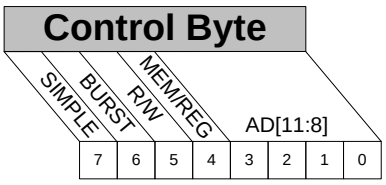


Figure 23. SPI Control Byte (Basic Addressing)

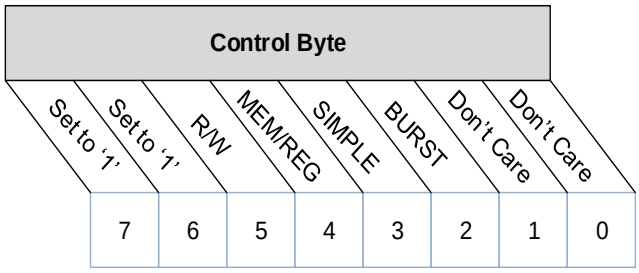


Figure 24. SPI Control Byte (Extended Addressing)

Both types of control bytes have a R/W bit, MEM/REG bit, SIMPLE bit and BURST bit. The R/W and MEM/REG bits identify if the transaction from the Host will be a read from memory or registers, or a write to memory or registers. The SIMPLE and BURST bits identify the transfer types from the Host (Simple, Single, and Burst).

Table 51 provides a summary of control byte values and the resulting transaction type specified by the control byte values.

Table 51. SPI Control Byte Description

SPI Control Byte								Description
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	BIT 1	BIT 0	
0	0	0	0	x	x	x	x	Basic Addressing, Single mode, write to reg
0	0	0	1	AD11	AD10	AD9	AD8	Basic Addressing, Single mode, write to mem
0	0	1	0	x	x	x	x	Basic Addressing, Single mode, read from reg
0	0	1	1	AD11	AD10	AD9	AD8	Basic Addressing, Single mode, read from mem
0	1	0	0	x	x	x	x	Basic Addressing, Burst mode, write to reg
0	1	0	1	AD11	AD10	AD9	AD8	Basic Addressing, Burst mode, write to mem
0	1	1	0	x	x	x	x	Basic Addressing, Burst mode, read from reg
0	1	1	1	AD11	AD10	AD9	AD8	Basic Addressing, Burst mode, read from mem
1	0	0	0	x	x	x	x	Basic Addressing, Simple mode, write to reg
1	0	0	1	AD11	AD10	AD9	AD8	Basic Addressing, Simple mode, write to mem
1	0	1	0	x	x	x	x	Basic Addressing, Simple mode, read from reg
1	0	1	1	AD11	AD10	AD9	AD8	Basic Addressing, Simple mode, read from mem
1	1	0	0	0	0	x	x	Extended Addressing, Single mode, write to reg
1	1	0	0	0	1	x	x	Extended Addressing, Burst mode, write to reg
1	1	0	0	1	0	x	x	Extended Addressing, Simple mode, write to reg
1	1	0	0	1	1	x	x	Reserved (Not Valid)
1	1	0	1	0	0	x	x	Extended Addressing, Single mode, write to mem
1	1	0	1	0	1	x	x	Extended Addressing, Burst mode, write to mem
1	1	0	1	1	0	x	x	Extended Addressing, Simple mode, write to mem
1	1	0	1	1	1	x	x	Reserved (Not Valid)
1	1	1	0	0	0	x	x	Extended Addressing, Single mode, read from reg
1	1	1	0	0	1	x	x	Extended Addressing, Burst mode, read from to reg
1	1	1	0	1	0	x	x	Extended Addressing, Simple mode, read from reg

Table 51. SPI Control Byte Description								
SPI Control Byte								Description
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	BIT 1	BIT 0	
1	1	1	0	1	1	x	x	Reserved (Not Valid)
1	1	1	1	0	0	x	x	Extended Addressing, Single mode, read from mem
1	1	1	1	0	1	x	x	Extended Addressing, Burst mode, read from mem
1	1	1	1	1	0	x	x	Extended Addressing, Simple mode, read from mem
1	1	1	1	1	1	x	x	Reserved (Not Valid)

8.11.1 Simple Transfers

A simple transfer is made up of 6 byte transfers organized as 3 word (16-bit) transfers for a register transfer or a transfer to a Nano-ACE with 4K words of RAM using basic addressing. A simple transfer to the RAM in a Nano-ACE with 32K words of RAM is made up of 7 byte transfers using extended addressing.

For a read transaction from registers or from a 4K RAM, the control word is configured with the Simple bit set to ‘1’, the Burst bit set to ‘0’, and the R/W bit set to ‘1’. The Control and Address are provided in the first word transmitted on MOSI (Control byte as byte 1 and Address[7:0] as byte 2), and are echoed back in the second word (bytes 3 and 4) received on MISO, with the read data provided in the third word received on MISO (Data[15:8] in byte 5 and Data[7:0] in byte 6).

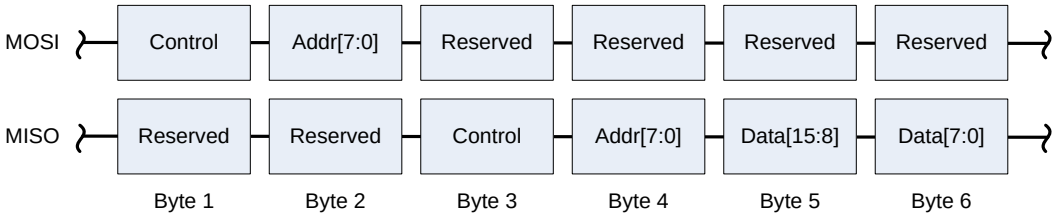


Figure 25. Simple Read (Basic Addressing)

Figure 26 illustrates a simple read transfer from a Nano-ACE’s 32K word RAM using extended addressing. The key difference between Figure 25 and Figure 26 is the insertion of Addr[15..8] as byte 2 in the transfer, which specifies the upper bits of the RAM address.

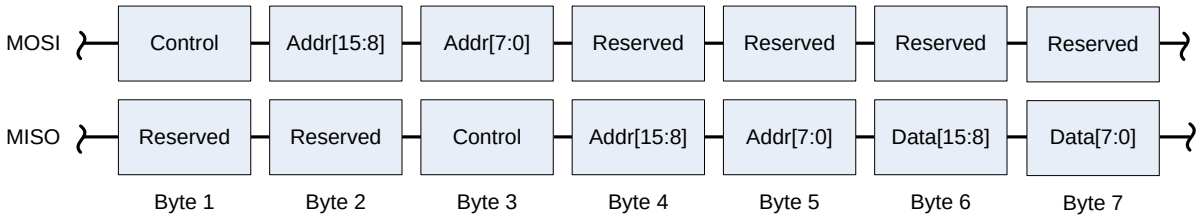


Figure 26. Simple Read (Extended Addressing)

For a write transaction to registers or to a 4K RAM, the control word is configured with the Simple bit set to '1', the Burst bit set to '0', and the R/W bit set to '0'. The Control and Address are provided in the first word transmitted on MOSI (Control byte as byte 1 and Address[7:0] as byte 2), and are echoed back in the second word (bytes 3 and 4) received on MISO. The write data is provided in the second word transmitted on MOSI (Data[15:8] in byte 3 and Data[7:0] in byte 4]), and is echoed back in the third word received on MISO (Data[15:8] in byte 5 and Data[7:0] in byte 6).

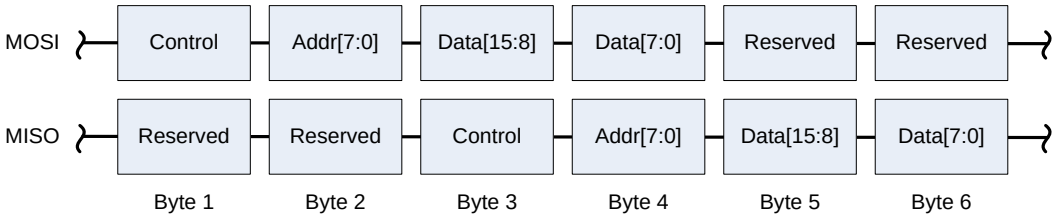


Figure 27. Simple Write (Basic Addressing)

Figure 28 illustrates a simple write transfer to a Nano-ACE with 32K words of RAM. Note that the transfer contains an extra address byte as compared to Figure 27.

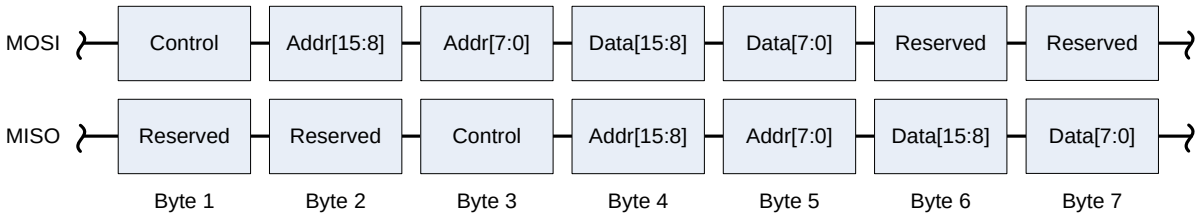


Figure 28. Simple Write (Extended Addressing)

8.11.2 Single Transfers

A single transfer packs the data more tightly in individual byte transfers rather than maintaining word alignment. This doesn't affect read latency, but it allows writes to registers or 4K word RAM to complete in only 4 byte transfers while write transfers to 32K SRAM complete in 5 byte transfers.

For a read transaction from registers or from a 4K RAM, the control word is configured with the Simple bit set to '0', the Burst bit set to '0', and the R/W bit set to '1'. The Control is provided in the first byte transmitted on MOSI and is echoed back in the second byte received on MISO. Address[7:0] is transmitted in the second byte on MOSI and echoed back in the third byte on MISO, with Data[15:8] provided on MISO in byte 5 and Data[7:0] in byte 6.

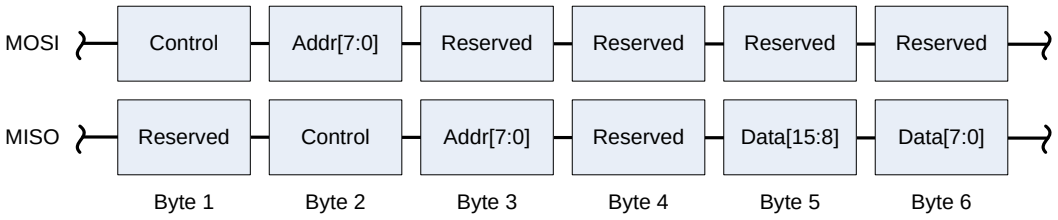


Figure 29. Single Read (Basic Addressing)

A single read transaction from a 32K RAM, as shown in Figure 30, consists of 7 byte transfers.

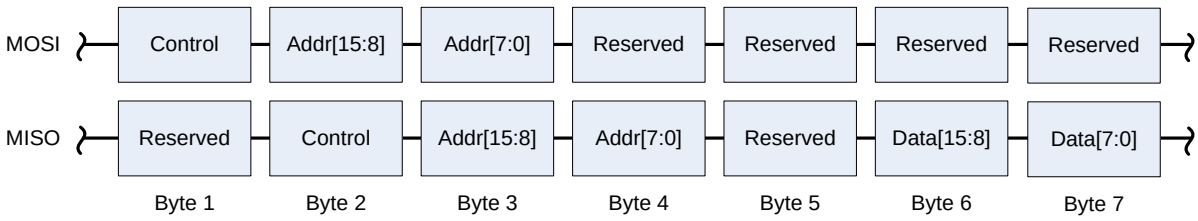


Figure 30. Single Read (Extended Addressing)

For a write transaction to registers or to a 4K RAM, the control word is configured with the Simple bit set to '0', the Burst bit set to '0', and the R/W bit set to '0'. The Control is provided in the first byte transmitted on MOSI and is echoed back in the second

byte received on MISO. Address[7:0] is transmitted in the second byte on MOSI and echoed back in the third byte on MISO. The Data[15:8] is written to MOSI in byte 3 and echoed back on MISO in byte 4, while Data[7:0] is written to MOSI in byte 4,

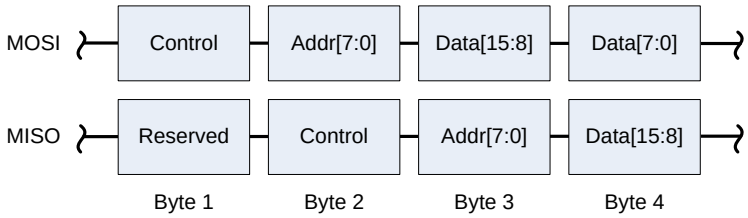


Figure 31. Single Write (Basic Addressing)

A single write transaction to a 32K RAM, as shown in Figure 32, consists of 5 byte transfers.

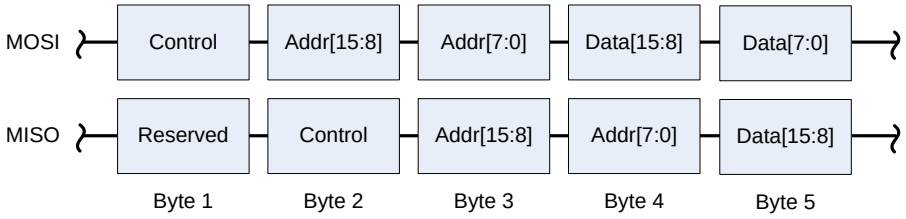


Figure 32. Single Write (Extended Addressing)

8.11.3 Burst Transfers

A burst transfer allows large chunks of data to be read or written more efficiently, as the control and address information only needs to be provided once for a burst of up to 256 16-bit words.

For a read transaction from registers or from a 4K RAM, the control word is configured with the Simple bit set to ‘0’, the Burst bit set to ‘1’, and the R/W bit set to ‘1’. The Control is provided in the first byte transmitted on MOSI and is echoed back in the second byte received on MISO. Address[7:0] is transmitted in the second byte on MOSI and echoed back in the third byte on MISO. The Burst count is then provided in the third word on MOSI and echoed as the fourth word received on MISO. After that the data is streamed on MISO, with Data[15:8] provided in byte 5 and Data[7:0] in byte

6 for the first address, Data[15:8] in byte 7 and Data[7:0] in byte 8 for the second address, and so on.

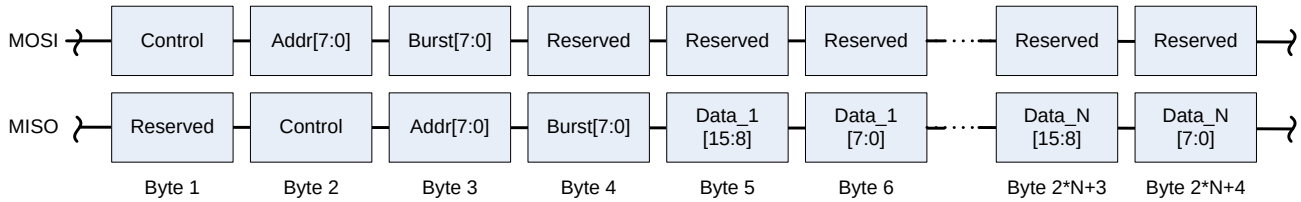


Figure 33. Burst Read (Basic Addressing)

A burst read transaction from a 32K RAM, as shown in Figure 34Figure 30, includes an extra address byte as compared to a burst from a 4K RAM.

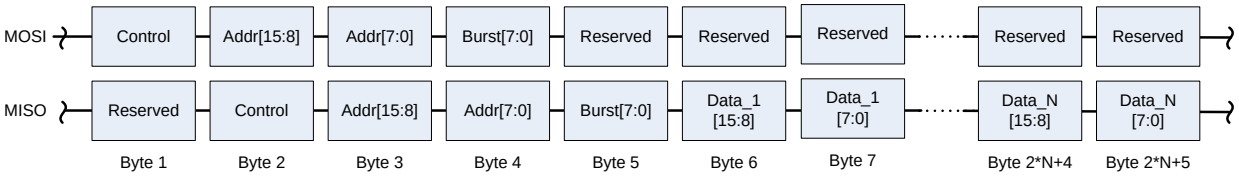


Figure 34. Burst Read (Extended Addressing)

For a write transaction to registers or to a 4K RAM, the control word is configured with the Simple bit set to ‘0’, the Burst bit set to ‘1’, and the R/W bit set to ‘0’. The Control is provided in the first byte transmitted on MOSI and is echoed back in the second byte received on MISO. Address[7:0] is transmitted in the second byte on MOSI and echoed back in the third byte on MISO. The Burst count is transmitted in the third byte sent on MOSI and echoed back in the fourth byte received. The Data to be written is streamed, with Data[15:8] of the first word on MOSI in byte 4 and echoed back on MISO in byte 5, while Data[7:0] is written to MOSI in byte 5 and echoed on MISO in byte 6. The second word is then sent on MOSI in bytes 6 and 7 and echoed back on MISO with a one byte delay, and so on until all words are sent. Note that the lower byte of the final word is not echoed back.

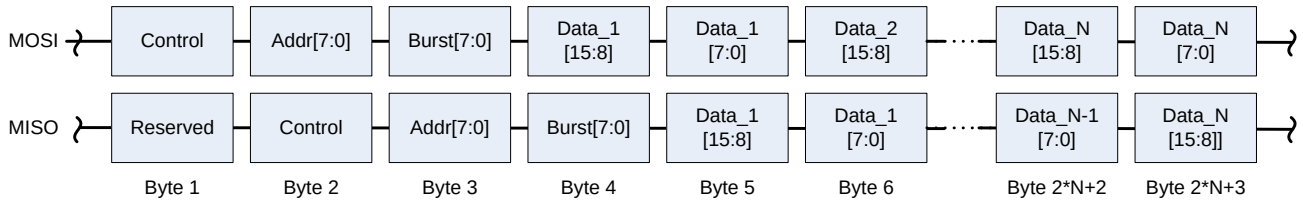


Figure 35. Burst Write (Basic Addressing)

A burst read transaction from a 32K RAM, as shown in Figure 36Figure 30, includes an extra address byte as compared to a burst to a 4K RAM.

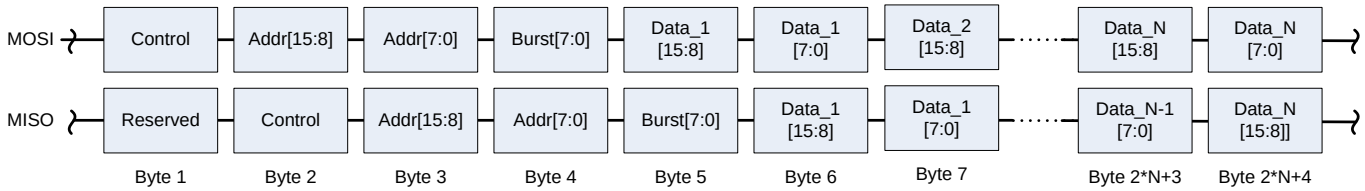


Figure 36. Burst Write (Extended Addressing)

8.12 +3.3 VOLT INTERFACE TO MIL-STD-1553 BUS

8.12.1 Interface to MIL-STD-1553 Bus

Figure 37 illustrate the two possible interface methods between the internal transceiver of the Nano-Ace® and a MIL-STD-1553 bus. Connections for both direct (short stub, 1:2.65) and transformer (long stub, 1:2.07) coupling, as well as nominal peak-to-peak voltage levels at various points (when transmitting), are indicated in the diagram.

The center tap of the primary winding (the side of the transformer that connects to the Nano-Ace) must be directly connected to ground.

Additionally, during transmission, large currents flow from the transceiver power supply, through the TX/RX pins into the transformer primaries and then out the center tap into the ground plane. The traces on this path should be sized accordingly and the connections to the ground plane should be as short as possible. A 10uF, low inductance tantalum or ceramic capacitor and a 0.01uF ceramic capacitor must be mounted as close as possible and with the shortest possible leads to the transceiver power inputs of the Nano-Ace.

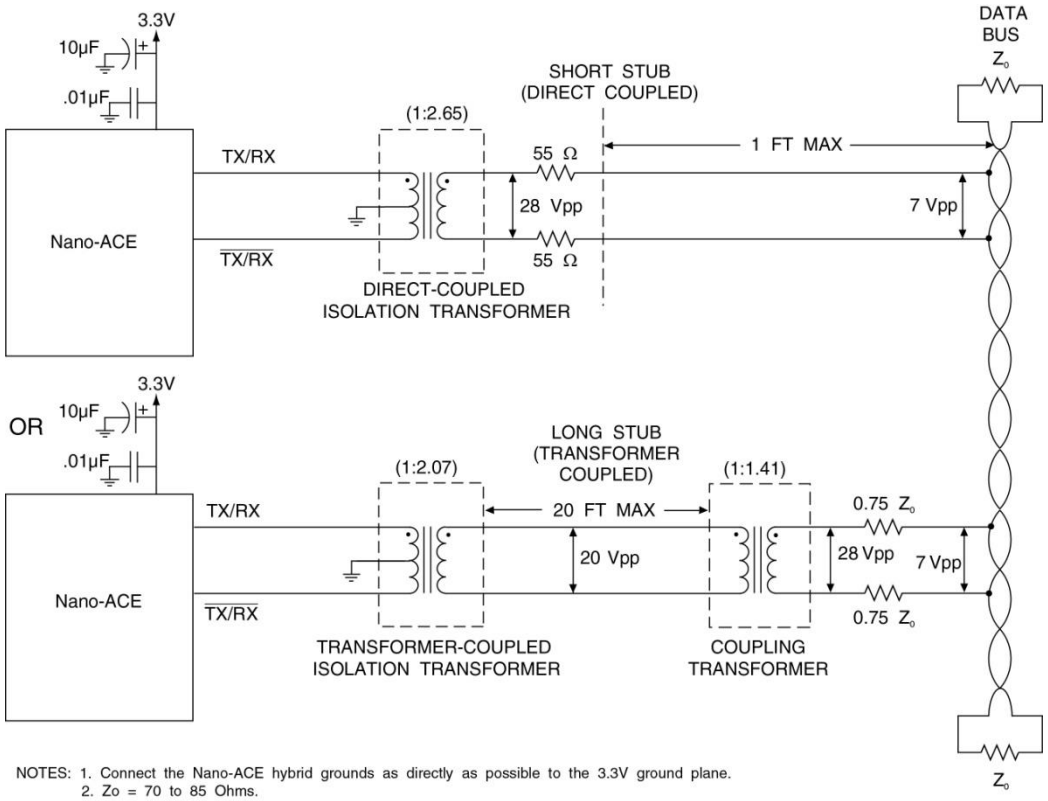


Figure 37. Nano-ACE Interface to MIL-STD-1553 Bus

8.12.2 Isolation Transformers

In selecting isolation transformers to be used with the Nano-Ace®, there is a limitation on the maximum amount of leakage inductance. If this limit is exceeded, the transmitter rise and fall times may increase, possible causing the bus amplitude to fall below the minimum level required by MIL-STD-1553.

In addition, an excessive leakage imbalance may result in a transformer dynamic offset that exceeds 1553 specifications. The maximum allowable leakage inductance is a function of the coupling method. For transformer coupled applications, it is a maximum of 5.0uH. For direct it is a maximum of 10.0uH, and is measured as follows:

The side of the transformer that connects to the Nano-Ace is defined as the “primary” winding. If one side of the primary is shorted to the primary center-tap, the inductance should be measured across the “secondary” (stub side) winding. This inductance must be less than 5.0 uH (Transformer Coupled) or 10.0 uH (Direct Coupled). Similarly, if the other side of the primary is shorted to the primary center-tap, the inductance measured across the “secondary” (stub side) winding must also be less than 5.0 uH (Transformer Coupled) or 10.0 uH (Direct Coupled).

The difference between these two measurements is the “differential” leakage inductance. This value must be less than 1.0 uH (Transformer Coupled) or 1.0 uH (Direct Coupled).

Beta Transformer Technology Corporation (BTTC), a subsidiary of DDC, manufactures transformers in a variety of mechanical configurations with the required turns ratios of 1:2.65 direct-coupled and 1:2.07 transformer coupled for the Nano-Ace. Table 52 provides a listing of these recommended transformers.

For further information, contact BTTC at 631-244-7393 or at www.bttc-beta.com.

Table 52. BTTC Transformers for use with Nano-Ace

BTTC Part Number	# of Channels, Configuration	Coupling Ratio Description	Coupling Ratio (1:x)	Mounting	Max Height	Width (Including Leads)	Length (Including Leads)
MLP-2030	Single	Direct	(1:2.65)	SMT	0.185”	0.4”	0.52”
MLP-2230	Single	Transformer	(1:2.07)	SMT	0.185”	0.4”	0.52”
LVB-4230	Single	Transformer	(1:2.07)	SMT	0.165”	1.125”	0.625”
DSS-3330	Dual (Side-by-Side)	Direct & Transformer	(1:2.65) & (1:2.07)	SMT	0.185”	0.52”	0.675”
DSS-1630	Dual (Side-by-Side)	Direct & Transformer	(1:2.65) & (1:2.07)	SMT	0.165”	0.72”	0.96”
DLVB-4230	Dual (Side-by-Side)	Transformer	(1:2.07)	SMT	0.165”	0.72”	0.96”
TSM-2230	Dual (Stacked)	Transformer	(1:2.07)	SMT	0.32”	0.4”	0.52”

8.13 THERMAL MANAGEMENT FOR NANO-ACE (48-Pad QFN Package)

Thermal management issues must be considered early in the design stage for MIL-STD-1553 terminals. The Nano-ACE® incorporates a center-pad heat sink on the bottom of the package which performs the dual function of transceiver circuit ground and thermal heat sink. Refer to the mechanical drawing in Figure 38 for the size and position of this pad. It is mandatory that this heat sink be directly soldered to a circuit ground/thermal plane (a circuit trace is insufficient). Operation without an adequate ground/thermal plane is not recommended and extended exposure to these conditions may affect device reliability.

The purpose of this ground/thermal plane is to conduct the heat being generated by the transceivers within the package and conduct this heat away from the Nano-ACE. In general, the circuit ground and thermal (chassis) ground are not the same ground plane. It is acceptable for the heat sink to be directly soldered to a ground plane but it must be located in close physical and thermal proximity ("0.003" pre-preg layer recommended) to the thermal plane.

8.14 Signal Descriptions by Functional Groups

Table 53. Power and Ground		
Signal Name	**Pad**	**Description**
+ 3.3V	5, 6, 11, 14, 22, 25, 31, 32, 40, 45	+ 3.3 Volt Power
Gnd	26, Heat sink	Ground. Heat sink pad must be connected to a thermal ground plane to dissipate heat and provide additional grounds.

Table 54. 1553 Stub Connection		
Signal Name	**Pad**	**Description**
TX_A (O)	38,39	1553 Transmit Outputs. Connect to primary winding of isolation transformer.
$\overline{\text{TX\_A (O)}}$	41,42	
TX_B (O)	43,44	
$\overline{\text{TX\_B (O)}}$	46,47	
RX_A (I)	24	1553 Receive Inputs. Connect to primary winding of isolation transformer.
$\overline{\text{RX\_A (I)}}$	23	
RX_B (I)	13	
$\overline{\text{RX\_B (I)}}$	12	

Table 55. Processor Interface		
Signal Name	**Pad**	**Description**
SCK (I)	27	SPI Serial Clock Data Clock from Host.
MISO (O)	28	SPI Master In Slave Out. Serial data from Nano-Ace to Host.
MOSI (I)	29	SPI Master Out Slave In. Serial data from Host to Nano-Ace
SS_L (I)	30	Slave Select. Active Low Select Signal for Nano-Ace SPI Interface.

Table 56. RT Address		
Signal Name	**Pad**	**Description**
RTAD4 (MSB) (I)	7	RT Address input. If bit 5 of Configuration Register #6, RT ADDRESS SOURCE, is programmed to logic "0" (default), then the Nano-ACE's RT address is provided by means of these 5
RTAD3 (I)	4	

Table 56. RT Address

Signal Name	Pad	Description
RTAD2 (I)	3	input signals. In addition, if RT ADDRESS SOURCE is logic "0", the source of RT address parity is RTADP. There are many methods for using these input signals for designating the Nano-ACE's RT address. For details, refer to the description of RT_AD_LAT. If RT ADDRESS SOURCE is programmed to logic "1", then the Nano-ACE's source for its RT address and parity is under software control, via data lines D5-D0. In this case, the RTAD4-RTAD0 and RTADP signals are not used.
RTAD1 (I)	2	
RTAD0 (LSB) (I)	1	
RTADP (I)	8	Remote Terminal Address Parity. This input signal must provide an odd parity sum with RTAD4-RTAD0 in order for the RT to respond to non-broadcast commands. That is, there must be an odd number of logic "1"s from among RTAD-4- RTAD0 and RTADP.
RT_AD_LAT (I)	9	RT Address Latch. Input signal used to control the Nano-ACE's internal RT address latch. If RT_AD_LAT is connected to logic "0", then the Nano-ACE RT is configured to accept a hardwired (transparent) RT address from RTAD4-RTAD0 and RTADP. If RT_AD_LAT is initially logic "0", and then transitions to logic "1", the values presented on RTAD4- RTAD0 and RTADP will be latched internally on the rising edge of RT_AD_LAT. If RT_AD_LAT is connected to logic "1", then the Nano-ACE's RT address is latchable under host processor control. In this case, there are two possibilities: (1) If bit 5 of Configuration Register #6, RT ADDRESS SOURCE, is programmed to logic "0" (default), then the source of the RT Address is the RTAD4-RTAD0 and RTADP input signals. (2) If RT ADDRESS SOURCE is programmed to logic "1", then the source of the RT Address is the lower 6 bits of the processor data bus, D5-D1 (for RTAD4- 0) and D0 (for RTADP). In either of these two cases (with RT_AD_LAT = "1"), the processor will cause the RT address to be latched by: (1) Writing bit 15 of Configuration Register #3, ENHANCED Mode ENABLE, to logic "1". (2) Writing bit 3 of Configuration Register #4, LATCH RT ADDRESS WITH CONFIGURATION REGISTER #5, to logic "1". (3) Writing to Configuration Register #5. In the case of RT ADDRESS SOURCE = "1", then the values of RT address and RT address parity must be written to the lower 6 bits of Configuration Register #5, via D5-D0. In the case where RT ADDRESS SOURCE = "0", the bit values presented on D5-D0 become "don't care".
$\overline{\text{RTBOOT}}$ (I)	15	If $\overline{\text{RTBOOT}}$ is connected to logic "0", the Nano-Ace will initialize in RT mode with the Busy status word bit set following power turn-on. If $\overline{\text{RTBOOT}}$ is hardwired to logic "1", the Nano-Ace will initialize in Idle mode.

Table 57. Miscellaneous		
Signal Name	**Pad**	**Description**
$\overline{\text{INT}}$ (O)	34	Interrupt Request output. If the LEVEL/ $\overline{\text{PULSE}}$ interrupt bit (bit 3) of Configuration Register #2 is logic "0", a negative pulse of approximately 500 ns in width is output on $\overline{\text{INT}}$ to signal an interrupt request. If LEVEL/ $\overline{\text{PULSE}}$ is high, a low level interrupt request output will be asserted on $\overline{\text{INT}}$. The level interrupt will be cleared (high) after either: (1) The processor writes a value of logic "1" to INTERRUPT RESET, bit 2 of the Start/Reset Register; or (2) If bit 4 of Configuration Register #2, INTERRUPT STATUS AUTO-CLEAR is logic "1" then it will only be necessary to read the Interrupt Status Register (#1 and/or #2) that is requesting an interrupt enabled by the corresponding Interrupt Mask Register. However, for the case where both Interrupt Status Register #1 and Interrupt Status Register #2 have bits set reflecting interrupt events, it will be necessary to read both interrupt status registers in order to clear $\overline{\text{INT}}$.
CLOCK_IN (I)	36	40 MHz clock input.
TX_INH (I)	10	Transmitter inhibit input for Channel A and Channel B, MIL-STD-1553 transmitters. For normal operation, this input should be connected to logic "0". To force a shutdown of Channel A and Channel B, a value of logic "1" should be applied to the TX_INH input.
$\overline{\text{MSTCLR}}$ (I)	35	Master Clear. Negative true Reset input, normally asserted low following power turn-on.
$\overline{\text{SSFLAG}}$ (I) / EXT_TRIG (I)	33	Subsystem Flag (RT) or External Trigger (Word Monitor) input. In RT mode, if this input is asserted low, the Subsystem Flag bit will be set in the Nano-ACE's RT Status Word. If the $\overline{\text{SSFLAG}}$ input is logic "0" while bit 8 of Configuration Register #1 has been programmed to logic "1" (cleared), the Subsystem Flag RT Status Word bit will become logic "1," but bit 8 of Configuration Register #1, $\overline{\text{SUBSYSTEM FLAG}}$, will return logic "1" when read. That is, the sense on the $\overline{\text{SSFLAG}}$ input has no effect on the SUBSYSTEM FLAG register bit. In the Word Monitor mode, if the external trigger is enabled (bit 7 of Configuration Register #1), a low to high transition on this input will initiate a monitor start. This input has no effect in Message Monitor mode.
SDA	37	I2C Interface for BU-67753LC and BU-67833LC only. These pins are ground pins on the BU-67743LC. SDA is Serial data line I/O and SCL is the serial clock line for an I2C interface to an external flash memory that can be used to implement the auto-initialization feature (see section 8.6). When not using an external flash memory device, these two signals must be tied to ground.
SCL	48	

Table 58. No User Connections		
Signal Name	**Pad**	**Description**
NC	16, 17, 18, 19, 20, 21	No User Connections to these balls allowed.

8.15 BU-67753L and BU-67833LC Pinout Table

Table 59. Nano-ACE Pinout					
Pad	**Signal**	**Notes**	**Pad**	**Signal**	**Notes**
1	RTAD0		25	+3.3V	
2	RTAD1		26	GND	
3	RTAD2		27	SCK	
4	RTAD3		28	MISO	
5	+3.3V		29	MOSI	
6	+3.3V		30	SS_L	
7	RTAD4		3`	+3.3V	
8	RTADP		32	+3.3V	
9	RT_AD_LAT		33	$\overline{\text{SSFLAG/EXT\_TRIG}}$	
10	TX_INH		34	$\overline{\text{INT}}$	
11	+3.3V		35	$\overline{\text{MSTCLR}}$	
12	$\overline{\text{RX\_B}}$		36	CLK	
13	RX_B		37	SDA or GND	SDA for BU-67753L and BU-67833L. GND for BU-67743L
14	+3.3V		38	TX_A	
15	$\overline{\text{RT\_BOOT}}$		39	TX_A	
16	NC		40	+3.3V	
17	NC		41	$\overline{\text{TX\_A}}$	
18	NC		42	$\overline{\text{TX\_A}}$	
19	NC		43	TX_B	
20	NC		44	TX_B	
21	NC		45	+3.3V	
22	+3.3V		46	$\overline{\text{TX\_B}}$	
23	$\overline{\text{RX\_A}}$		47	$\overline{\text{TX\_B}}$	
24	RX_A		48	SCL or GND	SCL for BU-67753L and BU-67833L. GND for BU-67743L
			Heat sink	GND	

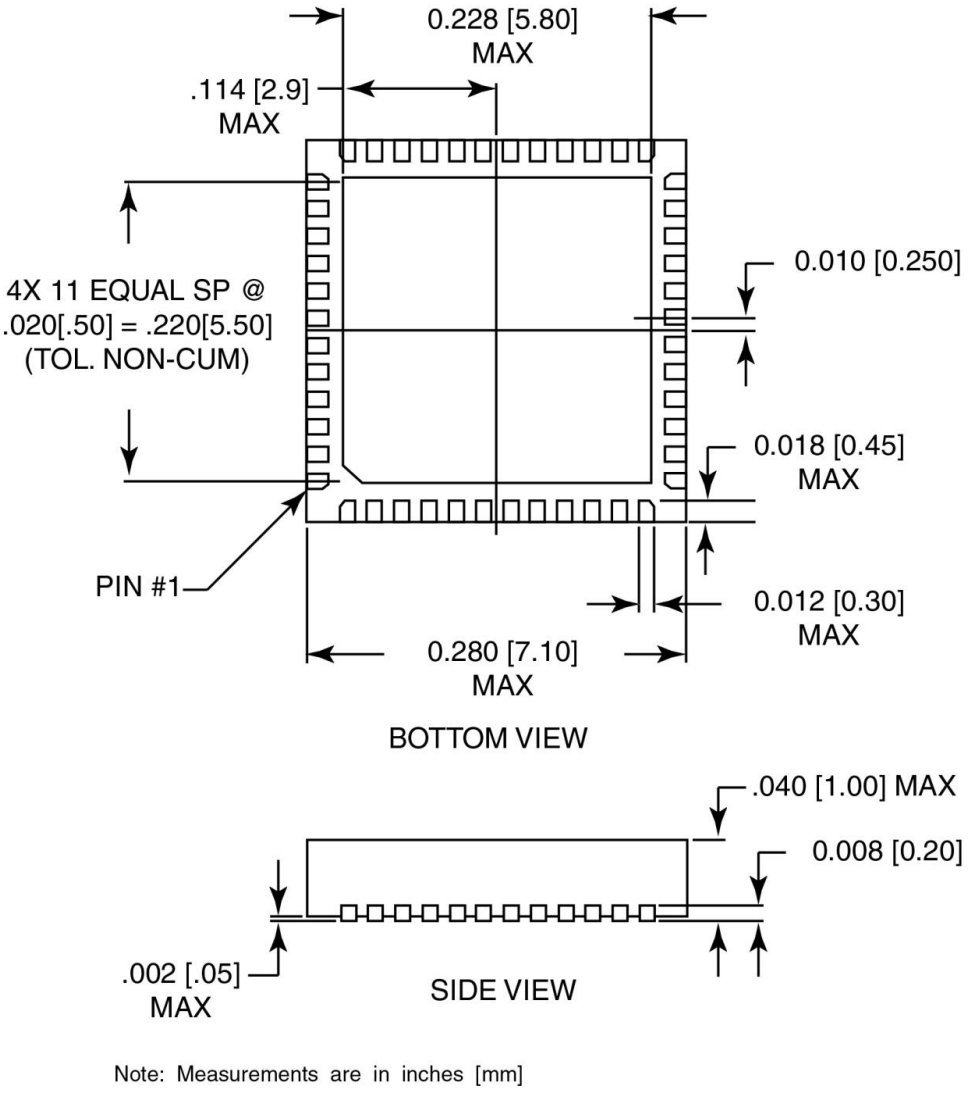


Figure 38. Mechanical Outline Drawing for Nano-Ace® QFN Package

- The package design uses the lead finish and thickness for each metal as shown (see grid below). This is an electrolytic finish.

0.50–2.00um Ni
0.02–0.15um Pd
0.003–0.015um Au

9 ORDERING INFORMATION

BU-6774 3 L C-1 0 2

Test Criteria:
2 = MIL-STD-1760 Amplitude

Process Requirements:
0 = Standard DDC practices, no Burn-In

Environmental Temperature Options:
1= -55°C to +125°C (Note 1)
2 = -40°C to +85°C (Note 1)

Voltage/Transceiver Option:
C = 3.3 Volts, rise/fall times = 100 to 300 ns (1553B)

Package Type:
L = QFN (leadless chip carrier) package

Logic / RAM Voltage:
3 = 3.3 Volt Logic/RAM

Product Type (see Product Matrix below):
BU-6774 = RT with 4K x 16 RAM and SPI host interface
BU-6783 = BC/RT/MT with 32K x 17 RAM and SPI host interface, auto-initialization and self test
BU-6775 = RT/MT with 4K x 17 RAM and SPI host interface, auto-initialization and self test

Notes:
1. Temperature Range applies to case temperature which is defined at the heat sink on bottom of package.

Standard DDC Processing for BGA Products		
Test	**MIL-STD-883**	
	Method(s)	**Condition(s)**
Inspection	2010, 2017, and 2032	—
Temperature Cycle	1010	B