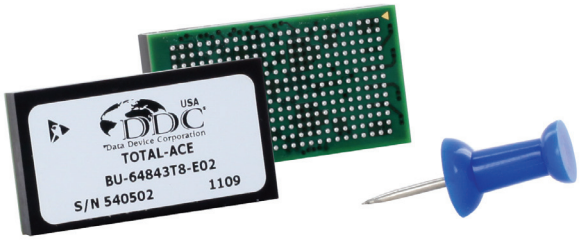
Total-ACE®
Complete MIL-STD-1553 Solution

Connectivity Power Control

Model: BU-648X3T/U/H/i8



Data Sheet

Save board space and simplify your 1553 design and layout with the world's first fully integrated MIL-STD-1553 component, complete with 1553 protocol, memory, transceivers, and isolation transformers—all in one small plastic BGA package with direct and/or transformer coupled 1553 connections inside.

Applications

- Mission Computers
- Digital Data Recorders
- LRU's
- Displays
- Radios/Modems
- Radar Systems/Situational Awareness
- Ground Vehicles
- Commercial Aerospace

Need a Custom Solution?
DDC can customize designs for all products, ranging from simple modifications of standard products to fully customized solutions for commercial, military, aerospace, and industrial applications.

For more information: www.ddc-web.com/BU-64843T

DDC's Data Networking Solutions

MIL-STD-1553 | ARINC 429 | Fibre Channel | Ethernet

As the leading global supplier of data bus components, boards, modules, computers, and software solutions for the military and commercial aerospace markets, DDC's data bus networking solutions encompass the full range of data interface protocols to support the real-time processing demands of field-critical data networking between systems and subsystems on the platform. These products, along with our traditional MIL-STD-1553 solutions, represent a wide and flexible array of performance and cost solutions, enabling DDC to support multi-generational programs.

Whether employed in increased bandwidth, high-speed serial communications, or traditional avionics and ground support applications, DDC's data bus solutions fulfill the expanse of military, civil aerospace, and space requirements including reliability, determinism, low CPU utilization, real-time performance, and ruggedness within harsh environments. Our use of in-house intellectual property ensures superior multi-generational support, independent of the life cycles of commercial devices. Moreover, we maintain software compatibility between product generations to protect our customers' investments in software development, system testing, and end-product qualification.

MIL-STD-1553

DDC, the world leader in MIL-STD-1553 technology, provides the broadest selection of quality MIL-STD-1553 rugged embedded and lab grade computers, boards and components to meet your data conversion and data interface needs. Our 1553 data bus board solutions are integral elements of military, aerospace, and industrial applications. Our extensive line of military and space grade components provide MIL-STD-1553 interface solutions for microprocessors, PCI buses, and simple systems. Our 1553 data bus solutions are designed into almost every aircraft, helicopter, unmanned vehicle, missile programs, and space system that utilizes MIL-STD-1553.

ARINC 429

DDC has a wide assortment of quality ARINC 429 embedded and lab grade boards, LRUs, and components, to serve your data conversion and data interface needs. DDC's ARINC 429 components ensure the accurate and reliable transfer of flight-critical data. Our 429 interfaces support data bus development, validation, and the transfer of flight-critical data aboard commercial aerospace platforms.

Fibre Channel

DDC has developed its line of high-speed Fibre Channel network access controllers and switches to support the real-time processing demands of field-critical data networking between sensors, computer nodes, data storage, displays, and weapons, for air, sea, and ground military vehicles. Fibre Channel's architecture is optimized to meet the performance,reliability, and demanding environmental requirements of embedded, real time, military applications, and designed to endure the multi-decade life cycle demands of military/aerospace programs.

Ethernet

DDC offers convenient solutions to convert MIL-STD-1553, ARINC 429, and Ethernet protocol in any direction, in real-time, without a host computer, enabling seamless and cost saving multi-protocol connectivity for test and embedded applications.

Extensions to MIL-STD-1553

DDC offers a wide variety of solutions based on extensions of MIL-STD-1553 for emerging aerospace applications. Turbo 1553 increases the data rate of 1553 from 1 Mbps to 5 Mbps while maintaining the architectural features of MIL-STD-1553. Hyper 1553 provides high speed communication (50 to 100+ Mbps) over MIL-STD-1553 buses while operating concurrently with legacy 1 Mbps 1553 (similar to ADSL for telephone networks).

Form Factors, Software, & Drivers

DDC supplies MIL-STD-1553 and ARINC 429 board level products in a variety of form factors including USB, PCI-Express, PCMCIA, ExpressCard, AMC, PMC, XMC, PCI-104, PC/104-Plus, PC/104, PCI, cPCI, VME, and ISAbus boards. Our laboratory simulation and in-flight products include multi-function and single-function for system integration and production test environments. Our extensive line of military and space grade components provide MIL-STD-1553 interface solutions for microprocessors and simple systems. Our software is supplied in the form of menus, libraries, and drivers. We also offer additional software to expand our data networking range of options.

TOTAL-ACE® COMPLETE MIL-STD-1553 SOLUTION

BU-64843X/64863X DATA SHEET

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Revision	Date	Pages	Description
A	5/2009	All	Initial Release
B	01/2010	-	Rev Skipped – Document Error.
C	02/2010	1-4, 38,40 - 43, 61	Added lead-free version of product to document. Updated figures 1, 12, &15. Updated table 1 and tables for figures 13 & 14. Updated Ordering Information.
D	3/2010	All	64K version added.
E	05/2010	4	Changed min storage temp from -55° to -65°
F	6/2010	3, 43	Updated Current Drain, Power Dissipation, and Hottest Die specs in Table 1, Updated Table 47
G	11/2010	4	renaming from “SOLDERING” to “SOLDERING/MOUNTING” and below the information on reflow temperatures included the following Refer to DDC’s Application Note #A/N49 “BGA User’s Guide” for additional important mounting information.
H	6/2011	All	Updated to new format. Updated RT-Only information
J	11/2011	8, 85, 87, 95,99	Updated Tables 1, 49, 51, 55, 56
K	07/2012	6, 7, 12, 14, 93, 106	Updated Table 1, added the BU-64863T(U)8 option.
L	11/2012	3, 10, 11, 82, 83, 86, 106, 107	Added -1xx -55 to +125C option and Rev B power numbers. Updated Figure 18.
M	12/2012	10	Updated max storage temperature
N	7/2017	7, 10, 92	Corrected typo “BU-64863X8” to “BU-64843X8” Corrected typo “$\overline{\text{DTGRT}}$“ to “$\overline{\text{DTREQ}}$“. Added Max peak body temperature to table 1.

1 PREFACE

This data sheet uses typographical conventions to assist the reader in understanding the content. This section will define the text formatting used in the rest of the data sheet.

1.1 Text Usage

- **BOLD**–indicates important information and table, figure, and chapter references.
- ***BOLD ITALIC***–designates DDC Part Numbers.
- `Courier New`–indicates code examples.
- <…> - indicates user-entered text or commands.

1.2 Special Handling and Cautions

Warnings: Turn off power to the computer hardware and unplug from wall.

Ensure that standard ESD precautions are followed. As a minimum, one hand should be grounded to the power supply in order to equalize the static potential.

Do not store disks in environments exposed to excessive heat, magnetic fields or radiation.

1.3 Trademarks

All trademarks are the property of their respective owners.

1.4 What is included in this data sheet?

This data sheet contains a complete description of component.

1.5 Technical Support

In the event that problems arise beyond the scope of this data sheet, you can contact DDC by the following:

US Toll Free Technical Support:
1-800-DDC-5757, ext. 7771

Outside of the US Technical Support:
1-631-567-5600, ext. 7771

Fax:
1-631-567-5758 to the attention of DATA BUS Applications

DDC Website:
www.ddc-web.com/ContactUs/TechSupport.aspx

Please note that the latest revisions of Software and Documentation are available for download at DDC's Web Site, www.ddc-web.com.

2 OVERVIEW

The Total-ACE is a complete and compact solution to MIL-STD-1553 applications. With a footprint of just 0.6 (transformer-coupled version) or 0.7 (transformer & direct coupled version) inches by 1.10 inches, it is the world's first MIL-STD-1553 terminal, including the isolation transformers, fully integrated into a single BGA package. The device is powered entirely by +3.3 volts.

Ideal for extended temperature range applications where PC board space is at a premium, the Total-ACE is available in a 312-ball (24 x 13 matrix) BGA package, and is rated for -40°C to +100°C operation at case.

The Total-ACE is software and architecturally compatible with DDC's Enhanced Mini-ACE series of devices. It integrates dual transceivers, dual transformers, protocol engine and either 4K or 64K words of internal RAM. The Total-ACE's flexible processor interface allows direct connection with little or no glue logic to a variety of 8, 16 and 32-bit processors.

The advanced architecture is key to the Total-ACE series' high performance. The advanced bus controller architecture gives the Total-ACE a high degree of flexibility and autonomy. This creates advantages in a number of areas: improving message scheduling control, minimizing host overhead for asynchronous message insertion, facilitating bulk data transfers and double buffering, message retry and bus switching strategies, and data logging and fault reporting. In addition, its remote terminal architecture provides flexibility in meeting all common MIL-STD-1553 protocols. RT data buffering and interrupt options offer support for synchronous and asynchronous messaging, ensure data sample consistency, and support bulk data transfers. The Total-Ace's Monitor mode includes filtering based on RT Address and Subaddress, and provides true message monitoring.

2.1 Features

- World's First, Fully Integrated, MIL-STD-1553 Terminal Solution, including Isolation Transformers
- Small Package 312 Ball BGA (1.1 in x 0.6 in, or 1.1 in x 0.7 in)
- Fully Compatible with Enhanced Mini-ACE® Software and Architecture
- Generic 8 or 16-bit Processor Interface
- Available in Full Military Temperature Range: -55°C to +125°C
- DO-254 Certifiable
- +3.3 Volt Only
- 4K x 16 or 64K x 17 RAM
- 0.185" Max Height

- Compliance with MIL-STD-1553A/B Notice 2, STANAG-3838, and MIL-STD-1760
- Highly Autonomous BC Architecture
- Built-In Message Sequence Controller with 20-Instruction Set
- Flexible RT Buffering with Single, Double, and Circular Buffering
- Selective Message Monitor with Filtering
- 50% Rollover Interrupts for Stacks and Circular Buffers
- Software and Register Compatible to ACE and Enhanced Mini-ACE devices
- Optional RT-Only Operation for Safety-Critical Applications

- **Applications Include:**
- Mission Computers
- Digital Data Recorders
- LRU's
- Radios/Modems
- Displays
- Ground Vehicles
- Commercial Aerospace
- Radar Systems/Situational Awareness

Figure 1. BU-648X3X Total-ACE

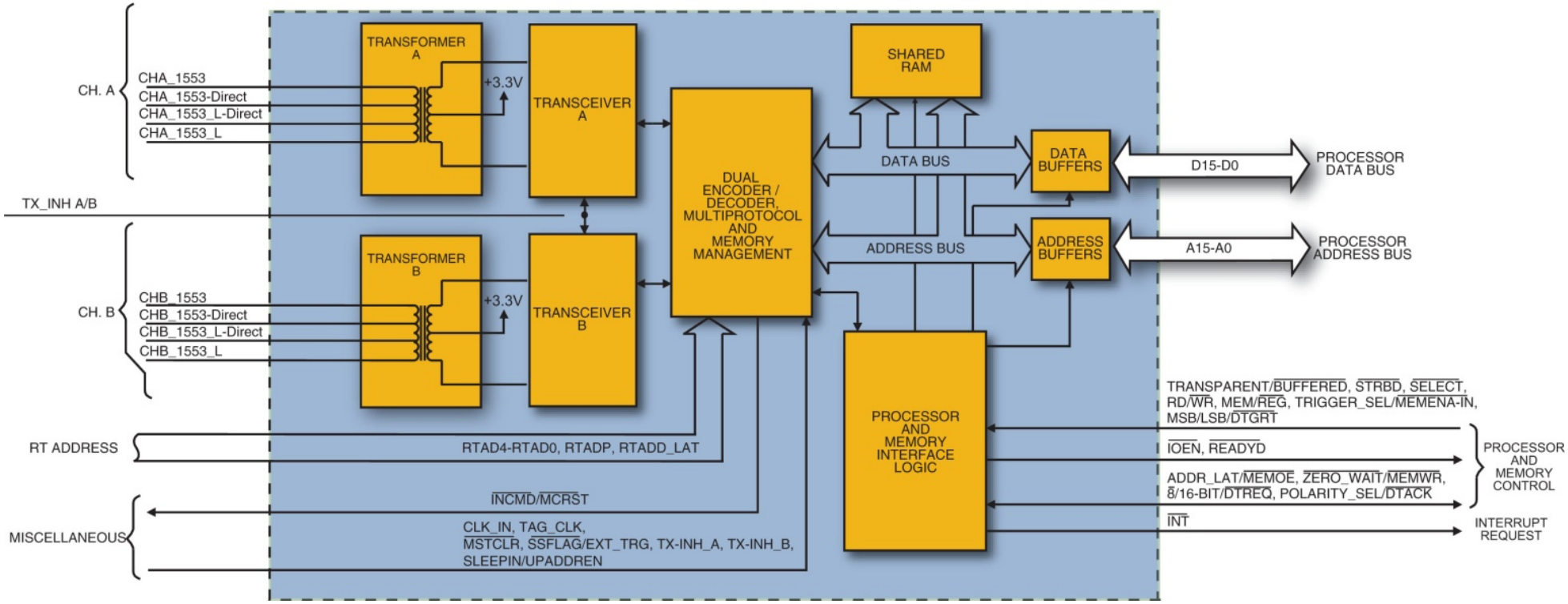


Figure 2. BU-64843T Total-ACE Architecture

Table 1. BU-64843T Specification Table				
PARAMETER	**MIN**	**TYP**	**MAX**	**UNITS**
ABSOLUTE MAXIMUM RATING				
Supply Voltage (Note 11)				
• BU-64843X8-XX2				
Logic +3.3 V	-0.3		6.0	V
• BU-64863X8-XX2				
Logic +3.3V	-0.3		4.1	V
• Transceivers +3.3V (not during transmit)	-0.3		6.0	V
• Transceivers +3.3V (during transmit)	-0.3		4.5	V
Logic				
+3.3V Logic Input Range	-0.3		6.0	V
POWER SUPPLY REQUIREMENTS				
Voltages/Tolerances (Note 11)				
• Logic +3.3V	3.00	3.3	3.60	V
• Transceivers +3.3V	3.14	3.3	3.46	V
Current Drain(Total Hybrid) (Note 13)				
BU-64843X8-E02 Rev A				
• Idle w/transceiver SLEEPIN enabled		32	48	mA
• Idle w/transceiver SLEEPIN disabled		81	117	mA
• 25% Transmitter Duty Cycle		255	309	mA
• 50% Transmitter Duty Cycle		428	517	mA
• 100% Transmitter Duty Cycle		776	931	mA
BU-64863H/i8-E02 Rev A				
• Idle w/transceiver SLEEPIN enabled		34	51	mA
• Idle w/transceiver SLEEPIN disabled		83	120	mA
• 25% Transmitter Duty Cycle		257	311	mA
• 50% Transmitter Duty Cycle		431	521	mA
• 100% Transmitter Duty Cycle		781	937	mA
BU-64843X8-E02 Rev B, BU-64843X8-102				
• Idle		51	73	mA
• 25% Transmitter Duty Cycle		197	219	mA
• 50% Transmitter Duty Cycle		367	381	mA
• 100% Transmitter Duty Cycle		685	703	mA
BU-64863T/U8-E02, BU-64863H/i8-E02 Rev B, BU-64863X8-102				
• Idle		53	76	mA
• 25% Transmitter Duty Cycle		199	221	mA
• 50% Transmitter Duty Cycle		370	385	mA
• 100% Transmitter Duty Cycle		690	709	mA

Table 1. BU-64843T Specification Table				
PARAMETER	**MIN**	**TYP**	**MAX**	**UNITS**
POWER DISSIPATION				
TOTAL HYBRID(Note 13 & 14)				
BU-64843X8-E02 Rev A				
• Idle w/transceiver SLEEPIN enabled		0.106	0.158	W
• Idle w/transceiver SLEEPIN disabled		0.267	0.386	W
• 25% Transmitter Duty Cycle		0.546	0.724	W
• 50% Transmitter Duty Cycle		0.821	1.116	W
• 100% Transmitter Duty Cycle		1.378	1.890	W
BU-64863H/i8-E02 Rev A				
• Idle w/transceiver SLEEPIN enabled		0.112	0.168	W
• Idle w/transceiver SLEEPIN disabled		0.274	0.396	W
• 25% Transmitter Duty Cycle		0.552	0.732	W
• 50% Transmitter Duty Cycle		0.831	1.128	W
• 100% Transmitter Duty Cycle		1.394	1.910	W
BU-64843X8-E02 Rev B, BU-64843X8-102				
• Idle		0.170	0.269	W
• 25% Transmitter Duty Cycle		0.273	0.347	W
• 50% Transmitter Duty Cycle		0.381	0.509	W
• 100% Transmitter Duty Cycle		0.514	0.683	W
BU-64863T/U8-E02, BU-64863H/i8-E02 Rev B, BU-64863X8-102				
• Idle		0.177	0.279	W
• 25% Transmitter Duty Cycle		0.279	0.355	W
• 50% Transmitter Duty Cycle		0.391	0.521	W
• 100% Transmitter Duty Cycle		0.530	0.703	W
ACTIVE TRANSCEIVER (HOTTEST DIE)				
BU-64843X8-E02 Rev A				
• 100% Transmitter Duty Cycle		1.103	1.494	W
BU-64863H/i8-E02 Rev A				
• 100% Transmitter Duty Cycle		1.117	1.512	W
BU-64863T/U8-E02, BU-648x3H/i8-E02 Rev B, BU-648X3X8-102				
• 100% Transmitter Duty Cycle		0.420	0.540	W
RECEIVER				
Differential Input Impedance (Note 1 – 6)				
• +3.3V Transformer Coupled	1.0			kΩ
• +3.3V Direct Coupled	2.0			kΩ
Threshold Voltage				
• Transformer Coupled, Measured on Stub	0.200		0.860	Vp-p
• Direct Coupled, Measured on Stub	0.280		1.20	Vp-p
Common-Mode Voltage			±10	Vpeak

Table 1. BU-64843T Specification Table				
PARAMETER	**MIN**	**TYP**	**MAX**	**UNITS**
TRANSMITTER				
Differential Output Voltage				
• Direct Coupled Across 35Ω, Measured on Bus	6	7.2	9.0	Vp-p
• Transformer Coupled Across 70Ω, Measured on Bus (Note 12)	20	21.5	27	Vp-p
Output Noise, Differential			14	mVRMS
Output Offset Voltage, Transfomer Coupled Across 70Ω	-250		250	mVp
Rise/Fall Time	100	150	300	nsec
LOGIC				
V_{IH}				
All signals except CLK_IN	2.1			V
CLK_IN	0.8•Vcc			V
V_{IL}				
All signals except CLK_IN			0.7	V
CLK_IN			0.2•Vcc	V
Schmidt Hysteresis				
All signals except CLK_IN	0.4			V
CLK_IN	0.8			V
I_{IH}, I_{IL}				
All signrals except CLK_IN				
I_{IH} (V_{cc} = 3.6V, V_{IN} = 2.5V)	-100	-32	-10	µA
I_{IL} (V_{cc} = 3.6V, V_{IN} = 0.0V)	-340	-50	-20	µA
CLK_IN				
I_{IH}	-10		10	µA
I_{IL}	-10		10	µA
V_{OH} (V_{CC} = 3.0V, V_{IH} = 2.7V, (V_{IL} = 0.2V, I_{OH} = max)	2.4			V
V_{OL} (V_{CC} = 3.0V, V_{IH} = 2.7V, (V_{IL} = 0.2V, I_{OH} = max)			0.5	V
IOL (VCC = 3.0V)	2.2			mA
IOH (VCC = 3.0V)			-2.2	mA
CI (Input Capacitance)		50		pF
CIO (Bidirectional signal input capacitance)		50		pF

Table 1. BU-64843T Specification Table				
PARAMETER	**MIN**	**TYP**	**MAX**	**UNITS**
CLOCK INPUT				
Frequency				
• Nominal Values				
- Default Mode		16.0		MHz
- Option		12.0		MHz
- Option		10.0		MHz
- Option		20.0		MHz
Long Term Tolerance				
• 1553A Compliance	-0.01		0.01	%
• 1553B Compliance	-0.10		0.10	%
Short Term Tolerance, 1 second				
• 1553A Compliance	-0.001		0.001	%
• 1553B Compliance	-0.01		0.01	%
Duty Cycle	40		60	%
15553 MESSAGE TIMING				
Completion of CPU Write (BC Start)-to-Start of First Message for Non-enhanced BC Mode	2.5			µs
BC Intermessage Gap (Note 7)				
• Non-enhanced (Mini-ACE compatible) BC mode		9.5		µs
• Enhanced BC mode (Note 8)		10 to 10.5		µs
BC/RT/MT Response Timeout (Note 9)				
• 18.5 nominal	17.5	18.0	19.5	µs
• 22.5 nominal	21.5	22.5	23.5	µs
• 50.5 nominal	49.5	50.5	51.5	µs
• 128.0 nominal	127	129.5	131	µs
RT Response Time (mid-parity to mid-sync) (Note 10)	4		7	µs
Transmitter Watchdog Timeout		660.5		µs
THERMAL				
TOTAL-ACE BGA				
312-ball BGA Package				
(See Thermal Management section 8.10)				
Active Transceiver (Hottest Die)				
BU-648X3T/U8 Transformer Coupled				
Single-Tap Versions				
• Junction-to-Ambient (θ_{JA} via simulation)				
- Per JESD 51-2 standard at 25°C θ_{JA} in Still Air		37.7		°C/W

Table 1. BU-64843T Specification Table				
PARAMETER	**MIN**	**TYP**	**MAX**	**UNITS**
THERMAL (con't)				
- Per JESD 51-6 standard at 25°C				
θ_{JA} @1M/S		30.5		°C/W
θ_{JA} @2M/S		28.3		°C/W
θ_{JA} @3M/S		27.2		°C/W
• Junction-to-Case (θ_{JC} via simulation)				
- Per JESD 51-12 standard at 25°C				
θ_{JC}		18.9		°C/W
• Junction-to-Board (θ_{JB} via simulation)				
- Per JESD 51-2 standard at 25°C				
θ_{JB}		25.4		°C/W
BU-648X3H/i8 Direct &Transformer Coupled Dual-Tap Versions				
• Junction-to-Ambient (θ_{JA} via simulation)				
- Per JESD 51-2 standard at 25°C				
θ_{JA} in Still Air		37.8		°C/W
- Per JESD 51-6 standard at 25°C				
θ_{JA} @1M/S		31.4		°C/W
θ_{JA} @2M/S		29.8		°C/W
θ_{JA} @3M/S		29.0		°C/W
• Junction-to-Case (θ_{JC} via simulation)				
- Per JESD 51-12 standard at 25°C				
θ_{JC}		26.2		°C/W
• Junction-to-Board (θ_{JB} via simulation)				
- Per JESD 51-2 standard at 25°C				
θ_{JB}		26.5		°C/W
ALL PACKAGES				
Operating Case Temperature				
- EXX	-40		+100	°C
- 1XX (Note 15)	-55		+125	°C
Operating Junction Temperature				
- Transceiver	-55		+150	°C
- Protocol	-55		+135	°C
- Memory	-55		+140	°C
Storage Temperature	-65		+150	°C
SOLDERING/MOUNTING				
312-BALL BGA PACKAGE				
Maximum Peak Body Temperature			260	°C
The reflow profile detailed in IPC/JEDEC J-STD-020 is applicable for both leaded and lead-free products				
(Refer to DDC's Application Note #A/N-49 "BGA User's Guide" for additional important mounting information.)				

Table 1. BU-64843T Specification Table

PARAMETER	MIN	TYP	MAX	UNITS
PHYSICAL CHARACTERISTICS				
Package Body Size				
312-ball BA				
• BU-64843T(U)8		1.100 x 0.600 x 0.185		in.
		(27.9 x 15.2 x 4.7)		(mm)
• BU-648x3H(i)8		1.100 x 0.700 x 0.185		in.
		(27.9 x 17.8 x 4.7)		(mm)
Total-ACE				
• Moisture Sensitivity Level		MSL-3		
• Electrostatic Discharge Sensitivity		ESD Class 0		
Weight				
312-ball BGA		0.167		oz.
		(4.8)		(g)

Table 1 Notes:
(Notes 1 through 6 are applicable to the Receiver Differential Input Impedance specification)

1. Specifications include contributions from the transformer, transmitter, and receiver.
2. Impedance parameters are specified directly between pins CHA(B)_1553 and $\overline{\text{CHA(B)\_1553}}$, and CHA(B)_1553-Direct and $\overline{\text{CHA(B)\_1553-Direct}}$ of the Total-ACE hybrid.
3. It is assumed that all power and ground inputs to the hybrid are connected.
4. The specifications are applicable for both unpowered and powered conditions.
5. The specifications assume a 2 volt rms balanced, differential, sinusoidal input. The applicable frequency range is 75kHz to 1 MHz.
6. Minimum resistance and maximum capacitance parameters are guaranteed over the operating range, but are not tested.
7. Typical value for minimum intermessage gap time. Under software control, this may be lengthened (to 65.535 ms – message time) in increments of 1 µs. If ENHANCED CPU ACCESS, bit 14 of Configuration Register #6, is set to logic “1”, then host accesses during BC Start-of-Message (SOM) and End-of-Message (EOM) transfer sequences could have effect of lengthening the intermessage gap time. For each host access during an SOM or EOM sequence, the intermessage gap time will be lengthened by 6 clock cycles. Since there are 7 internal transfers during SOM and 5 during EOM, this could theoretically lengthen the intermessage gap by up to 72 clock cycles; i.e., up to 7.2 ms with a 10 MHz clock, 6.0 µs with a 12 MHz clock, 4.5 µs with a 16 MHz clock, or 3.6 µs with a 20 MHz clock.
8. For Enhanced BC mode, the typical value for intermessage gap time is approximately 10 clock cycles longer that for the non-enhanced BC mode. That is, an addition of 1.0 µsat 10 MHz, 833 ns at 12 MHz, 625 ns at 16 MHz, or 500 ns at 20 MHz.
9. Software programmable (4 options). Includes RT-to-RT Timeout (measured mid-parity of transmit Command Word to mid-sync of transmitting RT Status Word).
10. Measured from mid-parity crossing of Command Word to mid-sync crossing of RT’s Status Word.
11. External 10 µF tantalum and 0.1 µF capacitors should be located as close as possible to the voltage input balls.
12. MIL-STD-1760 requires a 20 Vp-p minimum output on the transformer-coupled stub connection.
13. Current drain and power dissipation specs are preliminary and subject to change.
14. Power Dissipation is the input power minus the power delivered to the 1553 fault isolation resistors, the power delivered to the bus termination resistors, and the copper losses in the bus coupling transformer. The external power dissipation for the transformer-coupled configuration (while transmitting) is assumed to be as follows: 0.057 watts for the active bus coupling transformer, 0.422 watts for each of the two bus isolation resistors and 0.141 watts for each of the two bus termination resistors.
15. See section 8.10 for thermal management requirements at high transmit duty cycles.

3 INTRODUCTION

The Total-ACE is the industry's smallest, fully integrated MILSTD-1553 terminal solution including the isolation transformers, enabling its use in applications where PC board space is at a premium. The BU-64843/863X BC/RT/MT Total-ACE fully integrated terminal comprises a complete interface between a host processor and a MIL-STD-1553 bus. The Total-ACE is available in a 1.100 x 0.600 inch (transformer-coupled version) or 1.000 x 0.700 inch (transformer & direct-coupled version), plastic 312-ball BGA. The Total-ACE's architecture is identical to that of the Enhanced Mini-ACE family, and most features are both functionallycompatible and software compatible with the previous Mini-ACE (Plus) and ACE generations.

The Total-ACE provides complete multiprotocol support of MIL-STD-1553A/B/McAir, STANAG 3838, and MIL-STD-1760. The Total-ACE integrates dual +3.3V transceivers, protocol logic, 4K or 64K words of internal RAM, and isolation transformers.

The Total-ACE includes dual +3.3 volt, MIL-STD-1760 trimmed voltage source transceivers for improved line driving capability. 4K memory and Dual-Tap transceiver versions of Total-ACE offer an additional transceiver power-down (SLEEPIN) option to further reduce device power consumption. To provide further flexibility, the Total-ACE may operate with a choice of 10, 12, 16, or 20 MHz clock inputs.

One of the new salient features of the Total-ACE is its Enhanced bus controller architecture. The Enhanced BC's highly autonomous message sequence control engine provides a means for offloading the host processor for implementing multiframe message scheduling, message retry schemes, data double buffering, and asynchronous message insertion. For the purpose of performing messaging to the host processor, the Enhanced BC mode includes a General Purpose Queue, along with user-defined interrupts.

A second major new feature of the Total-ACE is the incorporation of a fully autonomous built-in self-test. This test provides comprehensive testing of the internal protocol logic. A separate test verifies the operation of the internal RAM. Since the self-tests are fully autonomous, they eliminate the need for the host to write and read stimulus and response vectors.

The Total-ACE in RT mode offers the same choices of single, double, and circular buffering for individual subaddresses as the ACE, Mini-ACE (Plus), Enhanced Mini-ACE, and Mini-ACE Mark3 terminals. New enhancements to the RT architecture include a global circular buffering option for multiple (or all) receive subaddresses, a 50% rollover interrupt for circular buffers, an interrupt status queue for logging up to 32 interrupt events, and an option to automatically initialize to RT mode with the Busy bit set. The interrupt status queue and 50% rollover interrupt features are also included as improvements to the Monitor architecture.

To minimize board space and "glue" logic, the Total-ACE terminal provides the same wide choice of host interface configurations as the ACE, Mini-ACE (Plus), Enhanced Mini-ACE, Mini-ACE Mark3, and Micro-ACE(TE) terminals. This includes support of interfaces to 16-bit or 8-bit processors, memory or port type interfaces, and multiplexed or non-multiplexed address/data buses. In addition, with respect to ACE/Mini-ACE, the worst case processor wait time has been significantly reduced. For example, assuming a 16 MHz clock, this time has been reduced from 2.8 µs to 632 ns for read accesses, and to 570 ns for write accesses.

The Total-ACE terminal operates over the temperature range of -40 to +100°C (case) and is ideal for industrial processor-to-1553 applications powered by 3.3 volts only.

3.1 Supporting Documentation

Enhanced Miniature Advanced Communications Engine
(Enhanced Mini-ACE® Series) Users Guide MN-6186X-001
Volume 1 – Architectural Reference

Enhanced Miniature Advanced Communications Engine
(Enhanced Mini-ACE® Series) User's Guide MN-6186X-002
Volume 2 – Hardware Reference

Enhanced Miniature Advanced Communications Engine
(Enhanced Mini-ACE® Series) MN-6186X-004
Reliability Reports

Enhanced Miniature Advanced Communications Engine
(Enhanced Mini-ACE® Series) MN-6186X-005
Test Evaluation Data

3.2 Total-ACE in Simple System RT (SSRT) Mode

The Total-ACE 4K RAM (BU-64843X) terminal can provide a complete interface between a simple system and a MIL-STD-1553 bus when configured as an SSRT. These terminals integrate dual transceiver, protocol logic, isolation transformers, and a FIFO memory for received messages in a 312-ball BGA. The internal architecture is identical to that of the original BU-61703/61705 Simple System RT (SSRT).

The SSRT configured Total-ACE incorporates a built-in self-test (BIT). This BIT, which is processed following power turn-on or after receipt of an Initiate self-test mode command, provides a comprehensive test of the encoders, decoders, protocol, transmitter watchdog timer, and protocol section.

The Total-ACE, when configured as an SSRT, is ideal for munitions stores and other simple systems that do not require a microprocessor. To streamline the interface to simple systems it includes an internal 32-word FIFO for received data words. This serves to ensure that only complete, consistent blocks of validated data words are transferred to a system. Please refer to the Micro-ACE-TE and Total-ACE in Simple System RT (SSRT) Mode Application Note AN/B-37 for detailed SSRT configuration information, available on our website, www.ddc-web.com.

3.3 Test Components

Daisy chain mechanical samples of the Total-ACE, 312-ball BGA (BU-64843T8-600) are available. These are used to verify both the electrical and mechanical integrity of the solder joints between the BGA package and the board. Ball pairs are internally wired so that the user can test for electrical continuity between balls. Refer to Table 57 for interconnection details.

Although these units are inoperative, they are fully populated with silicon die and isolation transformers so that they closely match the thermal and mechanical characteristics of standard production units. Internal daisy chain interconnections are made by copper PWB traces.

3.4 Transceiverless “Compatible” Version of Total-ACE

All versions of the Total-ACE 312-ball BGA can operate in a transceiverless configuration. These devices contain fully functional, dual-redundant, MIL-STD-1553 transceivers with internal/intermediate (digital) connections brought out to balls. These intermediate connections allow devices to be used in transceiverless mode for direct interfacing to MIL-STD-1773 (fiber optic) transceivers. Mandatory additional connections (See Table 48) are required when these devices are not utilized in transceiverless mode.

3.5 Transceivers

The transceivers in Total-ACE series terminals are fully monolithic, requiring only +3.3 power input. 4K memory and Dual-Tap transceiver versions of Total-ACE provide an additional transceiver power-down (SLEEPIN) option to further reduce device power consumption. Total-ACE transmitters inherently satisfy the MIL-STD-1760 requirement for a minimum of 20 volts peak-to-peak, transformer-coupled output.

Besides eliminating the demand for an additional power supply, the use of +3.3 volt only transceivers requires the use of a built-in step-up, rather than a step-down, isolation transformer. This provides the advantage of a higher terminal input impedance than is possible for a 15V, 12V or 5V transceiver. As a result, there is a greater margin for the input impedance test, mandated for the 1553 validation test.

This allows for longer cable lengths between a system connector and the isolation transformers of an embedded 1553 terminal.

The receiver sections of the Total-ACE are fully compliant with MIL-STD-1553B Notice 2 in terms of front end overvoltage protection, threshold, common-mode rejection, and word error rate.

3.6 Built-In Isolation Transformers

Total-ACE, in transformer-coupled (T/U) version, incorporates two MLP-2233 isolation transformers (1:2.70 Turns Ratio) from BETA Transformer Technology Corporation. Transformer and direct-coupled (H/I) versions of Total-ACE incorporate two DSS-3333 isolation transformers with both transformer and direct coupled ratios (1:2.70 & 1:3.75) from BETA Transformer Technology Corporation.

General specifications for MLP-2233 & DSS-3333 isolation transformers are available at http://www.bttc-beta.com/ in the "MLP-2000 Series" and "DSS-3000 Series" transformer data sheets.

3.7 Register and Memory Addressing

The software interface of the Total-ACE to the host processor consists of 24 internal operational registers for normal operation, an additional 24 test registers, plus 64K words of shared memory address space. The Total-ACE's 4K X 16 or 64K x 17 of internal RAM resides within this address space.

For normal operation, the host processor only needs to access the lower 32 register address locations (00-1F). The next 32 locations (20-3F) should be reserved, since many of these are used for factory test.

3.8 Internal Registers

The address mapping for the Total-ACE registers is illustrated in Table 2.

Table 2. Address Mapping

Address Lines					Register Description/Accessiblity
A4	A3	A2	A1	A0	
0	0	0	0	0	Interrupt Mask Register #1 (RD/WR)
0	0	0	0	1	Configuration Register #1 (RD/WR)
0	0	0	1	0	Configuration Register #2 (RD/WR)
0	0	0	1	1	Start/Reset Register (WR)
0	0	0	1	1	Non-Enhanced BC/RT Command Stack Pointer / Enhanced BC

Table 2. Address Mapping					
Address Lines					Register Description/Accessiblity
A4	A3	A2	A1	A0	
					Instruction List Pointer Regsiter (RD)
0	0	1	0	0	BC Control Word / RT Subaddress Control Word Register (RD/WR)
0	0	1	0	1	Time Tag Register (RD/WR)
0	0	1	1	0	Interrupt Status Register #1 (RD)
0	0	1	1	1	Configuration Register #3 (RD/WR)
0	1	0	0	0	Configuration Register #4 (RD/WR)
0	1	0	0	1	Configuration Register #5 (RD/WR)
0	1	0	1	0	RT/Monitor Data Stack Address Register (RD)
0	1	0	1	1	BC Frame Time Remaining Register (RD)
0	1	1	0	0	BC Time Remaining to Next Message Register (RD)
0	1	1	0	1	Non-Enhanced BC Frame Time / Enhanced BC Intital Instruction Pointer / RT Last Command / MT Trigger Word Register (RD/WR)
0	1	1	1	0	RT Status Word Register (RD)
0	1	1	1	1	RT BIT Word Register (RD)
1	0	0	0	0	Test Mode Register 0
1	0	0	0	1	Test Mode Register 1
1	0	0	1	0	Test Mode Register 2
1	0	0	1	1	Test Mode Register 3
1	0	1	0	0	Test Mode Register 4
1	0	1	0	1	Test Mode Register 5
1	0	1	1	0	Test Mode Register 6
1	0	1	1	1	Test Mode Register 7
1	1	0	0	0	Configuration Register #6 (RD/WR)
1	1	0	0	1	Configuration Register #7 (RD/WR)
1	1	0	1	0	RESERVED
1	1	0	1	1	BC Condition Code Register (RD)
1	1	0	1	1	BC General Purpose Flag Register
1	1	1	0	0	BIT Test Status Register (RD)
1	1	1	0	1	Interrupt Mask Register #2 (RD/WR)
1	1	1	1	0	Interrupt Status Register #2 (RD)
1	1	1	1	1	BC General Purpose Queue Pointer / RT-MT Interrupt Status Queue Pointer Register (RD/WR)

Table 3. Interrupt Mask Register #1 (Read/Write 00H)	
BIT	**Description**
15 (MSB)	RESERVED
14	RAM Parity Error
13	BC/RT Transmitter Timeout
12	BC/RT Command Stack Rollover
11	MT Command Stack Rollover
10	MT Data Stack Rollover
9	Handshake Fail
8	BC Retry
7	RT Address Parity Error
6	Time Tag Rollover
5	RT Circular Buffer Rollover
4	BC Control Word/RT Subaddress Control Word EOM
3	BC End of Frame
2	Format Error
1	BC Status Set/RT Mode Code/MT Pattern Trigger
0 (LSB)	End of Message

Table 4. Configuration Register #1 (Read/Write 01H)				
BIT	**BC Function (Bits 11-0 Enhanced Mode Only)**	**RT Without Alternate Status**	**RT With Alternate Status (Enhanced Only)**	**Montior Function (Enhanced Mode Only BITS 12-0)**
15 (MSB)	RT/$\overline{\text{BC-MT}}$ (logic 0)	(logic 1)	(logic 1)	(logic 0)
14	MT/$\overline{\text{BC-RT}}$ (logic 0)	(logic 0)	(logic 0)	(logic 1)
13	Current Area B/$\overline{\text{A}}$	Current Area B/$\overline{\text{A}}$	Current Area B/$\overline{\text{A}}$	Current Area B/$\overline{\text{A}}$
12	Message Stop-On-Error	Message Monitor Enabled (MMT)	Message Monitor Enabled	Message Monitor Enabled
11	Frame Stop-On-Error	$\overline{\text{Dynamic Bus Control}}$ $\overline{\text{Acceptance}}$	S10	Trigger Word Enabled
10	Status Set Stop-On-Message	$\overline{\text{BUSY}}$	S09	Start-On-Trigger

Table 4. Configuration Register #1 (Read/Write 01H)				
BIT	**BC Function (Bits 11-0 Enhanced Mode Only)**	**RT Without Alternate Status**	**RT With Alternate Status (Enhanced Only)**	**Montior Function (Enhanced Mode Only BITS 12-0)**
9	Status Set Stop-On-Frame	$\overline{\text{SERVICE REQUEST}}$	S08	Stop-On-Trigger
8	Frame Auto-Repeat	$\overline{\text{SSFLAG}}$	S07	Not Used
7	External Trigger Enabled	$\overline{\text{RT FLAG}}$ (Enhanced Mode Only)	S06	External Trigger Enabled
6	Internal Trigger Enabled	Not Used	S05	Not Used
5	Intermessage Gap Timer Enabled	Not Used	S04	Not Used
4	Retry Enabled	Not Used	S03	Not Used
3	Doubled / $\overline{\text{Single}}$ Retry	Note Used	S02	Not Used
2	BC Enabled (Read Only)	Not Used	S01	Monitor Enabled (Read Only)
1	BC Frame In Progress (Read Only)	Not Used	S00	Monitor Triggered (Read Only)
0 (LSB)	BC Message In Progress (Read Only)	RT Message In Progress (Enhanced mode only, Read Only)	RT Message in Progress (Read Only)	Monitor Active (Read Only)

Table 5. Configuration Register #2 (Read/Write 02H)	
BIT	**Description**
15 (MSB)	Enhanced Interrupts
14	RAM Parity Enable
13	Busy Lookup Table Enable
12	RX SA Double Buffer Enable
11	Overwrite Invalid Data
10	256-Word Boundary Disable
9	Time Tag Resolution 2
8	Time Tag Resolution 1
7	Time Tag Resolution 0
6	Clear Time Tag on Synchronize
5	Load Time Tag on Synchronize
4	Interrupt Status Auto Clear
3	Level / $\overline{\text{Pulse}}$ Interrupt Request
2	Clear Service Request
1	Enhanced RT Memory Management
0 (LSB)	Separate Broadcast Data

Table 6. Start/Reset Register (Write 03H)	
BIT	**Description**
15 (MSB)	Reserved
14	Reserved
13	Reserved
12	Reserved
11	Clear RT Halt
10	Clear Self-Test Register
9	Initiate RAM Self-Test
8	Reserved
7	Initiate Protocol Self-Test
6	BC/MT Stop-On-Message
5	BC Stop-On-Frame
4	Time Tag Test Clock
3	Time Tag Reset
2	Interrupt Reset
1	BC/MT Start
0 (LSB)	Reset

Table 7. BC/RT Command Stack Pointer Reg.(Read 03H)	
BIT	**Description**
15 (MSB)	Command Stack Pointer 15
•	•
•	•
•	•
0 (LSB)	Command Stack Pointer 0

Table 8. BC Control Word Register (Read/Write 04H)	
BIT	**Description**
15 (MSB)	Transmit Time Tag for Synchronize Mode Command
14	Message Error Mask
13	Service Request Bit Mask
12	Busy Bit Mask
11	Subsystem Flag Bit Mask
10	Terminal Flag Bit Mask
9	Reserved Bits Mask
8	Retry Enabled
7	Bus Channel A/$\overline{B}$
6	Off-Line Self-Test
5	Mask Broadcast Bit
4	EOM Interrupt Enable
3	1553A/B Select
2	Mode Code Format
1	Broadcast Format
0 (LSB)	RT-to-RT Format

Table 9. RT Subaddress Control Word (Read/Write 04H)	
BIT	**Description**
15 (MSB)	RX: Double/Global Buffer Enable
14	TX: EOM INT
13	TX: CIRC BUF INT
12	TX: Memory Management 2 (MM2)
11	TX: Memory Management 1 (MM1)
10	TX: Memory Management 0 (MM0)
9	RX: EOM INT
8	RX: CIRC BUF INT
7	RX: Memory Management 2 (MM2)
6	RX: Memory Management 1 (MM1)
5	RX: Memory Management 0 (MM0)
4	BCST: EOM INT
3	BCST: CIRC BUF INT
2	BCST: Memory Management 2 (MM2)
1	BCST: Memory Management 1 (MM1)
0 (LSB)	BCSTL Memory Management 0 (MM0)

Table 10. Time Tag Register. (Read/Write 05H)	
BIT	**Description**
15 (MSB)	Time Tag 15
•	•
•	•
•	•
0 (LSB)	Time Tag 0

Table 11. Interrupt Status Register #1 (Read 06H)	
BIT	**Description**
15 (MSB)	Master Interrupt
14	RAM Parity Error
13	Transmitter Timeout
12	BC/RT Command Stack Rollover
11	MT Command Stack Rollover
10	MT Data Stack Rollover
9	Handshake Fail
8	BC Retry
7	RT Address Parity Error
6	Time Tag Rollover
5	RT Circular Buffer Rollover
4	BC Control Word / RT Subaddress Control Word EOM
3	BC End of Frame
2	Format Error
1	BC Status Set / RT Mode Code / MT Pattern Trigger
0 (LSB)	End of Message

Table 12. Configuration Register #3 (Read/Write 07H)	
BIT	**Description**
15 (MSB)	Enhanced Mode Enable
14	BC/RT Command Stack Size 1
13	BC/RT Command Stack Size 0
12	MT Command Stack Size 1
11	MT Command Stack Size 0
10	MT Data Stack Size 2
9	MT Data Stack Size 1
8	MT Data Stack Size 0
7	Illegalization Disabled
6	Override Mode T/$\overline{R}$ Error
5	Alternate Status Word Enable
4	Illegal Rx Transfer Disable
3	Busy RX Transfer Disable
2	$\overline{RTFAIL}$ / $\overline{RTFLAG}$ Wrap Enable
1	1553A Mode Codes Enable
0 (LSB)	Enhanced Mode Code Handling

Table 13. Configuration Register #4 (Read/Write 08H)	
BIT	**Description**
15 (MSB)	External Bit Word Enable
14	Inhibit Bit Word If Busy
13	Mode Command Override Busy
12	Expanded BC Control Word Enable
11	Broadcast Mask ENA/XOR
10	Retry If –A and M.E.
9	Restry if Status Set
8	1st Retry ALT/$\overline{\text{SAME}}$ Bus
7	2nd Retry ALT/$\overline{\text{SAME}}$ Bus
6	Valid M.E./No Data
5	Valid Busy/No Data
4	MT Tag Gap Option
3	Latch RT Address with Config #5
2	Test Mode 2
1	Test Mode 1
0 (LSB)	Test Mode 0

Table 14. Configuration Register #5 (Read/Write 09H)	
BIT	**Description**
15 (MSB)	12/$\overline{16}$ MHz Clock Select
14	Single-Ended Select
13	External TX Inhibit A
12	External TX Inhibit B
11	Expanded Crossing Enabled
10	Response Timeout Select 1
9	Response Time out Select 0
8	Gap Check Enabled
7	Broadcast Disabled
6	RT Address Latch/$\overline{\text{Transparent}}$
5	RT Address 4
4	RT Address 3
3	RT Address 2
2	RT Address 1
1	RT Address 0
0 (LSB)	RT Address Parity

Table 15. RT/Monitor Data Stack Address Register (Read/Write 0AH)	
BIT	**Description**
15 (MSB)	RT / Monitor Data Stack Address 15
•	•
•	•
•	•
0 (LSB)	RT / Monitor Data Stack Address 0

Table 16. BC Frame Time Remaining Register (Read/Write 0BH)	
BIT	**Description**
15 (MSB)	BC Frame Time Remaining 15
•	•
•	•
•	•
0 (LSB)	BC Frame Time Remaining 0

Note: resolution = 100 µs per LSB

Table 17. BC Frame Time Remaining Register (Read/Write 0CH)	
BIT	**Description**
15 (MSB)	BC Frame Time Remaining 15
•	•
•	•
•	•
0 (LSB)	BC Frame Time Remaining 0

Note: resolution = 100 µs per LSB

Table 18. BC Frame Time/RT Last Command/MT Trigger Register (Read/Write 0DH)	
BIT	**Description**
15 (MSB)	BIT 15
•	•
•	•
•	•
0 (LSB)	BIT 0

Table 19. RT Status Word Register (Read/Write 0EH)	
BIT	**Description**
15 (MSB)	Logic “0”
14	Logic “0”
13	Logic “0”
12	Logic “0”
11	Logic “0”
10	Message Error
9	Instrumentation
8	Service Request
7	Reserved
6	Reserved
5	Reserved
4	Braodcast Command Received
3	Busy
2	SSFLAG
1	Dynamic Bus Control Accept
0 (LSB)	Terminal Flag

Table 20. RT BIT Word Register (Read/Write 0FH)	
BIT	**Description**
15 (MSB)	Transmitter Timeout
14	Loop Test Failure B
13	Loopt Test Failure A
12	Handshake Failure
11	Transmitter Shutdown B
10	Transmitter Shutdown A
9	Terminal Flag Inhibited
8	Bit Test Fail
7	High Word Count
6	Low Word Count
5	Incorrect Sync Received
4	Parity/Manchester Error Received
3	RT-to-RT Gap / Sync / Address Error
2	RT-to-RT No Response Error
1	RT-to-RT 2nd Command Word Error
0 (LSB)	Command Word Contents Error

Table 21. Configuration Register #6 (Read/Write 18H)	
BIT	**Description**
15 (MSB)	Enhanced Bus Controller
14	Enhanced CPU Access
13	Command Stack Pointer Increment on EOM (RT, MT)
12	Global Circular Buffer Enable
11	Global Circular Buffer Size 2
10	Global Circular Buffer Size 1
9	Global Circular Buffer Size 0
8	Disable Invalid Messages to Interrupt Statu Queue
7	Disbale Valid Messages to Interrupt Status Queue
6	Interrupt Status Queue Enable
5	RT Address Source
4	Enhanced Message Monitor
3	Reserved
2	64-Word Register Space
1	Clock Select 1
0 (LSB)	Clock Select 0

Table 22. Configuration Register #7 (Read/Write 19H)	
BIT	**Description**
15 (MSB)	Memory Management Base Address 15
14	Memory Management Base Address 14
13	Memory Management Base Address 13
12	Memory Management Base Address 12
11	Memory Management Base Address 11
10	Memory Management Base Address 10
9	Reserved
8	Reserved
7	Reserved
6	Reserved
5	Reserved
4	RT Halt Enable
3	1553B Response Time
2	Enhanced Time Tag Synchronize
1	Enahnced BC Watchdog Timer Enabled
0 (LSB)	Mode Code Reset / INCMD Select

Table 23. BC Condition Register (Read 1BH)	
BIT	**Description**
15 (MSB)	Logic “1”
14	Retry 1
13	Retry 0
12	Bad Message
11	Message Status Set
10	Good Block Transfer
9	Format Error
8	No Response
7	General Purpose Flag 7
6	General Purpose Flag 6
5	General Purpose Flag 5
4	General Purpose Flag 4
3	General Purpose Flag 3
2	General Purpose Flag 2
1	Equal Flag / General Purpose Flag 1
0 (LSB)	Less Than Flag / General Purpose Flag 1

Note: If the Total-ACE is not online in enhanced BC mode (i.e., processing instructions), the BC condition code register will always return a value of 0000.

Table 24. BC General Purpose Flag Register (Write 1BH)	
BIT	**Description**
15 (MSB)	Clear General Purpose Flag 7
14	Clear General Purpose Flag 6
13	Clear General Purpose Flag 5
12	Clear General Purpose Flag 4
11	Clear General Purpose Flag 3
10	Clear General Purpose Flag 2
9	Clear General Purpose Flag 1
8	Clear General Purpose Flag 0
7	Set General Purpose Flag 7
6	Set General Purpose Flag 6
5	Set General Purpose Flag 5
4	Set General Purpose Flag 4
3	Set General Purpose Flag 3
2	Set General Purpose Flag 2
1	Set General Purpose Flag 1
0 (LSB)	Set General Purpose Flag 0

Table 25. BIT Test Status Flag Register (Read 1CH)	
BIT	**Description**
15 (MSB)	Protocol Built-In Test Complete
14	Protocol Built-In Test In-Progress
13	Protocol Built-In Test Passed
12	Protocol Built-In Test Abort
11	Protocol Built-In Test Complete / In-Progress
10	Logic “0”
9	Logic “0”
8	Logic “0”
7	RAM Built-In Test Complete
6	RAM Built-In Test In-Progress
5	RAM Built-In Test In-Passed
4	Logic “0”
3	Logic “0”
2	Logic “0”
1	Logic “0”
0 (LSB)	Logic “0”

Table 26. Interrupt Mask Register #2 (Read/Write 1DH)	
BIT	**Description**
15 (MSB)	Not Used
14	BC Op Code Parity Error
13	RT Illegal Command/Message MT Message Received
12	General Purpose Queue / Interrupt Status Queue Rollover
11	Call Stack Pointer Register Error
10	BC Trap Op Code
9	RT Command Stack 50% Rollover
8	RT Circular Buffer 50% Rollover
7	Monitor Command Stack 50% Rollover
6	Monitor Data Stack 50% Rollover
5	Enhanced BC IRQ3
4	Enhanced BC IRQ2
3	Enhanced BC IRQ1
2	Enhanced BC IRQ0
1	Bit Test Complete
0 (LSB)	Not Used

Table 27. Interrupt Status Register #2 (Read 1EH)	
BIT	**Description**
15 (MSB)	Master Interrupt
14	BC Op Code Parity Error
13	RT Illegal Command/Message MT Message Received
12	General Purpose Queue / Interrupt Status Queue Rollover
11	Call Stack Pointer Register Error
10	BC Trap Op Code
9	RT Command Stack 50% Rollover
8	RT Circular Buffer 50% Rollover
7	Monitor Command Stack 50% Rollover
6	Monitor Data Stack 50% Rollover
5	Enhanced BC IRQ3
4	Enhanced BC IRQ2
3	Enhanced BC IRQ1
2	Enhanced BC IRQ0
1	Bit Test Complete
0 (LSB)	Interrupt Chain Bit

Table 28. BC General Purpose Queue Pointer Register RT, MT Interrupt Status Queue Pointer Register (Read/Write 1FH)	
BIT	**Description**
15 (MSB)	Queue Pointer Base Address 15
14	Queue Pointer Base Address 14
13	Queue Pointer Base Address 13
12	Queue Pointer Base Address 12
11	Queue Pointer Base Address 11
10	Queue Pointer Base Address 10
9	Queue Pointer Base Address 9
8	Queue Pointer Base Address 8
7	Queue Pointer Base Address 7
6	Queue Pointer Base Address 6
5	Queue Pointer Address 5
4	Queue Pointer Address 4
3	Queue Pointer Address 3
2	Queue Pointer Address 2
1	Queue Pointer Address 1
0 (LSB)	Queue Pointer Address 0

Note: *Table 29 to Table 35 are not Registers, but they are words stored in RAM.*

Table 29. BC Mode Block Status Word	
BIT	**Description**
15 (MSB)	EOM
14	SOM
13	Channel B/$\overline{A}$
12	Error Flag
11	Status Set
10	Format Error
9	No Response Timeout
8	Loop Test Fail
7	Masked Status Set
6	Retry Count 1
5	Retry Count 0
4	Good Data Block Transfer
3	Wrong Status Address / No Gap
2	Word Count Error
1	Incorrect Sync Type
0 (LSB)	Invalid Word

Table 30. RT Mode Block Status Word	
BIT	**Description**
15 (MSB)	EOM
14	SOM
13	Channel B/$\overline{\text{A}}$
12	Error Flag
11	RT-to-RT Format
10	Format Error
9	No Response Timeout
8	Loop Test Fail
7	Data Stack Rollover
6	Illegal Command Word
5	Word Count Error
4	Incorrect Data Sync
3	Invalid Word
2	RT-to-RT Gap / Sync / Address Error
1	RT-to-RT 2nd Command Error
0 (LSB)	Command Word Contents Error

Table 31. 1553 Command Word	
BIT	**Description**
15 (MSB)	Remote Terminal Address BIT 4
14	Remote Terminal Address BIT 3
13	Remote Terminal Address BIT 2
12	Remote Terminal Address BIT 1
11	Remote Terminal Address BIT 0
10	Transmit / $\overline{\text{Receive}}$
9	Subaddress / Mode Code BIT 4
8	Subaddress / Mode Code BIT 3
7	Subaddress / Mode Code BIT 2
6	Subaddress / Mode Code BIT 1
5	Subaddress / Mode Code BIT 0
4	Data Word Count / Mode Code Bit 4
3	Data Word Count / Mode Code Bit 3
2	Data Word Count / Mode Code Bit 2
1	Data Word Count / Mode Code Bit 1
0 (LSB)	Data Word Count / Mode Code Bit 0

Table 32. Word Monitor Identification Word	
BIT	**Description**
15 (MSB)	Gap Time (MSB)
•	•
•	•
•	•
8	Gap Time (LSB)
7	Word Flag
6	$\overline{\text{This}}$ $\overline{\text{RT}}$
5	$\overline{\text{Broadcast}}$
4	Error
3	Command / $\overline{\text{Data}}$
2	Channel B/ $\overline{\text{A}}$
1	Contiguous Data / $\overline{\text{Gap}}$
0 (LSB)	$\overline{\text{Mode\_Code}}$

Table 33. Message Monitor Mode Block Status Word	
BIT	**Description**
15 (MSB)	EOM
14	SOM
13	Channel B/ $\overline{\text{A}}$
12	Error Flag
11	RT-to-RT Transfer
10	Format Error
9	No Response Timeout
8	Good Data Block Transfer
7	Data Stack Rollover
6	Reserved
5	Word Count Error
4	Incorrect Sync
3	Invalid Word
2	RT-to-RT Gap / Sync / Address Error
1	RT-to-RT 2nd Command Error
0 (LSB)	Command Word Contents Error

Table 34. RT/Monitor Interrupt Status Word (For Interrupt Status Queue)

BIT	Definition for Message Interrupt Event	Definition for Non-Message Interrupt Event
15	Transmitter Timeout	Not Used
14	Illegal Command	Not Used
13	Monitor Data Stack 50% Rollover	Not Used
12	Monitor Data Stack Rollover	Not Used
11	RT Circular Buffer 50% Rollover	Not Used
10	RT Circular Buffer Rollover	Not Used
9	Monitor Command (Descriptor) Stack 50% Rollover	Not Used
8	Monitor Command (Descriptor) Stack Rollover	Not Used
7	RT Command (Descriptor) Stack 50% Rollover	Not Used
6	RT Command (Descriptor) Stack Rollover	Not Used
5	Handshake Fail	NotUsed
4	Format Error	Time Tag Rollover
3	Mode Code Interrupt	RT Address Parity Error
2	Subaddress Control Word EOM	Protocol Self-Test Complete
1	End-Of-Message (EOM)	RAM Parity Error
0	“1” For Message Interrupt Event “0” For Non-Message Interrupt Event	

Table 35. 1553B Status Word

BIT	Description
15 (MSB)	Remote Terminal Address BIT 4
14	Remote Terminal Address BIT 3
13	Remote Terminal Address BIT 2
12	Remote Terminal Address BIT 1
11	Remote Terminal Address BIT 0
10	Message Error
9	Instrumentation
8	Service Request
7	Reserved
6	Reserved
5	Reserved
4	Broadcast Command Received
3	Busy
2	SSFLAG
1	Dynamic Bus Control Acceptance
0 (LSB)	Terminal Flag

4 NON-TEST REGISTER FUNCTION SUMMARY

A summary of the Total-ACE's 24 non-test registers follows.

4.1 Interrupt Mask Registers #1 and #2

Interrupt Mask Registers #1 and #2 are used to enable and disable interrupt requests for various events and conditions.

NOTE: Please see Appendix "F" of the Enhanced Mini-ACE Users Guide for important information applicable only to RT Mode operation, enabling of the interrupt status queue and use of specific non-message interrupts.

4.2 Configuration Registers #1 and #2

Configuration Registers #1 and #2 are used to select the Total- ACE's mode of operation, and for software control of RT Status Word bits, Active Memory Area, BC Stop-On-Error, RT Memory Management mode selection, and control of the Time Tag operation.

4.3 Start/Reset Register

The Start/Reset Register is used for "command" type functions such as software reset, BC/MT Start, Interrupt reset, Time Tag Reset, Time Tag Register Test, Initiate protocol self-test, Initiate RAM self-test, Clear self-test register, and Clear RT Halt. The Start/Reset Register also includes provisions for stopping the BC in its auto-repeat mode, either at the end of the current message or at the end of the current BC frame.

4.4 BC/RT Command Stack Register

The BC/RT Command Stack Register allows the host CPU to determine the pointer location for the current or most recent message.

4.5 BC Instruction List Pointer Register

The BC Instruction List Pointer Register may be read to determine the current location of the Instruction List Pointer for the Enhanced BC mode.

4.6 BC Control Word/RT Subaddress Control Word Register

In BC mode, the BC Control Word/RT Subaddress Control Word Register allows host access to the current word or most recent BC Control Word. The BC Control Word contains bits that select the active bus and message format, enable off-line self-test, masking of Status Word bits, enable retries and interrupts, and specify MIL-STD-

1553A or -1553B error handling. In RT mode, this register allows host access to the current or most recent Subaddress Control Word. The Subaddress Control Word is used to select the memory management scheme and enable interrupts for the current message.

4.7 Time Tag Register

The Time Tag Register maintains the value of a real-time clock. The resolution of this register is programmable from among 2, 4, 8, 16, 32, and 64 µs/LSB. The Start-of-Message (SOM) and End-of-Message (EOM) sequences in BC, RT, and Message Monitor modes cause a write of the current value of the Time Tag Register to the stack area of the RAM.

4.8 Interrupt Status Registers #1 and #2

Interrupt Status Registers #1 and #2 allow the host processor to determine the cause of an interrupt request by means of one or two read accesses. The interrupt events of the two Interrupt Status Registers are mapped to correspond to the respective bit positions in the two Interrupt Mask Registers. Interrupt Status Register #2 contains an INTERRUPT CHAIN bit, used to indicate an interrupt event from Interrupt Status Register #1.

4.9 Configuration Registers #3, #4, and #5

Configuration Registers #3, #4, and #5 are used to enable many of the Total-ACE's advanced features that were implemented by the prior generation products, the ACE and Mini-ACE (Plus). For BC, RT, and MT modes, use of the Enhanced Mode enables the various read-only bits in Configuration Register #1. For BC mode, Enhanced Mode features include the expanded BC Control Word and BC Block Status Word, additional Stop-On-Error and Stop-On-Status Set functions, frame auto-repeat, programmable intermessage gap times, automatic retries, expanded Status Word Masking, and the capability to generate interrupts following the completion of any selected message. For RT mode, the Enhanced Mode features include the expanded RT Block Status Word, combined RT/Selective Message Monitor mode, automatic setting of the TERMINAL FLAG Status Word bit following a loop test failure; the double buffering scheme for individual receive (broadcast) subaddresses, and the alternate (fully software programmable) RT Status Word. For MT mode, use of the Enhanced Mode enables the Selective Message Monitor, the combined RT/Selective Monitor modes, and the monitor triggering capability.

4.10 RT/Monitor Data Stack Address Register

The RT/Monitor Data Stack Address Register provides a read/writable indication of the last data word stored for RT or Monitor modes.

4.11 BC Frame Time Remaining Register

The BC Frame Time Remaining Register provides a read-only indication of the time remaining in the current BC frame. In the enhanced BC mode, this timer may be used for minor or major frame control, or as a watchdog timer for the BC message sequence control processor. The resolution of this register is 100 µs/LSB.

4.12 BC Time Remaining to Next Message Register

The BC Time Remaining to Next Message Register provides a read-only indication of the time remaining before the start of the next message in a BC frame. In the enhanced BC mode, this timer may also be used for the BC message sequence control processor's Delay (DLY) instruction, or for minor or major frame control. The resolution of this register is 1 µs/LSB.

4.13 BC Frame Time / RT Last Command / MT Trigger Word Register

In BC mode, this register is used to program the BC frame time, for use in the frame auto-repeat mode. The resolution of this register is 100 µs/LSB, with a range up to 6.55 seconds. In RT mode, this register stores the current (or most previous) 1553 Command Word processed by the Total-ACE RT. In the Word Monitor mode, this register is used to specify a 16-bit Trigger (Command) Word. The Trigger Word may be used to start or stop the monitor, or to generate interrupts.

4.14 BC Initial Instruction List Point Register

The BC Initial Instruction List Pointer Register enables the host to assign the starting address for the enhanced BC Instruction List.

4.15 RT Status Word Register and BIT Word Registers

The RT Status Word Register and BIT Word Registers provide read-only indications of the RT Status and BIT Words.

4.16 Configuration Registers #6 and #7

Configuration Registers #6 and #7 are used to enable the Total-ACE features that extend beyond the architecture of the ACE/Mini-ACE (Plus). These include the Enhanced BC mode; RT Global Circular Buffer (including buffer size); the RT/MT Interrupt Status Queue, including valid/invalid message filtering; enabling a software-assigned RT address; clock frequency selection; a base address for the "non-data" portion of Total-ACE memory; LSB filtering for the Synchronize (with data) time tag operations; and enabling a watchdog timer for the Enhanced BC message sequence control engine.

Note: *Please see Appendix "F" of the Enhanced Mini-ACE User's Guide for important information applicable only to RT Mode operation, enabling of the interrupt status queue and use of specific non-message interrupts.*

4.17 BC Condition Code Register

The BC Condition Code Register is used to enable the host processor to read the current value of the Enhanced BC Message Sequence Control Engine's condition flags.

4.18 BC General Purpose Flag Register

The BC General Purpose Flag Register allows the host processor to be able to set, clear, or toggle any of the Enhanced BC Message Sequence Control Engine's General Purpose condition flags.

4.19 BIT Test Status Register

The BIT Test Status Register is used to provide read-only access to the status of the protocol and RAM built-in self-tests (BIT).

4.20 BC General Purpose Queue Pointer

The BC General Purpose Queue Pointer provides a means for initializing the pointer for the General Purpose Queue, for the Enhanced BC mode. In addition, this register enables the host to determine the current location of the General Purpose Queue pointer, which is incremented internally by the Enhanced BC message sequence control engine.

4.21 RT/MT Interrupt Status Queue Pointer

The RT/MT Interrupt Status Queue Pointer provides a means for initializing the pointer for the Interrupt Status Queue, for RT, MT, and RT/MT modes. In addition, this register enables the host to determine the current location of the Interrupt Status Queue pointer, which is incremented by the RT/MT message processor.

5 BUS CONTROLLER (BC) ARCHITECTURE

The BC functionality for the Total-ACE includes two separate architectures: (1) the older, non-Enhanced Mode, which provides complete compatibility with the previous ACE and Mini-ACE (Plus) generation products; and (2) the newer, Enhanced BC mode. The Enhanced BC mode offers several new powerful architectural features. These include the incorporation of a highly autonomous BC message sequence control engine, which greatly serves to offload the operation of the host CPU.

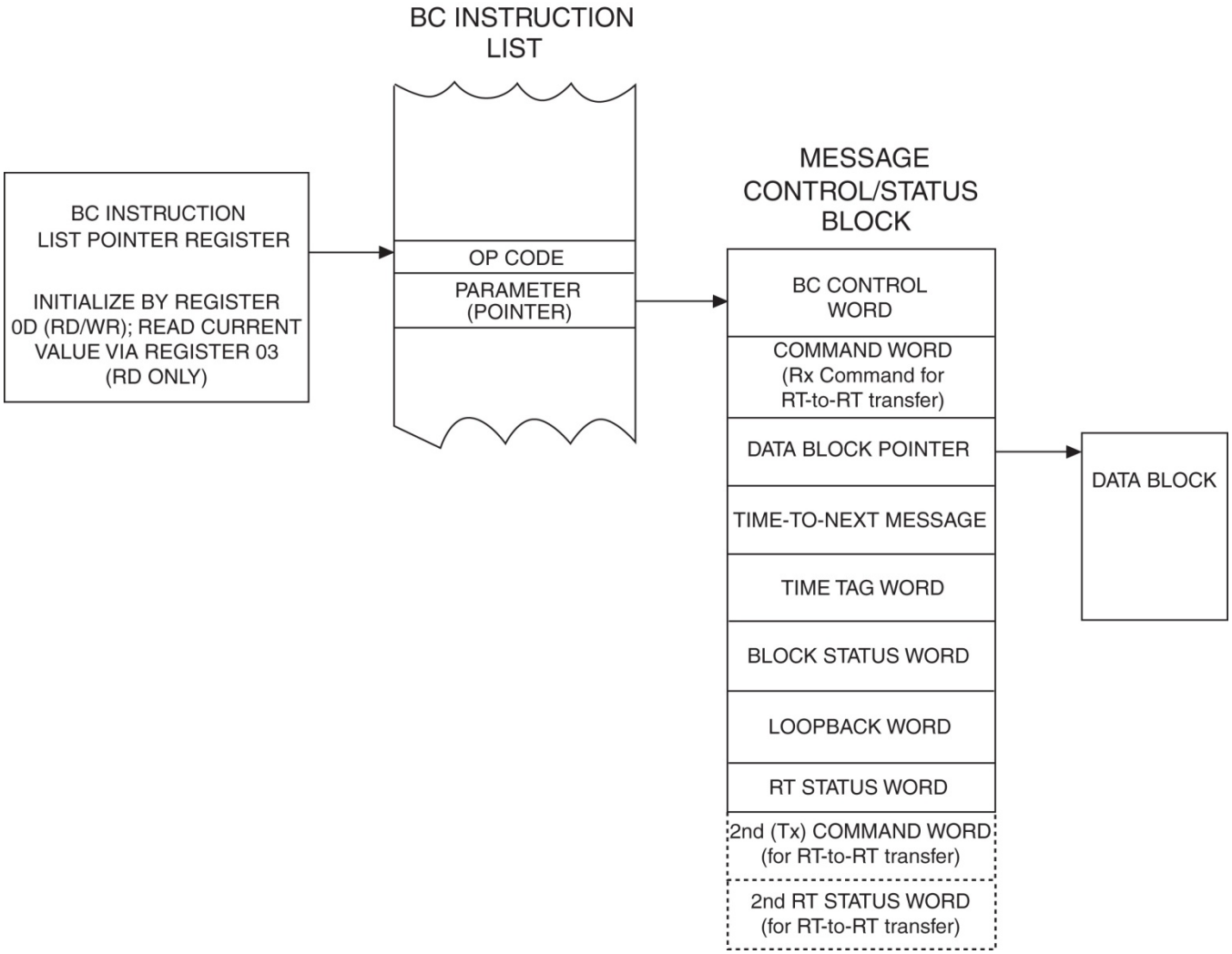


Figure 3. BC Message Sequence Control

The Enhanced BC's message sequence control engine provides a high degree of flexibility for implementing major and minor frame scheduling; capabilities for inserting asynchronous messages in the middle of a frame; to separate 1553 message data from control/status data for the purpose of implementing double buffering and performing bulk data transfers; for implementing message retry schemes, including the capability for automatic bus channel switchover for failed

messages; and for reporting various conditions to the host processor by means of four userdefined interrupts and a general purpose queue.

In both the non-Enhanced and Enhanced BC modes, the Total-ACE BC implements all MIL-STD-1553B message formats. Message format is programmable on a message-by-message basis by means of the BC Control Word and the T/R bit of the Command Word for the respective message. The BC Control Word allows 1553 message format, 1553A/B type RT, bus channel, self-test, and Status Word masking to be specified on an individual message basis. In addition, automatic retries and/or interrupt requests may be enabled or disabled for individual messages. The BC performs all error checking required by MILSTD- 1553B. This includes validation of response time, sync type and sync encoding, Manchester II encoding, parity, bit count, word count, Status Word RT Address field, and various RT-to-RT transfer errors. The Total-ACE BC response timeout value is programmable with choices of 18, 22, 50, and 130 µs. The longer response timeout values allow for operation over long buses and/ or the use of repeaters.

In its non-Enhanced Mode, the Total-ACE may be programmed to process BC frames of up to 512 messages with no processor intervention. In the Enhanced BC mode, there is no explicit limit to the number of messages that may be processed in a frame. In both modes, it is possible to program for either single frame or frame auto-repeat operation. In the auto-repeat mode, the frame repetition rate may be controlled either internally, using a programmable BC frame timer, or from an external trigger input.

5.1 Enhanced BC Mode: Message Sequence Control

One of the major new architectural features of the Total-ACE series is its advanced capability for BC message sequence control. The Total-ACE supports highly autonomous BC operation, which greatly offloads the operation of the host processor.

The operation of the Total-ACE's message sequence control engine is illustrated in Figure 3. The BC message sequence control involves an instruction list pointer register; an instruction list which contains multiple 2-word entries; a message control/status stack, which contains multiple 8-word or 10-word descriptors; and data blocks for individual messages.

The initial value of the instruction list pointer register is initialized by the host processor (via Register 0D), and is incremented by the BC message sequence processor (host readable via Register 03). During operation, the message sequence control processor fetches the operation referenced by the instruction list pointer register from the instruction list.

Note that the pointer parameter referencing the first word of a message's control/status block (the BC Control Word) must contain an address value that is **modulo 8**. Also, note that if the message is an RT-to-RT transfer, the pointer parameter must contain an address value that is **modulo 16**.

5.2 OP Codes

The instruction list pointer register references a pair of words in the BC instruction list: an op code word, followed by a parameter word. The format of the op code word, which is illustrated in Figure 4, includes a 5-bit op code field and a 5-bit condition code field. The op code identifies the instruction to be executed by the BC message sequence controller.

Most of the operations are conditional, with execution dependent on the contents of the condition code field. Bits 3-0 of the condition code field identifies a particular condition. Bit 4 of the condition code field identifies the logic sense ("1" or "0") of the selected condition code on which the conditional execution is dependent. Table 36 lists all the op codes, along with their respective mnemonic, code value, parameter, and description. Table 37 defines all the condition codes.

Eight of the condition codes (8 through F) are set or cleared as the result of the most recent message. The other eight are defined as "General Purpose" condition codes GP0 through GP7. There are three mechanisms for programming the values of the General Purpose Condition Code bits: (1) They may be set, cleared, or toggled by the host processor, by means of the BC GENERAL PURPOSE FLAG REGISTER; (2) they may be set, cleared, or toggled by the BC message sequence control processor, by means of the GP Flag Bits (FLG) instruction; and (3) GP0 and GP1 only (but none of the others) may be set or cleared by means of the BC message sequence control processor's Compare Frame Timer (CFT) or Compare Message Timer (CMT) instructions.

Figure 4. BC OP Code Format

The host processor also has read-only access to the BC condition codes by means of the BC CONDITION CODE REGISTER.

Note that four (4) instructions are **unconditional**. These are Compare to Frame Timer (CFT), Compare to Message Timer (CMT), GP Flag Bits (FLG), and Execute and Flip (XQF). For these instructions, the Condition Code Field is "don't care". That

is, these instructions are **always** executed, regardless of the result of the condition code test.

All of the other instructions are conditional. That is, they will only be executed if the condition code specified by the condition code field in the op code word tests true. If the condition code field tests false, the instruction list pointer will skip down to the next instruction.

As shown in Table 36, many of the operations include a singleword parameter. For an XEQ (execute message) operation, the parameter is a pointer to the start of the message's Control / Status block. For other operations, the parameter may be an address, a time value, an interrupt pattern, a mechanism to set or clear general purpose flag bits, or an immediate value. For several op codes, the parameter is "don't care" (not used).

As described above, some of the op codes will cause the message sequence control processor to execute messages. In this case, the parameter references the first word of a message Control/Status block. With the exception of RT-to-RT transfer messages, all message status/control blocks are eight words long: a block control word, time-to-next-message parameter, data block pointer, command word, status word, loopback word, block status word, and time tag word.

In the case of an RT-to-RT transfer message, the size of the message control/status block increases to 16 words. However, in this case, the last six words are not used; the ninth and tenth words are for the second command word and second status word.

The third word in the message control/status block is a pointer that references the first word of the message's data word block. Note that the data word block stores only data words, which are to be either transmitted or received by the BC. By segregating data words from command words, status words, and other control and "housekeeping" functions, this architecture enables the use of convenient, usable data structures, such as circular buffers and double buffers.

Other operations support program flow control; i.e., jump and call capability. The call capability includes maintenance of a call stack which supports a maximum of four (4) entries; there is also a return instruction. In the case of a call stack overrun or underrun, the BC will issue a CALL STACK POINTER REGISTER ERROR interrupt, if enabled.

Other op codes may be used to delay for a specified time; start a new BC frame; wait for an external trigger to start a new frame; perform comparisons based on frame time and time-to-next message; load the time tag or frame time registers; halt; and issue host interrupts. In the case of host interrupts, the message control processor

passes a 4-bit user-defined interrupt vector to the host, by means of the Total-ACE's Interrupt Status Register.

The purpose of the FLG instruction is to enable the message sequence controller to set, clear, or toggle the value(s) of any or all of the eight general purpose condition flags.

The op code parity bit encompasses all sixteen bits of the op code word. This bit must be programmed for odd parity. If the message sequence control processor fetches an undefined op code word, an op code word with even parity, or bits 9-5 of an op code word do not have a binary pattern of 01010, the message sequence control processor will immediately halt the BC's operation. In addition, if enabled, a BC TRAP OP CODE interrupt will be issued. Also, if enabled, a parity error will result in an OP CODE PARITY ERROR interrupt. Table 37 describes the Condition Codes.

Table 36. BC Operations for Message Sequence Control

Instruction	Mnemonic	OP Code (Hex)	Parameter	Conditional or Unconditional	Description
Execute Message	XEQ	0001	Message Control / Status Block Address	Conditional (see Note)	Executes the message at the specified Message Contro/Status Block Address if the condition flag tests TRUE, otherwise continue execution at the next OpCode in the instruction list.
Jump	JMP	0002	Instruction List Address	Conditional	Jump to the OpCode specified in the Instruction List if the condition flag test TRUE, otherwise continue execution at the next OpCode in the instruction list.
Subroutine Call	CAL	0003	Instruction List Address	Conditional	Jump to the OpCode specified by the Instruction List Address and push the Address of the Next OpCode on the Call Stack if the condition flag tests TRUE, otherwise continue execution at the next OpCode in the instruction list. Note that the maximum depth of the subroutine call stack is **four**.
Subroutine Return	RTN	0004	Not Used (Don't Care)	Conditional	Return to the OpCode popped off the Call Stack if the condition flag tests TRUE, otherwise continue execution at the next OpCode in the instruction list.
Interrupt Request	IRQ	0006	Interrupt Bit Pattern in 4 LS bits	Conditional	Generate an interrupt if the condition flag tests TRUE, otherwise continue execution at the next OpCode in the instruction list. The passed parameter (Interrupt Bit Pattern) specifies which of the ENHANCED BC IRQ bit(s) (bits 5-2) will be set in Interrupt Status Register #2. Only the four LSBs of the passed parameter are used. A parameter where the four LSBs are logic "0" will **not** generate an interrupt.

Table 36. BC Operations for Message Sequence Control					
Instruction	**Mnemonic**	**OP Code (Hex)**	**Parameter**	**Conditional or Unconditional**	**Description**
Halt	HLT	0007	Not Used (Don't Care)	Conditional	Stop execution of the Message Sequence Control Program until a new BC Start is issued by the host if the condition flag tests TRUE, otherwise continue execution at the next OpCode in the instruction list.
Delay	DLY	0008	Delay Time Value (Resolution = 1µs / LSB)	Conditional	Delay the time specified by the Time parameter before executing the next OpCode if the condition flag tests TRUE, otherwise continue execution at the next OpCode without delay. The delay generated will use the Time to Next Message Timer.
Wait Until Frame Timer = 0	WFT	0009	Not Used (Don't Care)	Conditional	Wait until Frame Time counter is equal to Zero before continuing execution of the Message Sequence Control Program if the condition flag tests TRUE, otherwise continue execution at the next OpCode without delay.
Compare to Frame Timer	CFT	000A	Delay Time Value (Resolution = 1µs / LSB)	Unconditional	Compare Time Value to Frame Time Counter. The LT/GP0 and EQ/GP1 flag bits are set or cleared based on the results of the compare. If the value of the CFT's parameter is less than the value of the frame time counter, then the LT/GP0 flag will be set, while the EQ/GP1 flag will be cleared. If the value of the CFT's parameter is equal to the value of the frame time counter, then the EQ/GP1 flag will be set, while the LT/GP0 flag will be cleared. If the value of the CFT's parameter is greater than the current value of the frame time counter, the LT/GP0 and EQ/GP1 flags will be cleared.
Compare to Message Timer	CMT	000B	Delay Time Value (Resolution = 1µs / LSB)	Unconditional	Compare Time Value to Message Time Counter. The LT/GP0 and EQ/GP1 flag bits are set or cleared based on the results of the compare. If the value of the CMT's parameter is less than the value of the message time counter, then the LT/GP0 flag will be set, while the GT-EQ/GP0 and EQ/GP1 flags will be cleared. If the value of the CMT's parameter is equal to the value of the message time counter, then the EQ/GP1 flag will be set, while the LT/GP0 flag will be cleared. If the value of the CMT's parameter is greater than the current value of the message time counter, then the LT/GP0 and EQ/GP1 flags

Table 36. BC Operations for Message Sequence Control

<table>
<tr><th>Instruction</th><th>Mnemonic</th><th>OP Code (Hex)</th><th>Parameter</th><th>Conditional or Unconditional</th><th>Description</th></tr>
<tr><td></td><td></td><td></td><td></td><td></td><td>will be cleared.</td></tr>
<tr><td>GP Flag Bits</td><td>FLG</td><td>000C</td><td>Used to set, clear, or toggle GP (General Purpose) Flag bits (see description)</td><td>Unconditional</td><td>Used to set, toggle, or clear any or all of the eight general purpose flags. The table below illustrates the use of the GP Flag Bits instruction for the case of GP0 (General Purpose Flag 0). Bits 1 and 9 of the parameter byte affect flag GP1, bits 2 and 10 effect GP2, etc., according to the following rules:
<table>
<tr><th>Bit 8</th><th>Bit 0</th><th>Effect on GP0</th></tr>
<tr><td>0</td><td>0</td><td>No Change</td></tr>
<tr><td>0</td><td>1</td><td>Set Flag</td></tr>
<tr><td>1</td><td>0</td><td>Clear Flag</td></tr>
<tr><td>1</td><td>1</td><td>Toggle Flag</td></tr>
</table></td></tr>
<tr><td>Load Time Tag Counter</td><td>LTT</td><td>000D</td><td>Time Value Resolution (µs/ LSB) is defined by bits 9, 8, & 7 of Configuration Register #2</td><td>Conditional</td><td>Load Time Tag Counter with Time Value if the condition flag tests TRUE, otherwise continue execution at the next OpCode in the instruction list.</td></tr>
<tr><td>Load Frame Timer</td><td>LFT</td><td>000E</td><td>Time Value (resolution = 100 µs/LSB)</td><td>Conditional</td><td>Load Frame Timer Register with the Time Value parameter if the condition flag tests TRUE, otherwise continue execution at the next OpCode in the instruction list.</td></tr>
<tr><td>Start Frame Timer</td><td>SFT</td><td>000F</td><td>Not Used (Don’t Care)</td><td>Conditional</td><td>Start Frame Time Counter with Time Value in Time Frame register if the condition flag tests TRUE, otherwise continue execution at the next OpCode in the instruction list.</td></tr>
<tr><td>Push Time Tag Register</td><td>PTT</td><td>0010</td><td>Not Used (Don’t Care)</td><td>Conditional</td><td>Push the value of the Time Tag Register on the General Purpose Queue if the condition flag tests TRUE, otherwise continue execution at the next OpCode in the instruction list.</td></tr>
<tr><td>Push Block Status Word</td><td>PBS</td><td>0011</td><td>Not Used (Don’t Care)</td><td>Conditional</td><td>Push the Block Status Word for the most recent message on the General Purpose Queue if the condition flag tests TRUE, otherwise continue execution at the next OpCode in the instruction list.</td></tr>
<tr><td>Push Immediate Value</td><td>PSI</td><td>0012</td><td>Immediate Value</td><td>Conditional</td><td>Push Immediate data on the General Purpose Queue if the condition flag tests TRUE, otherwise continue execution at the next OpCode in the</td></tr>
</table>

Table 36. BC Operations for Message Sequence Control					
Instruction	**Mnemonic**	**OP Code (Hex)**	**Parameter**	**Conditional or Unconditional**	**Description**
					instruction list.
Push Indirect	PSM	0013	Memory Address	Conditional	Push the data stored at the specified memory location on the General Purpose Queue if the condition flag tests TRUE, otherwise continue execution at the next OpCode in the instruction list.
Wait for External Trigger	WTG	0014	Not Used (Don't Care)	Conditional	Wait for a logic "0"-to-logic "1" transition on the EXT_TRIG input signal before proceeding to the next OpCode in the instruction list if the condition flag tests TRUE, otherwise continue execution at the next OpCode without delay.
Execute and Flip	XQF	0015	Message Control / Status Block Address	Unonditional	Execute (unconditionally) the message referenced by the Message Control/Status Block Address. Following the processing of this message, if the condition flag tests TRUE, the BC will toggle bit 4 in the Message Control/Status Block Address, and store the new Message Block Address as the updated value of the parameter following the XQF instruction code. As a result, the **next** time that this line in the instruction list is executed, the Message Control/Status Block at the **updated** address (**old address XOR 0010h**), rather than the old address, will be processed. If the condition flag tests FALSE, the value of the Message Control/Status Block Address parameter will not change.

Note: While the XEQ (Execute Message) instruction is conditional, not all condition codes may be used to enable its use. The ALWAYS and NEVER condition codes may be used. The eight general purpose flag bits, GP0 through GP7, may also be used. However, if GP0 through GP7 are used, it is imperative that the host processor not modify the value of the specific general purpose flag bit that enabled a particular message while that message is being processed. Similarly, the LT, GT-EQ, EQ, and NE flags, which the BC only updates by means of the CFT and CMT instructions, may also be used. However, these two flags are dual use. Therefore, if these are used, it is imperative that the host processor not modify the value of the specific flag (GP0 or GP1) that enabled a particular message while that message is being processed. The NORESP, FMT ERR, GD BLK XFER, MASKED STATUS SET, BAD MESSAGE, RETRY0, and RETRY1 condition codes are not available for use with the XEQ instruction and should not be used to enable its execution

Table 37. BC Condition Codes			
BIT Code	**Name (BIT 4 = 0)**	**Inverse (BIT 4 = 1)**	**Functional Description**
0	LT/GP0	GT-EQ / $\overline{\text{GP0}}$	Less than or GP0 flag. This bit is set or cleared based on the results of the compare. If the value of the CMT's parameter is less than the value of the message time counter, then the LT/GP0 flag will be set. If the value of the CMT's parameter is greater than or equal to the value of the message time counter, then the LT/GP0 flag will be cleared. Also, General Purpose Flag 1 may be set or cleared by a FLG operation.
1	EQ/GP1	NE/ $\overline{\text{GP1}}$	Equal Flag. This bit is set or cleared after CFT or CMT operation. If the value of the CMT's parameter is equal to the value of the message time counter, then the EQ/GP1 flag will be set. If the value of the CMT's parameter is not equal to the value of the message time counter, then the EQ/GP1 flag will be cleared. Also, General Purpose Flag 1 may be set or cleared by a FLG operation.
2	GP2	$\overline{\text{GP2}}$	General Purpose Flags may be set, cleared, or toggled by a FLG operation. The host processor can set, clear, or toggle these flags in the same way as the FLG instruction by means of the BC GENERAL PURPOSE FLAG REGISTER.
3	GP3	$\overline{\text{GP3}}$	
4	GP4	$\overline{\text{GP4}}$	
5	GP5	$\overline{\text{GP5}}$	
6	GP6	$\overline{\text{GP6}}$	
7	GP7	$\overline{\text{GP7}}$	
8	NORESP	$\overline{\text{RESP}}$	NORESP indicates that an RT has either not responded or has responded later than the BC No Response Timeout time. The Total-ACE's No Response Timeout Time is defined per MIL-STD-1553B as the time from the mid-bit crossing of the parity bit of the last word transmitted by the BC to the mid-sync crossing of the RT Status Word. The value of the No Response Timeout value is programmable from among the nominal values 18.5, 22.5, 50.5, and 130 µs (±1 µs) by means of bits 10 and 9 of Configuration Register #5.
9	FMT ERR	$\overline{\text{FMT ERR}}$	FMT ERR indicates that the received portion of the most recent message contained one or more violations of the 1553 message validation criteria (sync, encoding, parity, bit count, word count, etc.), or the RT's status word received from a responding RT contained an incorrect RT address field.
A	GD BLK XFER	$\overline{\text{GD BLK XFER}}$	For the most recent message, GD BLK XFER will be set to logic "1" following completion of a valid (error-free) RT-to-BC transfer, RT-to-RT transfer, or transmit mode code with data message. This bit is set to logic "0" following an invalid message. GOOD DATA BLOCK TRANSFER is **always** logic "0" following a BC-to-RT transfer, a mode code with data, or a mode code without data. The Loop Test has **no effect** on GOOD DATA BLOCK TRANSFER. GOOD DATA BLOCK TRANSFER may be used to determine if the transmitting portion of an RT-to-RT transfer was error free.
B	MASKED STATUS BIT	**Error!** $\overline{\text{BIT}}$	Indicates that one or both of the following conditions have occurred for the most recent message: (1) If one (or more) of the Status Mask bits (14 through 9) in the BC Control Word is logic

Table 37. BC Condition Codes

BIT Code	Name (BIT 4 = 0)	Inverse (BIT 4 = 1)	Functional Description
			"0" **and** the corresponding bit(s) is (are) set (logic "1") in the received RT Status Word. In the case of the RESERVED BITS MASK (bit 9) set to logic "0," any or all of the 3 Reserved Status Word bits being set will result in a MASKED STATUS SET condition; and/or (2) If BROADCAST MASK ENABLED/$\overline{\text{XOR}}$ (bit 11 of Configuration Register #4) is logic "1" **and** the MASK BROADCAST bit of the message's BC Control Word is logic "0" and the BROADCAST COMMAND RECEIVED bit in the received RT Status Word is logic "1."
C	BAD MESSAGE	GOOD MESSAGE	BAD MESSAGE indicates either a format error, loop test fail, or no response error for the most recent message. Note that a "Status Set" condition has **no effect** on the "BAD MESSAGE/GOOD MESSAGE" condition code.
D	RETRY0	$\overline{\text{RETRY0}}$	These two bits reflect the retry status of the most recent message. The number of times that the message was retried is delineated by these two bits as shown below: Retry Count 1 (bit 14) / Retry Count 2 (bit 13) / Number of Message Retries 0 / 0 / 0 0 / 1 / 1 1 / 0 / N/A 1 / 1 / 2
E	RETRY1	$\overline{\text{RETRY1}}$	
F	ALWAYS	NEVER	The ALWAYS flag should be set (bit 4 = 0) to designate an instruction as unconditional. The NEVER bit (bit 4 = 1) can be used to implement a NOP or "skip" instruction.

5.3 BC Message Sequence Control

The Total-ACE BC message sequence control capability enables a high degree of offloading of the host processor. This includes using the various timing functions to enable autonomous structuring of major and minor frames. In addition, by implementing conditional jumps and subroutine calls, the message sequence control processor greatly simplifies the insertion of asynchronous, or "out-of-band" messages.

5.4 Execute and Flip Operation

The Total-ACE BC's XQF, or "Execute and Flip" operation, provides some unique capabilities. Following execution of this unconditional instruction, if the condition code tests TRUE, the BC will modify the value of the current XQF instruction's pointer parameter by toggling bit 4 of the pointer. That is, if the selected condition flag tests true, the value of the parameter will be **updated** to the value = **old address XOR**

0010h. As a result, the next time that this line in the instruction list is executed, the Message Control/Status Block at the updated address (old address XOR 0010h) will be processed, rather than the one at the old address. The operation of the XQF instruction is illustrated in Figure 5.

There are multiple ways of utilizing the "execute and flip" instruction. One is to facilitate the implementation of a double buffering data scheme for individual messages. This allows the message sequence control processor to "ping-pong" between a pair of data buffers for a particular message. By doing so, the host processor can access one of the two Data Word blocks, while the BC reads or writes the alternate Data Word block.

A second application of the "execute and flip" capability is in conjunction with message retries. This allows the BC to not only switch buses when retrying a failed message, but to automatically switch buses **permanently** for all future times that the same message is to be processed. This not only provides a high degree of autonomy from the host CPU, but saves BC bandwidth, by eliminating the need for future attempts to process messages on an RT's failed channel.

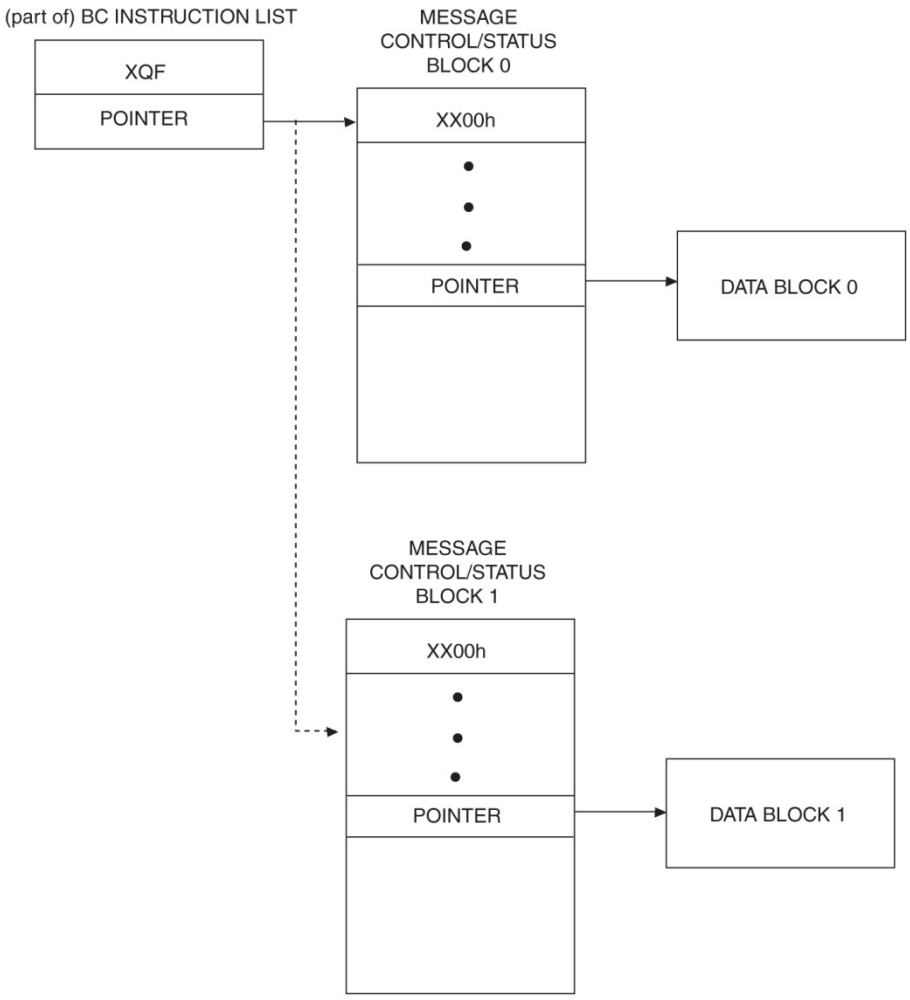


Figure 5. EXECUTE and FLIP (XQF) Operation

5.5 General Purpose Queue

The Total-ACE BC allows for the creation of a general purpose queue. This data structure provides a means for the message sequence processor to convey information to the BC host. The BC op code repertoire provides mechanisms to push various items on this queue. These include the contents of the Time Tag Register, the Block Status Word for the most recent message, an immediate data value, or the contents of a specified memory address.

Figure 6 illustrates the operation of the BC General Purpose Queue. Note that the BC General Purpose Queue Pointer Register will always point to the **next** address location (modulo 64); that is, the location **following** the last location written by the BC message sequence control engine.

If enabled, a BC GENERAL PURPOSE QUEUE ROLLOVER interrupt will be issued when the value of the queue pointer address rolls over at a 64-word boundary. The rollover will always occur at a modulo 64 address.

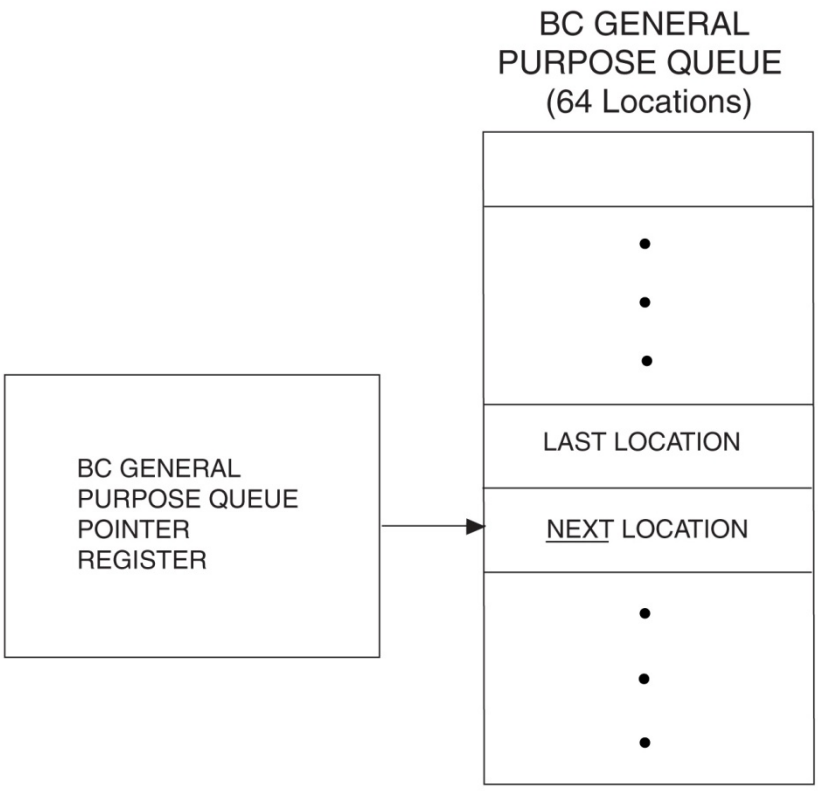


Figure 6. BC General Purpose Queue

6 REMOTE TERMINAL (RT) ARCHITECTURE

The Total-ACE's RT architecture builds upon that of the ACE and Mini-ACE. The Total-ACE provides multiprotocol support, with full compliance to all of the commonly used data bus standards, including MIL-STD-1553A, MIL-STD-1553B Notice 2, STANAG 3838, General Dynamics 16PP303, and McAir A3818, A5232, and A5690. For the Total-ACE RT mode, there is programmable flexibility enabling the RT to be configured to fulfill any set of system requirements. This includes the capability to meet the MIL-STD-1553A response time requirement of 2 to 5 µs, and multiple options for mode code subaddresses, mode codes, RT status word, and RT BIT word.

The Total-ACE RT protocol design implements all of the MILSTD- 1553B message formats and dual redundant mode codes. The design has passed validation testing for MIL-STD-1553B compliance. The Total-ACE RT performs comprehensive error checking including word and format validation, and checks for various RT-to-RT transfer errors. One of the main features of the Total-ACE RT is its choice of memory management options. These include single buffering by subaddress, double buffering for individual receive subaddresses, circular buffering by individual subaddresses, and global circular buffering for multiple (or all) subaddresses.

Other features of the Total-ACE RT include a set of interrupt conditions, a flexible status queue with filtering based on valid and/or invalid messages, flexible command illegalization, programmable busy by subaddress, multiple options on time tagging, and an "auto-boot" feature which allows the RT to initialize as an online RT with the busy bit set following power turn-on.

6.1 RT Memory Organization

Table 38 illustrates a typical memory map for an Total-ACE RT with 4K RAM. The two Stack Pointers reside in fixed locations in the shared RAM address space: address 0100 (hex) for the Area A Stack Pointer and address 0104 for the Area B Stack Pointer. In addition to the Stack Pointer, there are several other areas of the shared RAM address space that are designated as fixed locations (all shown in **bold**). These are for the Area A and Area B lookup tables, the illegalization lookup table, the busy lookup table, and the mode code data tables.

The RT lookup tables (see Table 39) provide a mechanism for allocating data blocks for individual transmit, receive, or broadcast subaddresses. The RT lookup tables include subaddress control words as well as the individual data block pointers. If command illegalization is used, address range 0300-03FF is used for command illegalizing. The descriptor stack RAM area, as well as the individual data blocks, may be located in any of the non-fixed areas in the shared RAM address space.

Note that in Table 38, there is no area allocated for "Stack B". This is shown for purpose of simplicity of illustration. Also, note that in Table 38, the allocated area for the RT command stack is 256 words. However, larger stack sizes are possible. That is, the RT command stack size may be programmed for 256 words (64 messages), 512, 1024, or 2048 words (512 messages) by means of bits 14 and 13 of Configuration Register 3.

Table 38. Typical RT Memory Map (Shown for 4K RAM)

Address (HEX)	Description
0000-00FF	Stack A
0100	**Stack Pointer A**
0101	**Global Circular Buffer A Pointer**
0102-0103	RESERVED
0104	**Stack Pointer B**
0105	**Global Circular Buffer B Pointer**
0106-0107	RESERVED
0108-010F	**Mode Code Selective Interrupt Table**
0110-013F	**Mode Code Data**
0140-01BF	**Lookup Table A**
01C0-023F	**Lookup Table B**
0240-0247	**Busy Bit Lookup Table**
0248-025F	(not used)
0260-027F	Data Block 0
0280-02FF	Data Block 1-4
0300-03FF	**Command Illegalization Table**
0400-041F	Data Block 5
0420-043F	Data Block 6
□	□
□	□
□	□
0FE0-0FFF	Data Block 100

Table 39. RT Look-up Tables			
Area A	**Area B**	**Description**	**Comment**
0140 □ □ □ 015F	01C0 □ □ □ 01DF	Rx(/Bcst) SA0 □ □ □ Rx(/Bcst) SA31	Receive (/Broadcast) Lookup Pointer Table
0160 □ □ □ 017F	01E0 □ □ □ 01FF	Tx SA0 □ □ □ Tx SA31	Transmit Lookup Pointer Table
0180 □ □ □ 019F	0200 □ □ □ 021F	Bcst SA0 □ □ □ Bcst SA31	Braodcast Lookup Pointer Table (Optional)
01A0 □ □ □ 01BF	0220 □ □ □ 023F	SACW SA0 □ □ □ SACW SA31	Subaddress Control Word Lookup Table (Optional)

6.2 RT Memory Management

The Total-ACE provides a variety of RT memory management capabilities. As with the ACE and Mini-ACE, the choice of memory management scheme is fully programmable on a transmit/receive/broadcast subaddress basis.

In compliance with MIL-STD-1553B Notice 2, received data from broadcast messages may be optionally separated from nonbroadcast received data. For each transmit, receive or broadcast subaddress, either a single-message data block, a double buffered configuration (two alternating Data Word blocks), or a variable-sized (128 to 8192 words) subaddress circular buffer may be allocated for data storage. The memory management scheme for individual subaddresses is designated by means of the subaddress control word (reference Table 40).

For received data, there is also a global circular buffer mode. In this configuration, the data words received from multiple (or all) subaddresses are stored in a common circular buffer structure. Like the subaddress circular buffer, the size of the global circular buffer is programmable, with a range of 128 to 8192 data words.

The double buffering feature provides a means for the host processor to easily access the most recent, complete received block of valid Data Words for any given subaddress. In addition to helping ensure data sample consistency, the circular buffer

options provide a means for greatly reducing host processor overhead for multi-message bulk data transfer applications.

End-of-message interrupts may be enabled either globally (following all messages), following error messages, on a transmit/receive/broadcast subaddress or mode code basis, or when a circular buffer reaches its midpoint (50% boundary) or lower (100%) boundary. A pair of interrupt status registers allow the host processor to determine the cause of all interrupts by means of a single read operation.

Table 40. RT Subaddress Control Word – Memory Management Options

Double-Buffered or Global circular Buffer (bit 15)	Subaddress Control Word Bits			Memory Management Subaddress Buffer Scheme Description	
	MM2	MM1	MM0		
0	0	0	0	Single Message	
1	0	0	0	For Receive or Broadcast: Double Buffered For Transmit: Single Message	
0	0	0	1	128-Word	Subaddress – specified circular buffer of specified size.
0	0	1	0	256-Word	
0	0	1	1	512-Word	
0	1	0	0	1024-Word	
0	1	0	1	2048-Word	
0	1	1	0	4096-Word	
0	1	1	1	8192-Word	
1	1	1	1	(for receive and/or broadcast subaddress only) Global Circular Buffer: The buffer size is specified by Configuration Register #6, bits 11-9. The pointer to the global circular buffer is stored at address 0101 (for Area A) or address 0105 (for Area B)	

6.3 Single Buffered Mode

The operation of the single buffered RT mode is illustrated in Figure 7. In the single buffered mode, the respective lookup table entry must be written by the host processor. Received data words are written to, or transmitted data words are read from the data word block with starting address referenced by the lookup table pointer. In the single buffered mode, the current lookup table pointer is not updated by the Total-ACE memory management logic. Therefore, if a subsequent message is received for the same subaddress, the **same** Data Word block will be overwritten or overread.

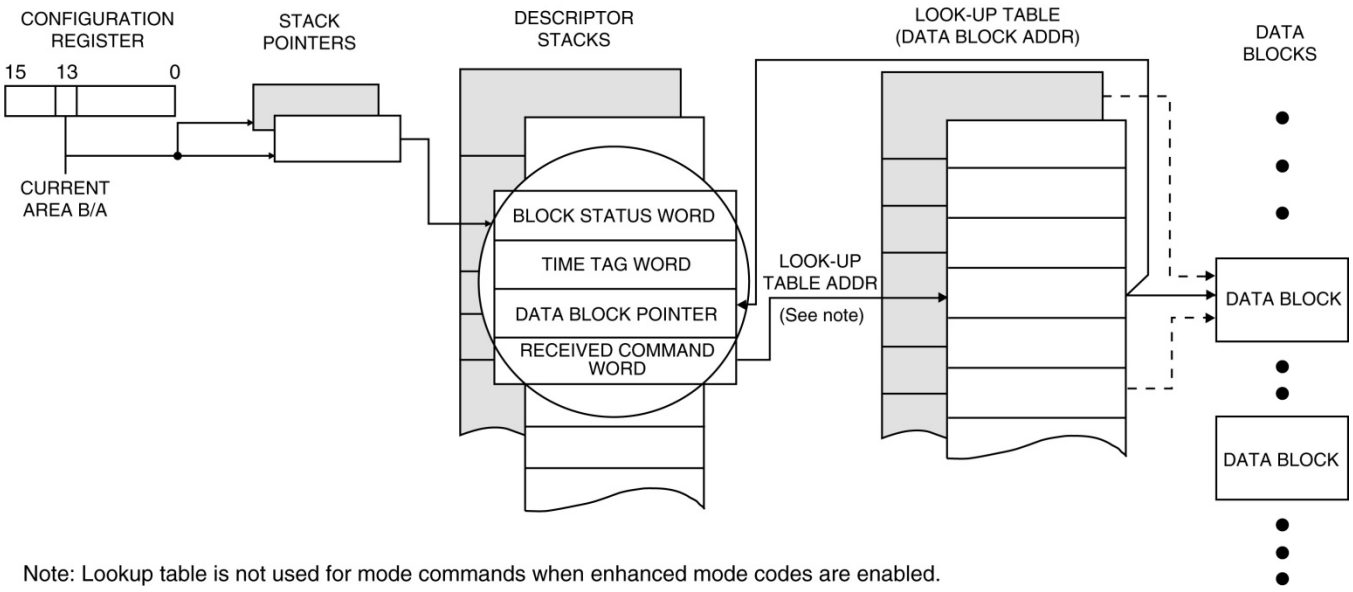


Figure 7. RT Single Buffered Mode

6.4 SUBADDRESS DOUBLE BUFFERING MODE

The Total-ACE provides a double buffering mechanism for received data, that may be selected on an individual subaddress basis for any or all receive (and/or broadcast) subaddresses. This is illustrated in Figure 8. It should be noted that the Subaddress Double Buffering mode is applicable for receive data only, **not for transmit data.** Double buffering of transmit messages may be easily implemented by software techniques.

The purpose of the subaddress double buffering mode is to provide data sample consistency to the host processor. This is accomplished by allocating **two** 32-word data word blocks for each individual receive (and/or broadcast receive) subaddress. At any given time, one of the blocks will be designated as the "active" 1553 block while the other will be considered as "inactive". The data words for the next receive command to that subaddress will be stored in the active block. Following receipt of a valid message, the Total-ACE will automatically switch the active and inactive blocks for that subaddress. As a result, the latest, valid, complete data block is always accessible to the host processor.

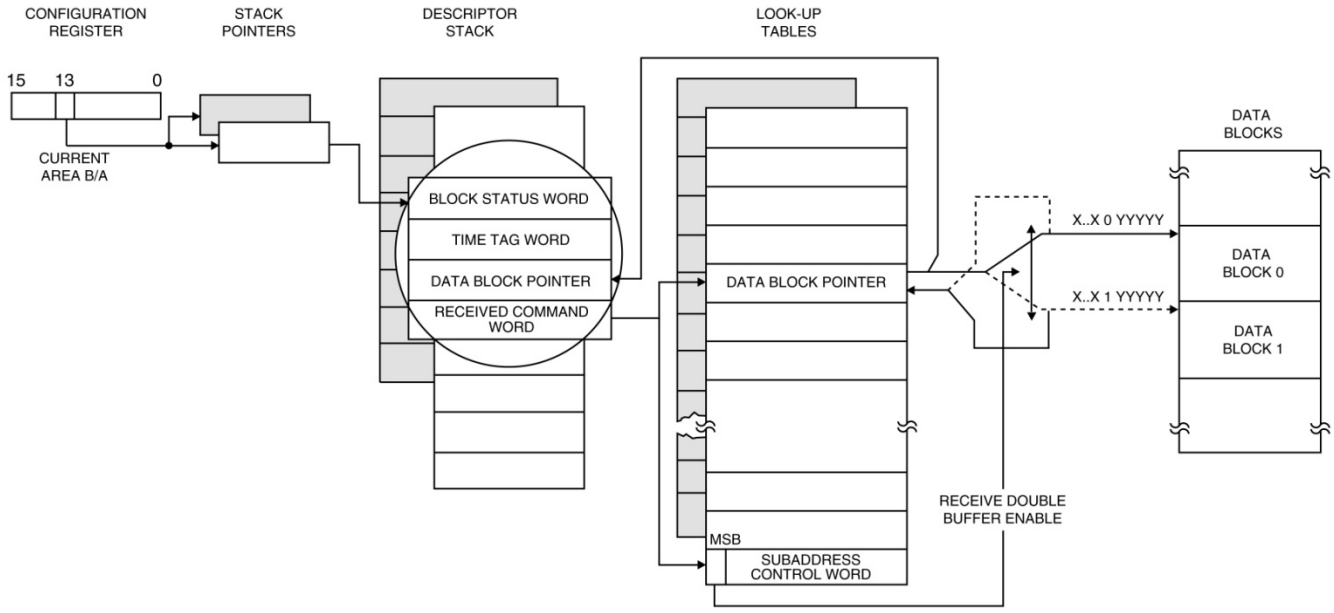


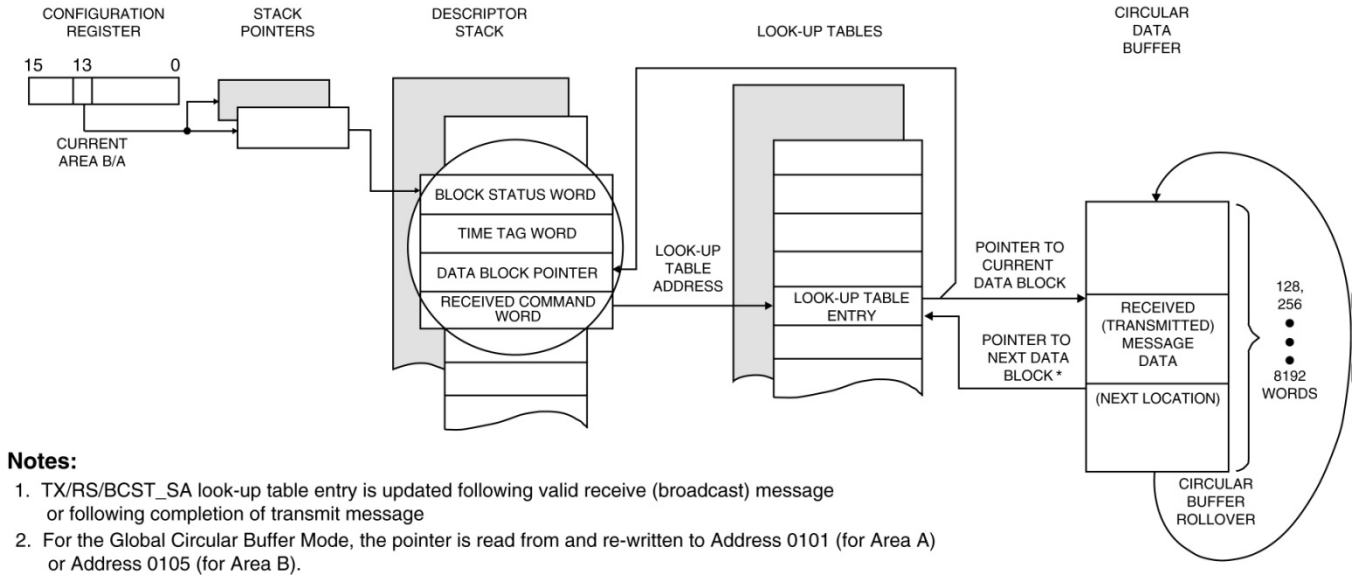
Figure 8. RT Double Buffered Mode

6.5 CIRCULAR BUFFER MODE

The operation of the Total-ACE's circular buffer RT memory management mode is illustrated in Figure 9. As in the single buffered and double buffered modes, the individual lookup table entries are initially loaded by the host processor. At the start of each message, the lookup table entry is stored in the third position of the respective message block descriptor in the descriptor stack area of RAM. Receive or transmit data words are transferred to (from) the circular buffer, starting at the location referenced by the lookup table pointer.

In general, the location after the last data word written or read (modulo the circular buffer size) during the message is written to the respective lookup table location during the end-of-message sequence. By so doing, data for the next message for the respective transmit, receive(/broadcast), or broadcast subaddress will be accessed from the next lower contiguous block of locations in the circular buffer.

For the case of a receive (or broadcast receive) message with a data word error, there is an option such that the lookup table pointer will only be updated following receipt of a **valid** message. That is, the pointer will **not** be updated following receipt of a message with an error in a data word. This allows failed messages in a bulk data transfer to be retried without disrupting the circular buffer data structure, and without intervention by the RT's host processor.



Notes:

1. TX/RS/BCST_SA look-up table entry is updated following valid receive (broadcast) message or following completion of transmit message
2. For the Global Circular Buffer Mode, the pointer is read from and re-written to Address 0101 (for Area A) or Address 0105 (for Area B).

Figure 9. RT Circular Buffered Mode

6.6 GLOBAL CIRCULAR BUFFER

Beyond the programmable choice of single buffer mode, double buffer mode, or circular buffer mode, programmable on an individual subaddress basis, the Total-ACE RT architecture provides an additional option, a variable sized **global** circular buffer. The Total-ACE RT allows for a mix of single buffered, double buffered, and individually circular buffered subaddresses, **along with** the use of the global double buffer for any arbitrary group of receive(/broadcast) or broadcast subaddresses.

In the global circular buffer mode, the data for **multiple** receive subaddresses is stored in the same circular buffer data structure. The size of the global circular buffer may be programmed for 128, 256, 512, 1024, 2048, 4096, or 8192 words, by means of bits 11, 10, and 9 of Configuration Register #6. As shown in Table 40, individual subaddresses may be mapped to the global circular buffer by means of their respective subaddress control words.

The pointer to the Global Circular Buffer will be stored in location 0101 (for Area A), or location 0105 (for Area B).

The global circular buffer option provides a highly efficient method for storing received message data. It allows for frequently used subaddresses to be mapped to individual data blocks, while also providing a method for asynchronously received messages to infrequently used subaddresses to be logged to a common area. Alternatively, the global circular buffer provides an efficient means for storing the received data words for all subaddresses. Under this method, all received data words are stored chronologically, regardless of subaddress.

6.7 RT DESCRIPTOR STACK

The descriptor stack provides a chronology of all messages processed by the Total-ACE RT. Reference Figure 7, Figure 8, and Figure 9. Similar to BC mode, there is a four-word block descriptor in the Stack for each message processed. The four entries to each block descriptor are the Block Status Word, Time Tag Word, the pointer to the start of the message's data block, and the 16-bit received Command Word.

The RT Block Status Word includes indications of whether a particular message is ongoing or has been completed, what bus channel it was received on, indications of illegal commands, and flags denoting various message error conditions. For the double buffering, subaddress circular buffering, and global circular buffering modes, the data block pointer may be used for locating the data blocks for specific messages. Note that for mode code commands, there is an option to store the transmitted or received data word as the third word of the descriptor, in place of the data block pointer.

The Time Tag Word provides a 16-bit indication of relative time for individual messages. The resolution of the Total-ACE's time tag is programmable from among 2, 4, 8, 16, 32, or 64 µs/LSB. There is also a provision for using an external clock input for the time tag. If enabled, there is a time tag rollover interrupt, which is issued when the value of the time tag rolls over from FFFF(hex) to 0. Other time tag options include the capabilities to clear the time tag register following receipt of a Synchronize (without data) mode command and/or to set the time tag following receipt of a Synchronize (with data) mode command. For the latter, there is an added option to filter the "set" capability based on the LSB of the received data word being equal to logic "0".

6.8 RT INTERRUPTS

The Total-ACE offers a great deal of flexibility in terms of RT interrupt processing. By means of the Total-ACE's two Interrupt Mask Registers, the RT may be programmed to issue interrupt requests for the following events/conditions: End-of-(every) Message, Message Error, Selected (transmit or receive) Subaddress, 100% Circular Buffer Rollover, 50% Circular Buffer Rollover, 100% Descriptor Stack Rollover, 50% Descriptor Stack Rollover, Selected Mode Code, Transmitter Timeout, Illegal Command, and Interrupt Status Queue Rollover.

Interrupts for 50% Rollovers of Stacks and Circular Buffers. The Total-ACE RT and Monitor are capable of issuing host interrupts when a subaddress circular buffer pointer or stack pointer crosses its mid-point boundary. For RT circular buffers, this is applicable for both transmit and receive subaddresses. Reference Figure 10. There are four interrupt mask and interrupt status register bits associated with the 50% rollover function:

1. RT circular buffer;
2. RT command (descriptor) stack;
3. Monitor command (descriptor) stack; and
4. Monitor data stack.

The 50% rollover interrupt is beneficial for performing bulk data transfers. For example, when using circular buffering for a particular receive subaddress, the 50% rollover interrupt will inform the host processor when the circular buffer is half full. At that time, the host may proceed to read the received data words in the upper half of the buffer, while the Total-ACE RT writes received data words to the lower half of the circular buffer. Later, when the RT issues a 100% circular buffer rollover interrupt, the host can proceed to read the received data from the lower half of the buffer, while the Total-ACE RT continues to write received data words to the upper half of the buffer.

Interrupt status queue. The Total-ACE RT, Monitor, and combined RT/Monitor modes include the capability for generating an interrupt status queue. As illustrated in Figure 11, this provides a chronological history of interrupt generating events and conditions. In addition to the Interrupt Mask Register, the Interrupt Status Queue provides additional filtering capability, such that only valid messages and/or only invalid messages may result in the creation of an entry to the Interrupt Status Queue. Queue entries for invalid and/or valid messages may be disabled by means of bits 8 and 7 of configuration register #6.

The interrupt status queue is 64 words deep, providing the capability to store entries for up to 32 messages. These events and conditions include both message-related and non-message related events. Note that the Interrupt Vector Queue Pointer Register will always point to the next location (modulo 64) following the last vector/pointer pair written by the Total-ACE RT.

The pointer to the Interrupt Status Queue is stored in the INTERRUPT VECTOR QUEUE POINTER REGISTER (register address 1F). This register must be initialized by the host, and is subsequently incremented by the RT message processor. The interrupt status queue is 64 words deep, providing the capability to store entries for up to 32 messages.

The queue rolls over at addresses of modulo 64. The events that result in queue entries include both message-related and nonmessage-related events. Note that the Interrupt Vector Queue Pointer Register will always point to the next location (modulo 64) **following** the last vector/pointer pair written by the Total-ACE RT, Monitor, or RT/Monitor.

Each event that causes an interrupt results in a two-word entry to be written to the queue. The first word of the entry is the interrupt vector. The vector indicates which interrupt event(s)/condition(s) caused the interrupt.

The interrupt events are classified into two categories: message interrupt events and non-message interrupt events. Messagebased interrupt events include End-of-Message, Selected mode code, Format error, Subaddress control word interrupt, RT Circular buffer Rollover, Handshake failure, RT Command stack rollover, transmitter timeout, MT Data Stack rollover, MT Command Stack rollover, RT Command Stack 50% rollover, MT Data Stack 50% rollover, MT Command Stack 50% rollover, and RT Circular buffer 50% rollover. Non-message interrupt events/conditions include time tag rollover, RT address parity error, RAM parity error, and BIT completed.

Bit 0 of the interrupt vector (interrupt status) word indicates whether the entry is for a message interrupt event (if bit 0 is logic "1") or a non-message interrupt event (if bit 0 is logic "0"). It is **not** possible for one entry on the queue to indicate both a message interrupt and a non-message interrupt.

As illustrated in Figure 11, for a message interrupt event, the parameter word is a pointer. The pointer will reference the first word of the RT or MT command stack descriptor (i.e., the Block Status Word).

For a RAM Parity Error non-message interrupt, the parameter will be the RAM address where the parity check failed. For the RT address Parity Error, Protocol Self-test Complete, and Time Tag rollover non-message interrupts, the parameter is not used; it will have a value of 0000.

If enabled, an INTERRUPT STATUS QUEUE ROLLOVER interrupt will be issued when the value of the queue pointer address rolls over at a 64-word address boundary.

Note: *Please see Appendix "F" of the Enhanced Mini-ACE User's Guide for important information applicable only to RT Mode operation, enabling of the interrupt status queue and use of specific non-message interrupts.*

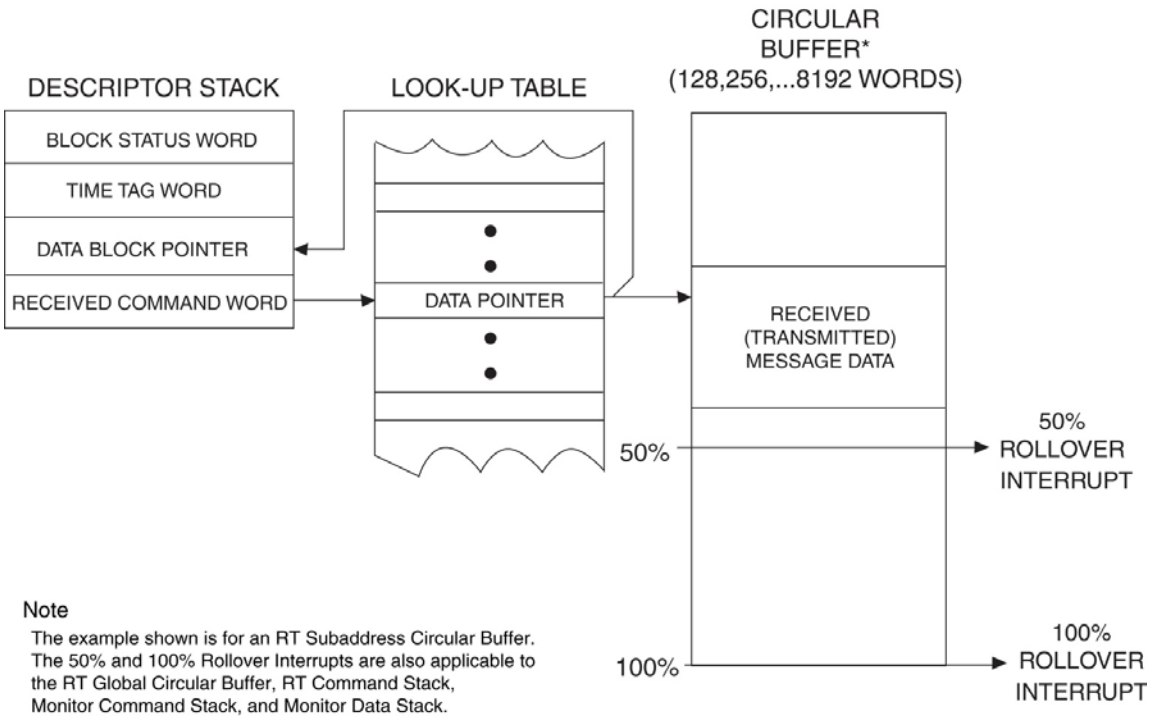


Figure 10. 50% and 100% Rollover Interrupts

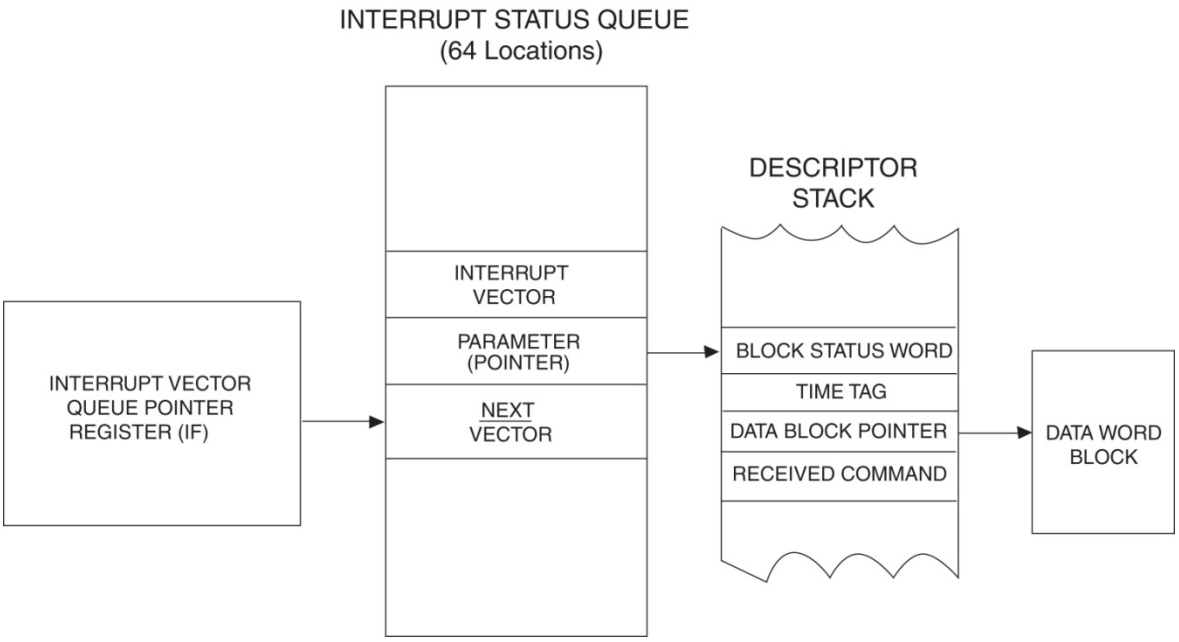


Figure 11. RT (and Monitor) Interrupt Status Queue

(shown for message interrupt event)

6.9 RT COMMAND ILLEGALIZATION

The Total-ACE provides an internal mechanism for RT Command Word illegalizing. By means of a 256-word area in shared RAM, the host processor may designate that any message be illegalized, based on the command word T/R bit, subaddress, and word count/mode code fields. The Total-ACE illegalization scheme provides the maximum in flexibility, allowing any subset of the 4096 possible combinations of broadcast/own address, T/R bit, subaddress, and word count/mode code to be illegalized.

The address map of the Total-ACE's illegalizing table is illustrated in Table 41.

Table 41. Illegalization Table Memory Map

Address	Description
300	Brdcst/Rx, SA 0. MC15-0
301	Brdcst/Rx, SA 0. MC31-16
302	Brdcst/Rx, SA 1. WC15-0
303	Brdcst/Rx, SA 1. WC31-16
□ □ □	□ □ □
33F	Brdcst/Rx, SA 31. MC31-16
340	Brdcst/Tx, SA 0. MC15-0
341	Brdcst/Tx, SA 0. MC31-16
342	Brdcst/Tx, SA 1. WC15-0
□ □ □	□ □ □
37D	Brdcst/Tx, SA 30. WC31-16
37E	Brdcst / Tx, SA 31. MC15-0
37F	Brdcst / Tx, SA 31. MC31-16
380	Own Addr / Rx, SA 0. MC15-0
381	Own Addr / Rx, SA 0. MC31-16
382	Own Addr / Rx, SA 1. WC15-0
383	Own Addr / Rx, SA 1. WC31-16
□ □ □	□ □ □
3BE	Own Addr / Rx, SA 31. MC15-0
3BF	Own Addr / Rx, SA 31. MC31-16
3C0	Own Addr / Tx, SA 0. MC15-0

Table 41. Illegalization Table Memory Map	
Address	**Description**
3C1	Own Addr / Tx, SA 0. MC31-16
3C2	Own Addr / Tx, SA 1. WC15-0
3C3	Own Addr / Tx, SA 1. WC31-16
□ □ □	□ □ □
3FC	Own Addr / Tx, SA 30. WC15-0
3FD	Own Addr / Tx, SA 30. WC31-16
3FE	Own Addr / Tx, SA 31. MC15-0
3FF	Own Addr / Tx, SA 31. MC31-16

6.10 BUSY BIT

The Total-ACE RT provides two different methods for setting the Busy status word bit: (1) globally, by means of Configuration Register #1; or (2) on a T/R-bit/subaddress basis, by means of a RAM lookup table. If the host CPU asserts the BUSY bit to logic “0” in Configuration Register #1, the Total-ACE RT will respond to **all** non-broadcast commands with the Busy bit set in its RT Status Word.

Alternatively, there is a Busy lookup table in the Total-ACE shared RAM. By means of this table, it is possible for the host processor to set the busy bit for any selectable subset of the 128 combinations of broadcast/own address, T/R bit, and subaddress.

If the busy bit is set for a transmit command, the Total-ACE RT will respond with the busy bit set in the status word, but will not transmit any data words. If the busy bit is set for a receive command, the RT will also respond with the busy status bit set. There are two programmable options regarding the reception of data words for a non-mode code receive command for which the RT is busy: (1) to transfer the received data words to shared RAM; or (2) to **not** transfer the data words to shared RAM.

6.11 RT ADDRESS

The Total-ACE offers several different options for designating the Remote Terminal address. These include the following: (1) hardwired, by means of the 5 RT ADDRESS inputs, and the RT ADDRESS PARITY input; (2) by means of the RT ADDRESS (and PARITY) inputs, but latched via hardware, on the rising edge of the RT_AD_LAT input signal; (3) input by means of the RT ADDRESS (and PARITY) inputs, but latched via host software; and (4) software programmable, by means of an internal register. In all four configurations, the RT address is readable by the host processor.

6.12 RT BUILT-IN-TEST (BIT) WORD

The bit map for the Total-ACE's internal RT Built-in-Test (BIT) Word is indicated in Table 42.

6.13 RT AUTO-BOOT OPTION

If utilized, the RT pin-programmable auto-boot option allows the Total-ACE RT to automatically initialize as an active remote terminal with the Busy status word bit set to logic "1" immediately following power turn-on. This is a useful feature for MIL-STD-1760 applications, in which the RT is required to be responding within 150 ms after power-up. This feature is available for versions of the Total-ACE with 4K words of RAM.

6.14 OTHER RT FEATURES

The Total-ACE includes options for the Terminal flag status word bit to be set either under software control and/or automatically following a failure of the loopback self-test. Other software programmable RT options include software programmable RT status and RT BIT words, automatic clearing of the Service Request bit following receipt of a Transmit vector word mode command, options regarding Data Word transfers for the Busy and Message error (illegal) Status word bits, and options for the handling of 1553A and reserved mode codes.

Table 42. RT BIT Word	
BIT	**Description**
15 (MSB)	Transmitter Timeout
14	Loop Test Failure B
13	Loop Test Failure A
12	Handshake Failure
11	Transmitter Shutdown B
10	Transmitter Shutdown A
9	Terminal Flag Inhibited
8	BIT Test Failure
7	High Word Count
6	Low Word Count
5	Incorrect Sync Received
4	Parity/Manchester error Received
3	RT-to-RT Gap/Sync Address Error
2	RT-to-RT No Response Error
1	RT-to-RT 2nd Command Word Error
0 (LSB)	Command Word Contents Error

7 MONITOR ARCHITECTURE

The Total-ACE includes three monitor modes:

1. A Word Monitor mode
2. A selective message monitor mode
3. A combined RT/message monitor mode

For new applications, it is recommended that the selective message monitor mode be used, rather than the word monitor mode. Besides providing monitor filtering based on RT address, T/R bit, and subaddress, the message monitor eliminates the need to determine the start and end of messages by software.

7.1 WORD MONITOR MODE

In the Word Monitor Terminal mode, the Total-ACE monitors both 1553 buses. After the software initialization and Monitor Start sequences, the Total-ACE stores all Command, Status, and Data Words received from both buses. For each word received from either bus, a pair of words is stored to the Total-ACE's shared RAM. The first word is the word received from the 1553 bus. The second word is the Monitor Identification (ID), or "Tag" word. The ID word contains information relating to bus channel, word validity, and inter-word time gaps. The data and ID words are stored in a circular buffer in the shared RAM address space.

7.2 WORD MONITOR MEMORY MAP

A typical word monitor memory map is illustrated in Table 43. Table 43 assumes a 64K address space for the Total-ACE's monitor. The Active Area Stack pointer provides the address where the first monitored word is stored. In the example, it is assumed that the Active Area Stack Pointer for Area A (location 0100) is initialized to 0000. The first received data word is stored in location 0000, the ID word for the first word is stored in location 0001, etc.

The current Monitor address is maintained by means of a counter register. This value may be read by the CPU by means of the Data Stack Address Register. It is important to note that when the counter reaches the Stack Pointer address of 0100 or 0104, the initial pointer value stored in this shared RAM location **will be overwritten** by the monitored data and ID Words. When the internal counter reaches an address of FFFF (or 0FFF, for an Total-ACE with 4K RAM), the counter rolls over to 0000.

7.3 WORD MONITOR TRIGGER

In the Word Monitor mode, there is a pattern recognition trigger and a pattern recognition interrupt. The 16-bit compare word for both the trigger and the interrupt is stored in the Monitor Trigger Word Register. The pattern recognition interrupt is

enabled by setting the MT Pattern Trigger bit in Interrupt Mask Register #1. The pattern recognition trigger is enabled by setting the Trigger Enable bit in Configuration Register #1 and selecting either the Start-on-trigger or the Stop-on-trigger bit in Configuration Register #1.

The Word Monitor may also be started by means of a low-to-high transition on the EXT_TRIG input signal.

7.4 SELECTIVE MESSAGE MONITOR MODE

The Total-ACE Selective Message Monitor provides monitoring of 1553 messages with filtering based on RT address, T/R bit, and subaddress with no host processor intervention. By autonomously distinguishing between 1553 command and status words, the Message Monitor determines when messages begin and end, and stores the messages into RAM, based on a programmable filter of RT address, T/R bit, and subaddress.

The selective monitor may be configured as just a monitor, or as a **combined RT/Monitor.** In the combined RT/Monitor mode, the Total-ACE functions as an RT for one RT address (including broadcast messages), and as a selective message monitor for the other 30 RT addresses. The Total-ACE Message Monitor contains two stacks, a command stack and a data stack, that are independent from the RT command stack. The pointers for these stacks are located at fixed locations in RAM.

Table 43. Typical Word Monitor Memory Map

Hex Address	Function
0000	First Received 1553 Word
0001	First Identification Word
0002	Second Received 1553 Word
0003	Second Identification 1553 Word
0004	Third Received 1553 Word
0005	Third Identification Word
□ □ □	□ □ □
0100	Stack Pointer (Fixed Location – gets overwritten)
□ □ □	□ □ □
FFFF	Received 1553 Words and Identification Word

7.5 MONITOR SELECTION FUNCTION

Following receipt of a valid command word in Selective Monitor mode, the Total-ACE will reference the selective monitor lookup table to determine if the particular command is enabled. The address for this location in the table is determined by means of an offset based on the RT Address, T/R bit, and Subaddress bit 4 of the current command word, and concatenating it to the monitor lookup table base address of 0280 (hex). The bit location within this word is determined by subaddress bits 3-0 of the current command word.

If the specified bit in the lookup table is logic "0", the command is not enabled, and the Total-ACE will ignore this command. If this bit is logic "1", the command is enabled and the Total-ACE will create an entry in the monitor command descriptor stack (based on the monitor command stack pointer), and store the data and status words associated with the command into sequential locations in the monitor data stack. In addition, for an RT-to-RT transfer in which the receive command is selected, the second command word (the transmit command) is stored in the monitor data stack.

The address definition for the Selective Monitor Lookup Table is illustrated in Table 44.

Table 44. RT BIT Word

BIT	Description
15 (MSB)	Logic “0”
14	Logic “0”
13	Logic “0”
12	Logic “0”
11	Logic “0”
10	Logic “0”
9	Logic “1”
8	Logic “0”
7	Logic “1”
6	RTAD_4
5	RTAD_3
4	RTAD_2
3	RTAD_1
2	RTAD_0
1	TRANSMIT/$\overline{\text{RECEIVE}}$
0 (LSB)	Subaddress 4

7.6 SELECTIVE MESSAGE MONITOR MEMORY ORGANIZATION

A typical memory map for the Total-ACE in the Selective Message Monitor mode, assuming a 4K RAM space, is illustrated in Table 45. This mode of operation defines several fixed locations in the RAM. These locations are allocated in a way in which none of them overlap with the fixed RT locations. This allows for the combined RT/Selective Message Monitor mode.

The fixed memory map consists of two Monitor Command Stack Pointers (locations 102 and 106 hex), two Monitor Data Stack Pointers (locations 103 and 107 hex), and a Selective Message Monitor Lookup Table (locations 0280 through 02FF hex). For this example, the Monitor Command Stack size is assumed to be 1K words, and the Monitor Data Stack size is assumed to be 2K words.

Figure 12 illustrates the Selective Message Monitor operation. Upon receipt of a valid Command Word, the Total-ACE will reference the Selective Monitor Lookup Table to determine if the current command is enabled. If the current command is disabled, the Total-ACE monitor will ignore (and not store) the current message. If the command is enabled, the monitor will create an entry in the Monitor Command Stack at the address location referenced by the Monitor Command Stack Pointer, and an entry in the monitor data stack starting at the location referenced by the Monitor Data Stack Pointer.

The format of the information in the data stack depends on the format of the message that was processed. For example, for a BC-to-RT transfer (receive command), the monitor will store the command word in the monitor command descriptor stack, with the data words and the receiving RT's status word stored in the monitor data stack.

The size of the monitor command stack is programmable, with choices of 256, 1K, 4K, or 16K words. The monitor data stack size is programmable with choices of 512, 1K, 2K, 4K, 8K, 16K, 32K or 64K words.

7.7 MONITOR INTERRUPTS

Selective monitor interrupts may be issued for End-of-message and for conditions relating to the monitor command stack pointer and monitor data stack pointer. The latter, as shown in Figure 10, include Command Stack 50% Rollover, Command Stack 100% Rollover, Data Stack 50% Rollover, and Data Stack 100% Rollover.

The 50% rollover interrupts may be used to inform the host processor when the command stack or data stack is half full. At that time, the host may proceed to read the received messages in the upper half of the respective stack, while the Total-ACE

monitor writes messages to the lower half of the stack. Later, when the monitor issues a 100% stack rollover interrupt, the host can proceed to read the received data from the lower half of the stack, while the Total-ACE monitor continues to write received data words to the upper half of the stack.

Table 45. Typical Selective Message Monitor Memory Map (shown for 4K RAM for "Monitor only" mode)

Address (Hex)	Function
0000-0101	Not Used
0102	Monitor Command Stack Pointer A (fixed location)
0103	Monitor Data Stack Pointer A (fixed location)
0104-0105	Not Used
0106	Monitor Command Stack Pointer B (fixed location)
0107	Monitor Data Stack Pointer B (fixed location)
0108-027F	Not Used
0280-02FF	Selective Monitor Lookup Table (fixed location)
0300-03FF	Not Used
0400-07FF	Monitor Command Stack A
0800-0FFF	Monitor Data Stack A

7.8 INTERRUPT STATUS QUEUE

Like the Total-ACE RT, the Selective Monitor mode includes the capability for generating an interrupt status queue. As illustrated in Figure 11, this provides a chronological history of interrupt generating events. Besides the two Interrupt Mask Registers, the Interrupt Status Queue provides additional filtering capability, such that only valid messages and/or only invalid messages may result in entries to the Interrupt Status Queue. The interrupt status queue is 64 words deep, providing the capability to store entries for up to 32 monitored messages.

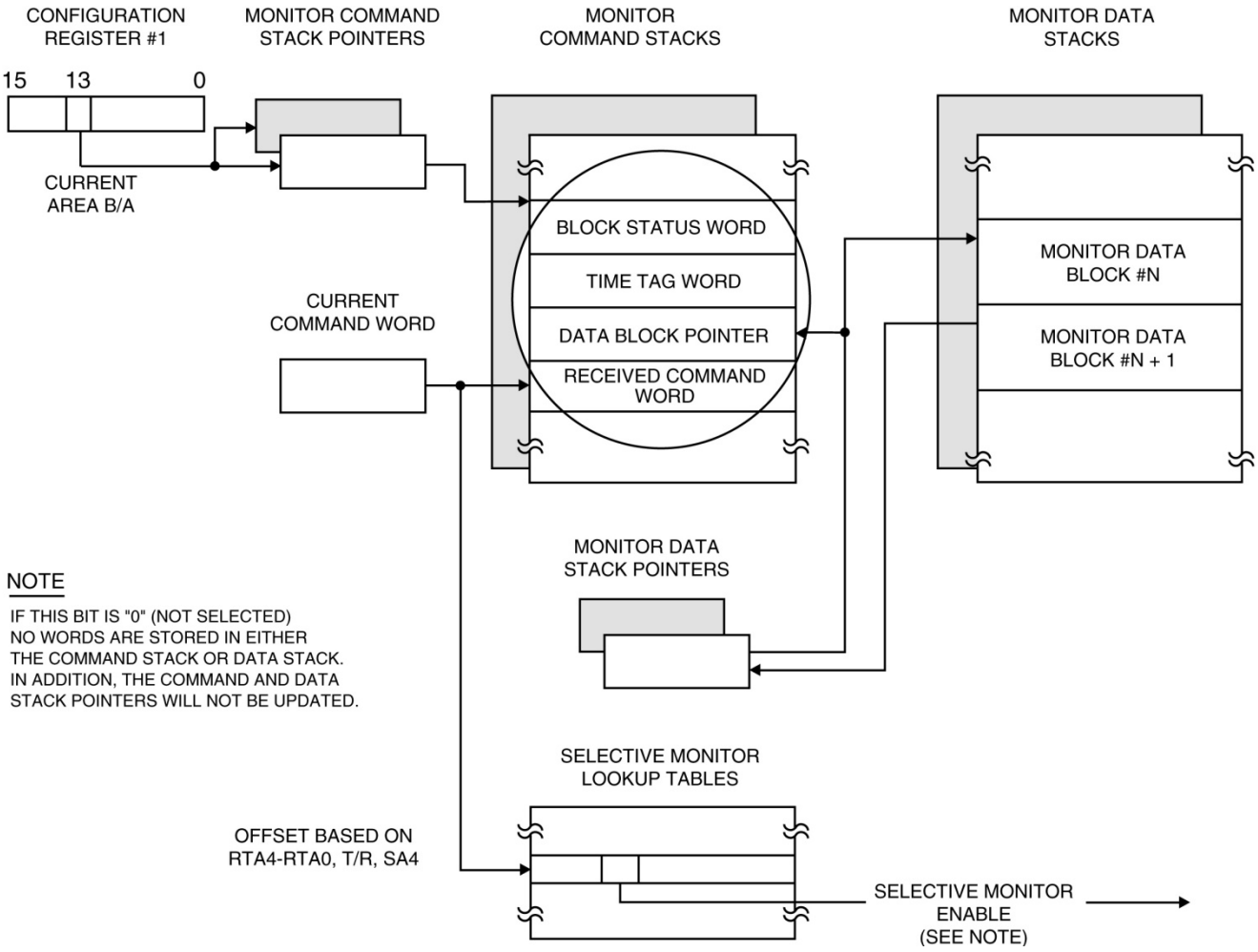


Figure 12. Selective Message Monitor Memory Management

8 MISCELLANEOUS

8.1 CLOCK INPUT

The Total-ACE decoder is capable of operating from a 10, 12, 16, or 20 MHz clock input. Depending on the configuration of the specific model Total-ACE terminal, the selection of the clock input frequency may be chosen by one of either two methods. For all versions, the clock frequency may be specified by means of the host processor writing to Configuration Register #6. With the second method, which is applicable only for versions incorporating 4K words of internal RAM, the clock frequency may be specified by means of the input signals that are otherwise used as the A15 and A14 address lines.

8.2 ENCODER/DECODERS

For the selected clock frequency, there is internal logic to derive the necessary clocks for the Manchester encoder and decoders. For all clock frequencies, the decoders sample the receiver outputs on **both** edges of the input clock. By in effect doubling the decoders' sampling frequency, this serves to widen the tolerance to zero-crossing distortion, and reduce the bit error rate.

For interfacing to fiber optic transceivers (e.g., for MIL-STD-1773 applications), the decoders are capable of operating with singleended, rather than double-ended, input signals.

8.3 TIME TAG

The Total-ACE includes an internal read/writable Time Tag Register. This register is a CPU read/writable 16-bit counter with a programmable resolution of either 2, 4, 8, 16, 32, or 64 µs per LSB. Another option allows software controlled incrementing of the Time Tag Register. This supports self-test for the Time Tag Register. For each message processed, the value of the TimeTag Register is loaded into the second location of the respective descriptor stack entry ("TIME TAG WORD") for both the BC and RT modes.

The functionality involving the Time Tag Register that's compatible with ACE/Mini-ACE (Plus) includes: the capability to issue an interrupt request and set a bit in the Interrupt Status Register when the Time Tag Register rolls over FFFF to 0000; for RT mode, the capability to automatically clear the Time Tag Register following reception of a Synchronize (without data) mode command, or to load the Time Tag Register following a Synchronize (with data) mode command.

Additional time tag features supported by the Total-ACE include the capability for the BC to transmit the contents of the Time Tag Register as the data word for a Synchronize (with data) mode command; the capability for the RT to "filter" the data word for the Synchronize with data mode command, by only loading the Time Tag

Register if the LSB of the received data word is "0"; an instruction enabling the BC Message Sequence Control engine to load the Time Tag Register with a specified value; and an instruction enabling the BC Message Sequence Control engine to write the value of the Time Tag Register to the General Purpose Queue.

8.4 INTERRUPTS

The Total-ACE series terminals provide many programmable options for interrupt generation and handling. The interrupt output pin (INT) has three software programmable modes of operation: a pulse, a level output cleared under software control, or a level output automatically cleared following a read of the Interrupt Status Register (#1 or #2).

Individual interrupts are enabled by the two Interrupt Mask Registers. The host processor may determine the cause of the interrupt by reading the two Interrupt Status Registers, which provide the current state of interrupt events and conditions. The Interrupt Status Registers may be updated in two ways. In one interrupt handling mode, a particular bit in Interrupt Status Register #1 or #2 will be updated only if the event occurs and the corresponding bit in Interrupt Mask Register #1 or #2 is enabled. In the enhanced interrupt handling mode, a particular bit in one of the Interrupt Status Registers will be updated if the event/condition occurs regardless of the value of the corresponding Interrupt Mask Register bit. In either case, the respective Interrupt Mask Register (#1 or #2) bit is used to enable an interrupt for a particular event/condition.

The Total-ACE supports all the interrupt events from ACE/Mini-ACE (Plus), including RAM Parity Error, Transmitter Timeout, BC/ RT Command Stack Rollover, MT Command Stack and Data Stack Rollover, Handshake Error, BC Retry, RT Address Parity Error, Time Tag Rollover, RT Circular Buffer Rollover, BC Message, RT Subaddress, BC End-of-Frame, Format Error, BC Status Set, RT Mode Code, MT Trigger, and End-of-Message.

For the Total-ACE's Enhanced BC mode, there are four userdefined interrupt bits. The BC Message Sequence Control Engine includes an instruction enabling it to issue these interrupts at any time.

For RT and Monitor modes, the Total-ACE architecture includes an Interrupt Status Queue. This provides a mechanism for logging messages that result in interrupt requests. Entries to the Interrupt Status Queue may be filtered such that only valid and/or invalid messages will result in entries on the queue.

The Total-ACE incorporates additional interrupt conditions beyond the ACE/Mini-ACE (Plus), based on the addition of Interrupt Mask Register #2 and Interrupt Status Register #2. This is accomplished by chaining the two Interrupt Status Registers

using the INTERRUPT CHAIN BIT (bit 0) in Interrupt Status Register #2 to indicate that an interrupt has occurred in Interrupt Status Register #1. Additional interrupts include "Self-Test Completed", masking bits for the Enhanced BC Control Interrupts, 0% Rollover interrupts for RT Command Stack, RT Circular Buffers, MT Command Stack, and MT Data Stack; BC Op Code Parity Error, (RT) Illegal Command, (BC) General Purpose Queue or (RT/MT) Interrupt Status Queue Rollover, Call Stack Pointer Register Error, BC Trap Op Code, and the four User-Defined interrupts for the Enhanced BC mode.

8.5 BUILT-IN TEST

A salient feature of the Total-ACE is its highly autonomous selftest capability. This includes both protocol and RAM self-tests. Either or both of these self-tests may be initiated by command(s) from the host processor.

The protocol test consists of a comprehensive toggle test of the terminal's logic. The test includes testing of all registers, Manchester decoders, protocol logic, and memory management logs. This test is completed in approximately 32,000 clock cycles. That is, about 1.6 ms with a 20 MHz clock, 2.0 ms at 16 MHz, 2.7 ms at 12 MHz, and 3.2 ms at 10 MHz.

There is also a separate built-in test (BIT) for the Total-ACE's 4K x 16 or 64K x 16 shared RAM. This test consists of writing and then reading/verifying the two walking patterns "data = address" and "data = address inverted". For a Total-ACE with 4K words of RAM, this is about 2.0 ms with a 20 MHz clock, 2.6 ms at 16 MHz, 3.4 ms at 12 MHz, or 4.1 ms at 10 MHz. For a Total-ACE with 64K words of RAM, this is about 32.8 ms with a 20 MHz clock, 40.1 ms at 16 MHz, 54.6 ms at 12 MHz, or 65.6 ms at 10 MHz.

The Total-ACE built-in protocol test is performed automatically at power-up. In addition, the protocol or RAM self-tests may be initiated by a command from the host processor, via the START/RESET REGISTER. For RT mode, this may include the host processor invoking self-test following receipt of an Initiate self-test mode command. The results of the self-test are host accessible by means of the BIT status register. For RT mode, the result of the self-test may be communicated to the bus controller via bit 8 of the RT BIT word ("0" = pass, "1" = fail).

Assuming that the protocol self-test passes, all of the register and shared RAM locations will be restored to their state prior to the self-test, with the exception of the 60 RAM address locations 0342-037D and the TIME TAG REGISTER. Note that for RT mode, these locations map to the illegalization lookup table for "broadcast transmit subaddresses 1 through 30" (non-mode code subaddresses). Since MIL-STD-1553 does not define these as valid command words, this section of the illegalization lookup table is normally not used during RT operation. The TIME TAG REGISTER will continue to increment during the self-test.

If there is a failure of the protocol self-test, it is possible to access information about the first failed vector. This may be done by means of the Total-ACE's upper registers (register addresses 32 through 63). Through these registers, it is possible to determine the self-test ROM address of the first failed vector, the expected response data pattern (from the ROM), the register or memory address, and the actual (incorrect) data value read from register or memory. The on-chip self-test ROM is 4K X 24.

Note that the RAM self-test is destructive. That is, following the RAM self-test, regardless of whether the test passes or fails, the shared RAM is **not** restored to its state prior to this test. Following a failed RAM self-test, the host may read the internal RAM to determine which location(s) failed the walking pattern test.

8.6 RAM PARITY

The BC/RT/MT version of the Total-ACE is available with options of 4K or 64K words of internal RAM. For the 64K option, the RAM is 17 bits wide. The 64K X 17 internal RAM allows for parity generation for RAM write accesses, and parity checking for RAM read accesses. This includes host RAM accesses, as well as accesses by the Total-ACE's internal logic. When the Total-ACE detects a RAM parity error, it reports it to the host processor by means of an interrupt and a register bit. Also, for the RT and Selective Message Monitor modes, the RAM address where a parity error was detected will be stored on the Interrupt Status Queue (if enabled).

8.7 RELOCATABLE MEMORY MANAGEMENT LOCATIONS

In the Total-ACE's default configuration, there is a *fixed* area of shared RAM addresses, 0000h-03FF, that is allocated for storage of the BC's or RT's pointers, counters, tables, and other "nonmessage" data structures. As a means of reducing the overall memory address space for using multiple Total-ACE's in a given system (e.g., for use with the DMA interface configuration), the Total-ACE allows this area of RAM to be relocated by means of 6 configuration register bits. To provide backwards compatibility to ACE and Mini-ACE, the default for this RAM area is 0000h-03FFh.

8.8 HOST PROCESSOR INTERFACE

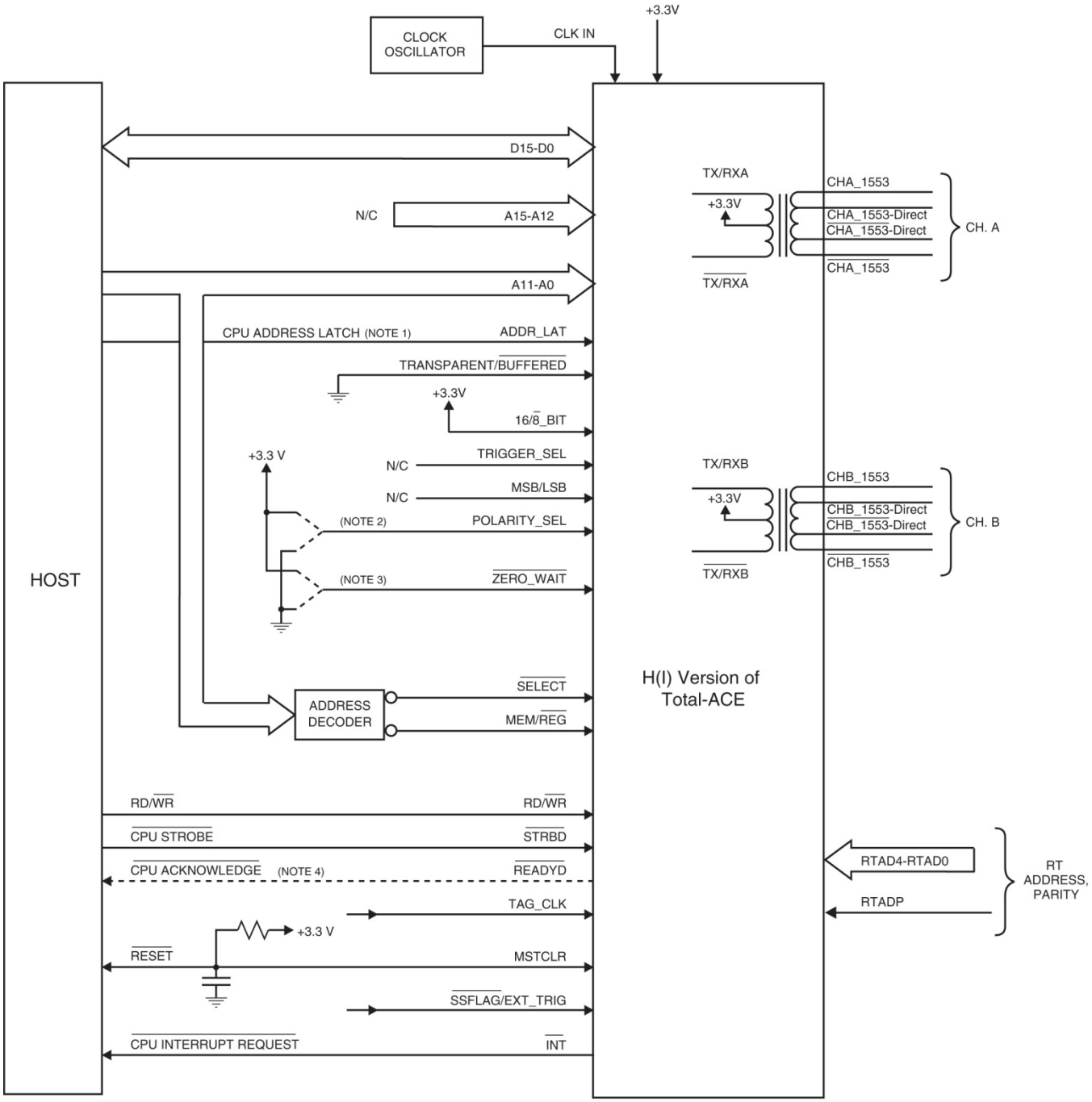
The Total-ACE supports a wide variety of processor interface configurations. These include shared RAM and DMA configurations, straightforward interfacing for 16-bit and 8-bit buses, support for both non-multiplexed and multiplexed address/data buses, non-zero wait mode for interfacing to a processor address/data buses, and zero wait mode for interfacing (for example) to microcontroller I/O ports. In addition, with respect to the ACE/Mini-ACE, the Total-ACE provides two major improvements: (1) reduced maximum host access time for shared RAM mode; and (2) increased maximum DMA grant time for the transparent/DMA mode.

The Total-ACE's maximum host holdoff time (time prior to the assertion of the READYD handshake signal) has been significantly reduced. For ACE/Mini-ACE, this maximum holdoff time is 17 internal word transfer cycles, resulting in an overall holdoff time of approximately 4.6 µs, using a 16 MHz clock. By comparison, using the Total-ACE's ENHANCED CPU ACCESS feature, this worst-case holdoff time is reduced significantly, to a single internal transfer cycle. For example, when operating the Total-ACE in its 16-bit buffered, non-zero wait configuration with a 16 MHz clock input, this results in a maximum overall host transfer cycle time of 632 ns for a read cycle, or 570 ns for a write cycle.

In addition, when using the ACE or Mini-ACE in the transparent/DMA configuration, the maximum request-to-grant time, which occurs prior to an RT start-of-message sequence, is 4.0 µs with a 16 MHz clock, or 3.5 µs with a 12 MHz clock. For the Total-ACE functioning as a MIL-STD-1553B RT, this time has been increased to 8.5 µs at 10 MHz, 9 µs at 12 MHz, 10 µs at 16 MHz, and 10.5 µs at 20MHz. This provides greater flexibility, particularly for systems in which a host has to arbitrate among multiple DMA requestors.

By far, the most commonly used processor interface configuration is the 16-bit buffered, non-zero wait mode. This configuration may be used to interface between 16-bit or 32-bit microprocessors and an Total-ACE. In this mode, only the Total-ACE's internal 4K or 64K words of internal RAM are used for storing 1553 message data and associated "housekeeping" functions. That is, in this configuration, the Total-ACE will never attempt to access memory on the host bus.

Figure 13 illustrates a generic connection diagram between a 16-bit (or 32-bit) microprocessor and an Total-ACE for the 16-bit buffered configuration, while Figure 14 and Figure 15, and associated tables illustrate the processor read and write timing respectively.



NOTES:

1. CPU ADDRESS LATCH SIGNAL PROVIDED BY PROCESSORS WITH MULTIPLEXED ADDRESS/DATA BUSES. FOR PROCESSORS WITH NON-MULTIPLEXED ADDRESS AND DATA BUSES, ADDR_LAT SHOULD BE CONNECTED TO +3.3V.
2. IF POLARITY_SEL = "1", RD/$\overline{WR}$ IS HIGH TO READ, LOW TO WRITE. IF POLARITY_SEL = "0", RD/$\overline{WR}$ IS LOW TO READ, HIGH TO WRITE.
3. $\overline{ZERO\_WAIT}$ SHOULD BE STRAPPED TO LOGIC "1" FOR NON-ZERO WAIT INTERFACE AND TO LOGIC "0" FOR ZERO WAIT INTERFACE.
4. CPU ACKNOWLEDGE PROCESSOR INPUT ONLY FOR NON-ZERO WAIT TYPE OF INTERFACE.

Figure 13. Host Processor Interface – 16-Bit Buffered Configuration

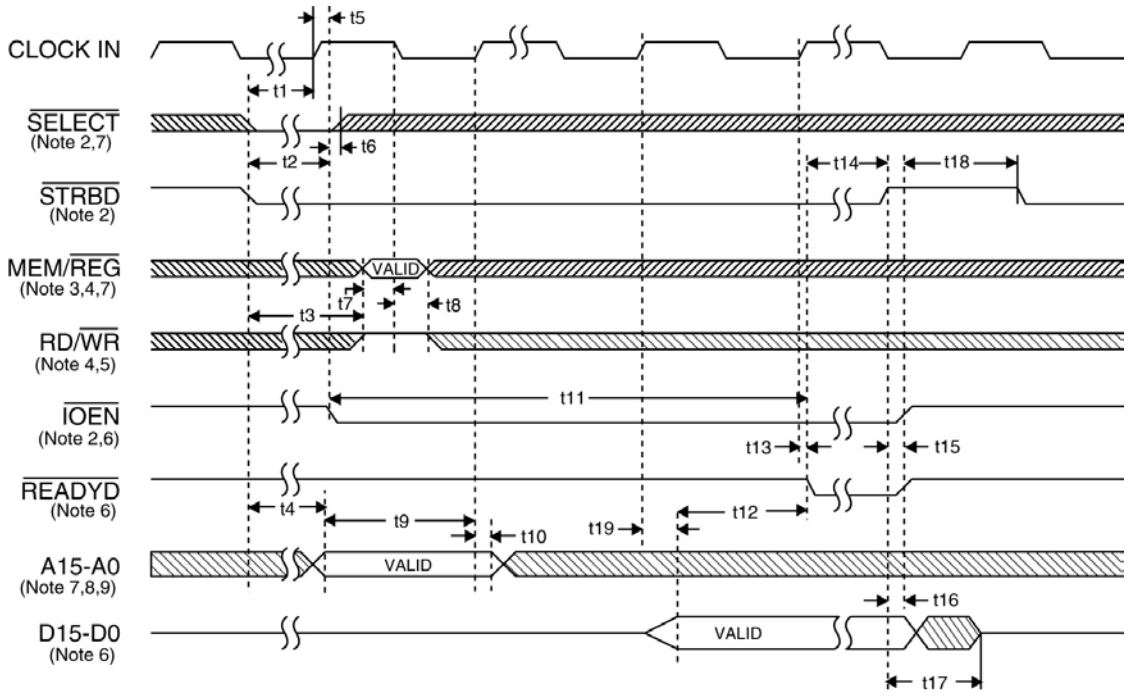


Figure 14. CPU Reading RAM/Register (16-BIT Buffered, Nonzero Wait)

Notes for Figure 14:

1. For the 16-bit buffered nonzero wait configuration, TRANSPARENT/$\overline{\text{BUFFERED}}$ must be connected to logic "0". $\overline{\text{ZERO\_WAIT}}$ and $\overline{\text{DTREQ}}$ / 16/8 must be connected to logic "1". The inputs TRIGGER_SEL and MSB/LSB may be connected to either Vcc or ground.
2. $\overline{\text{SELECT}}$ and $\overline{\text{STRBD}}$ may be tied together. $\overline{\text{IOEN}}$ goes low on the first rising CLK edge when $\overline{\text{SELECT}}$ • $\overline{\text{STRBD}}$ is sampled low (satisfying t1) and the Total-ACE's protocol/memory management logic is not accessing the internal RAM. When this occurs, $\overline{\text{IOEN}}$ goes low, starting the transfer cycle. After $\overline{\text{IOEN}}$ goes low, $\overline{\text{SELECT}}$ may be released high.
3. MEM/$\overline{\text{REG}}$ must be presented high for memory access, low for register access.
4. MEM/$\overline{\text{REG}}$ and RD/$\overline{\text{WR}}$ are buffered transparently until the first falling edge of CLK after $\overline{\text{IOEN}}$ goes low. After this CLK edge, MEM/$\overline{\text{REG}}$ and RD/$\overline{\text{WR}}$ become latched internally.
5. The logic sense for RD/$\overline{\text{WR}}$ in the diagram assumes that POLARITY_SEL is connected to logic "1". If POLARITY_SEL is connected to logic "0", RD/$\overline{\text{WR}}$ must be asserted low to read.
6. The timing for $\overline{\text{IOEN}}$, $\overline{\text{READYD}}$ and D15-D0 assumes a 50 pf load. For loading above 50 pf, the validity of $\overline{\text{IOEN}}$, $\overline{\text{READYD}}$ and D15-D0 is delayed by an additional 0.14 ns/pf typ, 0.28 ns/pf max.
7. The timing for A15-A0, MEM/$\overline{\text{REG}}$ and $\overline{\text{SELECT}}$ assumes that ADDR-LAT is connected to logic "1". Refer to Address Latch timing for additional details.
8. The address bus A15-A0 is internally buffered transparently until the first rising edge of CLK after $\overline{\text{IOEN}}$ goes low. After this CLK edge, A14-A0 become latched internally.
9. Setup time given for use in worst case timing calcutlation. None of the Total-ACE's input signals are required to be synchronized to the system clock. When $\overline{\text{SELECT}}$ and $\overline{\text{STRBD}}$ do not meet the setup time of t1, but occur during the setup window of an internal flip-flop, and additional clock cycle will be inserted between the falling clock edge that latches MEM/$\overline{\text{REG}}$ and RD/$\overline{\text{WR}}$ and the rising

clock edge that latches the Address (A15-A0). When this occurs, the delay from $\overline{\text{IOEN}}$ falling to $\overline{\text{READYD}}$ falling (t11) increases by one clock cycle and the address hold time (t10) must be increased by one clock cycle.

Table for Figure 14 CPU Reading RAM or Registers (shown for 16-BIT, Buffered, Nonzero Wait Mode)

REF	Description	Notes	3.3V Logic			Units
			MIN	TYP	MAX	
t1	$\overline{\text{SELECT}}$ and $\overline{\text{STRBD}}$ low setup time prior to clock rising edge	2, 9	15			ns
t2	$\overline{\text{SELECT}}$ and $\overline{\text{STRBD}}$ low to $\overline{\text{IOEN}}$ low (uncontended access @ 20 MHz)	2, 6			105	ns
	(contended access, with ENHANCED CPU ACCESS = “0” @ 20 MHz)	2, 6			3.6	µs
	(contended access, with ENHANCED CPU ACCESS = “1” @ 20 MHz)	2, 6			520	ns
	(uncontended access @ 16 MHz	2, 6			117	ns
	(contended access, with ENHANCED CPU ACCESS = “0” @ 16 MHz)	2, 6			4.6	µs
	(contended access, with ENHANCED CPU ACCESS = “1” @ 16 MHz)	2, 6			635	ns
	(uncontended access @ 12 MHz	2, 6			138	ns
	(contended access, with ENHANCED CPU ACCESS = “0” @ 12 MHz)	2, 6			6.0	µs
	(contended access, with ENHANCED CPU ACCESS = “1” @ 12 MHz)	2, 6			820	ns
	(uncontended access @ 10 MHz	2, 6			155	ns
	(contended access, with ENHANCED CPU ACCESS = “0” @ 10 MHz)	2, 6			7.2	µs
	(contended access, with ENHANCED CPU ACCESS = “1” @ 10 MHz)	2,6			970	ns
t3	Time for MEM/$\overline{\text{REG}}$ and RD/$\overline{\text{WR}}$ to become valid following $\overline{\text{SELECT}}$ and $\overline{\text{STRBD}}$ low (@ 20 MHz)	3, 4, 5, 7			10	ns
	@ 16 MHz	3, 4, 5, 7			16	ns
	@ 12 MHz	3, 4, 5, 7			27	ns
	@ 10 MHz	3, 4, 5, 7			35	ns
t4	Time for Address to become valid following $\overline{\text{SELECT}}$ and $\overline{\text{STRBD}}$ low (@ 20 MHz)				12	ns
	@ 16 MHz				25	ns
	@ 12 MHz				45	ns
	@ 10 MHz				62	ns
t5	CLOCK IN rising edge delay to $\overline{\text{IOEN}}$ falling edge	6			40	ns

Table for Figure 14 CPU Reading RAM or Registers (shown for 16-BIT, Buffered, Nonzero Wait Mode)						
REF	**Description**	**Notes**	**3.3V Logic**			**Units**
t6	$\overline{\text{SELECT}}$ hold time following $\overline{\text{IOEN}}$ falling	2	0			ns
t7	MEM/$\overline{\text{REG}}$, RD/$\overline{\text{WR}}$ setup time prior to CLOCK IN falling edge	3, 4, 5, 7	15			ns
t8	MEM/$\overline{\text{REG}}$, RD/$\overline{\text{WR}}$ hold time prior to CLOCK IN falling edge	3, 4, 5, 7	30			ns
t9	Address valid setup time prior to CLOCK IN rising edge	7, 8	35			ns
t10	Address hold time following CLOCK IN rising edge	7, 8, 9	30			ns
t11	$\overline{\text{IOEN}}$ falling delay to $\overline{\text{READYD}}$ falling (@ 20 MHz)	6, 9	135	150	165	ns
	@ 16 MHz	6, 9	170	187.5	205	ns
	@ 12 MHz	6, 9	235	250	265	ns
	@ 10 MHz	6, 9	285	300	315	ns
t12	Output Data valid prior to $\overline{\text{READYD}}$ falling (@ 20 MHz)	6	11			ns
	@ 16 MHz	6	23			ns
	@ 12 MHz	6	44			ns
	@ 10 MHz	6	61			ns
t13	CLOCK IN rising edge delay to $\overline{\text{READYD}}$ falling	6			40	ns
t14	$\overline{\text{READYD}}$ falling to $\overline{\text{STRBD}}$ rising release time				∞	ns
t15	$\overline{\text{STRBD}}$ rising edge delay to $\overline{\text{IOEN}}$ rising edge and $\overline{\text{READYD}}$ rising edge	6			40	ns
t16	Output Data hold time following $\overline{\text{STRBD}}$ rising edge		0			ns
t17	$\overline{\text{STRBD}}$ rising delay to output data tri-state				40	ns
t18	$\overline{\text{STRBD}}$ high hold time from $\overline{\text{READYD}}$ rising		0			ns
t19	CLOCK IN rising edge delay to output data valid				40	ns

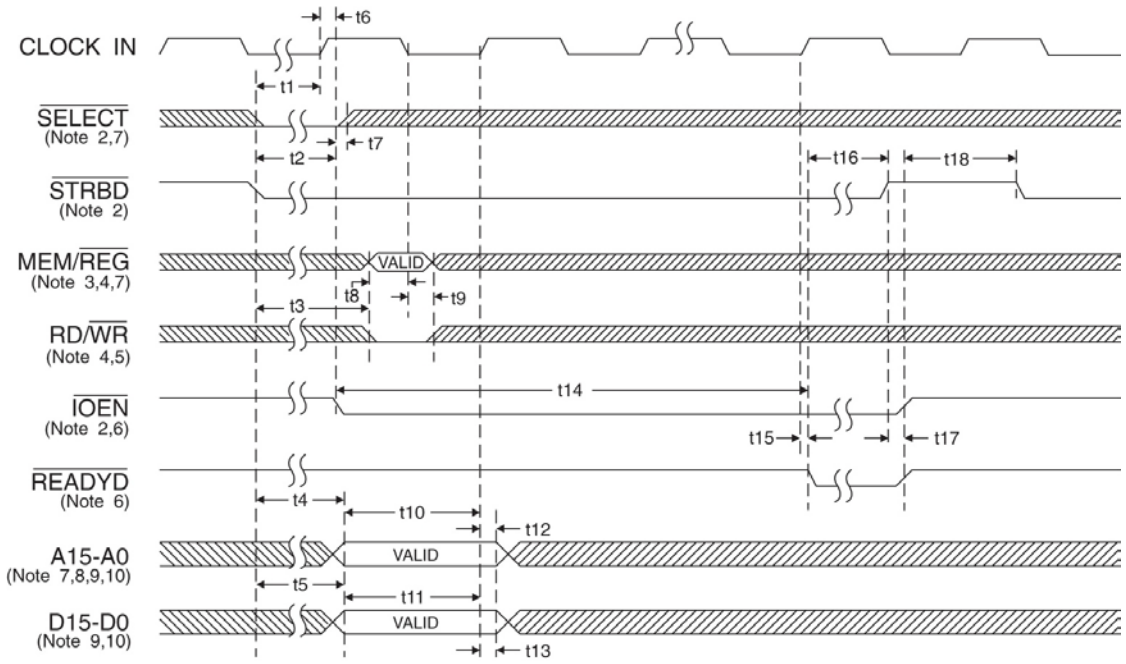


Figure 15. CPU Writing RAM/Register (16-BIT Buffered, Nonzero Wait)

Notes for Figure 15:

1. For the 16-bit buffered nonzero wait configuration TRANSPARENT/$\overline{\text{BUFFERED}}$ must be connected to logic "0", $\overline{\text{ZERO\_WAIT}}$ and $\overline{\text{DTREG}}$ / 16/$\overline{8}$ must be connected to logic "1". The inputs TRIGGER_SEL and MSB/LSB may be connected to either Vcc or ground.
2. $\overline{\text{SELECT}}$ and $\overline{\text{STRBD}}$ may be tied together. IOEN goes low on the first rising CLK edge when $\overline{\text{SELECT}}$ • $\overline{\text{STRBD}}$ is sampled low (satisfying t1) and the Total-ACE's protocol/memory management logic is not accessing the internal RAM. When this occurs, $\overline{\text{IOEN}}$ goes low, starting the transfer cycle. After $\overline{\text{IOEN}}$ goes low, $\overline{\text{SELECT}}$ may be released high.
3. MEM/$\overline{\text{REG}}$ must be presented high for memory access, low for register access.
4. MEM/$\overline{\text{REG}}$ and RD/$\overline{\text{WR}}$ are buffered transparently until the first falling edge of CLK after IOEN goes low. After this CLK edge, MEM/$\overline{\text{REG}}$ and RD/$\overline{\text{WR}}$ become latched internally.
5. The logic sense for RD/WR in the diagram assumes that POLARITY_SEL is connected to logic "1". If POLARITY_SEL is connected to logic "0", RD/$\overline{\text{WR}}$ must be asserted high to write.
6. The timing for the $\overline{\text{IOEN}}$ and $\overline{\text{READYD}}$ outputs assume a 50 pf load. For loading above 50 pf, the validity of $\overline{\text{IOEN}}$ and $\overline{\text{READYD}}$ is delayed by an additional 0.14 ns/pf typ, 0.28 ns/pf max.
7. The timing for A15-A0, MEM/$\overline{\text{REG}}$, and $\overline{\text{SELECT}}$ assumes that ADDR-LAT is connected to logic "1". Refer to Address Latch timing for additional details.
8. The address bus A15-A0 and data bus D15-D0 are internally buffered transparently until the first rising edge of CLK after $\overline{\text{IOEN}}$ goes low. After this CLK edge, A15-A0 and D15-D0 become latched internally.
9. Setup time given for use in worst case timing calculations. None of the Total-ACE's input signals are required to be synchronized to the system clock. When $\overline{\text{SELECT}}$ and $\overline{\text{STRBD}}$ do not meet the setup time of t1, but occur during the setup time of an internal flip-flop, an additional clock cycle may be inserted between the falling clock edge that latches MEM/$\overline{\text{REG}}$ and RD/$\overline{\text{WR}}$ and the rising clock edge that latches the address (A15-A0) and data (D15-D0). When this occurs, the delay from $\overline{\text{IOEN}}$ falling to $\overline{\text{READYD}}$ falling (t14) increases by one clock cycle and the address and data hold time (t12 and t13) must be increased by one clock.

Table for Figure 15 CPU Writing RAM or Registers (shown for 16-BIT, Buffered, Nonzero Wait Mode)						
REF	Description	Notes	3.3V Logic			Units
			MIN	TYP	MAX	
t1	$\overline{\text{SELECT}}$ and $\overline{\text{STRBD}}$ low setup time prior to clock rising edge	2, 10	15			ns
t2	$\overline{\text{SELECT}}$ and $\overline{\text{STRBD}}$ low to $\overline{\text{IOEN}}$ low (uncontended access @ 20 MHz)	2, 6			105	ns
	(contended access, with ENHANCED CPU ACCESS = "0" @ 20 MHz)	2, 6			3.6	µs
	(contended access, with ENHANCED CPU ACCESS = "1" @ 20 MHz)	2, 6			470	ns
	(uncontended access @ 16 MHz	2, 6			117	ns
	(contended access, with ENHANCED CPU ACCESS = "0" @ 16 MHz)	2, 6			4.6	µs
	(contended access, with ENHANCED CPU ACCESS = "1" @ 16 MHz)	2, 6			570	ns
	(uncontended access @ 12 MHz	2, 6			138	ns
	(contended access, with ENHANCED CPU ACCESS = "0" @ 12 MHz)	2, 6			6.0	µs
	(contended access, with ENHANCED CPU ACCESS = "1" @ 12 MHz)	2, 6			737	ns
	(uncontended access @ 10 MHz	2, 6			155	ns
	(contended access, with ENHANCED CPU ACCESS = "0" @ 10 MHz)	2, 6			7.2	µs
	(contended access, with ENHANCED CPU ACCESS = "1" @ 10 MHz)	2,6			870	ns
t3	Time for MEM/$\overline{\text{REG}}$ and RD/$\overline{\text{WR}}$ to become valid following $\overline{\text{SELECT}}$ and $\overline{\text{STRBD}}$ low (@ 20 MHz)	3, 4, 5, 7			10	ns
	@ 16 MHz	3, 4, 5, 7			16	ns
	@ 12 MHz	3, 4, 5, 7			27	ns
	@ 10 MHz	3, 4, 5, 7			35	ns
t4	Time for Address to become valid following $\overline{\text{SELECT}}$ and $\overline{\text{STRBD}}$ low (@ 20 MHz)				12	ns
	@ 16 MHz				25	ns
	@ 12 MHz				45	ns
	@ 10 MHz				62	ns
t5	Time for data to become valid following $\overline{\text{SELECT}}$ and $\overline{\text{STRBD}}$ low				32	ns

Table for Figure 15 CPU Writing RAM or Registers (shown for 16-BIT, Buffered, Nonzero Wait Mode)						
REF	**Description**	**Notes**	**3.3V Logic**			**Units**
	(@ 20 MHz)					
	@ 16 MHz				45	ns
	@ 12 MHz				65	ns
	@ 10 MHz				82	ns
t6	CLOCK IN rising edge delay to $\overline{\text{IOEN}}$ falling edge	6			40	ns
t7	$\overline{\text{SELECT}}$ hold time following $\overline{\text{IOEN}}$ falling	2	0			ns
t8	MEM/$\overline{\text{REG}}$, RD/$\overline{\text{WR}}$ setup time prior to CLOCK IN falling edge	3, 4, 5, 7	15			ns
t9	MEM/$\overline{\text{REG}}$, RD/$\overline{\text{WR}}$ setup time following to CLOCK IN falling edge	3, 4, 5, 7	35			ns
t10	Address valid setup time prior to CLOCK IN rising edge	7, 8	35			ns
t11	Data valid setup time prior to CLOCK IN rising edge		15			ns
t12	Address valid hold time following CLOCK IN rising edge	7, 8, 9	30			ns
t13	Data valid hold time following CLOCK IN rising edge	9	15			ns
t14	$\overline{\text{IOEN}}$ falling delay $\overline{\text{READYD}}$ falling @ 20 MHz	6, 9	85	100	115	ns
	@ 16 MHz	6, 9	110	125	140	ns
	@ 12 MHz	6, 9	152	167	182	ns
	@ 10 MHz	6, 9	185	200	215	ns
t15	CLOCK IN rising edge delay to $\overline{\text{READYD}}$ falling	6			40	ns
t16	$\overline{\text{READYD}}$ falling to $\overline{\text{STRBD}}$ rising release time				∞	ns
t17	$\overline{\text{STRBD}}$ rising edge delay to $\overline{\text{IOEN}}$ rising edge and $\overline{\text{READYD}}$ rising edge	6			40	ns
t18	$\overline{\text{STRBD}}$ high hold time from $\overline{\text{READYD}}$ rising		10			ns

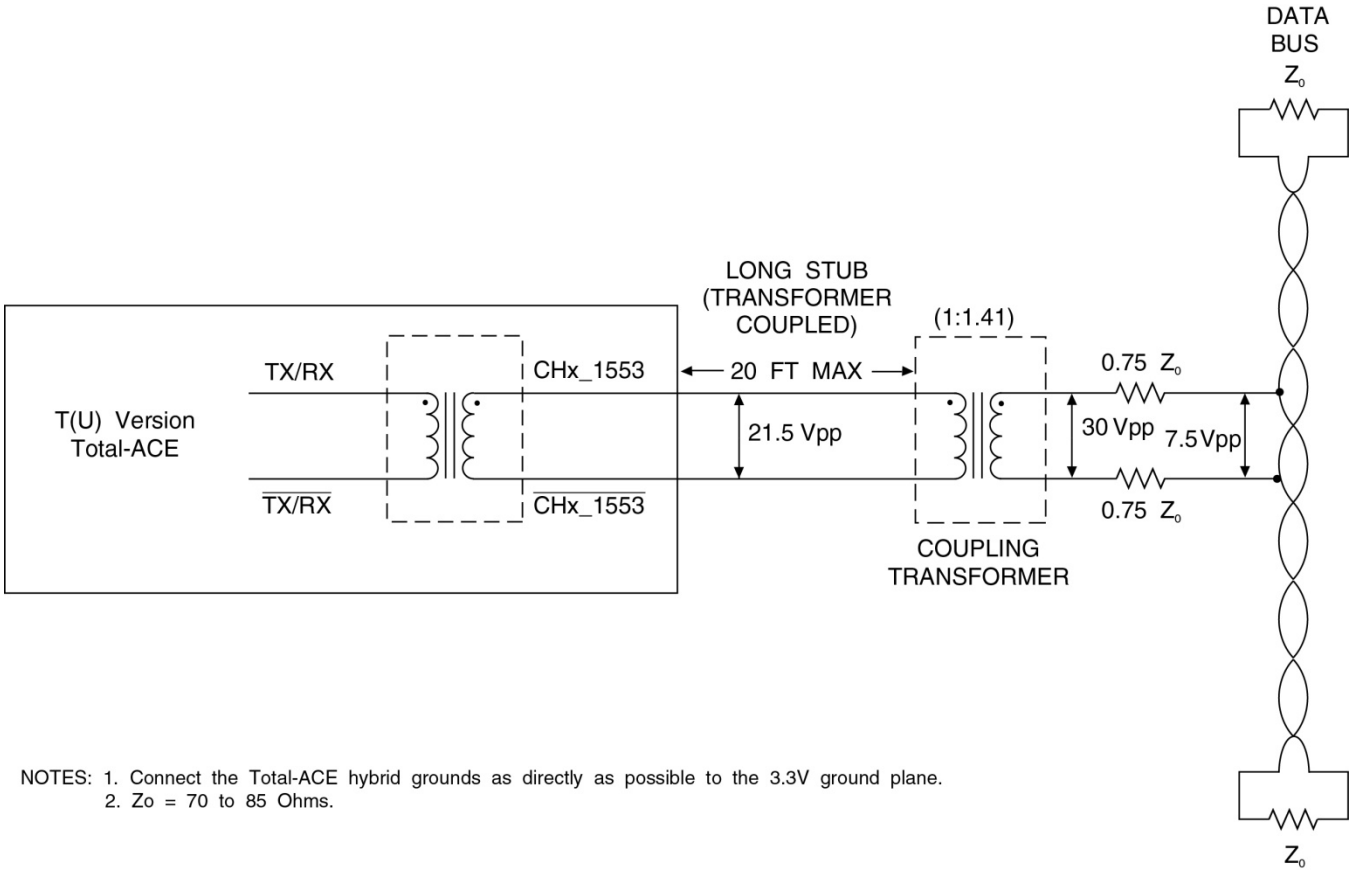
8.9 +3.3 VOLT INTERFACE TO MIL-STD-1553 BUS

The Total-ACE is the world's first fully integrated MIL-STD-1553 Terminal and Transformer solution.

Figure 16 and Figure 17 illustrate the interface method between the Total-ACE series and a MIL-STD-1553 bus. Depending on the version, connections for both transformer (long stub, 1:2.7) and direct (short stub 1:3.75) coupling, as well as

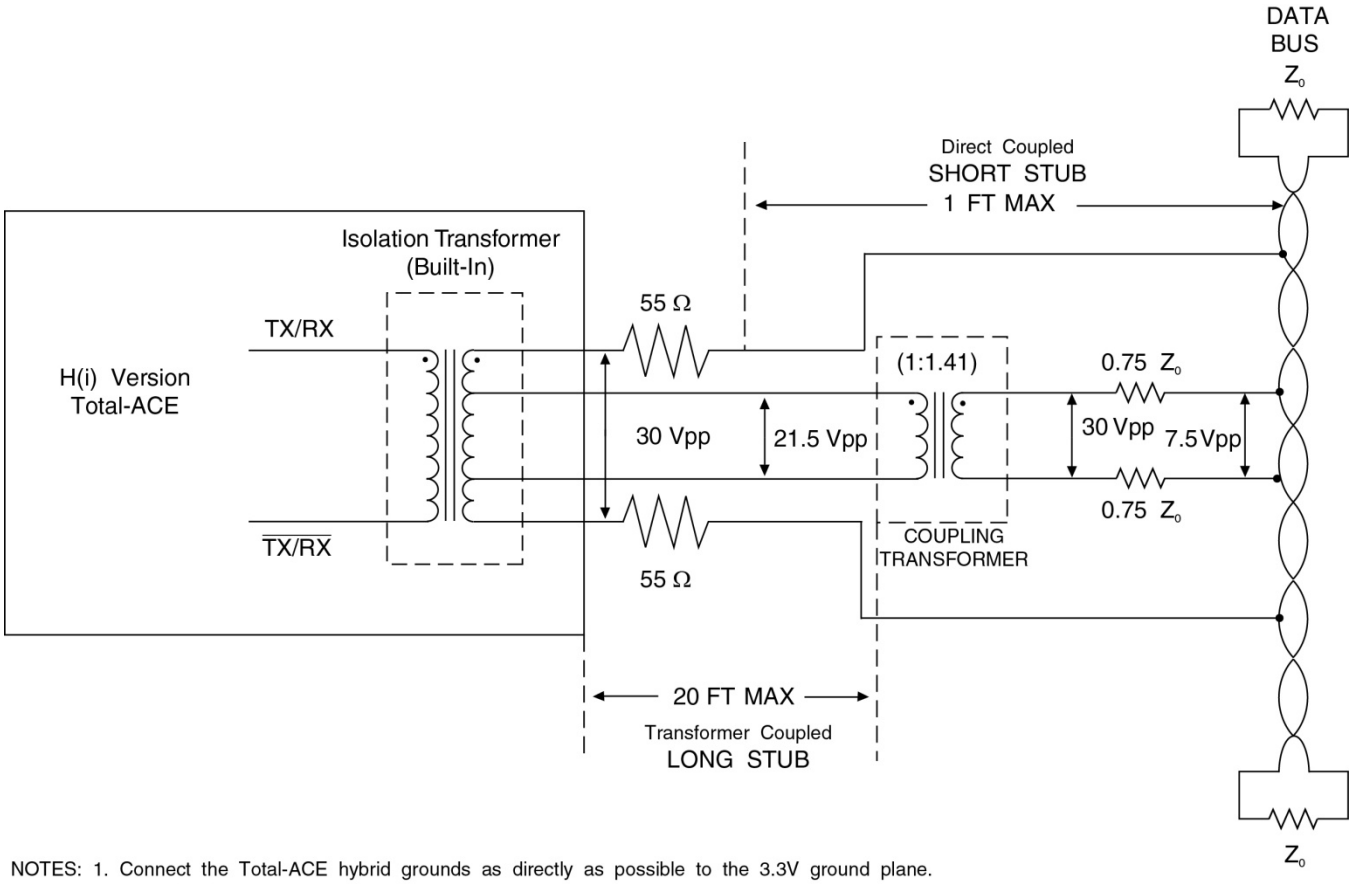
nominal peak-to-peak voltage levels at varions points (when transmitting), are indicated in this diagram.

A 10µf, low inductance tantalum capacitor and a 0.01µf ceramic capacitor must be mounted as close as possible and with the shortest leads between +3.3V_XCVR Input and ground plane.



NOTES: 1. Connect the Total-ACE hybrid grounds as directly as possible to the 3.3V ground plane.
2. Zo = 70 to 85 Ohms.

Figure 16. T(U) Version Total-ACE Interface to MIL-STD-1553 Bus



NOTES: 1. Connect the Total-ACE hybrid grounds as directly as possible to the 3.3V ground plane.
2. Zo = 70 to 85 Ohms.

Figure 17. H(I) Version Total-ACE Interface to MIL-STD-1553 Bus

8.10 THERMAL MANAGEMENT FOR TOTAL-ACE (312-BALL BGA PACKAGE)

Ball Grid Array (BGA) components necessitate that thermal management issues be considered early in the design stage for MIL-STD-1553 terminals. This is especially true if high transmitter duty cycles are expected. The temperature range specified for DDC's Total-ACE device refers to the case temperature. Any duty cycle is acceptable as long as the case temperature is maintained within the industrial temperature range specified for the –Exx parts. See below for an explanation of thermal management requirements for high transmitter duty cycles with the military temperature range components.

All Total-ACE devices incorporate multiple package connections which perform the dual function of transceiver circuit ground and thermal heat sink. Refer to the pinout tables for thermal ball connection locations. It is mandatory that these thermal balls be directly soldered to a circuit ground/thermal plane (a circuit trace is insufficient).

Operation without an adequate ground/thermal plane is not recommended and extended exposure to these conditions may affect device reliability.

The purpose of this ground/thermal plane is to conduct the heat being generated by the transceivers within the package and conduct this heat away from the Total-ACE. In general, the circuit ground and thermal (chassis) ground are not the same ground plane. It is acceptable for these balls to be directly soldered to a ground plane but it must be located in close physical and thermal proximity ("0.003" pre-preg layer recommended) to the thermal plane.

The temperature of each chip within the Total-Ace must be maintained below its respective maximum operating junction temperature as specified in Table 1. The simplest method to ensure this is to attribute all internal power dissipation to the transceiver, use the θ_{Jx} numbers also specified in Table 1 to calculate the temperature rise at the transceiver, and ensure that the temperature at the transceiver never exceeds the lowest maximum operating junction temperature allowed for any internal component (135°C for the protocol chip).

The general equation for the heat rise from ambient to the source of heat inside a component (typically the transistor junctions) is $\Delta T=P*\theta$, where P is the power dissipation of the component and θ is the thermal impedance from the junctions to ambient. Here there are two heat paths to the ambient, up through the top of the case, and down through the PCB, so we have a pair of equations:

$$\Delta T = P_C*(\theta_{JC}+\theta_{CA}) = P_B*(\theta_{JB}+\theta_{BA}) \text{ and } P = P_C+P_B.$$

Where P_C is the portion of the component power which flows through the top of the case to the ambient, θ_{JC} is the thermal impedance of the component from the junctions to the top of the case, and θ_{CA} is the thermal impedance of the system from the top of the case to ambient. Similarly, P_B is the portion of the component power which flows through the bottom of the case into the PCB, θ_{JB} is the thermal impedance of the component from the transistor junctions to the board, and θ_{BA} is the thermal impedance of the system from the board under the component to ambient.

For the case of a BU-64843H8-102 used as a monitor terminal, P=0.269W and θ_{JB}=26.5°C/W. This can be simplified by assuming that no heat flows out through the top of the case and only measuring the rise above package temperature without considering the whole path to ambient (ignoring θ_{BA}). The equation thus simplifies to:

$$\Delta T = P*(\theta_{JB}) = 0.269*(26.5+0) = 7.1°C$$

With a package temperature of 125°, this leaves the junction temperature below the maximum of 135°C.

The transmit duty cycle of a remote terminal is typically under 25%, with a few exceptions for high bandwidth devices like data loaders. Substituting the 25% duty cycle power (P=0.347W) into the equation above leads to a temperature rise of 9.2°C, which is still within acceptable limits as long as the board under the component is maintained at or below 125°C.

For a bus controller, higher duty cycles are common, so it may be necessary to add some form of heat sink to remove heat from the top of the component as well. For a BU-64863H8-102 with a duty cycle of 100%, P=0.703W. If the cooling paths from the top and bottom of the case to the ambient are assumed to be equally effective, ignoring θ_{CA} and θ_{BA} and setting the temperatures at both the top and bottom of the component to be the same, then the equations become:

$$\Delta T = P_C*(26.2) = P_B*(26.5)$$

And:

$$0.703 = P_C+P_B$$

Which turns into:

$$P_C = 0.703-P_B$$

Substituting for P_C and θ_{Jx} in the equation for ΔT, we get:

$$\Delta T = (0.703-P_B)*(26.2) = P_B*(26.5)$$
$$18.4186-26.2 *P_B = 26.5*P_B$$
$$18.4186 = 52.7*P_B$$
$$P_B = 0.3495$$

Substituting this result back into the ΔT equation, we get:

$$\Delta T = 0.2999*26.5 = 9.3°C$$

So as long as both the top and bottom of the case are maintained below 125°C, using heat sinks if necessary, the junction temperatures will remain within the acceptable limits.

For applications where high duty cycle operation is required at high ambient temperature, DDC also provides a thermal model that can be use with the FloTherm modeling tool from Mentor Graphics to assign power dissipation numbers to each internal component and determine the resulting operating junction temperature of

each, allowing the assurance of proper operation without requiring excessively conservative estimates that can hurt performance and increase costs.

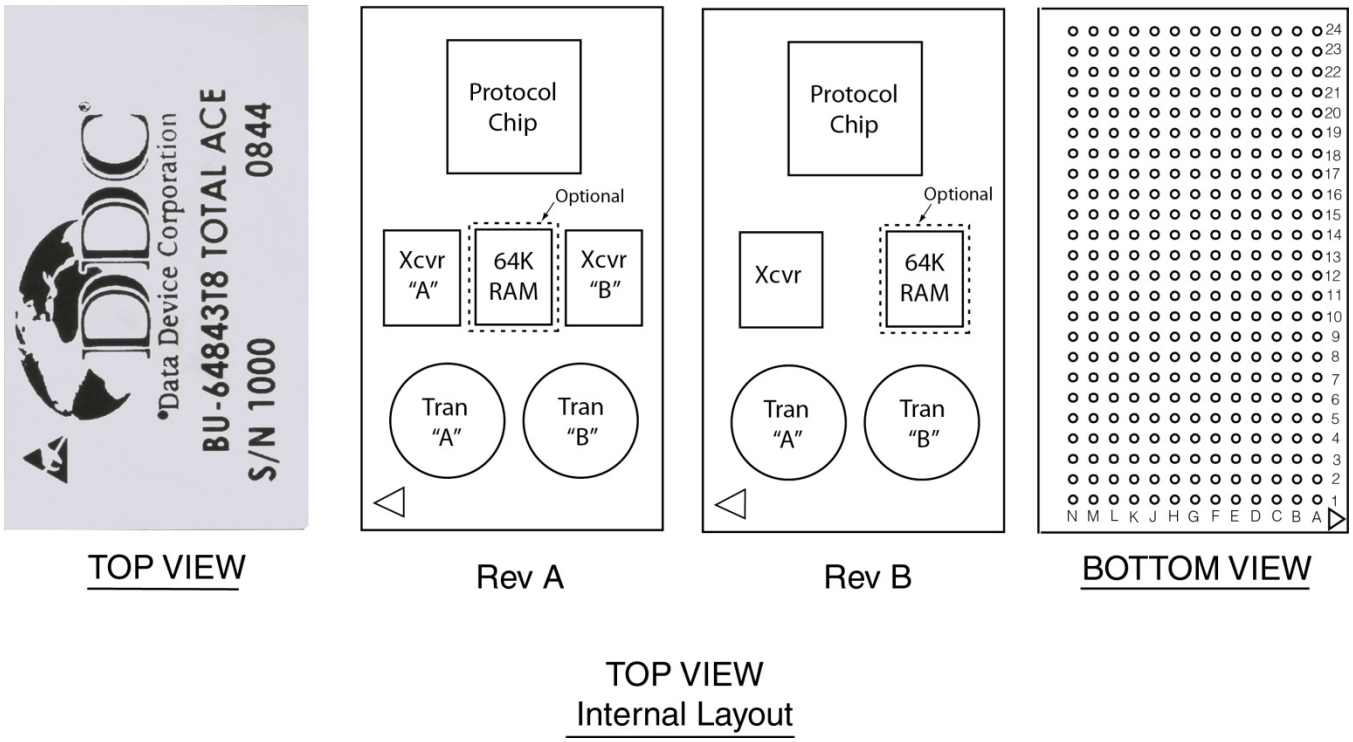


Figure 18. Ball Locations for Total-ACE (312-Ball BGA Package)

8.11 Ball Grid Array Package - Signal Descriptions by Functional Groups

Table 46. Power and Ground		
Signal Name	**All Versions Ball**	**Description**
+ 3.3V_Xcvr	B6, B7, B8, C6, C7, C12, D12, G6, G7, G8, G9, K12, L6, L7, L12, M6, M7, N9	+ 3.3 Volt Transceiver Power
+ 3.3V_Logic	B16, B17, C16, C17, F13, F14, G13, G14, M16, M17, N19, N20	+3.3 V Logic Power
GND_Xcvr	A1, A2, A3, B1, B2, B3, M1, M2, M3, N1, N2, N3	Transceiver Ground
Gnd_Xcvr/Thermal	B9, B10, B11, C8, C9, C10, C11, D8, D9, D10, D11, E9, E10, E11, J9, J10, J11, K8, K9, K10, K11, L8, L9, L10, L11, M9, M10, M11	Transceiver Ground/Thermal connections. See Thermal Management Section for important user information.
Gnd_Logic	A22, A23, A24, B20, B22, B23, B24, C22, C23, C24, E17, E18, E19, F17, F18, F19, G17, G18, G19, H17, H18, H19, H20, J17, J18, J19, J20, L14, L15, L22, L23, L24, M14, M15, M22, M23, M24, N22, N23, N24	Logic Ground

Note: *Logic ground and transceiver ground* ***are not*** *tied together inside the package.*

Table 47. 1553 Stub Connection			
Signal Name	**T(U) Version Ball**	**H(I) Version Ball**	**Description**
CHA_1553 (I/O)	D1, D2, D3	D1, D2, D3	1553 Transmit/Receive Input/Output. Connect directly to 1553 Long Stub.
$\overline{\text{CHA\_1553}}$ (I/O)	F1, F2, F3	F1, F2, F3	
CHB_1553 (I/O)	H1, H2, H3	H1, H2, H3	
$\overline{\text{CHB\_1553}}$ (I/O)	K1, K2, K3	K1, K2, K3	
CHA_1553-D (I/O)	—	D4, E4, F4	1553 Transmit/Receive Input/Output. Connect directly to 1553, 55-Ohm Fault Isolation Resistors
$\overline{\text{CHA\_1553-D}}$ (I/O)	—	E1, E2, E3	
CHB_1553-D (I/O)	—	H4, J4, K4	
$\overline{\text{CHB\_1553-D}}$ (I/O)	—	J1, J2, J3	

Table 48. Mandatory Additional Connections & Interface to External Transceiver			
Signal Name	**Using Internal "Built-In" Transceivers**	**All Versions Ball**	**For Use with External Transceivers "Transceiverless"**
$\overline{\text{SNGL\_END}}$ (I)	No Connect "NC" if utilizing "Built-In" Transceivers	A21	If $\overline{\text{SNGL\_END}}$ is connected to logic "0" the Manchester decoder inputs will be configured to accept single-ended input signals (e.g.,MIL-STD-1773 fiber optic receiver outputs). If $\overline{\text{SNGL\_END}}$ is connected to logic "1," the decoder inputs will be configured to accept standard double-ended Manchester bi-phase input signals (i.e., MILSTD-1553 receiver outputs).
TXINH_IN_A (I)	These two signals MUST be directly connected for normal "Built-In" transceiver operation.	A12	Do NOT connect these two signals together. Connect TXINH_OUT (Digital transmit inhibit output) to the TX INH input of external MIL-STD-1553 transceivers. Asserted high to inhibit when not transmitting in the respective bus.
TXINH_OUT_A (O)		A13	
TXDATA_IN_A (I)	These two signals MUST be directly connected for normal "Built-In" transceiver operation.	A9	Do NOT connect these two signals. Connect TXDATA_OUT (Digital Manchester biphase transmit data output) directly to the corresponding input of a MIL-STD-1553 or MIL-STD-1773 (fiber optic) transceiver.
TXDATA_OUT_A (O)		A10	
$\overline{\text{TXDATA\_IN\_A}}$ (I)	These two signals MUST be directly connected for normal "Built-In" transceiver operation.	B14	Do NOT connect these two signals. Connect $\overline{\text{TXDATA\_OUT}}$ (Digital Manchester biphase transmit data output) directly to the corresponding input of a MIL-STD-1553 or MIL-STD-1773 (fiber optic) transceiver.
$\overline{\text{TXDATA\_OUT\_A}}$ (O)		C14	
$\overline{\text{RXDATA\_IN\_A}}$ (I)	These two signals MUST be directly connected for normal "Built-In" transceiver operation.	G12	Do NOT connect these two signals. Connect $\overline{\text{RXDATA\_IN}}$ (Digital Manchester biphase transmit data output) directly to the corresponding input of a MIL-STD-1553 or MIL-STD-1773 (fiber optic) transceiver.
$\overline{\text{RXDATA\_OUT\_A}}$ (O)		F12	
RXDATA_IN_A (I)	These two signals MUST be directly connected for normal "Built-In" transceiver operation.	G11	Do NOT connect these two signals. Connect RXDATA_IN (Digital Manchester biphase transmit data output) directly to the corresponding input of a MIL-STD-1553 or MIL-STD-1773 (fiber optic) transceiver.
RXDATA_OUT_A (O)		F11	
TXINH_IN_B (I)	These two signals MUST be directly connected for normal "Built-In" transceiver operation.	M20	Do NOT connect these two signals. Connect TXINH_OUT (Digital Manchester biphase transmit data output) directly to the corresponding input of a MIL-STD-1553 or MIL-STD-1773 (fiber optic) transceiver.
TXINH_OUT_B (O)		M19	
TXDATA_IN_B (I)	These two signals MUST be directly connected for normal "Built-In" transceiver operation.	J16	Do NOT connect these two signals. Connect TXDATA_OUT (Digital Manchester biphase transmit data output) directly to the corresponding input of a MIL-STD-1553 or MIL-STD-1773 (fiber optic) transceiver.
TXDATA_OUT_B (O)		K16	

Table 48. Mandatory Additional Connections & Interface to External Transceiver			
Signal Name	**Using Internal "Built-In" Transceivers**	**All Versions Ball**	**For Use with External Transceivers "Transceiverless"**
$\overline{\text{TXDATA\_IN\_B}}$ (I)	These two signals MUST be directly connected for normal "Built-In" transceiver operation.	K18	Do NOT connect these two signals. Connect $\overline{\text{TXDATA\_OUT}}$ (Digital Manchester biphase transmit data output) directly to the corresponding input of a MIL-STD-1553 or MIL-STD-1773 (fiber optic) transceiver.
$\overline{\text{TXDATA\_OUT\_B}}$ (O)		K19	
$\overline{\text{RXDATA\_IN\_B}}$ (I)	These two signals MUST be directly connected for normal "Built-In" transceiver operation.	M13	Do NOT connect these two signals. Connect $\overline{\text{RXDATA\_IN}}$ (Digital Manchester biphase transmit data output) directly to the corresponding input of a MIL-STD-1553 or MIL-STD-1773 (fiber optic) transceiver.
$\overline{\text{RXDATA\_OUT\_B}}$ (O)		M12	
RXDATA_IN_B (I)	These two signals MUST be directly connected for normal "Built-In" transceiver operation.	N13	Do NOT connect these two signals. Connect RXDATA_IN (Digital Manchester biphase transmit data output) directly to the corresponding input of a MIL-STD-1553 or MIL-STD-1773 (fiber optic) transceiver.
RXDATA_OUT_B (O)		N12	

Note: The device can be operated with either their internal transceivers or with external transceivers. When the devices are operated with their internal transceivers the customer must supply PCB traces that connect the device's "inputs to outputs" (within the correct column) as described in this table.

Table 49. Data Bus		
Signal Name	**All Versions Ball**	**Description**
D15 (MSB)	D21	16-bit bi-directional data bus. This bus interfaces the host processor to the Total-ACE's internal registers and internal RAM. In addition, in transparent mode, this bus allows data transfers to take place between the internal protocol/memory management logic and up to 64K x 16 of external RAM. Most of the time, the outputs for D15 through D0 are in the high impedance state. They drive outward in the buffered or transparent mode when the host CPU reads the internal RAM or registers. Also, in the transparent mode, D15-D0 will drive outward (towards the host) when the protocol/management logic is accessing (either reading or writing) internal RAM, or writing to external RAM. In the transparent mode, D15-D0 drives inward when the CPU writes internal registers or RAM, or when the protocol/memory management logic reads external RAM.
D14	E24	
D13	E22	
D12	E23	
D11	E21	
D10	F24	
D09	F22	
D08	F23	
D07	F21	
D06	G23	
D05	G22	
D04	G24	
D03	G21	
D02	H23	
D01	H22	
D00 (LSB)	H24	

Table 50. Processor Address Bus

Signal Name		All Versions Ball	Description
With 64K RAM BU-6486X	With 4K RAM BU-6484X		
A15(MSB)	A15 / CLK_SEL_1	D17	16-bit bi-directional address bus. For 64K RAM versions, this signal is always configured as address line A15 (MSB). Refer to the description for A11-A0 below. For 4K RAM versions, if UPADDREN is connected to logic "1", this signal operates as address line A15. For 4K RAM versions, if UPADDREN is connected to logic "0", this signal operates as CLK_SEL_1. In this case, A15/CLK_SEL_1 and A14/CLK_SEL_0 are used to select the Total-ACE clock frequency, as follows: CLK_SEL_1 / CLK_SEL_0 / Clock Frequency 0 / 0 / 10 MHz 0 / 1 / 20 MHz 1 / 0 / 12 MHz 1 / 1 / 16 MHz
A14	A14 / CLK_SEL_0	A16	For 64K RAM versions, this signal is always configured as address line A14. Refer to the description of A11-A0 below. For 4K RAM versions, if UPADDREN is connected to logic "1", this signal operates as A14. For 4K RAM versions, if UPADDREN is connected to logic "0", then this signal operates as CLK_SEL_0. In this case, CLK_SEL_1 and CLK_SEL_0 are used to select the Total-ACE clock frequency, as defined in the description for A15/CLK_SEL1 above.
A13	A13 / LOGIC "1"	D16	For 64K RAM versions, this signal is always configured as address line A13. Refer to the description for A11-A0 below. For 4K RAM versions, if UPADDREN is connected to logic "1", this signal operates as A13. For 4K RAM versions, if UPADDREN is connected to logic "0", then this signal MUST be connected to +3.3V-LOGIC (logic "1").
A12	A12 / $\overline{\text{RTBOOT}}$	B15	For 64K RAM versions, this signal is always configured as address line A12. Refer to the description for A11-A0 below. For 4K RAM versions, if UPADDREN is connected to logic "1", this signal operates as A12. For 4K RAM versions, if UPADDREN is connected to logic "0", then this signal functions as $\overline{\text{RTBOOT}}$. If $\overline{\text{RTBOOT}}$ is connected to logic "0", the Total-ACE will initialize in RT mode with the Busy status word bit set following power turn-on. If $\overline{\text{RTBOOT}}$ is hardwired to logic "1", the Total-ACE will initialize in either Idle mode (if BC_Disable is high), or in BC mode (if BC_Disable is low).
A11	A11 (MSB)	C15	Lower 12 bits of 16-bit bi-directional address bus. In both the buffered and transparent modes, the host CPU accesses Total-
A10	A10	A15	

Table 50. Processor Address Bus			
Signal Name		**All Versions Ball**	**Description**
With 64K RAM BU-6486X	**With 4K RAM BU-6484X**		
A09	A09	A14	ACE registers and internal RAM by means of A11 - A0 (4K versions). For 64K versions, A15-A12 are also used for this purpose. In buffered mode, A12-A0 (or A15-A0) are inputs only. In the transparent mode, A12-A0 (or A15-A0) are inputs during CPU accesses and become outputs, driving outward (towards the CPU) when the 1553 protocol/memory management logic accesses up to 64K words of external RAM. In transparent mode, the address bus is driven outward only when the signal DTACK is low (indicating that the Total-ACE has control of the RAM interface bus) and IOEN is high, indicating a non-host access. Most of the time, including immediately after power turn-on, A12-A0 (or A15-A0) will be in high impedance (input) state.
A08	A08	D14	
A07	A07	B12	
A06	A06	D15	
A05	A05	E13	
A04	A04	E15	
A03	A03	E12	
A02	A02	F15	
A01	A01	E14	
A00 (LSB)	A00 (LSB)	F16	

Table 51. Processor Interface Control		
Signal Name	**All Versions Ball**	**Description**
$\overline{\text{SELECT}}$ (I)	B18	Device Select. Generally connected to a CPU address decoder output to select the Total-ACE for a transfer to/from either RAM or register.
$\overline{\text{STRBD}}$ (I)	A18	Strobe Data. Used in conjunction with $\overline{\text{SELECT}}$ to initiate and control the data transfer cycle between the host processor and the Total-ACE. $\overline{\text{STRBD}}$ must be asserted low through the full duration of the transfer cycle.
RD/$\overline{\text{WR}}$ (I)	A17	Read/Write. For host processor access, RD/$\overline{\text{WR}}$ selects between reading and writing. In the 16-bit buffered mode, if POL_SEL is logic "0", then RD/$\overline{\text{WR}}$ should be low (logic "0") for read accesses and high (logic "1") for write accesses. If POL_SEL is logic "1", or the interface is configured for a mode other than 16-bit buffered mode, then RD/$\overline{\text{WR}}$ is high (logic "1") for read accesses and low (logic "0") for write accesses.

Table 51. Processor Interface Control		
Signal Name	**All Versions Ball**	**Description**
ADDR_LAT(I) / $\overline{\text{MEMOE}}$ (O)	L16	Memory Output Enable or Address Latch. In buffered mode, the ADDR_LAT input is used to configure the buffers for A15-A0, $\overline{\text{SELECT}}$, MEM/$\overline{\text{REG}}$, and MSB/LSB (for 8-bit mode only) in latched mode (when low) or transparent mode (when high). That is, the Total-ACE's internal transparent latches will track the values on A15-A0, $\overline{\text{SELECT}}$, MEM/$\overline{\text{REG}}$, and MSB/LSB when ADDR_LAT is high, and latch the values when ADDR_LAT goes low. In general, for interfacing to processors with a non-multiplexed address/data bus, ADDR_LAT should be hardwired to logic "1". For interfacing to processors with a multiplexed address/data bus, ADDR_LAT should be connected to a signal that indicates a valid address when ADDR_LAT is logic "1". In transparent mode, $\overline{\text{MEMOE}}$ output signal is used to enable data outputs for external RAM read cycles (normally connected to the OE input signal on external RAM chips).
$\overline{\text{ZEROWAIT}}$ (I) / $\overline{\text{MEMWR}}$ (O)	N16	Memory Write or Zero Wait. In buffered mode, input signal ($\overline{\text{ZEROWAIT}}$) used to select between the zero wait mode ($\overline{\text{ZEROWAIT}}$ = "0") and the non-zero wait mode ($\overline{\text{ZEROWAIT}}$ = "1"). In transparent mode, active low output signal ($\overline{\text{MEMWR}}$) asserted low during memory write transfers to strobe data into external RAM (normally connected to the $\overline{\text{WR}}$ input signal on external RAM chips).
16/$\overline{8}$ (I) / $\overline{\text{DTREQ}}$ (O)	L17	Data Transfer Request or Data Bus Select. In buffered mode, input signal 16/8 used to select between the 16 bit data transfer mode (16/$\overline{8}$ = "1") and the 8-bit data transfer mode (16/$\overline{8}$ = "0"). In transparent mode (16-bit only), active low level output signal $\overline{\text{DTREQ}}$ used to request access to the processor/RAM interface bus (address and data buses).
MSB / LSB (I) / $\overline{\text{DTGRT}}$ (I)	J14	Data Transfer Grant or Most Significant Byte/Least Significant Byte. In 8-bit buffered mode, input signal (MSB/LSB) used to indicate which byte is currently being transferred (MSB or LSB). The logic sense of MSB/LSB is controlled by the POL_SEL input. MSB/LSB is not used in the 16-bit buffered mode. In transparent mode, active low input signal ($\overline{\text{DTGRT}}$) asserted in response to the $\overline{\text{DTREQ}}$ output to indicate that control of the external processor/RAM bus has been transferred from the host processor to the Total-ACE.

Table 51. Processor Interface Control		
Signal Name	**All Versions Ball**	**Description**
POL_SEL (I) / $\overline{\text{DTACK}}$ (O)	N17	Data Transfer Acknowledge or Polarity Select. In 16-bit buffered mode, if POL_SEL is connected to logic "1", RD/$\overline{\text{WR}}$ should be asserted high (logic "1") for a read operation and low (logic "0") for a write operation. In 16-bit buffered mode, if POL_SEL is connected to logic "0", RD/$\overline{\text{WR}}$ should be asserted low (logic "0") for a read operation and high (logic "1") for a write operation. In 8-bit buffered mode (TRANSPARENT/ BUFFERED = "0" and 16/8 = "0"), POL_SEL input signal used to control the logic sense of the MSB/$\overline{\text{LSB}}$ signal. If POL_SEL is connected to logic "0", MSB/$\overline{\text{LSB}}$ should be asserted low (logic "0") to indicate the transfer of the least significant byte and high (logic "1") to indicate the transfer of the most significant byte. If POL_SEL is connected to logic "1", MSB/$\overline{\text{LSB}}$ should be asserted high (logic "1") to indicate the transfer of the least significant byte and low (logic "0") to indicate the transfer of the most significant byte. In transparent mode, active low output signal ($\overline{\text{DTACK}}$) used to indicate acceptance of the processor/RAM interface bus in response to a data transfer grant ($\overline{\text{DTGRT}}$). Total-ACE RAM transfers over A15-A0 and D15-D0 will be framed by the time that $\overline{\text{DTACK}}$ is asserted low.
TRIG_SEL (I) / $\overline{\text{MEMENA\_IN}}$ (I)	M18	Memory Enable or Trigger Select input. In 8-bit buffered mode, input signal (TRIG-SEL) used to select the order in which byte pairs are transferred to or from the Total-ACE by the host processor. In the 8-bit buffered mode, TRIG_SEL should be asserted high (logic 1) if the byte order for both read operations and write operations is MSB followed by LSB. TRIG_SEL should be asserted low (logic 0) if the byte order for both read operations and write operations is LSB followed by MSB. This signal has no operation in the 16-bit buffered mode (it does not need to be connected). In transparent mode, active low input $\overline{\text{MEMENA\_IN}}$, used as a Chip Select (CS) input to the Total-ACE's internal shared RAM. If only internal RAM is used, should be connected directly to the output of a gate that is OR'ing the $\overline{\text{DTACK}}$ and $\overline{\text{IOEN}}$ output signals.
MEM/$\overline{\text{REG}}$ (I)	C18	Memory/Register. Generally connected to either a CPU address line or address decoder output. Selects between memory access (MEM/$\overline{\text{REG}}$ = "1") or register access (MEM/$\overline{\text{REG}}$ = "0").

Table 51. Processor Interface Control		
Signal Name	**All Versions Ball**	**Description**
$\overline{\text{SSFLAG}}$ (I) / EXT_TRIG (I)	K14	Subsystem Flag (RT) or External Trigger (BC/Word Monitor) input. In RT mode, if this input is asserted low, the Subsystem Flag bit will be set in the Total-ACE's RT Status Word. If the $\overline{\text{SSFLAG}}$ input is logic "0" while bit 8 of Configuration Register #1 has been programmed to logic "1" (cleared), the Subsystem Flag RT Status Word bit will become logic "1," but bit 8 of Configuration Register #1, $\overline{\text{SUBSYSTEM FLAG}}$, will return logic "1" when read. That is, the sense on the $\overline{\text{SSFLAG}}$ input has no effect on the SUBSYSTEM FLAG register bit. In the non-enhanced BC mode, this signal operates as an External Trigger input. In BC mode, if the external BC Start option is enabled (bit 7 of Configuration Register #1), a low to high transition on this input will issue a BC Start command, starting execution of the current BC frame. In the enhanced BC mode, during the execution of a Wait for External Trigger (WTG) instruction, the Total-ACE BC will wait for a low-to-high transition on EXT_TRIG before proceeding to the next instruction. In the Word Monitor mode, if the external trigger is enabled (bit 7 of Configuration Register #1), a low to high transition on this input will initiate a monitor start. This input has no effect in Message Monitor mode.
TRASNPARENT / $\overline{\text{BUFFERED}}$ (I)	D22	Used to select between the buffered mode (when strapped to logic "0") and transparent/DMA mode (when strapped to logic "1") for the host processor interface.
$\overline{\text{READYD}}$ (O)	C21	Handshake output to host processor. For a nonzero wait state read access, $\overline{\text{READYD}}$ is asserted at the end of a host transfer cycle to indicate that data is available to be read on D15 through D0 when asserted (low). For a nonzero wait state write cycle, $\overline{\text{READYD}}$ is asserted at the end of the cycle to indicate that data has been transferred to a register or RAM location. For both nonzero wait reads and writes, the host must assert $\overline{\text{STRBD}}$ low until $\overline{\text{READYD}}$ is asserted low. In the (buffered) zero wait state mode, this output is normally logic "1", indicating that the Total-ACE is in a state ready to accept a subsequent host transfer cycle. In zero wait mode, $\overline{\text{READYD}}$ will transition from high to low during (or just after) a host transfer cycle, when the Total-ACE initiates its internal transfer to or from registers or internal RAM. When the Total-ACE completes its internal transfer, $\overline{\text{READYD}}$ returns to logic "1", indicating it is ready for the host to initiate a subsequent transfer cycle.
$\overline{\text{IOEN}}$ (O)	C20	I/O Enable. Tri-state control for external address and data buffers. Generally not used in buffered mode. When low, indicates that the Total-ACE is currently performing a host access to an internal register, or internal (for transparent mode) external RAM. In transparent mode, $\overline{\text{IOEN}}$ (low) should be used to enable external address and data bus tri-state buffers.

Table 52. RT Address		
Signal Name	**All Versions Ball**	**Description**
RTAD4 (MSB) (I)	J21	RT Address input. If bit 5 of Configuration Register #6, RT ADDRESS SOURCE, is programmed to logic "0" (default), then the Total-ACE's RT address is provided by means of these 5 input signals. In addition, if RT ADDRESS SOURCE is logic "0", the source of RT address parity is RTADP. There are many methods for using these input signals for designating the Total-ACE's RT address. For details, refer to the description of RT_AD_LAT. If RT ADDRESS SOURCE is programmed to logic "1", then the Total-ACE's source for its RT address and parity is under software control, via data lines D5-D0. In this case, the RTAD4-RTAD0 and RTADP signals are not used.
RTAD3 (I)	J24	
RTAD2 (I)	J22	
RTAD1 (I)	K23	
RTAD0 (LSB) (I)	K21	
RTADP (I)	J23	Remote Terminal Address Parity. This input signal must provide an odd parity sum with RTAD4-RTAD0 in order for the RT to respond to non-broadcast commands. That is, there must be an odd number of logic "1"s from among RTAD-4- RTAD0 and RTADP.
RT_AD_LAT (I)	K24	RT Address Latch. Input signal used to control the Total-ACE's internal RT address latch. If RT_AD_LAT is connected to logic "0", then the Total-ACE RT is configured to accept a hardwired (transparent) RT address from RTAD4-RTAD0 and RTADP. If RT_AD_LAT is initially logic "0", and then transitions to logic "1", the values presented on RTAD4- RTAD0 and RTADP will be latched internally on the rising edge of RT_AD_LAT. If RT_AD_LAT is connected to logic "1", then the Total-ACE's RT address is latchable under host processor control. In this case, there are two possibilities: (1) If bit 5 of Configuration Register #6, RT ADDRESS SOURCE, is programmed to logic "0" (default), then the source of the RT Address is the RTAD4-RTAD0 and RTADP input signals. (2) If RT ADDRESS SOURCE is programmed to logic "1", then the source of the RT Address is the lower 6 bits of the processor data bus, D5-D1 (for RTAD4- 0) and D0 (for RTADP). In either of these two cases (with RT_AD_LAT = "1"), the processor will cause the RT address to be latched by: (1) Writing bit 15 of Configuration Register #3, ENHANCED Mode ENABLE, to logic "1". (2) Writing bit 3 of Configuration Register #4, LATCH RT ADDRESS WITH CONFIGURATION REGISTER #5, to logic "1". (3) Writing to Configuration Register #5. In the case of RT ADDRESS SOURCE = "1", then the values of RT address and RT address parity must be written to the lower 6 bits of Configuration Register #5, via D5-D0. In the case where RT ADDRESS SOURCE = "0", the bit values presented on D5-D0 become "don't care".

Table 53. Miscellaneous

Signal Name		All Versions Ball	Description
With 64K RAM BU-6486X	With 4K RAM BU-6484X		
+3.3V_Logic	UPADDREN (I)	A19	This signal is used to control the function of the upper 4 address inputs (A15-A12). If UPADDREN is connected to logic "1", then these four signals operate as address lines A15-A12. If UPADDREN is connected to logic "0", then A15 and A14 function as CLK_SEL_1 and CLK_ SEL_0 respectively; A13 MUST be connected to LOGIC "1"; and A12 functions as RTBOOT.
SLEEPIN (I)		H10	This signal is used to control the transceiver sleep (power-down) circuitry. If SLEEPIN is connected to logic "0", the transceivers are fully powered and operate normally. If SLEEPIN is connected to logic "1", the transceivers are in sleep mode (dormant, low-power mode) of operation and are NOT operational. This feature is not available on the BU-64863T(U)8.
$\overline{\text{INCMD}}$ (O)		H21	For BC, RT, or Selective Message Monitor modes, $\overline{\text{INCMD}}$ is asserted low whenever a message is being processed by the Total-ACE. In Word Monitor mode, $\overline{\text{INCMD}}$ will be asserted low for as long as the monitor is online.
$\overline{\text{MCRST}}$ (O)		D19	For RT mode $\overline{\text{MCRST}}$ will be asserted low for two clock cycles following receipt of a Reset remote terminal mode command.
RSTBITEN (I)		K22	If this input is set to logic "1", the Built-In-Self-Test (BIST) will be enabled after hardware reset (for example, following power-up). A logic "0" input disables both the power-up and user-initiated automatic BIST.
$\overline{\text{INT}}$ (O)		D24	Interrupt Request output. If the LEVEL/ $\overline{\text{PULSE}}$ interrupt bit (bit 3) of Configuration Register #2 is logic "0", a negative pulse of approximately 500 ns in width is output on $\overline{\text{INT}}$ to signal an interrupt request. If LEVEL/ $\overline{\text{PULSE}}$ is high, a low level interrupt request output will be asserted on $\overline{\text{INT}}$. The level interrupt will be cleared (high) after either: (1) The processor writes a value of logic "1" to INTERRUPT RESET, bit 2 of the Start/Reset Register; or (2) If bit 4 of Configuration Register #2, INTERRUPT STATUS AUTO-CLEAR is logic "1" then it will only be necessary to read the Interrupt Status Register (#1 and/or #2) that is requesting an interrupt enabled by the corresponding Interrupt Mask Register. However, for the case where both Interrupt Status Register #1 and Interrupt Status Register #2 have bits set reflecting interrupt events, it will be necessary to read both interrupt status registers in order to clear $\overline{\text{INT}}$.

Table 53. Miscellaneous			
Signal Name		**All Versions Ball**	**Description**
With 64K RAM BU-6486X	**With 4K RAM BU-6484X**		
CLOCK_IN (I)		N18	20 MHz, 16 MHz, 12 MHz, or 10 MHz clock input.
TX_INH_A (I)		A20	Transmitter inhibit inputs for Channel A and Channel B, MIL-STD-1553 transmitters. For normal operation, these inputs should be connected to logic "0". To force a shutdown of Channel A and/ or Channel B, a value of logic "1" should be applied to the respective TX_INH input.
TX_INH_B (I)		D20	
$\overline{\text{MSTCLR}}$ (I)		D18	Master Clear. Negative true Reset input, normally asserted low following power turn-on.
TAG_CLK (I)		D23	Time Tag Clock. External clock that may be used to increment the Time Tag Register. This option is selected by setting Bits 7, 8 and 9 of Configuration Register # 2 to Logic "1".
BC_Disable		B21	Hardware lockout to disable BC opertation and operate the part in RT-Only mode. Drive high to disable BC, low to enable all modes of operation.

Table 54. No User Connections			
Signal Name	**T(U) Version Ball**	**H (I) Version Ball**	**Description**
NC	A4, A5, A6, A7, A8, A11, B4, B5, B13, B19, C1, C2, C3, C4, C5, C13, C19, D4, D5, D6, D7, D13, E1, E2, E3, E4, E5, E6, E7, E8, E16, E20, F4, F5, F6, F7, F8, F9, F10, F20, G1, G2, G3, G4, G5, G10, G15, G16, G20, H4, H5, H6, H7, H8, H9, H11, H12, H13, H14, H15, H16, J1, J2, J3, J4, J5, J6, J7, J8, J12, J13, J15, K4, K5, K6, K7, K13, K15, K17, K20, L1, L2, L3, L4, L5, L13, L18, L19, L20, L21, M4, M5, M8, M21, N4, N5, N6, N7, N8, N10, N11, N14, N15, N21	A4, A5, A6, A7, A8, A11, B4, B5, B13, B19, C1, C2, C3, C4, C5, C13, C19, D5, D6, D7, D13, E5, E6, E7, E8, E16, E20, F5, F6, F7, F8, F9, F10, F20, G1, G2, G3, G4, G5, G10, G15, G16, G20, H5, H6, H7, H8, H9, H11, H12, H13, H14, H15, H16, J5, J6, J7, J8, J12, J13, J15, K5, K6, K7, K13, K15, K17, K20, L1, L2, L3, L4, L5, L13, L18, L19, L20, L21, M4, M5, M8, M21, N4, N5, N6, N7, N8, N10, N11, N14, N15, N21	No User Connections to these balls allowed.

Table 55. Total-ACE With 4K RAM (BU-6484X) All Versions Pinout					
Ball	**Signal**	**Notes**	**Ball**	**Signal**	**Notes**
A1	GND_Xcvr		C1	NC	
A2	GND_Xcvr		C2	NC	
A3	GND_Xcvr		C3	NC	
A4	NC		C4	NC	
A5	NC		C5	NC	
A6	NC		C6	+3.3V_Xcvr	
A7	NC		C7	+3.3V_Xcvr	
A8	NC		C8	GND_Xcvr/Thermal***	
A9	TXDATA_IN_A	connect to ball A10	C9	GND_Xcvr/Thermal***	
A10	TXDATA_OUT_A	connect to ball A9	C10	GND_Xcvr/Thermal***	
A11	NC		C11	GND_Xcvr/Thermal***	
A12	TXINH_IN_A	connect to ball A13	C12	+3.3V_Xcvr	
A13	TXINH_OUT_A	connect to ball A12	C13	NC	
A14	A09		C14	$\overline{\text{TXDATA\_OUT\_A}}$	connect to ball B14
A15	A10		C15	A11 (MSB)	
A16	A14 / CLK_SEL_0		C16	+3.3V_Logic	
A17	RD/ $\overline{\text{WR}}$		C17	+3.3V_Logic	
A18	$\overline{\text{STRBD}}$		C18	MEM/ $\overline{\text{REG}}$	
A19	UPADDREN		C19	NC	
A20	TX_INH_A		C20	$\overline{\text{IOEN}}$	
A21	$\overline{\text{SNGL\_END}}$		C21	$\overline{\text{READYD}}$	
A22	Gnd_Logic		C22	Gnd_Logic	
A23	Gnd_Logic		C23	Gnd_Logic	
A24	Gnd_Logic		C24	Gnd_Logic	
B1	GND_Xcvr		D1	CHA_1553	
B2	GND_Xcvr		D2	CHA_1553	
B3	GND_Xcvr		D3	CHA_1553	
B4	NC		D4	NC / CHA_1553-Direct$	
B5	NC		D5	NC	
B6	+3.3V_Xcvr		D6	NC	
B7	+3.3V_Xcvr		D7	NC	
B8	+3.3V_Xcvr		D8	GND_Xcvr/Thermal***	
B9	GND_Xcvr/Thermal***		D9	GND_Xcvr/Thermal***	
B10	GND_Xcvr/Thermal***		D10	GND_Xcvr/Thermal***	
B11	GND_Xcvr/Thermal***		D11	GND_Xcvr/Thermal***	
B12	A07		D12	+3.3V_Xcvr	
B13	NC		D13	NC	
B14	$\overline{\text{TXDATA\_IN\_A}}$	connect to ball C14	D14	A08	
B15	A12 / $\overline{\text{RTBOOT}}$		D15	A06	
B16	+3.3V_Logic		D16	A13 / LOGIC “1”	
B17	+3.3V_Logic		D17	A15 / CLK_SEL_1	
B18	$\overline{\text{SELECT}}$		D18	$\overline{\text{MSTCLR}}$	
B19	NC		D19	$\overline{\text{MCRST}}$	
B20	Gnd_Logic		D20	TX_INH_B	
B21	BC_Disable		D21	D15 (MSB)	
B22	Gnd_Logic		D22	TRANSPARENT / $\overline{\text{BUFFERED}}$	
B23	Gnd_Logic		D23	TAG_CLK	

Table 55. Total-ACE With 4K RAM (BU-6484X) All Versions Pinout					
Ball	**Signal**	**Notes**	**Ball**	**Signal**	**Notes**
B24	Gnd_Logic		D24	$\overline{\text{INT}}$	
E1	NC / CHA_1553-Direct$		G1	NC	
E2	NC / CHA_1553- Direct$		G2	NC	
E3	NC / CHA_1553- Direct$		G3	NC	
E4	NC / CHA_1553- Direct$		G4	NC	
E5	NC		G5	NC	
E6	NC		G6	+3.3V_Xcvr	
E7	NC		G7	+3.3V_Xcvr	
E8	NC		G8	+3.3V_Xcvr	
E9	GND_Xcvr/Thermal***		G9	+3.3V_Xcvr	
E10	GND_Xcvr/Thermal***		G10	NC	
E11	GND_Xcvr/Thermal***		G11	RXDATA_IN_A	connect to ball F11
E12	A03		G12	$\overline{\text{RXDATA\_IN\_A}}$	connect to ball F12
E13	A05		G13	+3.3V_Logic	
E14	A01		G14	+3.3V_Logic	
E15	A04		G15	NC	
E16	NC		G16	NC	
E17	Gnd_Logic		G17	Gnd_Logic	
E18	Gnd_Logic		G18	Gnd_Logic	
E19	Gnd_Logic		G19	Gnd_Logic	
E20	NC		G20	NC	
E21	D11		G21	D03	
E22	D13		G22	D05	
E23	D12		G23	D06	
E24	D14		G24	D04	
F1	$\overline{\text{CHA\_1553}}$		H1	CHB_1553	
F2	$\overline{\text{CHA\_1553}}$		H2	CHB_1553	
F3	$\overline{\text{CHA\_1553}}$		H3	CHB_1553	
F4	NC / CHA_1553- Direct$		H4	NC / CHB_1553- Direct$	
F5	NC		H5	NC	
F6	NC		H6	NC	
F7	NC		H7	NC	
F8	NC		H8	NC	
F9	NC		H9	NC	
F10	NC		H10	SLEEPIN	
F11	RXDATA_OUT_A	connect to ball G11	H11	NC	
F12	$\overline{\text{RXDATA\_OUT\_A}}$	connect to ball G12	H12	NC	
F13	+3.3V_Logic		H13	NC	
F14	+3.3V_Logic		H14	NC	
F15	A02		H15	NC	
F16	A00 (LSB)		H16	NC	
F17	Gnd_Logic		H17	Gnd_Logic	
F18	Gnd_Logic		H18	Gnd_Logic	
F19	Gnd_Logic		H19	Gnd_Logic	
F20	NC		H20	Gnd_Logic	
F21	D07		H21	$\overline{\text{INCMD}}$	
F22	D09		H22	D01	
F23	D08		H23	D02	

Table 55. Total-ACE With 4K RAM (BU-6484X) All Versions Pinout					
Ball	**Signal**	**Notes**	**Ball**	**Signal**	**Notes**
F24	D10		H24	D00 (LSB)	
J1	NC / CHB_1553- Direct$		L1	NC	
J2	NC / CHB_1553- Direct$		L2	NC	
J3	NC / CHB_1553- Direct$		L3	NC	
J4	NC / CHB_1553- Direct$		L4	NC	
J5	NC		L5	NC	
J6	NC		L6	+3.3V_Xcvr	
J7	NC		L7	+3.3V_Xcvr	
J8	NC		L8	GND_Xcvr/Thermal***	
J9	GND_Xcvr/Thermal***		L9	GND_Xcvr/Thermal***	
J10	GND_Xcvr/Thermal***		L10	GND_Xcvr/Thermal***	
J11	GND_Xcvr/Thermal***		L11	GND_Xcvr/Thermal***	
J12	NC		L12	+3.3V_Xcvr	
J13	NC		L13	NC	
J14	MSB / LSB / $\overline{\text{DTGRT}}$		L14	Gnd_Logic	
J15	NC		L15	Gnd_Logic	
J16	TXDATA_IN_B	connect to ball K16	L16	ADDR_LAT / $\overline{\text{MEMOE}}$	
J17	Gnd_Logic		L17	16/ $\overline{8}$ / $\overline{\text{DTREQ}}$	
J18	Gnd_Logic		L18	NC	
J19	Gnd_Logic		L19	NC	
J20	Gnd_Logic		L20	NC	
J21	RTAD4 (MSB)		L21	NC	
J22	RTAD2		L22	Gnd_Logic	
J23	RTADP		L23	Gnd_Logic	
J24	RTAD3		L24	Gnd_Logic	
K1	$\overline{\text{CHB\_1553}}$		M1	GND_Xcvr	
K2	$\overline{\text{CHB\_1553}}$		M2	GND_Xcvr	
K3	$\overline{\text{CHB\_1553}}$		M3	GND_Xcvr	
K4	NC / CHB_1553- Direct$		M4	NC	
K5	NC		M5	NC	
K6	NC		M6	+3.3V_Xcvr	
K7	NC		M7	+3.3V_Xcvr	
K8	GND_Xcvr/Thermal***		M8	NC	
K9	GND_Xcvr/Thermal***		M9	GND_Xcvr/Thermal***	
K10	GND_Xcvr/Thermal***		M10	GND_Xcvr/Thermal***	
K11	GND_Xcvr/Thermal***		M11	GND_Xcvr/Thermal***	
K12	+3.3V_Xcvr		M12	$\overline{\text{RXDATA\_OUT\_B}}$	connect to ball M13
K13	NC		M13	$\overline{\text{RXDATA\_IN\_B}}$	connect to ball M12
K14	$\overline{\text{SSFLAG}}$ / EXT_TRIG		M14	Gnd_Logic	
K15	NC		M15	Gnd_Logic	
K16	TXDATA_OUT_B	connect to ball J16	M16	+3.3V_Logic	
K17	NC		M17	+3.3V_Logic	
K18	$\overline{\text{TXDATA\_IN\_B}}$	connect to ball K19	M18	TRIG_SEL / $\overline{\text{MEMENA\_IN}}$	
K19	$\overline{\text{TXDATA\_OUT\_B}}$	connecto to ball K18	M19	TXINH_OUT_B	connect to ball M20
K20	NC		M20	TXINH_IN_B	connect to ball M19
K21	RTAD0 (LSB)		M21	NC	
K22	RSTBITEN		M22	Gnd_Logic	
K23	RTAD1		M23	Gnd_Logic	

Table 55. Total-ACE With 4K RAM (BU-6484X) All Versions Pinout					
Ball	**Signal**	**Notes**	**Ball**	**Signal**	**Notes**
K24	RT_AD_LAT		M24	Gnd_Logic	

Table 55. Total-ACE With 4K RAM (BU-6484X) All Versions Pinout		
Ball	**Signal**	**Notes**
N1	GND_Xcvr	
N2	GND_Xcvr	
N3	GND_Xcvr	
N4	NC	
N5	NC	
N6	NC	
N7	NC	
N8	NC	
N9	+3.3V_Xcvr	
N10	NC	
N11	NC	
N12	RXDATA_OUT_B	connect to ball N13
N13	RXDATA_IN_B	connect to ball N12
N14	NC	
N15	NC	
N16	$\overline{\text{ZEROWAIT}}$ / $\overline{\text{MEMWR}}$	
N17	POL_SEL / $\overline{\text{DTACK}}$	
N18	CLOCK_IN	
N19	+3.3V_Logic	
N20	+3.3V_Logic	
N21	NC	
N22	Gnd_Logic	
N23	Gnd_Logic	
N24	Gnd_Logic	

$ - Applicable to the H(I) Version only
***See Thermal Management Section for important user information

NC = Do not connect – no user connections to these balls allowed

GND_Xcvr /Thermal = Thermal Ball – must be connected to PWB Thermal Plane
“Connect to ball XXX” = Logic Transceiver Interconnect Signals

Table 56. Total-ACE With 64K RAM (BU-6486X) All Versions Pinout					
Ball	**Signal**	**Notes**	**Ball**	**Signal**	**Notes**
A1	GND_Xcvr		C1	NC	
A2	GND_Xcvr		C2	NC	
A3	GND_Xcvr		C3	NC	
A4	NC		C4	NC	
A5	NC		C5	NC	
A6	NC		C6	+3.3V_Xcvr	
A7	NC		C7	+3.3V_Xcvr	
A8	NC		C8	GND_Xcvr/Thermal***	
A9	TXDATA_IN_A	connect to ball A10	C9	GND_Xcvr/Thermal***	
A10	TXDATA_OUT_A	connect to ball A9	C10	GND_Xcvr/Thermal***	
A11	NC		C11	GND_Xcvr/Thermal***	
A12	TXINH_IN_A	connect to ball A13	C12	+3.3V_Xcvr	
A13	TXINH_OUT_A	connect to ball A12	C13	NC	
A14	A09		C14	$\overline{\text{TXDATA\_OUT\_A}}$	connect to ball B14
A15	A10		C15	A11 (MSB)	
A16	A14		C16	+3.3V_Logic	
A17	RD/ $\overline{\text{WR}}$		C17	+3.3V_Logic	
A18	$\overline{\text{STRBD}}$		C18	MEM/ $\overline{\text{REG}}$	
A19	+3.3V_Logic		C19	NC	
A20	TX_INH_A		C20	$\overline{\text{IOEN}}$	
A21	$\overline{\text{SNGL\_END}}$		C21	$\overline{\text{READYD}}$	
A22	Gnd_Logic		C22	Gnd_Logic	
A23	Gnd_Logic		C23	Gnd_Logic	
A24	Gnd_Logic		C24	Gnd_Logic	
B1	GND_Xcvr		D1	CHA_1553	
B2	GND_Xcvr		D2	CHA_1553	
B3	GND_Xcvr		D3	CHA_1553	
B4	NC		D4	NC / CHA_1553-D$	
B5	NC		D5	NC	
B6	+3.3V_Xcvr		D6	NC	
B7	+3.3V_Xcvr		D7	NC	
B8	+3.3V_Xcvr		D8	GND_Xcvr/Thermal***	
B9	GND_Xcvr/Thermal***		D9	GND_Xcvr/Thermal***	
B10	GND_Xcvr/Thermal***		D10	GND_Xcvr/Thermal***	
B11	GND_Xcvr/Thermal***		D11	GND_Xcvr/Thermal***	
B12	A07		D12	+3.3V_Xcvr	
B13	NC		D13	NC	
B14	$\overline{\text{TXDATA\_IN\_A}}$	connect to ball C14	D14	A08	
B15	A12		D15	A06	
B16	+3.3V_Logic		D16	A13	
B17	+3.3V_Logic		D17	A15	
B18	$\overline{\text{SELECT}}$		D18	$\overline{\text{MSTCLR}}$	
B19	NC		D19	$\overline{\text{MCRST}}$	
B20	Gnd_Logic		D20	TX_INH_B	
B21	BC_Disable		D21	D15 (MSB)	
B22	Gnd_Logic		D22	TRANSPARENT / $\overline{\text{BUFFERED}}$	
B23	Gnd_Logic		D23	TAG_CLK	

Table 56. Total-ACE With 64K RAM (BU-6486X) All Versions Pinout					
Ball	**Signal**	**Notes**	**Ball**	**Signal**	**Notes**
B24	Gnd_Logic		D24	$\overline{\text{INT}}$	
E1	NC / CHA_1553-D*$		G1	NC	
E2	NC / CHA_1553-D*$		G2	NC	
E3	NC / CHA_1553-D*$		G3	NC	
E4	NC / CHA_1553-D*$		G4	NC	
E5	NC		G5	NC	
E6	NC		G6	+3.3V_Xcvr	
E7	NC		G7	+3.3V_Xcvr	
E8	NC		G8	+3.3V_Xcvr	
E9	GND_Xcvr/Thermal***		G9	+3.3V_Xcvr	
E10	GND_Xcvr/Thermal***		G10	NC	
E11	GND_Xcvr/Thermal***		G11	RXDATA_IN_A	connect to ball F11
E12	A03		G12	$\overline{\text{RXDATA\_IN\_A}}$	connect to ball F12
E13	A05		G13	+3.3V_Logic	
E14	A01		G14	+3.3V_Logic	
E15	A04		G15	NC	
E16	NC		G16	NC	
E17	Gnd_Logic		G17	Gnd_Logic	
E18	Gnd_Logic		G18	Gnd_Logic	
E19	Gnd_Logic		G19	Gnd_Logic	
E20	NC		G20	NC	
E21	D11		G21	D03	
E22	D13		G22	D05	
E23	D12		G23	D06	
E24	D14		G24	D04	
F1	$\overline{\text{CHA\_1553}}$		H1	CHB_1553	
F2	$\overline{\text{CHA\_1553}}$		H2	CHB_1553	
F3	$\overline{\text{CHA\_1553}}$		H3	CHB_1553	
F4	NC / CHA_1553-D$		H4	NC / CHB_1553-D$	
F5	NC		H5	NC	
F6	NC		H6	NC	
F7	NC		H7	NC	
F8	NC		H8	NC	
F9	NC		H9	NC	
F10	NC		H10	SLEEPIN	
F11	RXDATA_OUT_A	connect to ball G11	H11	NC	
F12	$\overline{\text{RXDATA\_OUT\_A}}$	connect to ball G12	H12	NC	
F13	+3.3V_Logic		H13	NC	
F14	+3.3V_Logic		H14	NC	
F15	A02		H15	NC	
F16	A00 (LSB)		H16	NC	
F17	Gnd_Logic		H17	Gnd_Logic	
F18	Gnd_Logic		H18	Gnd_Logic	
F19	Gnd_Logic		H19	Gnd_Logic	
F20	NC		H20	Gnd_Logic	
F21	D07		H21	$\overline{\text{INCMD}}$	
F22	D09		H22	D01	
F23	D08		H23	D02	

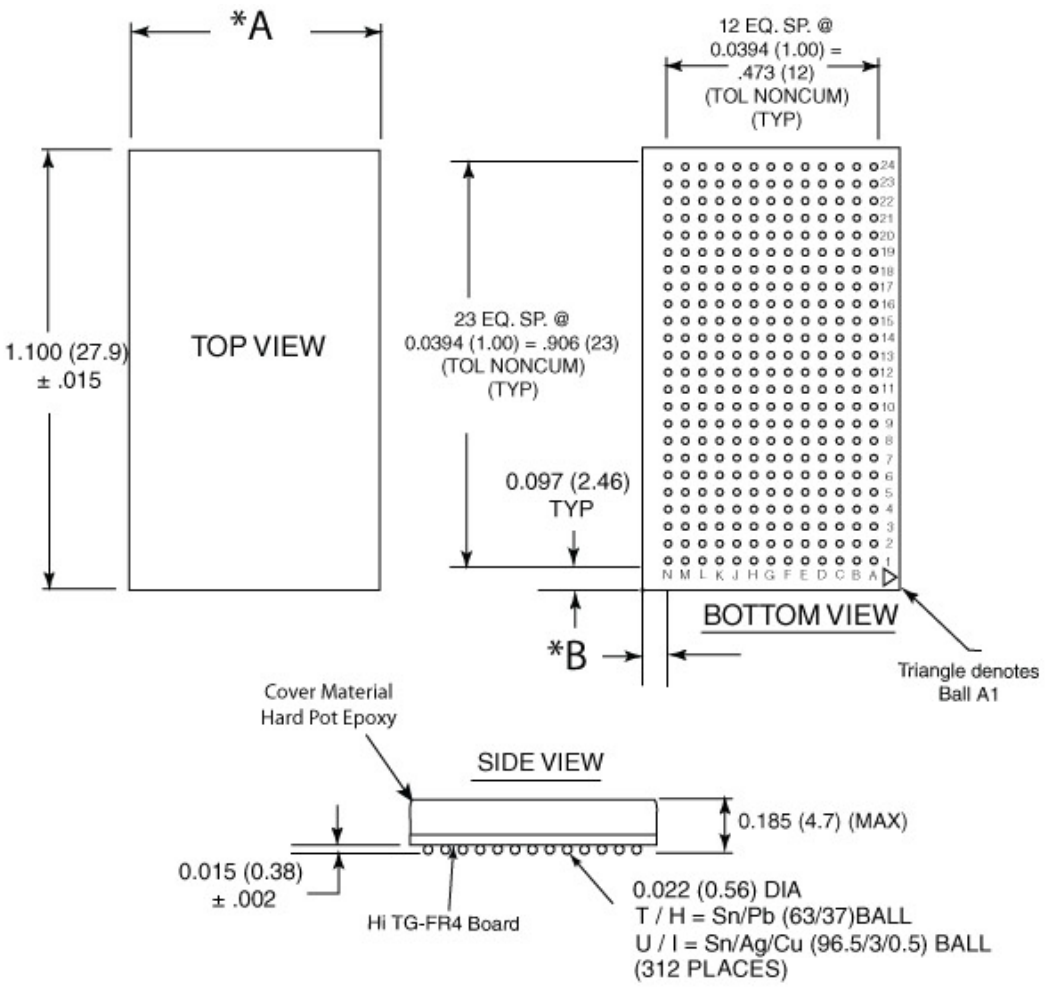
Table 56. Total-ACE With 64K RAM (BU-6486X) All Versions Pinout					
Ball	**Signal**	**Notes**	**Ball**	**Signal**	**Notes**
F24	D10		H24	D00 (LSB)	
J1	NC / CHB_1553-D*$		L1	NC	
J2	NC / CHB_1553-D*$		L2	NC	
J3	NC / CHB_1553-D*$		L3	NC	
J4	NC / CHB_1553-D*$		L4	NC	
J5	NC		L5	NC	
J6	NC		L6	+3.3V_Xcvr	
J7	NC		L7	+3.3V_Xcvr	
J8	NC		L8	GND_Xcvr/Thermal***	
J9	GND_Xcvr/Thermal***		L9	GND_Xcvr/Thermal***	
J10	GND_Xcvr/Thermal***		L10	GND_Xcvr/Thermal***	
J11	GND_Xcvr/Thermal***		L11	GND_Xcvr/Thermal***	
J12	NC		L12	+3.3V_Xcvr	
J13	NC		L13	NC	
J14	MSB / LSB / $\overline{\text{DTGRT}}$		L14	Gnd_Logic	
J15	NC		L15	Gnd_Logic	
J16	TXDATA_IN_B	connect to ball K16	L16	ADDR_LAT / $\overline{\text{MEMOE}}$	
J17	Gnd_Logic		L17	16/ $\overline{8}$ / $\overline{\text{DTREQ}}$	
J18	Gnd_Logic		L18	NC	
J19	Gnd_Logic		L19	NC	
J20	Gnd_Logic		L20	NC	
J21	RTAD4 (MSB)		L21	NC	
J22	RTAD2		L22	Gnd_Logic	
J23	RTADP		L23	Gnd_Logic	
J24	RTAD3		L24	Gnd_Logic	
K1	$\overline{\text{CHB\_1553}}$		M1	GND_Xcvr	
K2	$\overline{\text{CHB\_1553}}$		M2	GND_Xcvr	
K3	$\overline{\text{CHB\_1553}}$		M3	GND_Xcvr	
K4	NC / CHB_1553-D$		M4	NC	
K5	NC		M5	NC	
K6	NC		M6	+3.3V_Xcvr	
K7	NC		M7	+3.3V_Xcvr	
K8	GND_Xcvr/Thermal***		M8	NC	
K9	GND_Xcvr/Thermal***		M9	GND_Xcvr/Thermal***	
K10	GND_Xcvr/Thermal***		M10	GND_Xcvr/Thermal***	
K11	GND_Xcvr/Thermal***		M11	GND_Xcvr/Thermal***	
K12	+3.3V_Xcvr		M12	$\overline{\text{RXDATA\_OUT\_B}}$	connect to ball M13
K13	NC		M13	$\overline{\text{RXDATA\_IN\_B}}$	connect to ball M12
K14	$\overline{\text{SSFLAG}}$ / EXT_TRIG		M14	Gnd_Logic	
K15	NC		M15	Gnd_Logic	
K16	TXDATA_OUT_B	connect to ball J16	M16	+3.3V_Logic	
K17	NC		M17	+3.3V_Logic	
K18	$\overline{\text{TXDATA\_IN\_B}}$	connect to ball K19	M18	TRIG_SEL / $\overline{\text{MEMENA\_IN}}$	
K19	$\overline{\text{TXDATA\_OUT\_B}}$	connecto to ball K18	M19	TXINH_OUT_B	connect to ball M20
K20	NC		M20	TXINH_IN_B	connect to ball M19
K21	RTAD0 (LSB)		M21	NC	
K22	RSTBITEN		M22	Gnd_Logic	
K23	RTAD1		M23	Gnd_Logic	

Table 56. Total-ACE With 64K RAM (BU-6486X) All Versions Pinout					
Ball	**Signal**	**Notes**	**Ball**	**Signal**	**Notes**
K24	RT_AD_LAT		M24	Gnd_Logic	

Table 56. Total-ACE With 64K RAM (BU-6486X) All Versions Pinout		
Ball	**Signal**	**Notes**
N1	GND_Xcvr	
N2	GND_Xcvr	
N3	GND_Xcvr	
N4	NC	
N5	NC	
N6	NC	
N7	NC	
N8	NC	
N9	+3.3V_Xcvr	
N10	NC	
N11	NC	
N12	RXDATA_OUT_B	connect to ball N13
N13	RXDATA_IN_B	connect to ball N12
N14	NC	
N15	NC	
N16	$\overline{\text{ZEROWAIT}}$ / $\overline{\text{MEMWR}}$	
N17	POL_SEL / $\overline{\text{DTACK}}$	
N18	CLOCK_IN	
N19	+3.3V_Logic	
N20	+3.3V_Logic	
N21	NC	
N22	Gnd_Logic	
N23	Gnd_Logic	
N24	Gnd_Logic	

$ - Applicable to the H(I) Version only
***See Thermal Management Section for important user information

Table 57. Total-ACE BU-64843T8-600 (BGA Package) "Daisy Chain" Mechanical Sample Connections				
Ball Pairs Wired Together	**Ball Pairs Wired Together**	**Ball Pairs Wired Together**	**Ball Pairs Wired Together**	**Ball Pairs Wired Together**
A1-A2	D1-D2	G1-G2	K1-K2	N1-N2
A3-A4	D3-D4	G3-G4	K3-K4	N3-N4
A5-A6	D5-D6	G5-G6	K5-K6	N5-N6
A7-A8	D7-D8	G7-G8	K7-K8	N7-N8
A9-A10	D9-D10	G9-G10	K9-K10	N9-N10
A11-A12	D11-D12	G11-G12	K11-K12	N11-N12
A13-A14	D13-D14	G13-G14	K13-K14	N13-N14
A15-A16	D15-D16	G15-G16	K15-K16	N15-N16
A17-A18	D17-D18	G17-G18	K17-K18	N17-N18
A19-A20	D19-D20	G19-G20	K19-K20	N19-N20
A21-A22	D21-D22	G21-G22	K21-K22	N21-N22
A23-A24	D23-D24	G23-G24	K23-K24	N23-N24
B1-B2	E1-E2	H1-H2	L1-L2	
B3-B4	E3-E4	H3-H4	L3-L4	
B5-B6	E5-E6	H5-H6	L5-L6	
B7-B8	E7-E8	H7-H8	L7-L8	
B9-B10	E9-E10	H9-H10	L9-L10	
B11-B12	E11-E12	H11-H12	L11-L10	
B13-B14	E13-E14	H13-H14	L13-L14	
B15-B16	E15-E16	H15-H16	L15-L16	
B17-B18	E17-E18	H17-H18	L17-L18	
B19-B20	E19-E20	H19-H20	L19-L20	
B21-B22	E21-E22	H21-H22	L21-L22	
B23-B24	E23-E24	H23-H24	L23-L24	
C1-C2	F1-F2	J1-J2	M1-M2	
C3-C4	F3-F4	J3-J4	M3-M4	
C5-C6	F5-F6	J5-J6	M5-M6	
C7-C8	F7-F8	J7-J8	M7-M8	
C9-C10	F9-F10	J9-J10	M9-M10	
C11-C12	F11-F12	J11-J12	M11-M12	
C13-C14	F13-F14	J13-J14	M13-M14	
C15-C16	F15-F16	J15-J16	M15-M16	
C17-C18	F17-F18	J17-J18	M17-M18	
C19-C20	F19-F20	J19-J20	M19-M20	
C21-C22	F21-F22	J21-J22	M21-M22	
C33-C24	F23-F24	J23-J24	M23-M24	



Notes:
1) Dimensions are in inches (mm)
2) Cover material: Hard Pot Epoxy
3) Base material: Substrate is Hi TG-FR4, Enig plated 1/2 oz copper
4) Solder Ball Cluster to be centralized within ±.010 of outline dimensions
5) Solder ball is 0.022". Substrate pads are 0.030" copper that are Solder mask defined to 0.022". Solder ball after reflow has a height of 0.015" and Diameter of 0.028".

*DIMENSIONAL INFORMATION		
PART NUMBER	A	B
BU-648x3T(U)8	0.600 (15.2) ± .015	0.064 (1.63) TYP
BU-648x3H(I)8	0.700 (17.8) ± .015	0.114 (2.89) TYP

Figure 19. Mechanical Outline Drawing for Total-ACE BGA Packages

9 ORDERING INFORMATION

BU-648X 3 T 8-E 0 2

Test Criteria:
2 = MIL-STD-1760 Amplitude

Process Requirements:
0 = Standard DDC practices, no Burn-In

Environmental Temperature Options:
E = -40°C to +100°C (Note 2)
1= -55°C to +125°C (Notes 2, 3)

Voltage/Transceiver Option:
8 = *3.3 Volts rise/fall times = 100 to 300 ns (1553B)

Package Type:
T = 63 Sn/ 37 Pb Solder Ball
(transformer coupled)
U = 96.5 Sn/ 3 Ag/ 0.5 Cu – Pb-Free Solder Ball
(transformer coupled)
H = 63 Sn/ 37 Pb Solder Ball
(transformer & direct coupled)
I = 96.5 Sn/ 3 Ag/ 0.5 Cu – Pb-Free Solder Ball
(transformer & direct coupled)

Logic / RAM Voltage:
3 = 3.3 Volt Logic/RAM

Product Type (see Product Matrix below):
BU-6484 = BC/RT/MT with 4K x 16 RAM
BU-6486 = BC/RT/MT with 64K x 17 RAM

Notes:
1. See Application Note AN/B-37 for SSRT implemenration option if using BU-64843X (BC/RT/MT) with 4K x 16 RAM, available on the DDC website
2. Temperature Range applies to case temperature
3. See section 8.10 for thermal management requirements at high transmit duty cycles.
4. See Total-ACE Product Matrix below for valid ordering options
5. Unless otherwise specified, these products contain tin lead solder

Standard DDC Processing for BGA Products		
Test	**MIL-STD-883**	
	Method(s)	**Condition(s)**
Inspection	2010, 2017, and 2032	—
Temperature Cycle	1010	B

Total-ACE Product Matrix						
Part Number	**Transformer Coupled**	**Transformer & Direct Coupled**	**Logic Voltage**	**Memory**	**Ram Voltage**	**Transceiver Voltage**
BU-64843T(U)8-E02	✔		3.3V	4K x 16	3.3V	3.3V
BU-64843H(I)8-E02		✔	3.3V	4K x 16	3.3V	3.3V
BU-64863T(U)8-E02	✔		3.3V	64K x 17	3.3V	3.3V
BU-64863H(I)8-E02		✔	3.3V	64K x 17	3.3V	3.3V
BU-64843T(U)8-102	✔		3.3V	4K x 16	3.3V	3.3V
BU-64843H(I)8-102		✔	3.3V	4K x 16	3.3V	3.3V
BU-64863T(U)8-102	✔		3.3V	64K x 17	3.3V	3.3V
BU-64863H(I)8-102		✔	3.3V	64K x 17	3.3V	3.3V

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