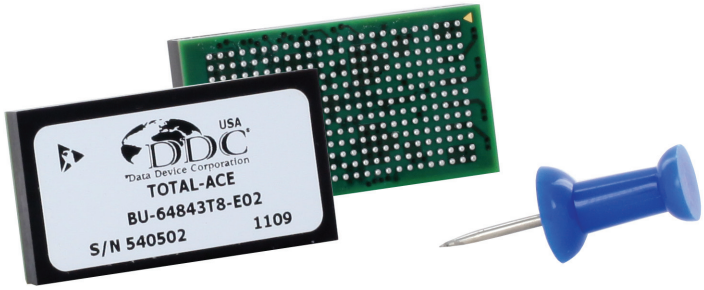
PCI Total-ACE®
Complete MIL-STD-1553 Solution

Data Sheet

Model: BU-658X3T/U/H/i8



Save board space and simplify your 1553 design and layout with the world's first fully integrated MIL-STD-1553 component, complete with 1553 protocol, memory, transceivers, and isolation transformers—all in one small plastic BGA package with direct and/or transformer coupled 1553 connections inside

Applications

- Mission Computers
- Digital Data Recorders
- LRU's
- Displays
- Radios/Modems
- Radar Systems/Situational Awareness
- Ground Vehicles
- Commercial Aerospace

Custom Design Capability - DDC can customize designs for all cards, ranging from simple modifications of standard products to fully customized solutions for commercial, military, aerospace, and industrial applications.

For more information: www.ddc-web.com/BU-64843T

DDC's Data Networking Solutions

MIL-STD-1553 | ARINC 429 | Fibre Channel

As the leading global supplier of data bus components, cards, and software solutions for the military, commercial, and aerospace markets, DDC's data bus networking solutions encompass the full range of data interface protocols from MIL-STD-1553 and ARINC 429 to USB, and Fibre Channel, for applications utilizing a spectrum of form-factors including PMC, PCI, Compact PCI, PC/104, ISA, and VME/VXI.

DDC has developed its line of high-speed Fibre Channel and Extended 1553 products to support the real-time processing of field-critical data networking netween sensors, compute notes, data storage displays, and weapons for air, sea, and ground military vehicles.

Whether employed in increased bandwidth, high-speed serial communications, or traditional avionics and ground support applications, DDC's data solutions fufill the expanse of military requirements including reliability, determinism, low CPU utilization, real-time performance, and ruggedness within harsh environments. Out use of in-house intellectual property ensures superior mutli-generational support, independent of the life cycles of commercial devices. Moreover, we maintain software compatibility between product generations to protect our customers' investments in software development, system testing, and end-product qualification.

MIL-STD-1553

DDC provides an assortment of quality MIL-STD-1553 commercial, military, and COTS grade cards and components to meet your data conversion and data interface needs. DDC supplies MIL-STD-1553 board level products in a variety of form factors including AMC, USB, PCI, cPCI, PCI-104, PCMCIA, PMC, PC/104, PC/104-Plus, VME/VXI, and ISAbus cards. Our 1553 data bus board solutions are integral elements of military, aerospace, and industrial applications. Our extensive line of military and space grade components provide MIL-STD-1553 interface solutions for microprocessors, PCI buses, and simple systems. Our 1553 data bus solutions are designed into a global network of aircraft, helicopter, and missle programs.

ARINC 429

DDC also has a wide assortment of quality ARINC-429 commercial, military, and COTS grade cards and components, which will meet your data conversion and data interface needs. DDC supplies ARINC-429 board level products in a variety of form factors including AMC, USB, PCI, PMC, PCI-104, PC/104 Plus, and PCMCIA boards. DDC's ARINC 429 components ensure the accurate and reliable transfer of flight-critical data. Our 429 interfaces support data bus development, validation, and the transfer of flight-critical data aboard commercial aerospace platforms.

Fibre Channel

DDC has developed its line of high-speed Fibre Channel network access controllers and switches to support the real-time processing demands of field-critical data networking between sensors, computer nodes, data storage, displays, and weapons, for air, sea, and ground military vehicles. Fibre Channel's architecture is optimized to meet the performance,reliability, and demanding environmental requirements of embedded, real time, military applications, and designed to endure the multi-decade life cycle demands of military/aerospace programs.

PCI TOTAL-ACE™ COMPLETE MIL-STD-1553 SOLUTION

BU-65843X/65863X DATA SHEET

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Revision	Date	Pages	Description
A	6/2010	All	Initial Release
B	9/2010	49, 55, 56, 58	Ball B20 and H10 were changed from “NC” to “GND” in order to improve the noise immunity.
C	11/2010	4	renaming from “SOLDERING” to “SOLDERING/MOUNTING” and below the information on reflow temperatures included the following Refer to DDC’s Application Note #A/N49 “BGA User’s Guide” for additional important mounting information.
D	11/2011	All	Updated to new format. Updates to Tables 1, 65, 70, and 74.
E	7/2012	All	Added the T/U package information.
F	4/2013	3, 6, 7, 10 -12, 93 – 19, 111	Added Mil Temp Option, Updated Table 1, Section 8.7, Figures 21, and Order Info.

1 PREFACE

This data sheet uses typographical conventions to assist the reader in understanding the content. This section will define the text formatting used in the rest of the data sheet.

1.1 Text Usage

- **BOLD**–indicates important information and table, figure, and chapter references.
- ***BOLD ITALIC***–designates DDC Part Numbers.
- `Courier New`–indicates code examples.
- <…> - indicates user-entered text or commands.

1.2 Special Handling and Cautions

Warnings: Turn off power to the computer hardware and unplug from wall.

Ensure that standard ESD precautions are followed. As a minimum, one hand should be grounded to the power supply in order to equalize the static potential.

Do not store disks in environments exposed to excessive heat, magnetic fields or radiation.

1.3 Trademarks

All trademarks are the property of their respective owners.

1.4 What is included in this data sheet?

This data sheet contains a complete description of component.

1.5 Technical Support

In the event that problems arise beyond the scope of this data sheet, you can contact DDC by the following:

US Toll Free Technical Support:
1-800-DDC-5757, ext. 7771

Outside of the US Technical Support:
1-631-567-5600, ext. 7771

Fax:
1-631-567-5758 to the attention of DATA BUS Applications

DDC Website:
www.ddc-web.com/ContactUs/TechSupport.aspx

Please note that the latest revisions of Software and Documentation are available for download at DDC's Web Site, www.ddc-web.com.

2 OVERVIEW

The PCI Total-ACE is a complete and compact solution to MILSTD-1553 applications. With a footprint of just 0.7 inches by 1.10 inches, it is the world's first, fully integrated PCI MIL-STD-1553 terminal and transformer combined into a single BGA package. The required isolation transformers (with both "Transformer Coupled" and "Direct Coupled" output ratios) are integrated within the plastic BGA package, and the device is powered entirely by +3.3 volts.

Ideal for military temperature range applications where PC board space is at a premium, the PCI Total-ACE is available in a 312-ball (24 x 13 matrix) BGA package, and is rated for -55°C to +125°C operation at case. The PCI Total-ACE integrates dual transceivers, dual transformers, protocol engine and either 4K or 64K words of internal RAM and provides a complete interface between a PCI host processor (32-Bit/33Mhz 3.3V-only signaling) and a MIL-STD-1553 bus. The PCI Total-ACE is software compatible with PCI Mini-ACE MARK3, PCI Micro-ACE-TE, and architecturally compatible with Enhanced Mini-ACE MARK3, Enhanced Mini-ACE, Mini-ACE and ACE Generations. The PCI interface is not 5V tolerant.

Advanced architecture is the key to the PCI Total-ACE series' high performance. The advanced bus controller architecture gives the PCI Total-ACE a high degree of flexibility and autonomy. This creates advantages in a number of areas: improving message scheduling control, minimizing host overhead for asynchronous message insertion, facilitating bulk data transfers and double buffering, message retry and bus switching strategies, and data logging and fault reporting.

The PCI Total-ACE, RT mode offers single and circular subaddress buffering schemes, along with a global circular buffering option, 50% rollover interrupt for circular buffers, and an interrupt status queue. This RT architecture provides flexibility in meeting all common MILSTD-1553 protocols. Available RT data buffering and interrupt options offer support for synchronous and asynchronous messaging, ensure data sample consistency, and support bulk data transfers.

2.1 Features

- Both “Transformer Coupled” and “Direct Coupled” Output Ratio Available
- 32-Bit/33MHz, 3.3 Volt, PCI Targe Interface
- World’s First, Fully Integrated, MIL-STD-1553 Terminal and Transformer Solution
- Small Package 312 Ball BGA (1.1 in x 0.7 in)
- Compatible with PCI Mini-ACE Mark3, PCI Micro-ACE-TE, Enhanced Mini-ACE Mark3, Enhanced Mini-ACE, Mini-ACE, and ACE Generations
- Military Temperature Range: -55°C to +125°C

- DO-254 Certifiable
- +3.3 Volt Only
- 4K x 16 or 64K x 17 RAM
- 0.185” Max Height
- Fully Integrated MIL-STD-1553A/B Notice 2, MIL-STD-1760
- Highly Autonomous BC Architecture
- Built-In Message Sequence Controller with 20-Instruction Set
- Advanced RT Buffering
    - Global Circular Buffering
    - Interrupt Status Queue
    - 50% Circular Buffer Rollover Interrupts
- Selective Message Monitor with Filtering
- 50% Rollover Interrupts for Stacks and Circular Buffers
- Option for RT-Only Operation for Safety-Critical Applications

- **Applications Include:**
- Mission Computers
- Digital Data Recorders
- LRU’s
- Radios/Modems
- Displays
- Ground Vehicles
- Commercial Aerospace
- Radar Systems/Situational Awareness

Figure 1. BU-658X3X PCI Total-ACE

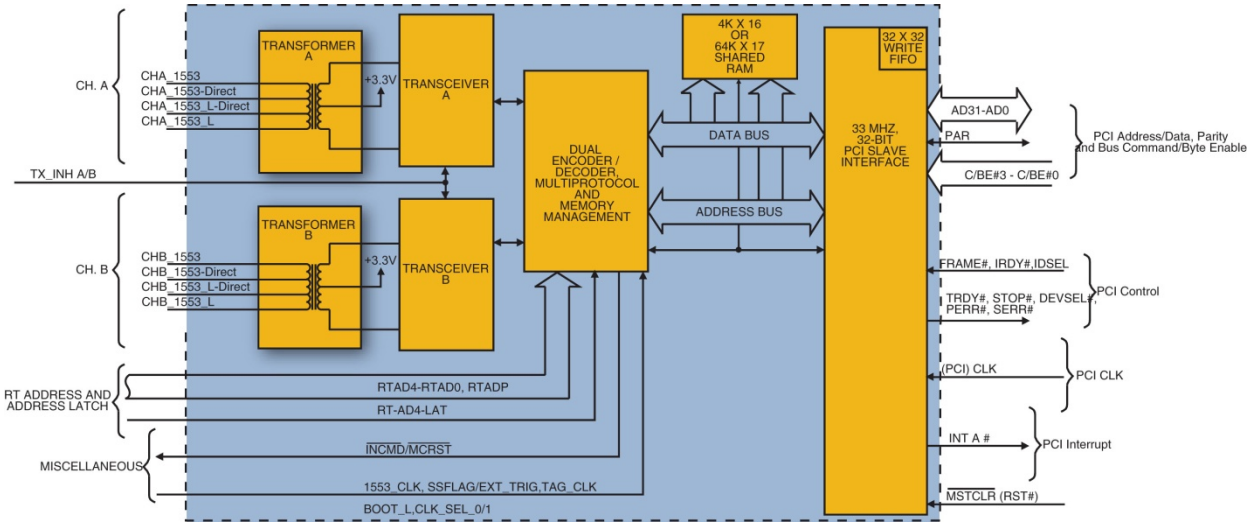


Figure 2. BU-65843X PCI Total-ACE Architecture

Table 1. BU-658X3X Specification Table				
PARAMETER	**MIN**	**TYP**	**MAX**	**UNITS**
ABSOLUTE MAXIMUM RATING				
Supply Voltage (Note 11)				
• Logic +3.3 V	-0.3		4.0	V
• Transceivers +3.3V (not during transmit)	-0.3		6.0	V
• Transceivers +3.3V (during transmit)	-0.3		4.5	V
Logic				
• Voltage Input Range	-0.3		Vdd+0.3	V
• Voltage Input Range, +5V Tolerant Pins (Note 15)	-0.3		6.0	V
POWER SUPPLY REQUIREMENTS				
Voltages/Tolerances (Note 11)				
• Logic +3.3V	3.00	3.3	3.60	V
• Transceivers +3.3V	3.14	3.3	3.46	V
Current Drain(Total Hybrid) (Note 13)				
BU-65863H(i)8-E02 Rev A				
• Idle		70	101	mA
• 25% Transmitter Duty Cycle		245	297	mA
• 50% Transmitter Duty Cycle		420	508	mA
• 100% Transmitter Duty Cycle		769	923	mA
BU-65843H(i)8-E02 Rev A				
• Idle		68	98	mA
• 25% Transmitter Duty Cycle		243	294	mA
• 50% Transmitter Duty Cycle		418	505	mA
• 100% Transmitter Duty Cycle		767	920	mA
BU-65843H(i)8-E02 Rev B, BU-65843H(i)8-102, BU-65843T(U)8-XX2				
• Idle		38	54	mA
• 25% Transmitter Duty Cycle		185	204	mA
• 50% Transmitter Duty Cycle		357	369	mA
• 100% Transmitter Duty Cycle		676	692	mA
BU-65863H(i)8-E02 Rev B, BU-65863H(i)8-102, BU-65863T(U)8-XX2				
• Idle		40	57	mA
• 25% Transmitter Duty Cycle		187	207	mA
• 50% Transmitter Duty Cycle		359	372	mA
• 100% Transmitter Duty Cycle		678	695	mA

Table 1. BU-658X3X Specification Table				
PARAMETER	**MIN**	**TYP**	**MAX**	**UNITS**
POWER DISSIPATION				
TOTAL HYBRID(Note 13 & 14)				
BU-65863H(i)8-E02 Rev A				
• Idle		.231	.334	W
• 25% Transmitter Duty Cycle		.513	.684	W
• 50% Transmitter Duty Cycle		.795	1.084	W
• 100% Transmitter Duty Cycle		1.355	1.862	W
BU-65843H(i)8-E02 Rev A				
• Idle		.224	.324	W
• 25% Transmitter Duty Cycle		.506	.676	W
• 50% Transmitter Duty Cycle		.788	1.076	W
• 100% Transmitter Duty Cycle		1.348	1.854	W
BU-65843H(i)8-E02 Rev B, BU-65843H(i)8-102, BU-65843T(U)8-XX2				
• Idle		.080	.204	W
• 25% Transmitter Duty Cycle		.230	.316	W
• 50% Transmitter Duty Cycle		.270	.369	W
• 100% Transmitter Duty Cycle		.460	.664	W
BU-65863H(i)8-E02 Rev B, BU-65863H(i)8-102, BU-65863T(U)-XX2				
• Idle		.134	.217	W
• 25% Transmitter Duty Cycle		.239	.307	W
• 50% Transmitter Duty Cycle		.355	.477	W
• 100% Transmitter Duty Cycle		.491	.655	W
ACTIVE TRANSCEIVER (HOTTEST DIE)				
BU-658X3H(i)8-E02 Rev A				
• 100% Transmitter Duty Cycle		1.122	1.519	W
BU-65863H(i)8-E02 Rev B, BU-658X3H(i)8-102, BU-658X3T(U)8-XX2				
• 100% Transmitter Duty Cycle		0.420	0.540	W
RECEIVER				
Differential Input Impedance (Note 1 – 6)				
• +3.3V Transformer Coupled	1.0			kΩ
• +3.3V Direct Coupled	2.0			kΩ
Threshold Voltage, Transformer Coupled, Measured on Stub	0.200		0.860	Vp-p
Threshold Voltage, Direct Coupled, Measured on Stub	0.280		1.20	Vp-p
Common-Mode Voltage			±10	Vpeak

Table 1. BU-658X3X Specification Table				
PARAMETER	**MIN**	**TYP**	**MAX**	**UNITS**
TRANSMITTER				
Differential Output Voltage				
• Direct Coupled Across 35Ω, Measured on Bus	6	7.2	9.0	Vp-p
• Transformer Coupled Across 70Ω, Measured on Bus (Note 12)	20	21.5	27	Vp-p
Output Noise, Differential			14	mVRMS
Output Offset Voltage, Transfomer Coupled Across 70Ω	-250		250	mVp
Rise/Fall Time	100	150	300	nsec
LOGIC				
V_{IH}				
All signals except PCI	2.1			V
V_{IL}				
All signals except PCI			0.7	V
Schmidt Hysteresis				
All signals except PCI	0.4			V
I_{IH}, I_{IL}				
All signrals except PCI				
I_{IH} (V_{cc} = 3.6V, V_{IN} = V_{cc})	-10		10	µA
I_{IH} (V_{cc} = 3.6V, V_{IN} = 2.7V)	-100		-33	µA
I_{IL} (V_{cc} = 3.6V, V_{IN} = 0.0V)	-340		-33	µA
V_{OH} (V_{CC} = 3.0V, I_{OH} = max	2.4			V
V_{OL} (V_{CC} = 3.0V, I_{OH} = max			0.4	V
IOL	3.4			mA
IOH			-3.4	mA
CI (Input Capacitance)			20	pF
PCI LOGIC see PCI spec 3.3V signaling environment				
CI (Input Capacitance) all PCI except PCI_CLK & IDSEL			10	pF
CI (Input Capacitance) PCI_CLK			4	pF
CI (Input Capacitance) IDSEL			6	pF

Table 1. BU-658X3X Specification Table				
PARAMETER	**MIN**	**TYP**	**MAX**	**UNITS**
CLOCK INPUT				
PCI Clock Input Frequency			33.3	MHz
Frequency:				
• Nominal Values				
- Default Mode		16.0		MHz
- Option		12.0		MHz
- Option		10.0		MHz
- Option		20.0		MHz
Long Term Tolerance				
• 1553A Compliance	-0.01		0.01	%
• 1553B Compliance	-0.10		0.10	%
Short Term Tolerance, 1 second				
• 1553A Compliance	-0.001		0.001	%
• 1553B Compliance	-0.01		0.01	%
15553 MESSAGE TIMING				
Completion of CPU Write (BC Start)-to-Start of First Message for Non-enhanced BC Mode	2.5			µs
BC Intermessage Gap (Note 7)				
• Non-enhanced Mini-ACE compatible) BC mode		9.5		µs
• Enhanced BC mode (Note 8)		10 to 10.5		µs
BC/RT/MT Response Timeout (Note 9)				
• 18.5 nominal	17.5	18.0	19.5	µs
• 22.5 nominal	21.5	22.5	23.5	µs
• 50.5 nominal	49.5	50.5	51.5	µs
• 128.0 nominal	127	129.5	131	µs
RT Response Time (mid-parity to mid-sync) (Note 10)	4		7	µs
Transmitter Watchdog Timeout		660.5		µs

Table 1. BU-658X3X Specification Table				
PARAMETER	**MIN**	**TYP**	**MAX**	**UNITS**
THERMAL				
TOTAL-ACE BGA				
312-ball BGA Package				
(See Thermal Management section)				
Active Transceiver (Hottest Die)				
BU-658X3T/U8 Transformer Coupled Single-Tap Versions				
• Junction-to-Ambient (θ_{JA} via simulation)				
- Per JESD 51-2 standard at 25°C				
θ_{JA} in Still Air		37.7		°C/W
- Per JESD 51-6 standard at 25°C				
θ_{JA} @1M/S		30.5		°C/W
θ_{JA} @2M/S		28.3		°C/W
θ_{JA} @3M/S		27.2		°C/W
• Junction-to-Case (θ_{JC} via simulation)				
- Per JESD 51-12 standard at 25°C				
θ_{JC}		18.9		°C/W
• Junction-to-Board (θ_{JB} via simulation)				
- Per JESD 51-2 standard at 25°C				°C/W
θ_{JB}		25.4		
BU-658X3H/i8 Direct &Transformer Coupled Dual-Tap Versions				
• Junction-to-Ambient (θ_{JA} via simulation)				
- Per JESD 51-2 standard at 25°C				
θ_{JA} in Still Air		37.8		°C/W
- Per JESD 51-6 standard at 25°C				
θ_{JA} @1M/S		31.4		°C/W
θ_{JA} @2M/S		29.8		°C/W
θ_{JA} @3M/S		29.0		°C/W
• Junction-to-Case (θ_{JC} via simulation)				
- Per JESD 51-12 standard at 25°C				
θ_{JC}		26.2		°C/W
• Junction-to-Board (θ_{JB} via simulation)				
- Per JESD 51-2 standard at 25°C				
θ_{JB}		26.5		°C/W
ALL PACKAGES				
Operating Case Temperature				
- EXX	-40		+100	°C
- 1XX (Note16)	-55		+125	°C
Operating Junction Temperature				
- Transceiver	-55		+125	°C
- Protocol	-55		+125	°C
- Memory	-55		+125	°C
Storage Temperature	-65		+150	°C

Table 1. BU-658X3X Specification Table				
PARAMETER	**MIN**	**TYP**	**MAX**	**UNITS**
SOLDERING/MOUNTING **312-BALL BGA PACKAGE** The reflow profile detailed in IPC/JEDEC J-STD-020 is applicable for both leaded and lead-free products (Refer to DDC's Application Note #A/N-49 "BGA User's Guide" for additional important mounting information.)				
PHYSICAL CHARACTERISTICS Package Body Size 312-ball BA • BU-64843T(U)8 • BU-648x3H(i)8 Total-ACE • Moisture Sensitivity Level • Electrostatic Discharge Sensitivity Weight 312-ball BGA		1.100 x 0.600 x 0.185 (27.9 x 15.2 x 4.7) 1.100 x 0.700 x 0.185 (27.9 x 17.8 x 4.7) MSL-3 ESD Class 0 0.167 (4.8)		 in. (mm) in. (mm) oz. (g)

Table 1. BU-658X3X Specification Table				
PARAMETER	**MIN**	**TYP**	**MAX**	**UNITS**

Table 1 Notes:

(Notes 1 through 6 are applicable to the Receiver Differential Input Impedance specification)

1. Specifications include contributions from the transformer, transmitter, and receiver.
2. Impedance parameters are specified directly between pins CHA(B)_1553 and $\overline{\text{CHA(B)\_1553}}$, and CHA(B)_1553-Direct and $\overline{\text{CHA(B)\_1553-Direct}}$ of the PCI Total-ACE hybrid.
3. It is assumed that all power and ground inputs to the hybrid are conntected.
4. The specifications are applicable for both unpowered and powered conditions.
5. The specifications assume a 2 volt rms balanced, differential, sinusoidal input. The applicable frequency range is 75kHz to 1 MHz.
6. Minimum resistance and maximum capacitance parameters are guaranteed over the operating range, but are not tested.
7. Typical value for minimum intermessage gap time. Under software control, this may be lengthened (to 65.535 ms – message time) in increments of 1 µs. If ENHANCED CPU ACCESS, bit 14 of Configuration Register #6, is set to logic “1”, then host accesses during BC Start-of-Message (SOM) and End-of-Message (EOM) transfer sequences could have effect of lengthening the intermessage gap time. For each host access during an SOM or EOM sequence, the intermessage gap time will be lengthened by 6 clock cycles. Since there are 7 internal transfers during SOM and 5 during EOM, this could theoretically lengthen the intermessage gap by up to 72 clock cycles; i.e., up to 7.2 ms with a 10 MHz clock, 6.0 µs with a 12 MHz clock, 4.5 µs with a 16 MHz clock, or 3.6 µs with a 20 MHz clock.
8. For Enhanced BC mode, the typical value for intermessage gap time is approximately 10 clock cycles longer that for the non-enhanced BC mode. That is, an addition of 1.0 µsat 10 MHz, 833 ns at 12 MHz, 625 ns at 16 MHz, or 500 ns at 20 MHz.
9. Software programmable (4 options). Includes RT-to-RT Timeout (measured mid-parity of transmit Command Word to mid-sync of transmitting RT Status Word).
10. Measured from mid-parity crossing of Command Word to mid-sync crossing of RT’s Status Word.
11. External 10 µF tantalum and 0.1 µF capacitors should be located as close as possible to the voltage input pins/balls.
12. MIL-STD-1760 requires a 20 Vp-p minimum output on the stub connection.
13. Current drain and power dissipation specs are preliminary and subject to change.
14. Power Dissipation is the input power minus the power delivered to the 1553 fault isolation resistors, the power delivered to the bus termination resistors, and the copper losses in the bus coupling transformer. An illusion of external power dissipation for transformer coupled configuration (while transmitting) is: 0.057 watts for the active bus coupling transformer, 0.422 watts for each of the two bus isolation resistors and 0.141 watts for each of the two bus termination resistors.
15. The 5V tolerant pins are RTAD0-5, RTAD_PAR, RTAD_LAT, TXINH_A/B, $\overline{\text{SSFLAG}}$ /EXT_TRIG, TAG_CLK, RTBOOT_L, CLK_SEL_0, and CLK_SEL_1.
16. See section 8.7 for thermal management requirements at high transmit duty cycles.

3 INTRODUCTION

The PCI Total-ACE is the industry's smallest, fully integrated, PCI MIL-STD-1553 terminal & transformer solution, enabling its use in applications where PC board space is at a premium. The BU-65863H BC/RT/MT fully integrated terminal comprises a complete interface between a PCI host processor (32-Bit/33Mhz, 3.3V-only signaling) and a MIL-STD-1553 bus. The PCI Total-ACE is available in a 1.100 x 0.700 inch, plastic 312-ball BGA. The PCI Total-ACE is software compatible with PCI Mini-ACE MARK3, PCI Micro-ACE-TE, and architecturally compatible with Enhanced Mini-ACE MARK3, Enhanced Mini-ACE, Mini-ACE and ACE Generations. The PCI interface is not 5V tolerant.

The PCI Total-ACE provides complete multiprotocol support of MIL-STD-1553A/B/McAir and STANAG 3838. A BU-65863H integrates a dual transceiver; along with protocol, host interface, memory management logic, transformer and direct coupled ratio isolation transformers; and 4K or 64K words of internal RAM with built-in parity checking.

The PCI Total-ACE incorporates +3.3 volt, MIL-STD-1760 trimmed voltage source transceivers with improved line driving capability. To provide further flexibility, the PCI Total-ACE has internal 1553 master clock dividers that allow operation with a choice of 10, 12, 16, or 20 MHz clock inputs. The 1553 master clock divider is software programmable or can be controlled via pins when the RTBoot mode is strapped.

The PCI Total-ACE is a fully compliant target, as defined by the PCI Local Bus Specification Revision 2.2, using a 32 bit interface that operates at clock speeds of up to 33 MHz, from a 3.3V bus. The interface supports PCI interrupts and contains a FIFO that handles PCI burst write transfer cycles. The FIFO is deep enough to accept an entire 1553 message. The PCI interface is NOT 5V tolerant and cannot be used in a 5V PCI signaling environment.

One of the salient features of the PCI Total-ACE is its Enhanced Bus Controller architecture. The Enhanced BC's highly autonomous message sequence control engine provides a means for offloading the host processor for implementing multi-frame message scheduling, message retry schemes, data double buffering, and asynchronous message insertion. For the purpose of performing messaging to the host processor, the Enhanced BC mode includes a General Purpose Queue, along with user-defined interrupts.

The PCI Total-ACE (in RT mode) offers the same choices of single and circular buffering for individual subaddresses as ACE, Mini-ACE(Plus), Enhanced Mini-ACE, and Enhanced Mini-ACE MARK3. New enhancements to the RT architecture include a global circular buffering option for multiple (or all) receive subaddresses, a 50% rollover interrupt for circular buffers, an interrupt status queue for logging up to 32 interrupt events, and an option to automatically initialize to RT mode with the Busy bit

set. The interrupt status queue and 50% rollover interrupt features are also included as improvements to the PCI Total-ACE Monitor architecture.

The PCI Total-ACE terminal operates over the temperature range of -40 to +100°C (case) and is ideal for industrial processor-to-1553 applications powered by 3.3 volts only.

3.1 Supporting Documentation

Enhanced Miniature Advanced Communications Engine
(Enhanced Mini-ACE® Series) Users Guide MN-6186X-001
Volume 1 – Architectural Reference

Enhanced Miniature Advanced Communications Engine
(Enhanced Mini-ACE® Series) User's Guide MN-6186X-002
Volume 2 – Hardware Reference

PCI Enhanced Mini-ACE Supplement to
Enhanced Mini-ACE User Guide

Enhanced Miniature Advanced Communications Engine
(Enhanced Mini-ACE® Series) MN-6186X-004
Reliability Reports

Enhanced Miniature Advanced Communications Engine
(Enhanced Mini-ACE® Series) MN-6186X-005
Test Evaluation Data

3.2 TEST COMPONENTS

Daisy chain mechanical samples of the PCI Total-ACE, 312-ball BGA (BU-64843T8-600) are available. These are used to verify both the electrical and mechanical integrity of the solder joints between the BGA package and the board. Ball pairs are internally wired so that the user can test for electrical continuity between balls. Refer to TABLE 76 for interconnection details.

Although these units are inert, they are fully populated with silicon die and isolation transformers so that they closely match the thermal and mechanical characteristics of standard production units. Internal daisy chain interconnections are made by copper PWB traces.

3.3 TRANSCEIVERLESS "COMPATIBLE" VERSION OF PCI TOTAL-ACE

All versions of the PCI Total-ACE, 312-ball BGA are transceiverless "Compatible". These devices contain fully functional, dualredundant, MIL-STD-1553 transceivers with internal / intermediate connections brought out to balls. These intermediate connections allow devices to be used in transceiverless mode for direct interfacing to MIL-STD-1773 (fiber optic) transceivers. Mandatory Additional Connections (See TABLE 67) are required when these devices are not utilized in transceiverless mode.

3.4 TRANSCEIVERS

The transceivers in PCI Total-ACE series terminals are fully monolithic, requiring only +3.3 power input. The transmitters are voltage sources, providing improved line driving capability over current sources. This serves to improve performance on long buses with many taps. PCI Total-ACE transmitters natively satisfy the MIL-STD-1760 requirement for a minimum of 20 volts peakto-peak, transformer coupled output.

Besides eliminating the demand for an additional power supply, the use of +3.3 volt only transceivers requires the use of a built-in step-up, rather than a step-down, isolation transformer. This provides the advantage of a higher terminal input impedance than is possible for a 15V, 12V or 5V transmitter. As a result, there is a greater margin for the input impedance test, mandated as part of 1553 validation test. This allows for longer cable lengths between a system connector and the isolation transformers of an embedded 1553 terminal.

The receiver sections of the PCI Total-ACE are fully compliant with MIL-STD-1553B Notice 2 in terms of front end overvoltage protection, threshold, common-mode rejection, and word error rate.

3.5 BUILT-IN ISOLATION TRANSFORMERS

The PCI Total-ACE incorporates two DSS-3333 isolation transformers with both transformer and direct coupled ratios (1:2.70 & 1:3.75) from BETA Transformer Technology Corporation.

General specifications for DSS-3333 isolation transformers are available at http://www.bttc-beta.com/ in the "DSS-3000 SERIES" transformer data sheet.

3.6 PCI Register and Memory Addressing

The PCI Interface contains a set of "Type 00h" PCI configuration registers that are used to map the device into the host system. There are two Base Address Registers that are used to implement ACE memory space (BAR0) and register space (BAR1).

The PCI configuration register space is mapped in accordance with PCI revision 2.2 specifications.

The PCI Total-ACE acts as a target and responds to the following PCI commands:

Table 2. PCI Target Command Codes

Command Type	Code (C/BE[3:0]#)
Memory Read	0110 (6h)
Memory Write	0111 (7h)
Configuration Read	1010 (Ah)
Configuration Write	1011 (Bh)
Memory Read Multiple	1100 (Ch)
Memory Read Line	1110 (Eh)
Memory Write & Invalidate	1111 (Fh)

The PCI Total-ACE does **not** implement the Memory Read Multiple, Memory Read Line or Memory Write and Invalidate commands. However, in accordance with PCI rules, the PCI Total-ACE will accept these requests and alias them to the basic memory commands. For example, Memory Read Multiple and Memory Read Line commands will be accepted and treated as Memory Read commands. Similarly, the PCI Total-ACE will accept a memory Write and Invalidate command and treat it as a Memory Write command.

ACE memory is accessed internally in 16-bit words, but memory is accessed sequentially allowing for 32-bits of data to be read from the PCI bus. In other words, if a 32-bit PCI read is requested the first 16 bits of data would be read from the requested internal address, the next 16 bits of data would be read from the initial internal address + 1, and then the resulting 32-bit double word would be transferred to the PCI bus. The PCI Total-ACE supports 32-bit and 16-bit read and write operations, 8 bit reads will return 16 bit data, and 8 bit writes are illegal and will cause targetaborts.

Table 3. Configuration Register Space for the PCI Total-ACE				
Address	**31 24**	**23 16**	**15 8**	**7 0**
00h	Device ID		Vendor ID	
	04h	0Xh (X varies with part #, see text)	DDC Manufacturer Device ID value (4DDCH)	
04h	Status Register		Command Register	
08h	Class Code = 078000h			REV ID = 02h
0Ch	BIST 00h	Header Type 00h	Latency Timer 00h	Cache Line Size 00h
10h	Base Address Register 0 (for ACE memory)			
	R/W	R/W and 0's (see text)	00h	00h
14h	Base Address Register 1 (for Ace registers)			
	R/W	R/W	R/W and 0's (see text)	00h
18h – 24h	Base Address Registers 2 through 5 (not used) 00000000h			
28h	Card Bus CIS pointer (not used) 00000000h			
2Ch	Subsystem Device and Subsystem Vendor ID Same as Configuration Register 0, Alias Reads to Configuration Register 00			
30h	Expansion ROM Base Address (not Used, bit = 0)			
34h – 38h	Reserved			
3Ch	Max Lat 00h	Min Gnt 00h	Interrupt Pin 01h	Interrupt Line R/W

The ACE register mapping is located in PCI memory space. Although the PCI Total-ACE can be accessed in 32-bit words, all ACE registers are accessed in 16 bit word reads / writes. If a 32-bit read is performed from the PCI bus in ACE register space only the first 16 bits of data are valid.

This data sheet will only describe the PCI registers that are specific to configuring the integrated terminal and shared RAM. For specifics or definitions on other PCI bus configuration registers, please see the PCI Local Bus specification revision 2.2.

Vendor ID field contains the vendor's ID configuration register. Data Device Corporation's ID code is 4DDCh.

Device ID field is used to indicate the device being used. This field is configured by DDC to reflect the part value of the device. The following TABLE 4 represents all possible combinations for the Device ID field:

Table 4. Device ID Field Mapping	
Device ID	**Description**
0400h	BC/RT/MT with 4K of RAM (BU-65843)
0402h	BC/RT/MT with 64K of RAM (BU-65863)
0404h	RT Only with 4K of RAM

Table 5. PCI Command Register	
BIT	**Description**
15:10	Reserved, 0's
9	0
8	SERR# Enable
7	0
6	Parity Error Control
5:2	0
1	Memory Space
0 (LSB)	0

3.7 PCI COMMAND REGISTER

Reserved: These bits are read-only and return zeroes when read.

SERR# Enable: This is an enable bit for the SERR# driver. A value of 0b disables the driver. A value of 1b enables the driver. The value after RST# is 0b.

Parity Error Control: This bit controls the device's response to parity errors. When the bit is 1b, the device will take its normal action when a parity error is detected. When this bit is 0b, the device will ignore any parity errors that it detects and continue normal operation. The value after RST# is 0b.

Memory Space: This bit controls the device's response to memory space accesses. A value of 0b disables the device response. A value of 1b allows the device to respond to memory space accesses. The value after RST# is 0b.

3.8 PCI STATUS REGISTER

This register records status information for PCI bus related events. Reads to this register behave normally, but writes can only reset bits. A bit is reset whenever the register is written and the data in the corresponding bit location is a 1.

Detected Parity Error: This bit will be set by the device whenever it detects a parity error, even if the Parity Error Control bit in the PCI Control register is 0b.

Signaled System Error: This bit indicates when the device has asserted SERR#. The value after RST# is 0b.

Signaled Target Abort: This bit is set whenever the device terminates a transaction with a Target-Abort. The value after RST# is 0b.

DEVSEL# Timing: The PCI Total-ACE is 01b, medium.

Fast Back-to-Back Capable: This bit is set to 1b and indicates that the device is capable of accepting fast back-to-back transactions.

Reserved: These bits are read-only and return zeroes when read.

Subsystem Vendor ID/Subsystem Device ID: Field is an alias of the Vendor ID/Device ID fields in Configuration Register 00h.

Base Address Registers: Used to implement ACE memory space (BAR0) and ACE register space (BAR1). Base Address Registers 2 through 5 are not used.

BAR0: Used to access ACE memory space. The ACE is allotted a maximum of 64K words, 128K bytes, for its memory space. BAR0 will read back as FFFE0000 after all Fs are written to it. BAR0 will read back the same for both 4K word PCI Total-ACE parts (BU-65843) and the 64K word PCI Total-ACE (BU-65863).

PCI Total-ACE Memory Space: The least significant bit (LSB) of the PCI address is dropped to form the ACE memory address.

BAR1: Used to access ACE register locations. The ACE is allotted a maximum of 4K bytes for its register space. BAR1 will read back as FFFFF000h after all Fs are written to it. All ACE register locations are accessible through the PCI host via the BAR1 offsets 000h to 0FCh. The PCI-to-ACE interface control/status registers are at 800h to 81Ch. PCI accesses outside of these specific regions (e.g., to offset 100h or 820h, etc.) will produce Target Aborts.

PCI Total-ACE Register Space: Register accesses are on a 32-bit boundary: the last 2 bits of the PCI address are dropped to form the internal ACE address. (e.g. 000 = ACE Reg 0, 004 = ACE Reg1, 008 = ACE Reg2, etc.). Refer to TABLE 18 for a listing of these registers. These registers are nearly 100% compatible with the Enhanced Mini-ACE registers. For an exhaustive discussion of these registers and 1553 BC/RT/MT operation, please refer to the "Enhanced Mini-ACE User Guide".

Table 6. PCI Status Register

BIT	Description
31	Detected Parity Error
30	Signaled System Error
29:28	0
27	Signaled Target Abort
26:25	DEVSEL# Timing = 01 (Medium)
24	0
23	Fast Back-to-Back Capable = 1
22:21	0
20:16	Reserved, 0's

Table 7. (BAR0) Ace Memory

Address Off-Set	Definition
00000-1FFFFC	PCI Total-ACE Memory Space

Table 8. (BAR1) ACE/Control Registers – 4K Byte Total Space

Address Offset	Name	Definition/Accessibility
000-0FC	ACE	PCI Total-ACE Register Space
100-7FC	—	Reserved (Target Abort if Accessed)
800	REG0	Global Activity (RD)
804	REG1	Fail-Safe Operation/Interrupt (RW/WR)
808	REG2	Fail-Safe Timer (RD)
80C	REG3	Fail-Safe Timer Preload (RD/WR)
810	REG4	Discard Timer (RD)
814	REG5	Discard Timer Preload (RD/WR)
818	REG6	General Purpose, Customer Use (RD/WR)
81C	REG7	Clear Fail-Safe INT/Reset ACE (WR)
820-FFC	—	Reserved (Target Abort if Accessed)

Table 9. REG0 Global Activity Register (Read 800H)	
BIT	**Description**
31 (MSB)	PCI Interrupt Active
30	FIFO Not Empty
29	0
28	0
27	0
26	0
25	0
24	1
23	BAR1 DRR_DATA_DISCARD
22	FAIL_SAFE Error
21	0
20	0
19	0
18	0
17	0
16	PCI Total-ACE Interrupt Active
15	0
•	•
•	•
•	•
0 (LSB)	0

This register will be all 0s after RST#, except for bit 24

PCI INTERRUPT ACTIVE: When set to '1', indicates that PCI Total-ACE has asserted it's interrupt pin. The three possible sources (if enabled and active) are the ACE core, FailSafe timer and BAR1 DRR_DATA_DISCARD.

FIFO NOT EMPTY: When set to '1', indicates that the write FIFO is not empty.

BAR1 DRR DATA DISCARD: If the data discard timer times out while waiting for a retry on a BAR1 access, this bit will be set. If BAR1 read is discarded, it may have caused an action (for example clearing an ACE interrupt) that has not been recognized by the PCI MASTER.

FAIL SAFE ERROR: If not in FAIL_SAFE OFF mode and fail safe error occurs (ACE does not respond), this bit will be set. Failsafe errors are extremely unlikely.

DRR_HOLD: When '0', a delayed read request is discarded if the PCI Total-ACE has obtained requested data and a different transaction is requested. When '1', delayed read request is held until master repeats original request or timeout occurs.

BITS 30 - 22: Reserved, write as 0s

PCI TOTAL-ACE INTERRUPT ENABLE: Must be set to "1".

Note: *Interrupts will not function unless this bit is set to "1".*

BAR1 DRR_DATA_DISCARD INTERRUPT ENABLE: Enables interrupt to occur on a BAR1 delayed read timeout.

FAILSAFE INTERRUPT ENABLE: When set to a "1", an interrupt is generated if not in FAILSAFE OFF mode and a FAILSAFE error is detected.

FAILSAFE INTERRUPT AUTOCLEAR ENABLE: If set, causes interrupt and the FAIL_SAFE ERROR bit (REG0-bit 22) to be cleared whenever upper word of REG0 is read by the PCI MASTER. If not set, bit 1 in Reg 7 must be used to clear Failsafe interrupts.

FAILSAFE MODE: Fail Safe Errors occur when the internal ACE fails to assert it's hand-shake signal within 1 millisecond (programmable) of when the internal Strobe or Request signal is asserted. Four possible FAILSAFE Modes determine how this situation is handled.

Table 10. REG1 Fail-Safe Operation/Interrupt Register (Read/Write 804H)

BIT	Description
31 (MSB)	DRR_HOLD
30	Reserved. Write as 0
•	•
•	•
•	•
22	Reserved, Write as 0
21	PCI Total-ACE Interrupt Enable

Table 10. REG1 Fail-Safe Operation/Interrupt Register (Read/Write 804H)	
BIT	**Description**
20	BAR1 DRR_DATA_DISCARD Interrupt Enable
19	Failsafe Interrupt Enable
18	Failsafe Interrupt Autoclear Enable
17	Failsafe Mode – BIT 1 (MSB)
16	Failsafe Mode – BIT 0 (LSB)
15	Reserved, Write as 0
•	•
•	•
•	•
0 (LSB)	0

This register will be all 0s after RST#, except for bit 17 will be 1 (Fail-safe mode = fail-safe halt). Note that Failsafe errors are extremely unlikely.

Table 11. Failsafe Mode		
BIT 17	**BIT 16**	**Failsafe Mode**
0	0	Failsafe Off
0	1	Failsafe Retry
1	0	Failsafe Halt
1	1	Failsafe Skip

Note: Failsafe errors are extremely unlikely.

MODE 1 - FAILSAFE OFF:. PCI Total-ACE will wait indefinitely for the transaction to complete. The local bus could hang as a result. The FAILSAFE ERROR bit and interrupt will not be generated even if the enable bit is set.

MODE 2 - FAILSAFE RETRY:. PCI Total-ACE will retry the transfer on the local bus when the FAILSAFE timer times out.

MODE 3 - FAILSAFE HALT:. Once the FAILSAFE timer times out, all future transfers will be terminated with a target abort until the PCI master clears the interrupt.

MODE 4 - FAILSAFE SKIP:. Once the FAILSAFE timer times out, the current transaction is discarded or skipped and the next transaction, whether a stored write in the FIFO or a new transaction, will be attempted.

BITS 15-0 ARE RESERVED: Write these bits as 0s.

Table 12. REG2 Fail-Safe Timer Register (Read 808H)

BIT	Description
31 (MSB)	0
•	•
•	•
•	•
16	0
15	Fail-Safe Timer Count – BIT 15 (LSB)
•	•
•	•
•	•
0 (LSB)	Fail-Safe Timer Count – BIT 0 (LSB)

FAIL-SAFE TIMER COUNT: Read this register to obtain the current value of the fail-safe timer. Default is 8400h.

Table 13. REG3 Fail-Safe Timer Preload Register (Read/Write 80CH)

BIT	Description
31 (MSB)	0
•	•
•	•
•	•
16	0
15	Fail-Safe Timer Value – BIT 15 (LSB)
•	•
•	•
•	•
0 (LSB)	Fail-Safe Timer Value – BIT 0 (LSB)

FAIL-SAFE TIMER VALUE: Write to this register to set the value for the fail-safe timer. The default value is 8400h and no access to this register is needed for normal applications.

Table 14. REG4 Discard Timer Register (Read 810H)	
BIT	**Description**
31 (MSB)	0
•	•
•	•
•	•
16	0
15	Discard Timer Current – BIT 15 (LSB)
•	•
•	•
•	•
0 (LSB)	Discard Timer Current – BIT 0 (LSB)

DISCARD TIMER CURRENT: Read this register to obtain the current value of the DISCARD TIMER. Default is 0000h.

Table 15. REG5 Discard Timer Preload Register (Read/Write 814H)	
BIT	**Description**
31 (MSB)	0
•	•
•	•
•	•
16	0
15	Discard Timer Value – BIT 15 (LSB)
•	•
•	•
•	•
0 (LSB)	Discard Timer Value – BIT 0 (LSB)

DISCARD TIMER VALUE: Write this register to set the value to be used for the discard timer. The default value is "0". The default value meets the PCI spec and no access to this register is needed for normal applications.

Table 16. REG6 General Purpose Register (Read/Write 818H)

BIT	Description
31 (MSB)	Reserved – BIT 31 (MSB)
•	•
•	•
•	•
0 (LSB)	Reserved – BIT 0 (LSB)

This register will be all 0s after RST#. This read/write register is available for customer use, perhaps as a flag register for signaling between bus masters.

Table 17. REG7 Reserved Register (Write 81CH)

BIT	Description
31 (MSB)	Reserved, Write as 0 – BIT 31 (MSB)
•	•
•	•
•	•
1	Clear Failsafe Interrupt
0 (LSB)	Reserved – BIT 0 (LSB)

This register will be all 0s after RST#. No access to this register is needed for normal applications.

BITS 31-2 ARE RESERVED AND MUST BE WRITTEN AS 0s

CLEAR FAILSAFE INTERRUPT: Clears the Failsafe Interrupt when set to "1". Failsafe interrupts can also be cleared via the Failsafe Interrupt Autoclear mechanism, enabled by bit 18 in Reg 1.

ACE RESET: Resets the ACE when set to "1".

3.9 PCI TOTAL-ACE REGISTER AND MEMORY ADDRESSING

The software interface of the enhanced Mini-ACE portion of the PCI Total-ACE to the host processor consists of 24 internal operational registers for normal operation, an additional 24 test registers, plus 64K words of shared memory address space. The PCI Total-ACE's 4K X 16 or 64K X 17 internal RAM resides in this address space.

For normal operation, the host processor only needs to access the lower 32 register address locations (internal address 00-1F). The next 32 locations (internal address 20-3F) should be reserved, since many of these are used for factory test.

3.10 Internal Registers

The internal address mapping,with the corresponding PCI BAR1 address offset, for the PCI Total-ACE registers is illustrated in Table 18. Note that the address lines shown are the PCI Total-ACES's internal ACE register bus and are left shifted 2 bits with respect to the PCI address: A0 = PCI A2, A1 = PCI A3, etc. For example, Interrupt mask register #1 is located at PCI address BAR1 offset + 0h, Configuration Register #1 is at BAR1 offset + 4h, etc. Note that the table below does not show the internal A5 register address line, which is normally 0 and is set only for access to the reserved factory test registers.

Also note that the ACE registers are internally 16 bits wide, appear in the lower 16 bits of a 32-bit PCI DWord and that the upper 16 bits will read as zeroes during a 32-bit PCI read.

The configuration registers will be cleared to 0000h after hardware or software reset, with the exception of the Enhanced CPU Access bit (bit 14 in Configuration register #6).

Table 18. Address Mapping

Address Lines					BAR1 ADDR Offset	Register Description/Accessiblity
A4	A3	A2	A1	A0		
0	0	0	0	0	00h	Interrupt Mask Register #1 (RD/WR)
0	0	0	0	1	04h	Configuration Register #1 (RD/WR)
0	0	0	1	0	08h	Configuration Register #2 (RD/WR)
0	0	0	1	1	0Ch	Start/Reset Register (WR)
0	0	0	1	1	0Ch	Non-Enhanced BC/RT Command Stack Pointer / Enhanced BC Instruction List Pointer Regsiter (RD)
0	0	1	0	0	10h	BC Control Word / RT Subaddress Control Word Register (RD/WR)
0	0	1	0	1	14h	Time Tag Register (RD/WR)

Table 18. Address Mapping						
Address Lines					BAR1 ADDR Offset	Register Description/Accessiblity
A4	A3	A2	A1	A0		
0	0	1	1	0	18h	Interrupt Status Register #1 (RD)
0	0	1	1	1	1Ch	Configuration Register #3 (RD/WR)
0	1	0	0	0	20h	Configuration Register #4 (RD/WR)
0	1	0	0	1	24h	Configuration Register #5 (RD/WR)
0	1	0	1	0	28h	RT/Monitor Data Stack Address Register (RD/WR)
0	1	0	1	1	2Ch	BC Frame Time Remaining Register (RD)
0	1	1	0	0	30h	BC Time Remaining to Next Message Register (RD)
0	1	1	0	1	34h	Non-Enhanced BC Frame Time / Enhanced BC Intital Instruction Pointer / RT Last Command / MT Trigger Word Register (RD/WR)
0	1	1	1	0	38h	RT Status Word Register (RD)
0	1	1	1	1	3Ch	RT BIT Word Register (RD)
1	0	0	0	0	40h	Test Mode Register 0
1	0	0	0	1	44h	Test Mode Register 1
1	0	0	1	0	48h	Test Mode Register 2
1	0	0	1	1	4Ch	Test Mode Register 3
1	0	1	0	0	50h	Test Mode Register 4
1	0	1	0	1	54h	Test Mode Register 5
1	0	1	1	0	58h	Test Mode Register 6
1	0	1	1	1	5Ch	Test Mode Register 7
1	1	0	0	0	60h	Configuration Register #6 (RD/WR)
1	1	0	0	1	64h	Configuration Register #7 (RD/WR)
1	1	0	1	0	68h	RESERVED
1	1	0	1	1	6Ch	BC Condition Code Register (RD)
1	1	0	1	1	6Ch	BC General Purpose Flag Register
1	1	1	0	0	70h	BIT Test Status Register (RD)
1	1	1	0	1	74h	Interrupt Mask Register #2 (RD/WR)
1	1	1	1	0	78h	Interrupt Status Register #2 (RD)
1	1	1	1	1	7Ch	BC General Purpose Queue Pointer / RT-MT Interrupt Status Queue Pointer Register (RD/WR)

Table 19. Interrupt Mask Register #1 (Read/Write 00H, PCI 00H)	
BIT	**Description**
15 (MSB)	RESERVED
14	RAM Parity Error
13	BC/RT Transmitter Timeout
12	BC/RT Command Stack Rollover
11	MT Command Stack Rollover
10	MT Data Stack Rollover
9	Handshake Fail
8	BC Retry
7	RT Address Parity Error
6	Time Tag Rollover
5	RT Circular Buffer Rollover
4	BC Control Word/RT Subaddress Control Word EOM
3	BC End of Frame
2	Format Error
1	BC Status Set/RT Mode Code/MT Pattern Trigger
0 (LSB)	End of Message

Table 20. Configuration Register #1 (Read/Write 01H, PCI 04H)				
BIT	**BC Function (Bits 11-0 Enhanced Mode Only)**	**RT Without Alternate Status**	**RT With Alternate Status (Enhanced Only)**	**Montior Function (Enhanced Mode Only BITS 12-0)**
15 (MSB)	RT/ $\overline{\text{BC-MT}}$ (logic 0)	(logic 1)	(logic 1)	(logic 0)
14	MT/ $\overline{\text{BC-RT}}$ (logic 0)	(logic 0)	(logic 0)	(logic 1)
13	Current Area B/ $\overline{\text{A}}$	Current Area B/ $\overline{\text{A}}$	Current Area B/ $\overline{\text{A}}$	Current Area B/ $\overline{\text{A}}$
12	Message Stop-On-Error	Message Monitor Enabled (MMT)	Message Monitor Enabled	Message Monitor Enabled
11	Frame Stop-On-Error	$\overline{\text{Dynamic Bus Control}}$ / $\overline{\text{Acceptance}}$	S10	Trigger Word Enabled
10	Status Set Stop-On-Message	$\overline{\text{BUSY}}$	S09	Start-On-Trigger
9	Status Set Stop-On-Frame	$\overline{\text{SERVICE REQUEST}}$	S08	Stop-On-Trigger

Table 20. Configuration Register #1 (Read/Write 01H, PCI 04H)				
BIT	**BC Function (Bits 11-0 Enhanced Mode Only)**	**RT Without Alternate Status**	**RT With Alternate Status (Enhanced Only)**	**Montior Function (Enhanced Mode Only BITS 12-0)**
8	Frame Auto-Repeat	$\overline{\text{SSFLAG}}$	S07	Not Used
7	External Trigger Enabled	$\overline{\text{RT FLAG}}$ (Enhanced Mode Only)	S06	External Trigger Enabled
6	Internal Trigger Enabled	Not Used	S05	Not Used
5	Intermessage Gap Timer Enabled	Not Used	S04	Not Used
4	Retry Enabled	Not Used	S03	Not Used
3	Doubled / $\overline{\text{Single}}$ Retry	Note Used	S02	Not Used
2	BC Enabled (Read Only)	Not Used	S01	Monitor Enabled (Read Only)
1	BC Frame In Progress (Read Only)	Not Used	S00	Monitor Triggered (Read Only)
0 (LSB)	BC Message In Progress (Read Only)	RT Message In Progress (Enhanced mode only, Read Only)	RT Message in Progress (Read Only)	Monitor Active (Read Only)

Table 21. Configuration Register #2 (Read/Write 02H, PCI 08H)	
BIT	**Description**
15 (MSB)	Enhanced Interrupts
14	RAM Parity Enable
13	Busy Lookup Table Enable
12	RX SA Double Buffer Enable
11	Overwrite Invalid Data
10	256-Word Boundary Disable
9	Time Tag Resolution 2
8	Time Tag Resolution 1
7	Time Tag Resolution 0
6	Clear Time Tag on Synchronize
5	Load Time Tag on Synchronize
4	Interrupt Status Auto Clear
3	Level / $\overline{\text{Pulse}}$ Interrupt Request
2	Clear Service Request
1	Enhanced RT Memory Management
0 (LSB)	Separate Broadcast Data

Table 22. Start/Reset Register (Write 03H, PCI 0CH)	
BIT	**Description**
15 (MSB)	Reserved
14	Reserved
13	Reserved
12	Reserved
11	Clear RT Halt
10	Clear Self-Test Register
9	Initiate RAM Self-Test
8	Reserved
7	Reserved
6	BC/MT Stop-On-Message
5	BC Stop-On-Frame
4	Time Tag Test Clock
3	Time Tag Reset
2	Interrupt Reset
1	BC/MT Start
0 (LSB)	Reset

Table 23. BC/RT Command Stack Pointer Reg.(Read 03H, PCI 0CH)	
BIT	**Description**
15 (MSB)	Command Stack Pointer 15
•	•
•	•
•	•
0 (LSB)	Command Stack Pointer 0

Table 24. BC Control Word Register (Read/Write 04H, PCI 10H)	
BIT	**Description**
15 (MSB)	Transmit Time Tag for Synchronize Mode Command
14	Message Error Mask
13	Service Request Bit Mask
12	Busy Bit Mask
11	Subsystem Flag Bit Mask
10	Terminal Flag Bit Mask
9	Reserved Bits Mask
8	Retry Enabled
7	Bus Channel A/ $\overline{B}$
6	Off-Line Self-Test
5	Mask Broadcast Bit
4	EOM Interrupt Enable
3	1553A/B Select
2	Mode Code Format
1	Broadcast Format
0 (LSB)	RT-to-RT Format

Table 25. RT Subaddress Control Word (Read/Write 04H, PCI 10H)	
BIT	**Description**
15 (MSB)	RX: Double/ Global Circular Buffer Enable
14	TX: EOM INT
13	TX: CIRC BUF INT
12	TX: Memory Management 2 (MM2)
11	TX: Memory Management 1 (MM1)
10	TX: Memory Management 0 (MM0)
9	RX: EOM INT
8	RX: CIRC BUF INT
7	RX: Memory Management 2 (MM2)
6	RX: Memory Management 1 (MM1)
5	RX: Memory Management 0 (MM0)
4	BCST: EOM INT
3	BCST: CIRC BUF INT
2	BCST: Memory Management 2 (MM2)
1	BCST: Memory Management 1 (MM1)
0 (LSB)	BCSTL Memory Management 0 (MM0)

Table 26. Time Tag Register. (Read/Write 05H, PCI 14H)	
BIT	**Description**
15 (MSB)	Time Tag 15
•	•
•	•
•	•
0 (LSB)	Time Tag 0

Table 27. Interrupt Status Register #1 (Read 06H, PCI 18H)

BIT	Description
15 (MSB)	Master Interrupt
14	RAM Parity Error
13	Transmitter Timeout
12	BC/RT Command Stack Rollover
11	MT Command Stack Rollover
10	MT Data Stack Rollover
9	Handshake Fail
8	BC Retry
7	RT Address Parity Error
6	Time Tag Rollover
5	RT Circular Buffer Rollover
4	BC Control Word / RT Subaddress Control Word EOM
3	BC End of Frame
2	Format Error
1	BC Status Set / RT Mode Code / MT Pattern Trigger
0 (LSB)	End of Message

Table 28. Configuration Register #3 (Read/Write 07H, PCI 1CH)

BIT	Description
15 (MSB)	Enhanced Mode Enable
14	BC/RT Command Stack Size 1
13	BC/RT Command Stack Size 0
12	MT Command Stack Size 1
11	MT Command Stack Size 0
10	MT Data Stack Size 2
9	MT Data Stack Size 1
8	MT Data Stack Size 0
7	Illegalization Disabled
6	Override Mode T/$\overline{R}$ Error
5	Alternate Status Word Enable
4	Illegal Rx Transfer Disable
3	Reserved, Set to 0
2	$\overline{\text{RTFAIL}}$ / $\overline{\text{RTFLAG}}$ Wrap Enable
1	1553A Mode Codes Enable
0 (LSB)	Enhanced Mode Code Handling

Table 29. Configuration Register #4 (Read/Write 08H, PCI 20H)	
BIT	**Description**
15 (MSB)	External Bit Word Enable
14	Inhibit Bit Word If Busy
13	Mode Command Override Busy
12	Expanded BC Control Word Enable
11	Broadcast Mask ENA/XOR
10	Retry If –A and M.E.
9	Restry if Status Set
8	1st Retry ALT/ $\overline{\text{SAME}}$ Bus
7	2nd Retry ALT/ $\overline{\text{SAME}}$ Bus
6	Valid M.E./No Data
5	Valid Busy/No Data
4	MT Tag Gap Option
3	Latch RT Address with Config #5
2	Test Mode 2
1	Test Mode 1
0 (LSB)	Test Mode 0

Table 30. Configuration Register #5 (Read/Write 09H, PCI 24H)	
BIT	**Description**
15 (MSB)	12/ $\overline{16}$ MHz Clock Select
14	Single-Ended Select
13	External TX Inhibit A
12	External TX Inhibit B
11	Expanded Crossing Enabled
10	Response Timeout Select 1
9	Response Time out Select 0
8	Gap Check Enabled
7	Broadcast Disabled
6	RT Address Latch/ $\overline{\text{Transparent}}$
5	RT Address 4
4	RT Address 3
3	RT Address 2
2	RT Address 1
1	RT Address 0
0 (LSB)	RT Address Parity

Table 31. RT/Monitor Data Stack Address Register (Read/Write 0AH, PCI 28H)	
BIT	**Description**
15 (MSB)	RT / Monitor Data Stack Address 15
•	•
•	•
•	•
0 (LSB)	RT / Monitor Data Stack Address 0

Table 32. BC Frame Time Remaining Register (Read/Write 0BH, PCI 2CH)	
BIT	**Description**
15 (MSB)	BC Frame Time Remaining 15
•	•
•	•
•	•
0 (LSB)	BC Frame Time Remaining 0

Note: resolution = 100 µs per LSB

Table 33. BC Frame Time Remaining Register (Read/Write 0CH, PCI 30H)	
BIT	**Description**
15 (MSB)	BC Frame Time Remaining 15
•	•
•	•
•	•
0 (LSB)	BC Frame Time Remaining 0

Note: resolution = 100 µs per LSB

Table 34. BC Frame Time/RT Last Command/MT Trigger Register (Read/Write 0DH, PCI 34H)	
BIT	**Description**
15 (MSB)	BIT 15
•	•
•	•
•	•
0 (LSB)	BIT 0

Table 35. RT Status Word Register (Read/Write 0EH, PCI 38H)	
BIT	**Description**
15 (MSB)	Logic “0”
14	Logic “0”
13	Logic “0”
12	Logic “0”
11	Logic “0”
10	Message Error
9	Instrumentation
8	Service Request
7	Reserved
6	Reserved
5	Reserved
4	Braodcast Command Received
3	Busy
2	SSFLAG
1	Dynamic Bus Control Accept
0 (LSB)	Terminal Flag

Table 36. RT BIT Word Register (Read/Write 0FH, PCI 3CH)	
BIT	**Description**
15 (MSB)	Transmitter Timeout
14	Loop Test Failure B
13	Loopt Test Failure A
12	Handshake Failure
11	Transmitter Shutdown B
10	Transmitter Shutdown A
9	Terminal Flag Inhibited
8	Bit Test Fail
7	High Word Count
6	Low Word Count
5	Incorrect Sync Received
4	Parity/Manchester Error Received
3	RT-to-RT Gap / Sync / Address Error
2	RT-to-RT No Response Error
1	RT-to-RT 2nd Command Word Error
0 (LSB)	Command Word Contents Error

Table 37. Configuration Register #6 (Read/Write 18H, PCI 60H)	
BIT	**Description**
15 (MSB)	Enhanced Bus Controller
14	Enhanced CPU Access
13	Command Stack Pointer Increment on EOM (RT, MT)
12	Global Circular Buffer Enable
11	Global Circular Buffer Size 2
10	Global Circular Buffer Size 1
9	Global Circular Buffer Size 0
8	Disable Invalid Messages to Interrupt Statu Queue
7	Disbale Valid Messages to Interrupt Status Queue
6	Interrupt Status Queue Enable
5	RT Address Source
4	Enhanced Message Monitor
3	Reserved
2	64-Word Register Space
1	Clock Select 1
0 (LSB)	Clock Select 0

Table 38. Configuration Register #7 (Read/Write 19H, PCI 64H)	
BIT	**Description**
15 (MSB)	Memory Management Base Address 15
14	Memory Management Base Address 14
13	Memory Management Base Address 13
12	Memory Management Base Address 12
11	Memory Management Base Address 11
10	Memory Management Base Address 10
9	Reserved
8	Reserved
7	Reserved
6	Reserved
5	Reserved
4	RT Halt Enable
3	1553B Response Time
2	Enhanced Time Tag Synchronize
1	Enahnced BC Watchdog Timer Enabled
0 (LSB)	Mode Code Reset / INCMD Select

Table 39. BC Condition Register (Read 1BH, PCI 6CH)	
BIT	**Description**
15 (MSB)	Logic ‘1’
14	Retry 1
13	Retry 0
12	Bad Message
11	Message Status Set
10	Good Block Transfer
9	Format Error
8	No Response
7	General Purpose Flag 7
6	General Purpose Flag 6
5	General Purpose Flag 5
4	General Purpose Flag 4
3	General Purpose Flag 3
2	General Purpose Flag 2
1	Equal Flag / General Purpose Flag 0
0 (LSB)	Less Than Flag / General Purpose Flag 1

Note: If the PCI Total-ACE is not online in enhanced BC mode (i.e., processing instructions), the BC condition code register will always return a value of 0000.

Table 40. BC General Purpose Flag Register (Write 1BH, PCI 6CH)	
BIT	**Description**
15 (MSB)	Clear General Purpose Flag 7
14	Clear General Purpose Flag 6
13	Clear General Purpose Flag 5
12	Clear General Purpose Flag 4
11	Clear General Purpose Flag 3
10	Clear General Purpose Flag 2
9	Clear General Purpose Flag 1
8	Clear General Purpose Flag 0
7	Set General Purpose Flag 7
6	Set General Purpose Flag 6
5	Set General Purpose Flag 5
4	Set General Purpose Flag 4
3	Set General Purpose Flag 3
2	Set General Purpose Flag 2
1	Set General Purpose Flag 1
0 (LSB)	Set General Purpose Flag 0

Table 41. BIT Test Status Flag Register (Read 1CH, PCI 70H)	
BIT	**Description**
15 (MSB)	Logic “0”
14	Logic “0”
13	Logic “0”
12	Logic “0”
11	Logic “0”
10	Logic “0”
9	Logic “0”
8	Logic “0”
7	RAM Built-In Test Complete
6	RAM Built-In Test In-Progress
5	RAM Built-In Test In-Passed
4	Logic “0”
3	Logic “0”
2	Logic “0”
1	Logic “0”
0 (LSB)	Logic “0”

Table 42. Interrupt Mask Register #2 (Read/Write 1DH, PCI 74H)	
BIT	**Description**
15 (MSB)	Not Used
14	BC Op Code Parity Error
13	RT Illegal Command/Message MT Message Received
12	General Purpose Queue / Interrupt Status Queue Rollover
11	Call Stack Pointer Register Error
10	BC Trap Op Code
9	RT Command Stack 50% Rollover
8	RT Circular Buffer 50% Rollover
7	Monitor Command Stack 50% Rollover
6	Monitor Data Stack 50% Rollover
5	Enhanced BC IRQ3
4	Enhanced BC IRQ2
3	Enhanced BC IRQ1
2	Enhanced BC IRQ0
1	Bit Test Complete
0 (LSB)	Not Used

Table 43. Interrupt Status Register #2 (Read 1EH, PCI 78H)	
BIT	**Description**
15 (MSB)	Master Interrupt
14	BC Op Code Parity Error
13	RT Illegal Command/Message MT Message Received
12	General Purpose Queue / Interrupt Status Queue Rollover
11	Call Stack Pointer Register Error
10	BC Trap Op Code
9	RT Command Stack 50% Rollover
8	RT Circular Buffer 50% Rollover
7	Monitor Command Stack 50% Rollover
6	Monitor Data Stack 50% Rollover
5	Enhanced BC IRQ3
4	Enhanced BC IRQ2
3	Enhanced BC IRQ1
2	Enhanced BC IRQ0
1	Bit Test Complete
0 (LSB)	Interrupt Chain Bit

Table 44. BC General Purpose Queue Pointer Register RT, MT Interrupt Status Queue Pointer Register (Read/Write 1FH, PCI 7CH)	
BIT	**Description**
15 (MSB)	Queue Pointer Base Address 15
14	Queue Pointer Base Address 14
13	Queue Pointer Base Address 13
12	Queue Pointer Base Address 12
11	Queue Pointer Base Address 11
10	Queue Pointer Base Address 10
9	Queue Pointer Base Address 9
8	Queue Pointer Base Address 8
7	Queue Pointer Base Address 7
6	Queue Pointer Base Address 6
5	Queue Pointer Address 5
4	Queue Pointer Address 4
3	Queue Pointer Address 3
2	Queue Pointer Address 2
1	Queue Pointer Address 1
0 (LSB)	Queue Pointer Address 0

Note: *Table 45 to Table 51 are not Registers, but they are words stored in RAM.*

Table 45. BC Mode Block Status Word	
BIT	**Description**
15 (MSB)	EOM
14	SOM
13	Channel B/ $\overline{A}$
12	Error Flag
11	Status Set
10	Format Error
9	No Response Timeout
8	Loop Test Fail
7	Masked Status Set
6	Retry Count 1
5	Retry Count 0
4	Good Data Block Transfer
3	Wrong Status Address / No Gap
2	Word Count Error
1	Incorrect Sync Type
0 (LSB)	Invalid Word

Table 46. RT Mode Block Status Word	
BIT	**Description**
15 (MSB)	EOM
14	SOM
13	Channel B/ $\overline{A}$
12	Error Flag
11	RT-to-RT Format
10	Format Error
9	No Response Timeout
8	Loop Test Fail
7	Data Stack Rollover
6	Illegal Command Word
5	Word Count Error
4	Incorrect Data Sync
3	Invalid Word
2	RT-to-RT Gap / Sync / Address Error
1	RT-to-RT 2nd Command Error
0 (LSB)	Command Word Contents Error

Table 47. 1553 Command Word	
BIT	**Description**
15 (MSB)	Remote Terminal Address BIT 4
14	Remote Terminal Address BIT 3
13	Remote Terminal Address BIT 2
12	Remote Terminal Address BIT 1
11	Remote Terminal Address BIT 0
10	Transmit / $\overline{\text{Receive}}$
9	Subaddress / Mode Code BIT 4
8	Subaddress / Mode Code BIT 3
7	Subaddress / Mode Code BIT 2
6	Subaddress / Mode Code BIT 1
5	Subaddress / Mode Code BIT 0
4	Data Word Count / Mode Code Bit 4
3	Data Word Count / Mode Code Bit 3
2	Data Word Count / Mode Code Bit 2
1	Data Word Count / Mode Code Bit 1
0 (LSB)	Data Word Count / Mode Code Bit 0

Table 48. Word Monitor Identification Word	
BIT	**Description**
15 (MSB)	Gap Time (MSB)
•	•
•	•
•	•
8	Gap Time (LSB)
7	Word Flag
6	$\overline{\text{This}}$ $\overline{\text{RT}}$
5	$\overline{\text{Broadcast}}$
4	Error
3	Command / $\overline{\text{Data}}$
2	Channel B/ $\overline{\text{A}}$
1	Contiguous Data / $\overline{\text{Gap}}$
0 (LSB)	$\overline{\text{Mode\_Code}}$

Table 49. Message Monitor Mode Block Status Word	
BIT	**Description**
15 (MSB)	EOM
14	SOM
13	Channel B/ $\overline{\text{A}}$
12	Error Flag
11	RT-to-RT Transfer
10	Format Error
9	No Response Timeout
8	Good Data Block Transfer
7	Data Stack Rollover
6	Reserved
5	Word Count Error
4	Incorrect Sync
3	Invalid Word
2	RT-to-RT Gap / Sync / Address Error
1	RT-to-RT 2nd Command Error
0 (LSB)	Command Word Contents Error

Table 50. RT/Monitor Interrupt Status Word (For Interrupt Status Queue)

BIT	Definition for Message Interrupt Event	Definition for Non-Message Interrupt Event
15	Transmitter Timeout	Not Used
14	Illegal Command	Not Used
13	Monitor Data Stack 50% Rollover	Not Used
12	Monitor Data Stack Rollover	Not Used
11	RT Circular Buffer 50% Rollover	Not Used
10	RT Circular Buffer Rollover	Not Used
9	Monitor Command (Descriptor) Stack 50% Rollover	Not Used
8	Monitor Command (Descriptor) Stack Rollover	Not Used
7	RT Command (Descriptor) Stack 50% Rollover	Not Used
6	RT Command (Descriptor) Stack Rollover	Not Used
5	Handshake Fail	NotUsed
4	Format Error	Time Tag Rollover
3	Mode Code Interrupt	RT Address Parity Error
2	Subaddress Control Word EOM	Not Used
1	End-Of-Message (EOM)	RAM Parity Error
0	“1” For Message Interrupt Event “0” For Non-Message Interrupt Event	

Table 51. 1553B Status Word

BIT	Description
15 (MSB)	Remote Terminal Address BIT 4
14	Remote Terminal Address BIT 3
13	Remote Terminal Address BIT 2
12	Remote Terminal Address BIT 1
11	Remote Terminal Address BIT 0
10	Message Error
9	Instrumentation
8	Service Request
7	Reserved
6	Reserved
5	Reserved
4	Broadcast Command Received
3	Busy
2	SSFLAG
1	Dynamic Bus Control Acceptance
0 (LSB)	Terminal Flag

4 NON-TEST REGISTER FUNCTION SUMMARY

A summary of the PCI Total-ACE's 24 non-test registers follows.

4.1 Interrupt Mask Registers #1 and #2

Interrupt Mask Registers #1 and #2 are used to enable and disable interrupt requests for various events and conditions.

NOTE: Please see Appendix "F" of the Enhanced Mini-ACE Users Guide for important information applicable only to RT Mode operation, enabling of the interrupt status queue and use of specific non-message interrupts.

4.2 Configuration Registers #1 and #2

Configuration Registers #1 and #2 are used to select the PCI Total- ACE's mode of operation, and for software control of RT Status Word bits, Active Memory Area, BC Stop-On-Error, RT Memory Management mode selection, and control of the Time Tag operation.

Note: *The LEVEL/ $\overline{\text{PULSE}}$ INTERRUPT REQUEST bit in Configuration Register #2 MUST be set to 1 for correct PCI operation.*

4.3 Start/Reset Register

The Start/Reset Register is used for "command" type functions such as software reset, BC/MT Start, Interrupt reset, Time Tag Reset, Time Tag Register Test, Initiate protocol self-test, Initiate RAM self-test, Clear self-test register, and Clear RT Halt. The Start/Reset Register also includes provisions for stopping the BC in its auto-repeat mode, either at the end of the current message or at the end of the current BC frame.

4.4 BC/RT Command Stack Register

The BC/RT Command Stack Register allows the host CPU to determine the pointer location for the current or most recent message.

4.5 BC Instruction List Pointer Register

The BC Instruction List Pointer Register may be read to determine the current location of the Instruction List Pointer for the Enhanced BC mode.

4.6 BC Control Word/RT Subaddress Control Word Register

In BC mode, the BC Control Word/RT Subaddress Control Word Register allows host access to the current word or most recent BC Control Word. The BC Control Word contains bits that select the active bus and message format, enable off-line self-test, masking of Status Word bits, enable retries and interrupts, and specify MIL-STD-1553A or -1553B error handling. In RT mode, this register allows host access to the current or most recent Subaddress Control Word. The Subaddress Control Word is used to select the memory management scheme and enable interrupts for the current message.

4.7 Time Tag Register

The Time Tag Register maintains the value of a real-time clock. The resolution of this register is programmable from among 2, 4, 8, 16, 32, and 64 µs/LSB. The Start-of-Message (SOM) and End-of-Message (EOM) sequences in BC, RT, and Message Monitor modes cause a write of the current value of the Time Tag Register to the stack area of the RAM.

4.8 Interrupt Status Registers #1 and #2

Interrupt Status Registers #1 and #2 allow the host processor to determine the cause of an interrupt request by means of one or two read accesses. The interrupt events of the two Interrupt Status Registers are mapped to correspond to the respective bit positions in the two Interrupt Mask Registers. Interrupt Status Register #2 contains an INTERRUPT CHAIN bit, used to indicate an interrupt event from Interrupt Status Register #1.

4.9 Configuration Registers #3, #4, and #5

Configuration Registers #3, #4, and #5 are used to enable many of the PCI Total-ACE's advanced features that were implemented by the prior generation products, the ACE and Mini-ACE (Plus). For BC, RT, and MT modes, use of the Enhanced Mode enables the various read-only bits in Configuration Register #1. For BC mode, Enhanced Mode features include the expanded BC Control Word and BC Block Status Word, additional Stop-On-Error and Stop-On-Status Set functions, frame auto-repeat, programmable intermessage gap times, automatic retries, expanded Status Word Masking, and the capability to generate interrupts following the completion of any selected message. For RT mode, the Enhanced Mode features include the expanded RT Block Status Word, combined RT/Selective Message Monitor mode, internal wrapping of the $\overline{\text{RTFAIL}}$ output signal to the $\overline{\text{RTFLAG}}$ RT Status Word bit, and the alternate (fully software. programmable) RT Status Word. For MT mode, use of the Enhanced Mode enables the Selective Message Monitor, the combined RT/Selective Monitor modes, and the monitor triggering capability.

4.10 RT/Monitor Data Stack Address Register

The RT/Monitor Data Stack Address Register provides a read/writable indication of the last data word stored for RT or Monitor modes.

4.11 BC Frame Time Remaining Register

The BC Frame Time Remaining Register provides a read-only indication of the time remaining in the current BC frame. In the enhanced BC mode, this timer may be used for minor or major frame control, or as a watchdog timer for the BC message sequence control processor. The resolution of this register is 100 µs/LSB.

4.12 BC Time Remaining to Next Message Register

The BC Time Remaining to Next Message Register provides a read-only indication of the time remaining before the start of the next message in a BC frame. In the enhanced BC mode, this timer may also be used for the BC message sequence control processor's Delay (DLY) instruction, or for minor or major frame control. The resolution of this register is 1 µs/LSB.

4.13 BC Frame Time / RT Last Command / MT Trigger Word Register

In BC mode, this register is used to program the BC frame time, for use in the frame auto-repeat mode. The resolution of this register is 100 µs/LSB, with a range up to 6.55 seconds. In RT mode, this register stores the current (or most previous) 1553 Command Word processed by the PCI Total-ACE RT. In the Word Monitor mode, this register is used to specify a 16-bit Trigger (Command) Word. The Trigger Word may be used to start or stop the monitor, or to generate interrupts.

4.14 BC Initial Instruction List Point Register

The BC Initial Instruction List Pointer Register enables the host to assign the starting address for the enhanced BC Instruction List.

4.15 RT Status Word Register and BIT Word Registers

The RT Status Word Register and BIT Word Registers provide read-only indications of the RT Status and BIT Words.

4.16 Configuration Registers #6 and #7

Configuration Registers #6 and #7 are used to enable the PCI Total-ACE features that extend beyond the architecture of the ACE/Mini-ACE (Plus). These include the Enhanced BC mode; Enhanced CPU Access (note that this bit is the only

configuration bit that is SET after reset), RT Global Circular Buffer (including buffer size); the RT/MT Interrupt Status Queue, including valid/invalid message filtering; enabling a software-assigned RT address; clock frequency selection; a base address for the "non-data" portion of PCI Total-ACE memory; LSB filtering for the Synchronize (with data) time tag operations; and enabling a watchdog timer for the Enhanced BC message sequence control engine.

Note: *Please see Appendix "F" of the Enhanced Mini-ACE User's Guide for important information applicable only to RT Mode operation, enabling of the interrupt status queue and use of specific non-message interrupts.*

4.17 BC Condition Code Register

The BC Condition Code Register is used to enable the host processor to read the current value of the Enhanced BC Message Sequence Control Engine's condition flags.

4.18 BC General Purpose Flag Register

The BC General Purpose Flag Register allows the host processor to be able to set, clear, or toggle any of the Enhanced BC Message Sequence Control Engine's General Purpose condition flags.

4.19 BIT Test Status Register

The BIT Test Status Register is used to provide read-only access to the status of the protocol and RAM built-in self-tests (BIT).

4.20 BC General Purpose Queue Pointer

The BC General Purpose Queue Pointer provides a means for initializing the pointer for the General Purpose Queue, for the Enhanced BC mode. In addition, this register enables the host to determine the current location of the General Purpose Queue pointer, which is incremented internally by the Enhanced BC message sequence control engine.

4.21 RT/MT Interrupt Status Queue Pointer

The RT/MT Interrupt Status Queue Pointer provides a means for initializing the pointer for the Interrupt Status Queue, for RT, MT, and RT/MT modes. In addition, this register enables the host to determine the current location of the Interrupt Status Queue pointer, which is incremented by the RT/MT message processor.

5 BUS CONTROLLER (BC) ARCHITECTURE

The BC functionality for the PCI Total-ACE includes two separate architectures: (1) the older, non-Enhanced Mode, which provides complete compatibility with the previous ACE and Mini-ACE (Plus) generation products; and (2) the newer, Enhanced BC mode. The Enhanced BC mode offers several new powerful architectural features. These include the incorporation of a highly autonomous BC message sequence control engine, which greatly serves to offload the operation of the host CPU.

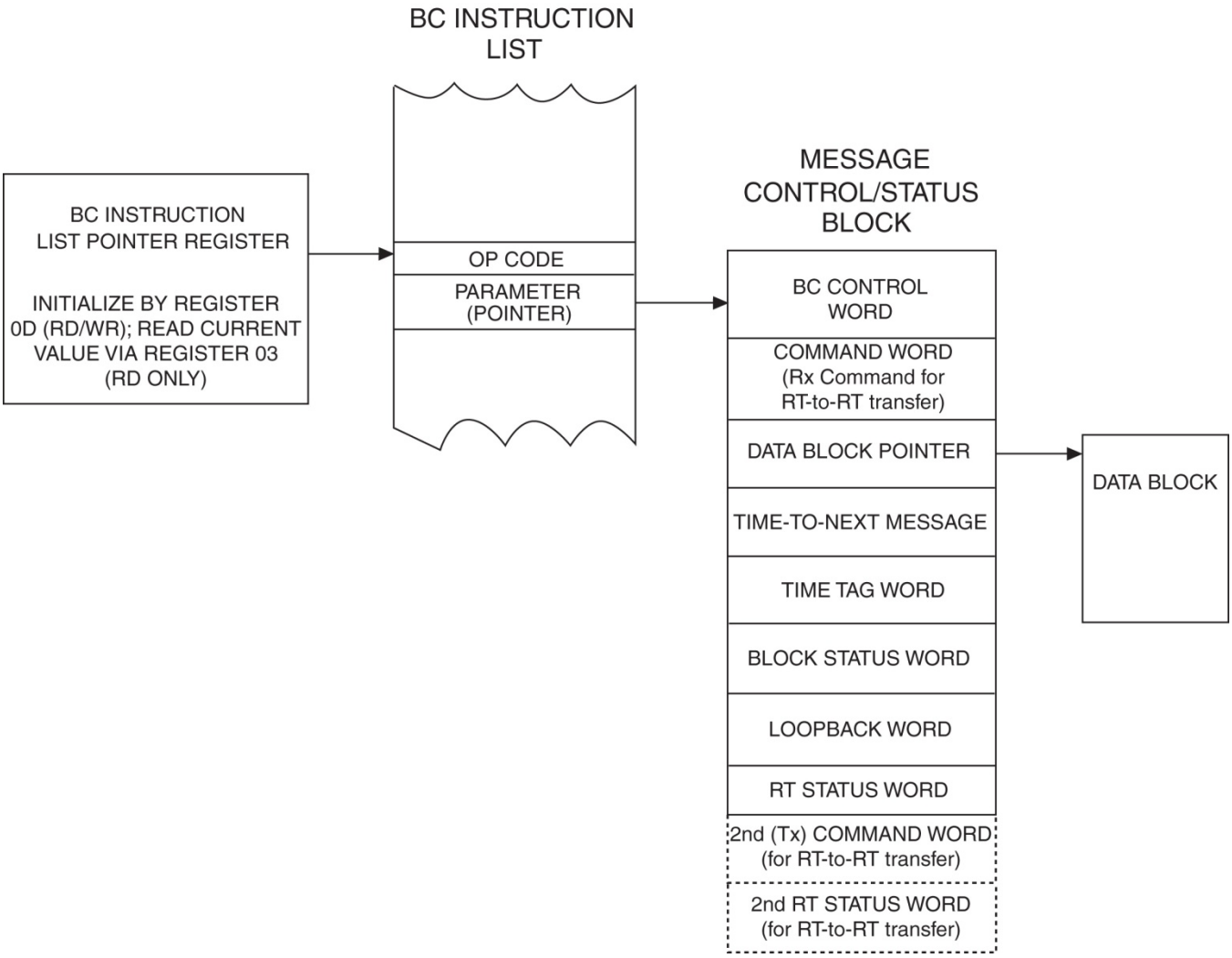


Figure 3. BC Message Sequence Control

The Enhanced BC's message sequence control engine provides a high degree of flexibility for implementing major and minor frame scheduling; capabilities for inserting asynchronous messages in the middle of a frame; to separate 1553 message data from control/status data for the purpose of implementing double buffering and performing bulk data transfers; for implementing message retry

schemes, including the capability for automatic bus channel switchover for failed messages; and for reporting various conditions to the host processor by means of four userdefined interrupts and a general purpose queue.

In both the non-Enhanced and Enhanced BC modes, the PCI Total-ACE BC implements all MIL-STD-1553B message formats. Message format is programmable on a message-by-message basis by means of the BC Control Word and the T/R bit of the Command Word for the respective message. The BC Control Word allows 1553 message format, 1553A/B type RT, bus channel, self-test, and Status Word masking to be specified on an individual message basis. In addition, automatic retries and/or interrupt requests may be enabled or disabled for individual messages. The BC performs all error checking required by MIL-STD-1553B. This includes validation of response time, sync type and sync encoding, Manchester II encoding, parity, bit count, word count, Status Word RT Address field, and various RT-to-RT transfer errors. The PCI Total-ACE BC response timeout value is programmable with choices of 18, 22, 50, and 130 µs. The longer response timeout values allow for operation over long buses and/or the use of repeaters.

In its non-Enhanced Mode, the PCI Total-ACE may be programmed to process BC frames of up to 512 messages with no processor intervention. In the Enhanced BC mode, there is no explicit limit to the number of messages that may be processed in a frame. In both modes, it is possible to program for either single frame or frame auto-repeat operation. In the auto-repeat mode, the frame repetition rate may be controlled either internally, using a programmable BC frame timer, or from an external trigger input.

5.1 Enhanced BC Mode: Message Sequence Control

One of the major new architectural features of the PCI Total-ACE series is its advanced capability for BC message sequence control. The PCI Total-ACE supports highly autonomous BC operation, which greatly offloads the operation of the host processor.

The operation of the PCI Total-ACE's message sequence control engine is illustrated in Figure 3. The BC message sequence control involves an instruction list pointer register; an instruction list which contains multiple 2-word entries; a message control/status stack, which contains multiple 8-word or 10-word descriptors; and data blocks for individual messages.

The initial value of the instruction list pointer register is initialized by the host processor (via Register 0D), and is incremented by the BC message sequence processor (host readable via Register 03). During operation, the message sequence control processor fetches the operation referenced by the instruction list pointer register from the instruction list.

Note that the pointer parameter referencing the first word of a message's control/status block (the BC Control Word) must contain an address value that is **modulo 8**. Also, note that if the message is an RT-to-RT transfer, the pointer parameter must contain an address value that is **modulo 16**.

5.2 OP Codes

The instruction list pointer register references a pair of words in the BC instruction list: an op code word, followed by a parameter word. The format of the op code word, which is illustrated in Figure 4, includes a 5-bit op code field and a 5-bit condition code field. The op code identifies the instruction to be executed by the BC message sequence controller.

Most of the operations are conditional, with execution dependent on the contents of the condition code field. Bits 3-0 of the condition code field identifies a particular condition. Bit 4 of the condition code field identifies the logic sense ("1" or "0") of the selected condition code on which the conditional execution is dependent. Table 52 lists all the op codes, along with their respective mnemonic, code value, parameter, and description. Table 53 defines all the condition codes.

Eight of the condition codes (8 through F) are set or cleared as the result of the most recent message. The other eight are defined as "General Purpose" condition codes GP0 through GP7. There are three mechanisms for programming the values of the General Purpose Condition Code bits: (1) They may be set, cleared, or toggled by the host processor, by means of the BC GENERAL PURPOSE FLAG REGISTER; (2) they may be set, cleared, or toggled by the BC message sequence control processor, by means of the GP Flag Bits (FLG) instruction; and (3) GP0 and GP1 only (but none of the others) may be set or cleared by means of the BC message sequence control processor's Compare Frame Timer (CFT) or Compare Message Timer (CMT) instructions.

Figure 4. BC OP Code Format

The host processor also has read-only access to the BC condition codes by means of the BC CONDITION CODE REGISTER.

Note that four (4) instructions are **unconditional**. These are Compare to Frame Timer (CFT), Compare to Message Timer (CMT), GP Flag Bits (FLG), and Execute and Flip (XQF). For these instructions, the Condition Code Field is "don't care". That

is, these instructions are **always** executed, regardless of the result of the condition code test.

All of the other instructions are conditional. That is, they will only be executed if the condition code specified by the condition code field in the op code word tests true. If the condition code field tests false, the instruction list pointer will skip down to the next instruction.

As shown in Table 52, many of the operations include a singleword parameter. For an XEQ (execute message) operation, the parameter is a pointer to the start of the message's Control / Status block. For other operations, the parameter may be an address, a time value, an interrupt pattern, a mechanism to set or clear general purpose flag bits, or an immediate value. For several op codes, the parameter is "don't care" (not used).

As described above, some of the op codes will cause the message sequence control processor to execute messages. In this case, the parameter references the first word of a message Control/Status block. With the exception of RT-to-RT transfer messages, all message status/control blocks are eight words long: a block control word, time-to-next-message parameter, data block pointer, command word, status word, loopback word, block status word, and time tag word.

In the case of an RT-to-RT transfer message, the size of the message control/status block increases to 16 words. However, in this case, the last six words are not used; the ninth and tenth words are for the second command word and second status word.

The third word in the message control/status block is a pointer that references the first word of the message's data word block. Note that the data word block stores only data words, which are to be either transmitted or received by the BC. By segregating data words from command words, status words, and other control and "housekeeping" functions, this architecture enables the use of convenient, usable data structures, such as circular buffers and double buffers.

Other operations support program flow control; i.e., jump and call capability. The call capability includes maintenance of a call stack which supports a maximum of four (4) entries; there is also a return instruction. In the case of a call stack overrun or underrun, the BC will issue a CALL STACK POINTER REGISTER ERROR interrupt, if enabled.

Other op codes may be used to delay for a specified time; start a new BC frame; wait for an external trigger to start a new frame; perform comparisons based on frame time and time-to-next message; load the time tag or frame time registers; halt; and issue host interrupts. In the case of host interrupts, the message control processor

passes a 4-bit user-defined interrupt vector to the host, by means of the Total-ACE's Interrupt Status Register.

The purpose of the FLG instruction is to enable the message sequence controller to set, clear, or toggle the value(s) of any or all of the eight general purpose condition flags.

The op code parity bit encompasses all sixteen bits of the op code word. This bit must be programmed for odd parity. If the message sequence control processor fetches an undefined op code word, an op code word with even parity, or bits 9-5 of an op code word do not have a binary pattern of 01010, the message sequence control processor will immediately halt the BC's operation. In addition, if enabled, a BC TRAP OP CODE interrupt will be issued. Also, if enabled, a parity error will result in an OP CODE PARITY ERROR interrupt. Table 53 describes the Condition Codes.

Table 52. BC Operations for Message Sequence Control

Instruction	Mnemonic	OP Code (Hex)	Parameter	Conditional or Unconditional	Description
Execute Message	XEQ	0001	Message Control / Status Block Address	Conditional (see Note)	Executes the message at the specified Message Contro/Status Block Address if the condition flag tests TRUE, otherwise continue execution at the next OpCode in the instruction list.
Jump	JMP	0002	Instruction List Address	Conditional	Jump to the OpCode specified in the Instruction List if the condition flag test TRUE, otherwise continue execution at the next OpCode in the instruction list.
Subroutine Call	CAL	0003	Instruction List Address	Conditional	Jump to the OpCode specified by the Instruction List Address and push the Address of the Next OpCode on the Call Stack if the condition flag tests TRUE, otherwise continue execution at the next OpCode in the instruction list. Note that the maximum depth of the subroutine call stack is **four**.
Subroutine Return	RTN	0004	Not Used (Don't Care)	Conditional	Return to the OpCode popped off the Call Stack if the condition flag tests TRUE, otherwise continue execution at the next OpCode in the instruction list.
Interrupt Request	IRQ	0006	Interrupt Bit Pattern in 4 LS bits	Conditional	Generate an interrupt if the condition flag tests TRUE, otherwise continue execution at the next OpCode in the instruction list. The passed parameter (Interrupt Bit Pattern) specifies which of the ENHANCED BC IRQ bit(s) (bits 5-2) will be set in Interrupt Status Register #2. Only the four LSBs of the passed parameter are used. A parameter where the four LSBs are logic "0" will **not** generate an interrupt.

Table 52. BC Operations for Message Sequence Control					
Instruction	**Mnemonic**	**OP Code (Hex)**	**Parameter**	**Conditional or Unconditional**	**Description**
Halt	HLT	0007	Not Used (Don't Care)	Conditional	Stop execution of the Message Sequence Control Program until a new BC Start is issued by the host if the condition flag tests TRUE, otherwise continue execution at the next OpCode in the instruction list.
Delay	DLY	0008	Delay Time Value (Resolution = 1µs / LSB)	Conditional	Delay the time specified by the Time parameter before executing the next OpCode if the condition flag tests TRUE, otherwise continue execution at the next OpCode without delay. The delay generated will use the Time to Next Message Timer.
Wait Until Frame Timer = 0	WFT	0009	Not Used (Don't Care)	Conditional	Wait until Frame Time counter is equal to Zero before continuing execution of the Message Sequence Control Program if the condition flag tests TRUE, otherwise continue execution at the next OpCode without delay.
Compare to Frame Timer	CFT	000A	Delay Time Value (Resolution = 1µs / LSB)	Unconditional	Compare Time Value to Frame Time Counter. The LT/GP0 and EQ/GP1 flag bits are set or cleared based on the results of the compare. If the value of the CFT's parameter is less than the value of the frame time counter, then the LT/GP0 flag will be set, while the EQ/GP1 flag will be cleared. If the value of the CFT's parameter is equal to the value of the frame time counter, then the EQ/GP1 flag will be set, while the LT/GP0 flag will be cleared. If the value of the CFT's parameter is greater than the current value of the frame time counter, the LT/GP0 and EQ/GP1 flags will be cleared.
Compare to Message Timer	CMT	000B	Delay Time Value (Resolution = 1µs / LSB)	Unconditional	Compare Time Value to Message Time Counter. The LT/GP0 and EQ/GP1 flag bits are set or cleared based on the results of the compare. If the value of the CMT's parameter is less than the value of the message time counter, then the LT/GP0 flag will be set, while the GT-EQ/GP0 and EQ/GP1 flags will be cleared. If the value of the CMT's parameter is equal to the value of the message time counter, then the EQ/GP1 flag will be set, while the LT/GP0 flag will be cleared. If the value of the CMT's parameter is greater than the current value of the message time counter, then the LT/GP0 and EQ/GP1 flags will be cleared.

Table 52. BC Operations for Message Sequence Control

Instruction	Mnemonic	OP Code (Hex)	Parameter	Conditional or Unconditional	Description
GP Flag Bits	FLG	000C	Used to set, clear, or toggle GP (General Purpose) Flag bits (see description)	Unconditional	Used to set, toggle, or clear any or all of the eight general purpose flags. The table below illustrates the use of the GP Flag Bits instruction for the case of GP0 (General Purpose Flag 0). Bits 1 and 9 of the parameter byte affect flag GP1, bits 2 and 10 effect GP2, etc., according to the following rules:

Bit 8	Bit 0	Effect on GP0
0	0	No Change
0	1	Set Flag
1	0	Clear Flag
1	1	Toggle Flag

Load Time Tag Counter	LTT	000D	Time Value Resolution (µs/ LSB) is defined by bits 9, 8, & 7 of Configuration Register #2	Conditional	Load Time Tag Counter with Time Value if the condition flag tests TRUE, otherwise continue execution at the next OpCode in the instruction list.
Load Frame Timer	LFT	000E	Time Value (resolution = 100 µs/LSB)	Conditional	Load Frame Timer Register with the Time Value parameter if the condition flag tests TRUE, otherwise continue execution at the next OpCode in the instruction list.
Start Frame Timer	SFT	000F	Not Used (Don't Care)	Conditional	Start Frame Time Counter with Time Value in Time Frame register if the condition flag tests TRUE, otherwise continue execution at the next OpCode in the instruction list.
Push Time Tag Register	PTT	0010	Not Used (Don't Care)	Conditional	Push the value of the Time Tag Register on the General Purpose Queue if the condition flag tests TRUE, otherwise continue execution at the next OpCode in the instruction list.
Push Block Status Word	PBS	0011	Not Used (Don't Care)	Conditional	Push the Block Status Word for the most recent message on the General Purpose Queue if the condition flag tests TRUE, otherwise continue execution at the next OpCode in the instruction list.
Push Immediate Value	PSI	0012	Immediate Value	Conditional	Push Immediate data on the General Purpose Queue if the condition flag tests TRUE, otherwise continue execution at the next OpCode in the instruction list.
Push Indirect	PSM	0013	Memory Address	Conditional	Push the data stored at the specified memory location on the General Purpose Queue if the condition flag tests TRUE, otherwise continue execution at the next OpCode in the instruction list.

Table 52. BC Operations for Message Sequence Control					
Instruction	**Mnemonic**	**OP Code (Hex)**	**Parameter**	**Conditional or Unconditional**	**Description**
Wait for External Trigger	WTG	0014	Not Used (Don't Care)	Conditional	Wait for a logic "0"-to-logic "1" transition on the EXT_TRIG input signal before proceeding to the next OpCode in the instruction list if the condition flag tests TRUE, otherwise continue execution at the next OpCode without delay.
Execute and Flip	XQF	0015	Message Control / Status Block Address	Unonditional	Execute (unconditionally) the message referenced by the Message Control/Status Block Address. Following the processing of this message, if the condition flag tests TRUE, the BC will toggle bit 4 in the Message Control/Status Block Address, and store the new Message Block Address as the updated value of the parameter following the XQF instruction code. As a result, the **next** time that this line in the instruction list is executed, the Message Control/Status Block at the **updated** address (**old address XOR 0010h**), rather than the old address, will be processed. If the condition flag tests FALSE, the value of the Message Control/Status Block Address parameter will not change.

Note: While the XEQ (Execute Message) instruction is conditional, not all condition codes may be used to enable its use. The ALWAYS and NEVER condition codes may be used. The eight general purpose flag bits, GP0 through GP7, may also be used. However, if GP0 through GP7 are used, it is imperative that the host processor not modify the value of the specific general purpose flag bit that enabled a particular message while that message is being processed. Similarly, the LT, GT-EQ, EQ, and NE flags, which the BC only updates by means of the CFT and CMT instructions, may also be used. However, these two flags are dual use. Therefore, if these are used, it is imperative that the host processor not modify the value of the specific flag (GP0 or GP1) that enabled a particular message while that message is being processed. The NORESP, FMT ERR, GD BLK XFER, MASKED STATUS SET, BAD MESSAGE, RETRY0, and RETRY1 condition codes are not available for use with the XEQ instruction and should not be used to enable its execution

Table 53. BC Condition Codes			
BIT Code	**Name (BIT 4 = 0)**	**Inverse (BIT 4 = 1)**	**Functional Description**
0	LT/GP0	GT-EQ / $\overline{\text{GP0}}$	Less than or GP0 flag. This bit is set or cleared based on the results of the compare. If the value of the CMT's parameter is less than the value of the message time counter, then the LT/GP0 flag will be set. If the value of the CMT's parameter is greater than or equal to the value of the message time counter, then the LT/GP0 flag will be cleared. Also, General Purpose Flag 1 may be set or cleared by a FLG operation.
1	EQ/GP1	NE/ $\overline{\text{GP1}}$	Equal Flag. This bit is set or cleared after CFT or CMT operation. If the value of the CMT's parameter is equal to the value of the message time counter, then the EQ/GP1 flag will be set. If the value of the CMT's parameter is not equal to the value of the message time counter, then the EQ/GP1 flag will be cleared. Also, General Purpose Flag 1 may be set or cleared by a FLG operation.
2	GP2	$\overline{\text{GP2}}$	General Purpose Flags may be set, cleared, or toggled by a FLG operation. The host processor can set, clear, or toggle these flags in the same way as the FLG instruction by means of the BC GENERAL PURPOSE FLAG REGISTER.
3	GP3	$\overline{\text{GP3}}$	
4	GP4	$\overline{\text{GP4}}$	
5	GP5	$\overline{\text{GP5}}$	
6	GP6	$\overline{\text{GP6}}$	
7	GP7	$\overline{\text{GP7}}$	
8	NORESP	$\overline{\text{RESP}}$	NORESP indicates that an RT has either not responded or has responded later than the BC No Response Timeout time. The Total-ACE's No Response Timeout Time is defined per MIL-STD-1553B as the time from the mid-bit crossing of the parity bit of the last word transmitted by the BC to the mid-sync crossing of the RT Status Word. The value of the No Response Timeout value is programmable from among the nominal values 18.5, 22.5, 50.5, and 130 µs (±1 µs) by means of bits 10 and 9 of Configuration Register #5.
9	FMT ERR	$\overline{\text{FMT ERR}}$	FMT ERR indicates that the received portion of the most recent message contained one or more violations of the 1553 message validation criteria (sync, encoding, parity, bit count, word count, etc.), or the RT's status word received from a responding RT contained an incorrect RT address field.
A	GD BLK XFER	$\overline{\text{GD BLK XFER}}$	For the most recent message, GD BLK XFER will be set to logic "1" following completion of a valid (error-free) RT-to-BC transfer, RT-to-RT transfer, or transmit mode code with data message. This bit is set to logic "0" following an invalid message. GOOD DATA BLOCK TRANSFER is **always** logic "0" following a BC-to-RT transfer, a mode code with data, or a mode code without data. The Loop Test has **no effect** on GOOD DATA BLOCK TRANSFER. GOOD DATA BLOCK TRANSFER may be used to determine if the transmitting portion of an RT-to-RT transfer was error free.

Table 53. BC Condition Codes

BIT Code	Name (BIT 4 = 0)	Inverse (BIT 4 = 1)	Functional Description
B	MASKED STATUS BIT	$\overline{\text{MASKED STATUS BIT}}$	Indicates that one or both of the following conditions have occurred for the most recent message: (1) If one (or more) of the Status Mask bits (14 through 9) in the BC Control Word is logic "0" **and** the corresponding bit(s) is (are) set (logic "1") in the received RT Status Word. In the case of the RESERVED BITS MASK (bit 9) set to logic "0," any or all of the 3 Reserved Status Word bits being set will result in a MASKED STATUS SET condition; and/or (2) If BROADCAST MASK ENABLED/ $\overline{\text{XOR}}$ (bit 11 of Configuration Register #4) is logic "1" **and** the MASK BROADCAST bit of the message's BC Control Word is logic "0" and the BROADCAST COMMAND RECEIVED bit in the received RT Status Word is logic "1."
C	BAD MESSAGE	GOOD MESSAGE	BAD MESSAGE indicates either a format error, loop test fail, or no response error for the most recent message. Note that a "Status Set" condition has **no effect** on the "BAD MESSAGE/GOOD MESSAGE" condition code.
D	RETRY0	$\overline{\text{RETRY0}}$	These two bits reflect the retry status of the most recent message. The number of times that the message was retried is delineated by these two bits as shown below: Retry Count 1 (bit 14) / Retry Count 2 (bit 13) / Number of Message Retries 0 / 0 / 0 0 / 1 / 1 1 / 0 / N/A 1 / 1 / 2
E	RETRY1	$\overline{\text{RETRY1}}$	
F	ALWAYS	NEVER	The ALWAYS flag should be set (bit 4 = 0) to designate an instruction as unconditional. The NEVER bit (bit 4 = 1) can be used to implement a NOP or "skip" instruction.

5.3 BC Message Sequence Control

The PCI Total-ACE BC message sequence control capability enables a high degree of offloading of the host processor. This includes using the various timing functions to enable autonomous structuring of major and minor frames. In addition, by implementing conditional jumps and subroutine calls, the message sequence control processor greatly simplifies the insertion of asynchronous, or "out-of-band" messages.

5.3.1 Execute and Flip Operation

The PCI Total-ACE BC's XQF, or "Execute and Flip" operation, provides some unique capabilities. Following execution of this unconditional instruction, if the condition code tests TRUE, the BC will modify the value of the current XQF

instruction's pointer parameter by toggling bit 4 of the pointer. That is, if the selected condition flag tests true, the value of the parameter will be **updated** to the value = **old address XOR 0010h**. As a result, the next time that this line in the instruction list is executed, the Message Control/Status Block at the updated address (old address XOR 0010h) will be processed, rather than the one at the old address. The operation of the XQF instruction is illustrated in Figure 5.

There are multiple ways of utilizing the "execute and flip" instruction. One is to facilitate the implementation of a double buffering data scheme for individual messages. This allows the message sequence control processor to "ping-pong" between a pair of data buffers for a particular message. By doing so, the host processor can access one of the two Data Word blocks, while the BC reads or writes the alternate Data Word block.

A second application of the "execute and flip" capability is in conjunction with message retries. This allows the BC to not only switch buses when retrying a failed message, but to automatically switch buses **permanently** for all future times that the same message is to be processed. This not only provides a high degree of autonomy from the host CPU, but saves BC bandwidth, by eliminating the need for future attempts to process messages on an RT's failed channel.

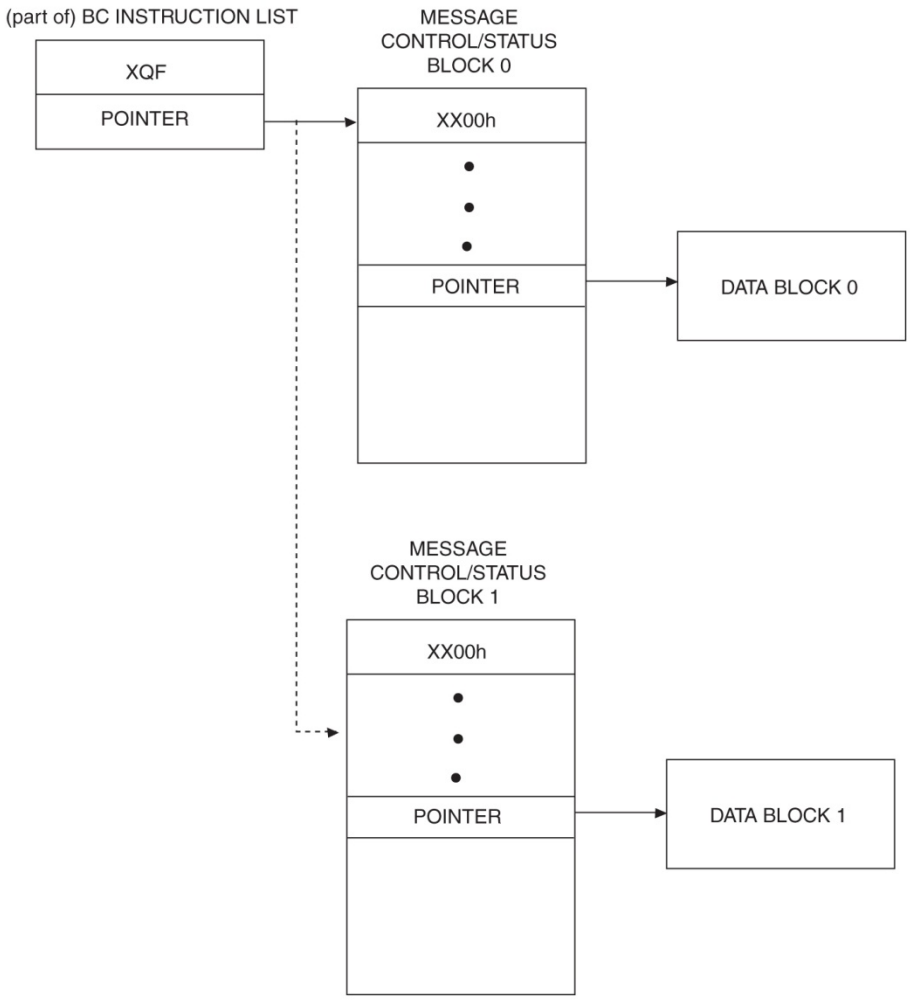


Figure 5. EXECUTE and FLIP (XQF) Operation

5.3.2 General Purpose Queue

The PCI Total-ACE BC allows for the creation of a general purpose queue. This data structure provides a means for the message sequence processor to convey information to the BC host. The BC op code repertoire provides mechanisms to push various items on this queue. These include the contents of the Time Tag Register, the Block Status Word for the most recent message, an immediate data value, or the contents of a specified memory address.

Figure 6 illustrates the operation of the BC General Purpose Queue. Note that the BC General Purpose Queue Pointer Register will always point to the **next** address location (modulo 64); that is, the location **following** the last location written by the BC message sequence control engine.

If enabled, a BC GENERAL PURPOSE QUEUE ROLLOVER interrupt will be issued when the value of the queue pointer address rolls over at a 64-word boundary. The rollover will always occur at a modulo 64 address.

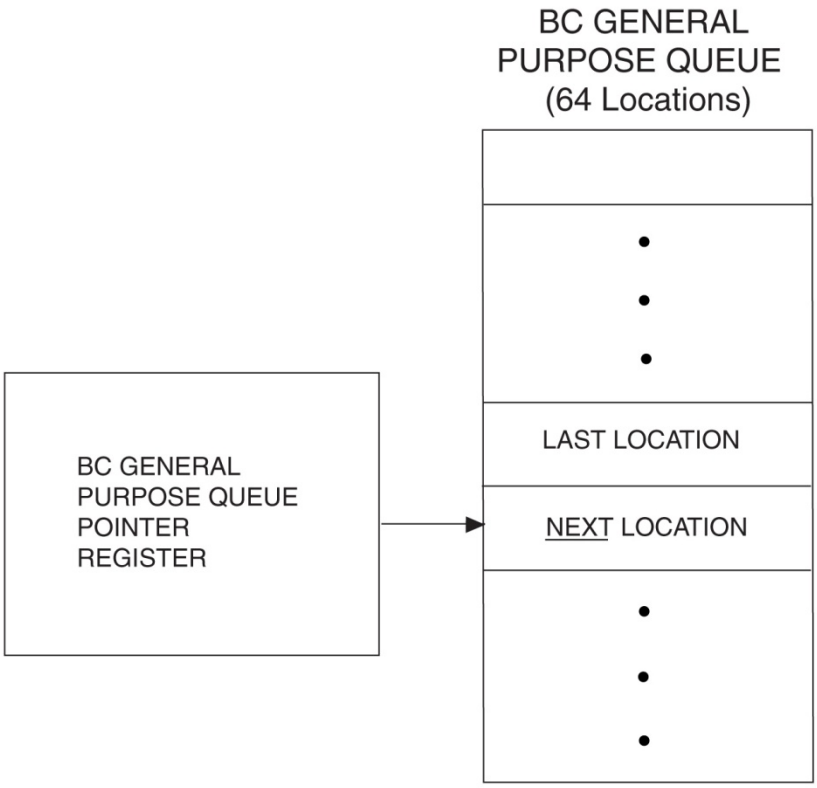


Figure 6. BC General Purpose Queue

6 REMOTE TERMINAL (RT) ARCHITECTURE

The PCI Total-ACE's RT architecture builds upon that of the ACE and Mini-ACE. The PCI Total-ACE provides multiprotocol support, with full compliance to all of the commonly used data bus standards, including MIL-STD-1553A, MIL-STD-1553B Notice 2, STANAG 3838, General Dynamics 16PP303, and McAirA3818, A5232, and A5690. For the PCI Total-ACE RT mode, there is programmable flexibility enabling the RT to be configured to fulfill any set of system requirements. This includes the capability to meet the MIL-STD-1553A response time requirement of 2 to 5 µs, and multiple options for mode code subaddresses, mode codes, RT status word, and RT BIT word.

The PCI Total-ACE RT protocol design implements all of the MILSTD-1553B message formats and dual redundant mode codes. The design has passed validation testing for MIL-STD-1553B compliance. The PCI Total-ACE RT performs comprehensive error checking including word and format validation, and checks for various RT-to-RT transfer errors. One of the main features of the PCI Total-ACE RT is its choice of memory management options. These include single buffering by subaddress, circular buffering by individual subaddresses, and global circular buffering for multiple (or all) subaddresses.

Other features of the PCI Total-ACE RT include a set of interrupt conditions, an interrupt status queue with filtering based on valid and/or invalid messages, internal command illegalization, programmable busy by subaddress, multiple options on time tagging.

6.1 RT Memory Organization

Table 54 illustrates a typical memory map for an PCI Total-ACE RT with 4K RAM. Note that this table and subsequent references to it are using word addressing: PCI BAR0 address offsets (byte addresses) are TWO times the word addresses indicated. The two Stack Pointers reside in fixed locations in the shared RAM address space: address 0100h (PCI BAR0 offset 0200h) for the Area A Stack Pointer and address 0104h (PCI BAR0 offset 208h) for the Area B Stack Pointer. In addition to the Stack Pointer, there are several other areas of the shared RAM address space that are designated as fixed locations (all shown in bold). These are for the Area A and Area B lookup tables, the illegalization lookup table, the busy lookup table, and the mode code data tables.

The RT lookup tables (see Table 55) provide a mechanism for allocating data blocks for individual transmit, receive, or broadcast subaddresses. The RT lookup tables include subaddress control words as well as the individual data block pointers. If command illegalization is used, address range 0300-03FF is used for command illegalizing. The descriptor stack RAM area, as well as the individual data blocks, may be located in any of the non-fixed areas in the shared RAM address space.

Note that in Table 54, there is no area allocated for "Stack B". This is shown for purpose of simplicity of illustration. Also, note that in Table 54, the allocated area for the RT command stack is 256 words. However, larger stack sizes are possible. That is, the RT command stack size may be programmed for 256 words (64 messages), 512, 1024, or 2048 words (512 messages) by means of bits 14 and 13 of Configuration Register 3.

Table 54. Typical RT Memory Map (Shown for 4K RAM)

Word Address (HEX)	PCI Bar0 Offset (HEX)	Description
0000-00FF	0000-01FE	Stack A
0100	0200	**Stack Pointer A**
0101	0202	**Global Circular Buffer A Pointer**
0102-0103	0204-0206	RESERVED
0104	0208	**Stack Pointer B**
0105	020A	**Global Circular Buffer B Pointer**
0106-0107	020C-020E	RESERVED
0108-010F	0210-021E	**Mode Code Selective Interrupt Table**
0110-013F	0220-027E	**Mode Code Data**
0140-01BF	0280-037E	**Lookup Table A**
01C0-023F	0380-047E	**Lookup Table B**
0240-0247	0480-048E	**Busy Bit Lookup Table**
0248-025F	0490-04BE	(not used)
0260-027F	04C0-04FE	Data Block 0
0280-02FF	0500-05FE	Data Block 1-4
0300-03FF	0600-07FE	**Command Illegalization Table**
0400-041F	0800-083FE	Data Block 5
0420-043F	0800-083E	Data Block 6
□	•	□
□	•	□
□	•	□
0FE0-0FFF	1FC0-1FFE	Data Block 100

Table 55. RT Look-up Tables					
Area A (Internal Memory Offset)	**Area A (PCI Bar0 Offset)**	**Area B (Internal Memory Offset)**	**Area B (PCI Bar0 Offset)**	**Description**	**Comment**
0140 □ □ □ 015F	0280 □ □ □ 02BE	01C0 □ □ □ 01DF	0380 □ □ □ 03BE	Rx(/Bcst) SA0 □ □ □ Rx(/Bcst) SA31	Receive (/Broadcast) Lookup Pointer Table
0160 □ □ □ 017F	02C0 □ □ □ 02FE	01E0 □ □ □ 01FF	03C0 □ □ □ 03FE	Tx SA0 □ □ □ Tx SA31	Transmit Lookup Pointer Table
0180 □ □ □ 019F	0300 □ □ □ 033E	0200 □ □ □ 021F	0400 □ □ □ 043F	Bcst SA0 □ □ □ Bcst SA31	Braodcast Lookup Pointer Table (Optional)
01A0 □ □ □ 01BF	0340 □ □ □ 037E	0220 □ □ □ 023F	0440 □ □ □ 047E	SACW SA0 □ □ □ SACW SA31	Subaddress Control Word Lookup Table (Optional)

6.2 RT Memory Management

The PCI Total-ACE provides a variety of RT memory management capabilities. As with the ACE and Mini-ACE (Plus), and Enhanced Mini-ACE the choice of memory management scheme is fully programmable on a transmit/receive/broadcast subaddress basis.

In compliance with MIL-STD-1553B Notice 2, received data from broadcast messages may be optionally separated from nonbroadcast received data. For each transmit, receive or broadcast subaddress, either a single-message data block, a double buffered configuration (two alternating Data Word blocks), or a variable-sized (128 to 8192 words) subaddress circular buffer may be allocated for data storage. The memory management scheme for individual subaddresses is designated by means of the subaddress control word (reference Table 56).

For received data, there is also a global circular buffer mode. In this configuration, the data words received from multiple (or all) subaddresses are stored in a common circular buffer structure. Like the subaddress circular buffer, the size of the global circular buffer is programmable, with a range of 128 to 8192 data words.

The double buffering feature provides a means for the host processor to easily access the most recent, complete received block of valid Data Words for any given

subaddress. In addition to helping ensure data sample consistency, the circular buffer options provide a means for greatly reducing host processor overhead for multi-message bulk data transfer applications.

End-of-message interrupts may be enabled either globally (following all messages), following error messages, on a transmit/receive/broadcast subaddress or mode code basis, or when a circular buffer reaches its midpoint (50% boundary) or lower (100%) boundary. A pair of interrupt status registers allow the host processor to determine the cause of all interrupts by means of a single read operation.

Table 56. RT Subaddress Control Word – Memory Management Options

Double-Buffered or Global circular Buffer (bit 15)	Subaddress Control Word Bits			Memory Management Subaddress Buffer Scheme Description	
	MM2	MM1	MM0		
0	0	0	0	Single Message	
1	0	0	0	For Receive or Broadcast: Double Buffered For Transmit: Single Message	
0	0	0	1	128-Word	Subaddress – specified circular buffer of specified size.
0	0	1	0	256-Word	
0	0	1	1	512-Word	
0	1	0	0	1024-Word	
0	1	0	1	2048-Word	
0	1	1	0	4096-Word	
0	1	1	1	8192-Word	
1	1	1	1	(for receive and/or broadcast subaddress only) Global Circular Buffer: The buffer size is specified by Configuration Register #6, bits 11-9. The pointer to the global circular buffer is stored at address 0101 (for Area A) or address 0105 (for Area B)	

6.3 Single Buffered Mode

The operation of the single buffered RT mode is illustrated in Figure 7. In the single buffered mode, the respective lookup table entry must be written by the host processor. Received data words are written to, or transmitted data words are read from the data word block with starting address referenced by the lookup table pointer. In the single buffered mode, the current lookup table pointer is not updated by the Total-ACE memory management logic. Therefore, if a subsequent message is received for the same subaddress, the **same** Data Word block will be overwritten or overread.

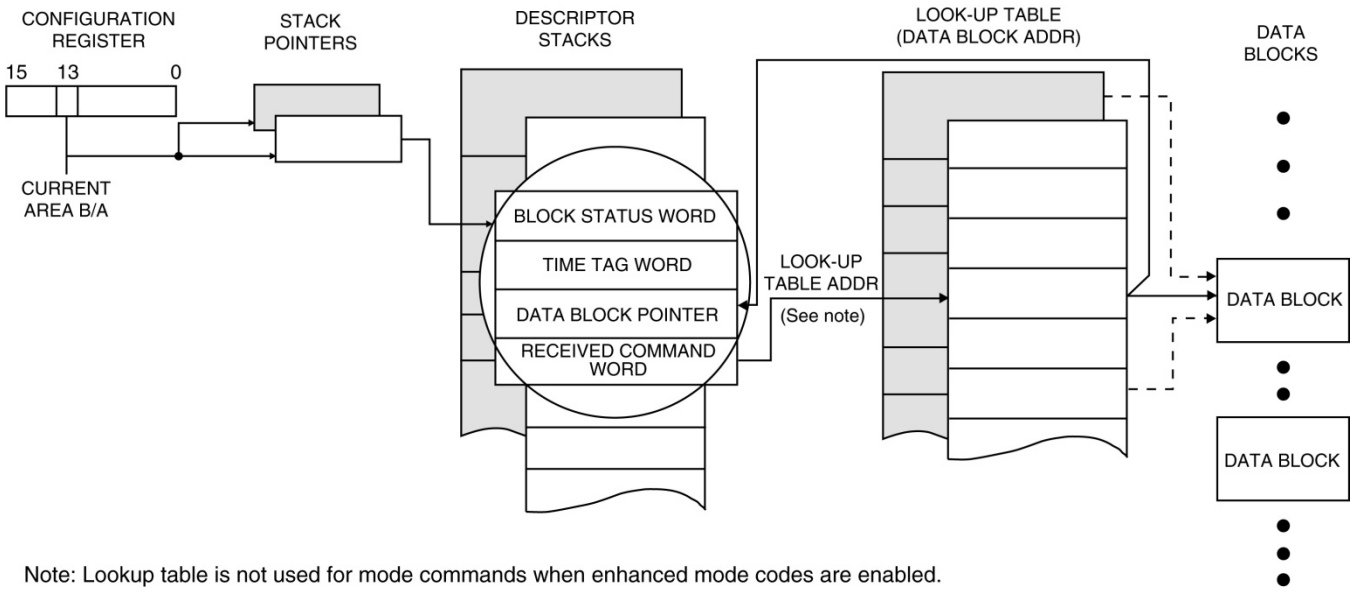


Figure 7. RT Single Buffered Mode

6.4 CIRCULAR BUFFER MODE

The operation of the PCI Total-ACE's circular buffer RT memory management mode is illustrated in Figure 8. As in the single buffered and double buffered modes, the individual lookup table entries are initially loaded by the host processor. At the start of each message, the lookup table entry is stored in the third position of the respective message block descriptor in the descriptor stack area of RAM. Receive or transmit data words are transferred to (from) the circular buffer, starting at the location referenced by the lookup table pointer.

In general, the location after the last data word written or read (modulo the circular buffer size) during the message is written to the respective lookup table location during the end-of-message sequence. By so doing, data for the next message for the respective transmit, receive(/broadcast), or broadcast subaddress will be accessed from the next lower contiguous block of locations in the circular buffer.

For the case of a receive (or broadcast receive) message with a data word error, there is an option such that the lookup table pointer will only be updated following receipt of a **valid** message. That is, the pointer will **not** be updated following receipt of a message with an error in a data word. This allows failed messages in a bulk data transfer to be retried without disrupting the circular buffer data structure, and without intervention by the RT's host processor.

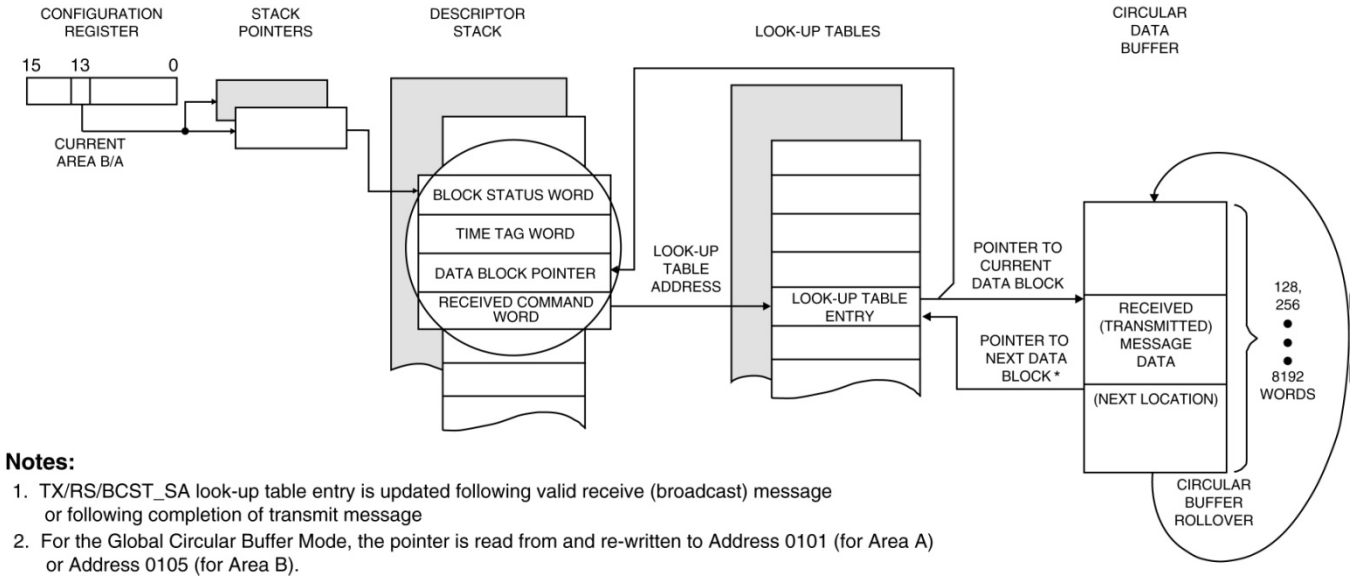
6.5 GLOBAL CIRCULAR BUFFER

Beyond the programmable choice of single buffer mode or circular buffer mode, programmable on an individual subaddress basis, the PCI Total-ACE architecture provides an additional option, a variable sized **global** circular buffer.

In the global circular buffer mode, the data for **multiple** receive subaddresses is stored in the same circular buffer data structure. The size of the global circular buffer may be programmed for 128, 256, 512, 1024, 2048, 4096, or 8192 words, by means of bits 11, 10, and 9 of Configuration Register #6. As shown in Table 56, individual subaddresses may be mapped to the global circular buffer by means of their respective subaddress control words.

The pointer to the Global Circular Buffer will be stored in location 0101 (for Area A, PCI BAR0 offset 0202h), or location 0105h (for Area B, PCI BAR0 offset 020Ah)

The global circular buffer option provides a highly efficient method for storing received message data. It allows for frequently used subaddresses to be mapped to individual data blocks, while also providing a method for asynchronously received messages to infrequently used subaddresses to be logged to a common area. Alternatively, the global circular buffer provides an efficient means for storing the received data words for all subaddresses. Under this method, all received data words are stored chronologically, regardless of subaddress.



Notes:

1. TX/RS/BCST_SA look-up table entry is updated following valid receive (broadcast) message or following completion of transmit message
2. For the Global Circular Buffer Mode, the pointer is read from and re-written to Address 0101 (for Area A) or Address 0105 (for Area B).

Figure 8. RT Circular Buffered Mode

6.6 RT DESCRIPTOR STACK

The descriptor stack provides a chronology of all messages processed by the PCI Total-ACE RT. Reference Figure 7 and Figure 8. Similar to BC mode, there is a four-word block descriptor in the Stack for each message processed. The four entries to each block descriptor are the Block Status Word, Time Tag Word, the pointer to the start of the message's data block, and the 16-bit received Command Word.

The RT Block Status Word includes indications of whether a particular message is ongoing or has been completed, what bus channel it was received on, indications of illegal commands, and flags denoting various message error conditions. For the double buffering, subaddress circular buffering, and global circular buffering modes, the data block pointer may be used for locating the data blocks for specific messages. Note that for mode code commands, there is an option to store the transmitted or received data word as the third word of the descriptor, in place of the data block pointer.

The Time Tag Word provides a 16-bit indication of relative time for individual messages. The resolution of the Total-ACE's time tag is programmable from among 2, 4, 8, 16, 32, or 64 µs/LSB. There is also a provision for using an external clock input for the time tag. If enabled, there is a time tag rollover interrupt, which is issued when the value of the time tag rolls over from FFFF(hex) to 0. Other time tag options include the capabilities to clear the time tag register following receipt of a Synchronize (without data) mode command and/or to set the time tag following receipt of a Synchronize (with data) mode command. For the latter, there is an added option to filter the "set" capability based on the LSB of the received data word being equal to logic "0".

6.7 RT INTERRUPTS

The PCI Total-ACE offers a great deal of flexibility in terms of RT interrupt processing. By means of the PCI Total-ACE’s two Interrupt Mask Registers, the RT may be programmed to issue interrupt requests for the following events/conditions: End-of-(every) Message, Message Error, Selected (transmit or receive) Subaddress, 100% Circular Buffer Rollover, 50% Circular Buffer Rollover, 100% Descriptor Stack Rollover, 50% Descriptor Stack Rollover, Selected Mode Code, Transmitter Timeout, Illegal Command, and Interrupt Status Queue Rollover.

6.7.1 Interrupts for 50% Rollovers of Stacks and Circular Buffers.

The PCI Total-ACE RT and Monitor are capable of issuing host interrupts when a subaddress circular buffer pointer or stack pointer crosses its mid-point boundary. For RT circular buffers, this is applicable for both transmit and receive subaddresses. Reference Figure 9. There are four interrupt mask and interrupt status register bits associated with the 50% rollover function:

1. RT circular buffer;
2. RT command (descriptor) stack;
3. Monitor command (descriptor) stack; and
4. Monitor data stack.

The 50% rollover interrupt is beneficial for performing bulk data transfers. For example, when using circular buffering for a particular receive subaddress, the 50% rollover interrupt will inform the host processor when the circular buffer is half full. At that time, the host may proceed to read the received data words in the upper half of the buffer, while the PCI Total-ACE RT writes received data words to the lower half of the circular buffer. Later, when the RT issues a 100% circular buffer rollover interrupt, the host can proceed to read the received data from the lower half of the buffer, while the PCI Total-ACE RT continues to write received data words to the upper half of the buffer.

6.7.2 Interrupt status queue.

The PCI Total-ACE RT, Monitor, and combined RT/Monitor modes include the capability for generating an interrupt status queue. As illustrated in Figure 10, this provides a chronological history of interrupt generating events and conditions. In addition to the Interrupt Mask Register, the Interrupt Status Queue provides additional filtering capability, such that only valid messages and/or only invalid messages may result in the creation of an entry to the Interrupt Status Queue. Queue entries for invalid and/or valid messages may be disabled by means of bits 8 and 7 of configuration register #6.

The pointer to the Interrupt Status Queue is stored in the INTERRUPT VECTOR QUEUE POINTER REGISTER (register address 1F). This register must be initialized by the host, and is subsequently incremented by the RT message processor. The interrupt status queue is 64 words deep, providing the capability to store entries for up to 32 messages.

The queue rolls over at addresses of modulo 64. The events that result in queue entries include both message-related and nonmessage-related events. Note that the Interrupt Vector Queue Pointer Register will always point to the next location (modulo 64) **following** the last vector/pointer pair written by the PCI Total-ACE RT, Monitor, or RT/Monitor.

Each event that causes an interrupt results in a two-word entry to be written to the queue. The first word of the entry is the interrupt vector. The vector indicates which interrupt event(s)/condition(s) caused the interrupt.

The interrupt events are classified into two categories: message interrupt events and non-message interrupt events. Messagebased interrupt events include End-of-Message, Selected mode code, Format error, Subaddress control word interrupt, RT Circular buffer Rollover, Handshake failure, RT Command stack rollover, transmitter timeout, MT Data Stack rollover, MT Command Stack rollover, RT Command Stack 50% rollover, MT Data Stack 50% rollover, MT Command Stack 50% rollover, and RT Circular buffer 50% rollover. Non-message interrupt events/conditions include time tag rollover, RT address parity error, RAM parity error, and BIT completed.

Bit 0 of the interrupt vector (interrupt status) word indicates whether the entry is for a message interrupt event (if bit 0 is logic "1") or a non-message interrupt event (if bit 0 is logic "0"). It is **not** possible for one entry on the queue to indicate both a message interrupt and a non-message interrupt.

As illustrated in Figure 10, for a message interrupt event, the parameter word is a pointer. The pointer will reference the first word of the RT or MT command stack descriptor (i.e., the Block Status Word).

For a RAM Parity Error non-message interrupt, the parameter will be the RAM address where the parity check failed. For the RT address Parity Error, Protocol Self-test Complete, and Time Tag rollover non-message interrupts, the parameter is not used; it will have a value of 0000.

If enabled, an INTERRUPT STATUS QUEUE ROLLOVER interrupt will be issued when the value of the queue pointer address rolls over at a 64-word address boundary.

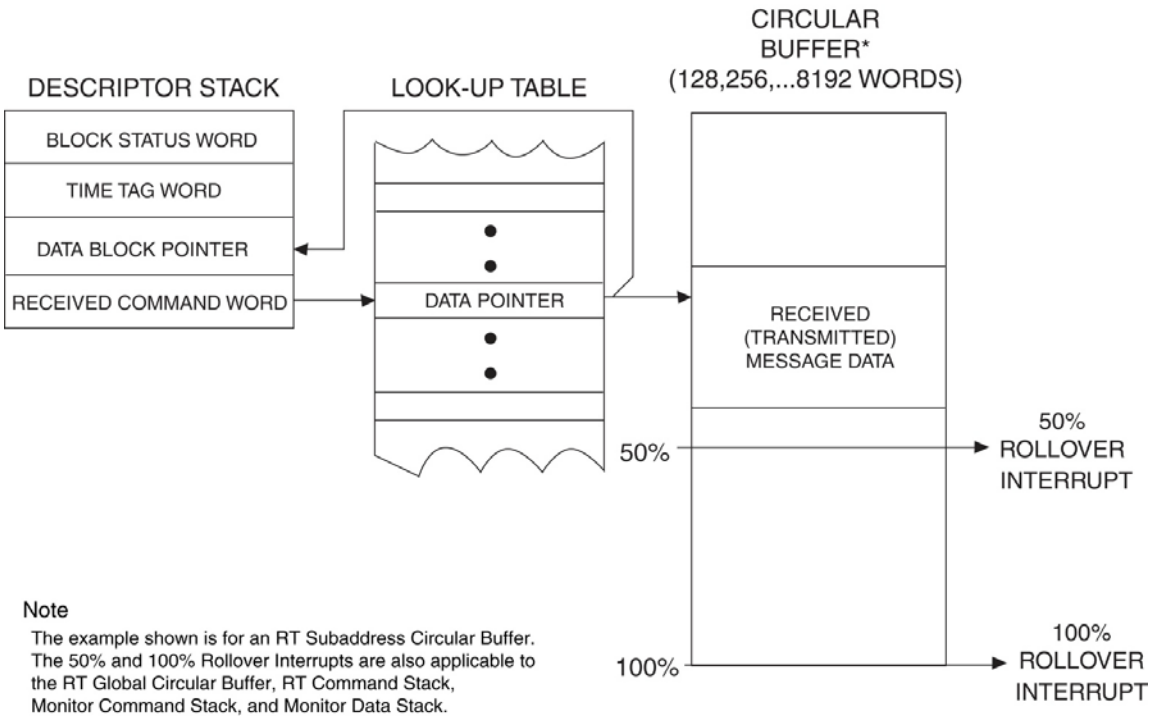


Figure 9. 50% and 100% Rollover Interrupts

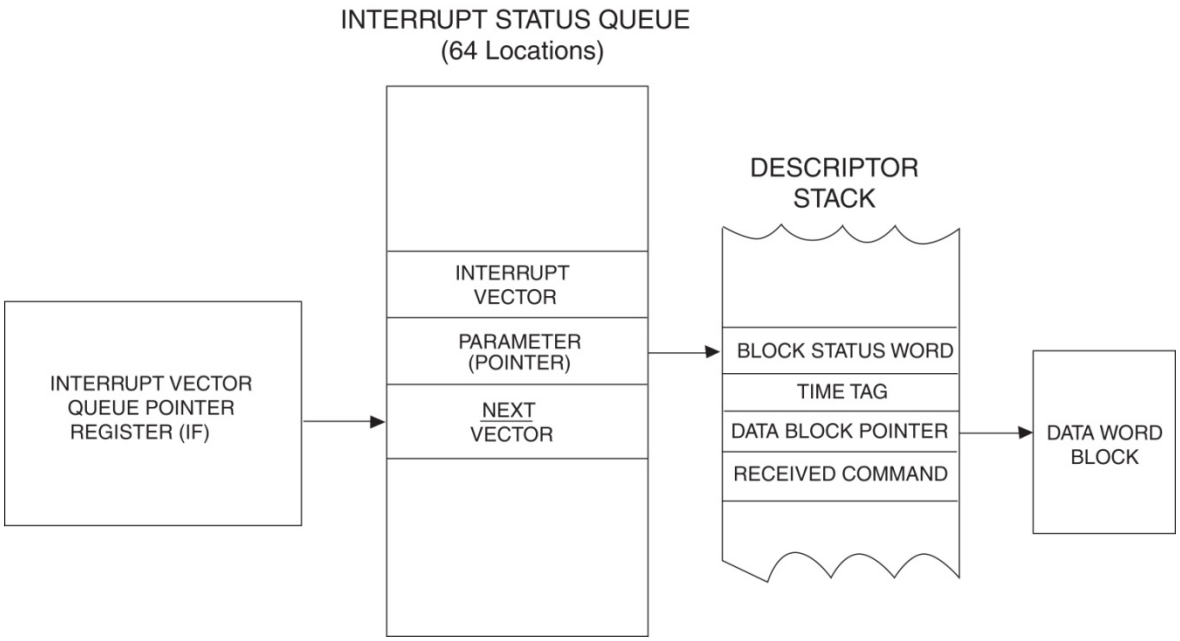


Figure 10. RT (and Monitor) Interrupt Status Queue

(shown for message interrupt event)

6.8 RT COMMAND ILLEGALIZATION

The PCI Total-ACE provides an internal mechanism for RT Command Word illegalizing. By means of a 256-word area in shared RAM, the host processor may designate that any message be illegalized, based on the command word T/R bit, subaddress, and word count/mode code fields. The PCI Total-ACE illegalization scheme provides the maximum in flexibility, allowing any subset of the 4096 possible combinations of broadcast/own address, T/R bit, subaddress, and word count/mode code to be illegalized.

The address map of the PCI Total-ACE's illegalizing table is illustrated in Table 57.

Table 57. Illegalization Table Memory Map

Address	PCI Bar0 Offset	Description
300	600	Brdcst/Rx, SA 0. MC15-0
301	602	Brdcst/Rx, SA 0. MC31-16
302	604	Brdcst/Rx, SA 1. WC15-0
303	606	Brdcst/Rx, SA 1. WC31-16
□ □ □	□ □ □	□ □ □
33F	67E	Brdcst/Rx, SA 31. MC31-16
340	680	Brdcst/Tx, SA 0. MC15-0
341	682	Brdcst/Tx, SA 0. MC31-16
342	684	Brdcst/Tx, SA 1. WC15-0
□ □ □	□ □ □	□ □ □
37D	6FA	Brdcst/Tx, SA 30. WC31-16
37E	6FC	Brdcst / Tx, SA 31. MC15-0
37F	6FE	Brdcst / Tx, SA 31. MC31-16
380	700	Own Addr / Rx, SA 0. MC15-0
381	702	Own Addr / Rx, SA 0. MC31-16
382	704	Own Addr / Rx, SA 1. WC15-0
383	706	Own Addr / Rx, SA 1. WC31-16
□ □ □	□ □ □	□ □ □
3BE	77C	Own Addr / Rx, SA 31. MC15-0
3BF	77E	Own Addr / Rx, SA 31. MC31-16
3C0	780	Own Addr / Tx, SA 0. MC15-0

Table 57. Illegalization Table Memory Map		
Address	**PCI Bar0 Offset**	**Description**
3C1	782	Own Addr / Tx, SA 0. MC31-16
3C2	784	Own Addr / Tx, SA 1. WC15-0
3C3	786	Own Addr / Tx, SA 1. WC31-16
□ □ □	□ □ □	□ □ □
3FC	7F8	Own Addr / Tx, SA 30. WC15-0
3FD	7FA	Own Addr / Tx, SA 30. WC31-16
3FE	7FC	Own Addr / Tx, SA 31. MC15-0
3FF	7FE	Own Addr / Tx, SA 31. MC31-16

6.9 BUSY BIT

The PCI Total-ACE RT provides two different methods for setting the Busy status word bit: (1) globally, by means of Configuration Register #1; or (2) on a T/R-bit/subaddress basis, by means of a RAM lookup table. If the host CPU asserts the BUSY bit to logic “0” in Configuration Register #1, the PCI Total-ACE RT will respond to **all** non-broadcast commands with the Busy bit set in its RT Status Word.

Alternatively, there is a Busy lookup table in the PCI Total-ACE shared RAM. By means of this table, it is possible for the host processor to set the busy bit for any selectable subset of the 128 combinations of broadcast/own address, T/R bit, and subaddress.

If the busy bit is set for a transmit command, the PCI Total-ACE RT will respond with the busy bit set in the status word, but will not transmit any data words. If the busy bit is set for a receive command, the RT will also respond with the busy status bit set. There are two programmable options regarding the reception of data words for a non-mode code receive command for which the RT is busy: (1) to transfer the received data words to shared RAM; or (2) to **not** transfer the data words to shared RAM.

6.10 RT ADDRESS

The PCI Total-ACE offers several different options for designating the Remote Terminal address. These include the following: (1) hardwired, by means of the 5 RT ADDRESS inputs, and the RT ADDRESS PARITY input; (2) by means of the RT ADDRESS (and PARITY) inputs, but latched via hardware, on the rising edge of the RT_AD_LAT input signal; (3) input by means of the RT ADDRESS (and PARITY) inputs, but latched via host software; and (4) software programmable, by means of an

internal register. In all four configurations, the RT address is readable by the host processor.

6.11 RT BUILT-IN-TEST (BIT) WORD

The bit map for the PCI Total-ACE's internal RT Built-in-Test (BIT) Word is indicated in Table 58.

6.12 OTHER RT FEATURES

The PCI Total-ACE includes options for the Terminal flag status word bit to be set either under software control and/or automatically following a failure of the loopback self-test. Other software programmable RT options include software programmable RT status and RT BIT words, automatic clearing of the Service Request bit following receipt of a Transmit vector word mode command, options regarding Data Word transfers for the Busy and Message error (illegal) Status word bits, and options for the handling of 1553A and reserved mode codes.

Table 58. RT BIT Word

BIT	Description
15 (MSB)	Transmitter Timeout
14	Loop Test Failure B
13	Loop Test Failure A
12	Handshake Failure
11	Transmitter Shutdown B
10	Transmitter Shutdown A
9	Terminal Flag Inhibited
8	BIT Test Failure
7	High Word Count
6	Low Word Count
5	Incorrect Sync Received
4	Parity/Manchester error Received
3	RT-to-RT Gap/Sync Address Error
2	RT-to-RT No Response Error
1	RT-to-RT 2nd Command Word Error
0 (LSB)	Command Word Contents Error

7 MONITOR ARCHITECTURE

The PCI Total-ACE includes three monitor modes:

1. A Word Monitor mode
2. A selective message monitor mode
3. A combined RT/message monitor mode

For new applications, it is recommended that the selective message monitor mode be used, rather than the word monitor mode. Besides providing monitor filtering based on RT address, T/R bit, and subaddress, the message monitor eliminates the need to determine the start and end of messages by software.

7.1 WORD MONITOR MODE

In the Word Monitor Terminal mode, the PCI Total-ACE monitors both 1553 buses. After the software initialization and Monitor Start sequences, the PCI Total-ACE stores all Command, Status, and Data Words received from both buses. For each word received from either bus, a pair of words is stored to the PCI Total-ACE's shared RAM. The first word is the word received from the 1553 bus. The second word is the Monitor Identification (ID), or "Tag" word. The ID word contains information relating to bus channel, word validity, and inter-word time gaps. The data and ID words are stored in a circular buffer in the shared RAM address space.

7.2 WORD MONITOR MEMORY MAP

A typical word monitor memory map is illustrated in Table 59. Table 59 assumes a 64K address space for the PCI Total-ACE's monitor. The Active Area Stack pointer provides the address where the first monitored word is stored. In the example, it is assumed that the Active Area Stack Pointer for Area A (location 0100) is initialized to 0000. The first received data word is stored in location 0000, the ID word for the first word is stored in location 0001, etc.

The current Monitor address is maintained by means of a counter register. This value may be read by the CPU by means of the Data Stack Address Register. It is important to note that when the counter reaches the Stack Pointer address of 0100 or 0104, the initial pointer value stored in this shared RAM location **will be overwritten** by the monitored data and ID Words. When the internal counter reaches an address of FFFF (or 0FFF, for an Total-ACE with 4K RAM), the counter rolls over to 0000.

7.3 WORD MONITOR TRIGGER

In the Word Monitor mode, there is a pattern recognition trigger and a pattern recognition interrupt. The 16-bit compare word for both the trigger and the interrupt is stored in the Monitor Trigger Word Register. The pattern recognition interrupt is

enabled by setting the MT Pattern Trigger bit in Interrupt Mask Register #1. The pattern recognition trigger is enabled by setting the Trigger Enable bit in Configuration Register #1 and selecting either the Start-on-trigger or the Stop-on-trigger bit in Configuration Register #1. The Word Monitor may also be started by means of a low-to-high transition on the EXT_TRIG input signal.

7.4 SELECTIVE MESSAGE MONITOR MODE

The PCI Total-ACE Selective Message Monitor provides monitoring of 1553 messages with filtering based on RT address, T/R bit, and subaddress with no host processor intervention. By autonomously distinguishing between 1553 command and status words, the Message Monitor determines when messages begin and end, and stores the messages into RAM, based on a programmable filter of RT address, T/R bit, and subaddress.

The selective monitor may be configured as just a monitor, or as a **combined RT/Monitor.** In the combined RT/Monitor mode, the PCI Total-ACE functions as an RT for one RT address (including broadcast messages), and as a selective message monitor for the other 30 RT addresses. The PCI Total-ACE Message Monitor contains two stacks, a command stack and a data stack, that are independent from the RT command stack. The pointers for these stacks are located at fixed locations in RAM.

Table 59. Typical Word Monitor Memory Map

Hex Address	Function
0000	First Received 1553 Word
0001	First Identification Word
0002	Second Received 1553 Word
0003	Second Identification 1553 Word
0004	Third Received 1553 Word
0005	Third Identification Word
□ □ □	□ □ □
0100	Stack Pointer (Fixed Location – gets overwritten)
□ □ □	□ □ □
FFFF	Received 1553 Words and Identification Word

7.5 MONITOR SELECTION FUNCTION

Following receipt of a valid command word in Selective Monitor mode, the PCI Total-ACE will reference the selective monitor lookup table to determine if the particular command is enabled. The address for this location in the table is determined by means of an offset based on the RT Address, T/$\overline{R}$ bit, and Subaddress bit 4 of the current command word, and concatenating it to the monitor lookup table base address of 0280 (hex). The bit location within this word is determined by subaddress bits 3-0 of the current command word.

If the specified bit in the lookup table is logic "0", the command is not enabled, and the PCI Total-ACE will ignore this command. If this bit is logic "1", the command is enabled and the Total-ACE will create an entry in the monitor command descriptor stack (based on the monitor command stack pointer), and store the data and status words associated with the command into sequential locations in the monitor data stack. In addition, for an RT-to-RT transfer in which the receive command is selected, the second command word (the transmit command) is stored in the monitor data stack.

The address definition for the Selective Monitor Lookup Table is illustrated in Table 60.

Table 60. RT BIT Word

BIT	Description
15 (MSB)	Logic “0”
14	Logic “0”
13	Logic “0”
12	Logic “0”
11	Logic “0”
10	Logic “0”
9	Logic “1”
8	Logic “0”
7	Logic “1”
6	RTAD_4
5	RTAD_3
4	RTAD_2
3	RTAD_1
2	RTAD_0
1	TRANSMIT/$\overline{\text{RECEIVE}}$
0 (LSB)	Subaddress 4

7.6 SELECTIVE MESSAGE MONITOR MEMORY ORGANIZATION

A typical memory map for the PCI Total-ACE in the Selective Message Monitor mode, assuming a 4K RAM space, is illustrated in Table 61. This mode of operation defines several fixed locations in the RAM. These locations are allocated in a way in which none of them overlap with the fixed RT locations. This allows for the combined RT/Selective Message Monitor mode.

The fixed memory map consists of two Monitor Command Stack Pointers (locations 102 and 106 hex), two Monitor Data Stack Pointers (locations 103 and 107 hex), and a Selective Message Monitor Lookup Table (locations 0280 through 02FF hex). For this example, the Monitor Command Stack size is assumed to be 1K words, and the Monitor Data Stack size is assumed to be 2K words.

Figure 11 illustrates the Selective Message Monitor operation. Upon receipt of a valid Command Word, the PCI Total-ACE will reference the Selective Monitor Lookup Table to determine if the current command is enabled. If the current command is disabled, the PCI Total-ACE monitor will ignore (and not store) the current message. If the command is enabled, the monitor will create an entry in the Monitor Command Stack at the address location referenced by the Monitor Command Stack Pointer, and an entry in the monitor data stack starting at the location referenced by the Monitor Data Stack Pointer.

The format of the information in the data stack depends on the format of the message that was processed. For example, for a BC-to-RT transfer (receive command), the monitor will store the command word in the monitor command descriptor stack, with the data words and the receiving RT's status word stored in the monitor data stack.

The size of the monitor command stack is programmable, with choices of 256, 1K, 4K, or 16K words. The monitor data stack size is programmable with choices of 512, 1K, 2K, 4K, 8K, 16K, 32K or 64K words.

7.7 MONITOR INTERRUPTS

Selective monitor interrupts may be issued for End-of-message and for conditions relating to the monitor command stack pointer and monitor data stack pointer. The latter, as shown in Figure 9, include Command Stack 50% Rollover, Command Stack 100% Rollover, Data Stack 50% Rollover, and Data Stack 100% Rollover.

The 50% rollover interrupts may be used to inform the host processor when the command stack or data stack is half full. At that time, the host may proceed to read the received messages in the upper half of the respective stack, while the PCI Total-

ACE monitor writes messages to the lower half of the stack. Later, when the monitor issues a 100% stack rollover interrupt, the host can proceed to read the received data from the lower half of the stack, while the PCI Total-ACE monitor continues to write received data words to the upper half of the stack.

Table 61. Typical Selective Message Monitor Memory Map (shown for 4K RAM for "Monitor only" mode)

Address (Hex)	Function
0000-0101	Not Used
0102	Monitor Command Stack Pointer A (fixed location)
0103	Monitor Data Stack Pointer A (fixed location)
0104-0105	Not Used
0106	Monitor Command Stack Pointer B (fixed location)
0107	Monitor Data Stack Pointer B (fixed location)
0108-027F	Not Used
0280-02FF	Selective Monitor Lookup Table (fixed location)
0300-03FF	Not Used
0400-07FF	Monitor Command Stack A
0800-0FFF	Monitor Data Stack A

7.8 INTERRUPT STATUS QUEUE

Like the PCI Total-ACE RT, the Selective Monitor mode includes the capability for generating an interrupt status queue. As illustrated in Figure 10, this provides a chronological history of interrupt generating events. Besides the two Interrupt Mask Registers, the Interrupt Status Queue provides additional filtering capability, such that only valid messages and/or only invalid messages may result in entries to the Interrupt Status Queue. The interrupt status queue is 64 words deep, providing the capability to store entries for up to 32 monitored messages.

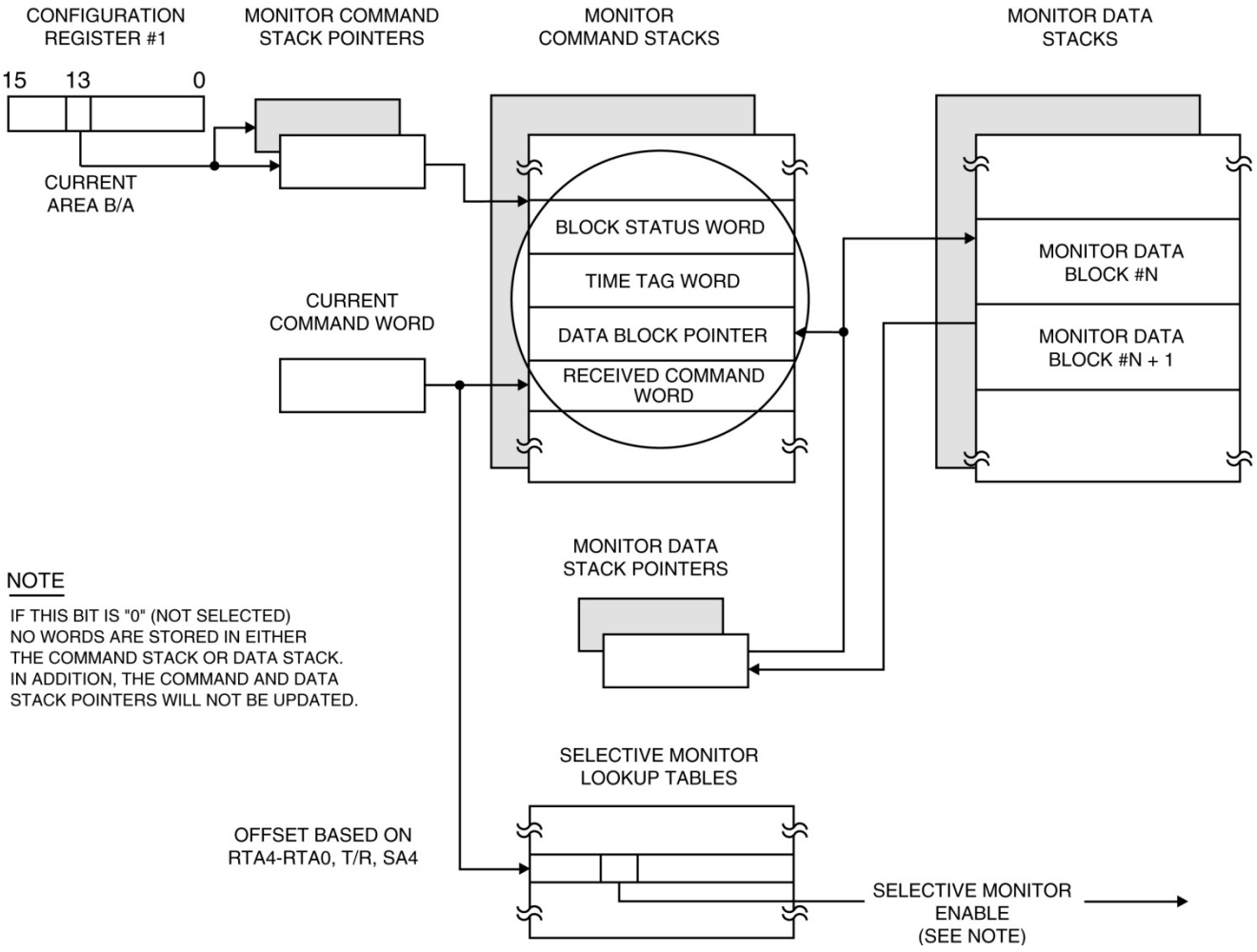


Figure 11. Selective Message Monitor Memory Management

8 MISCELLANEOUS

8.1 1553 CLOCK INPUT

The PCI Total-ACE decoder is capable of operating from a 10, 12, 16, or 20 MHz clock input. The clock frequency may be specified by means of the host processor writing to Configuration Register #6. In addition when PCI Total-ACE parts have their RTBOOT_L ball asserted, the 1553 input clock divider is controlled by the CLK_SEL 0 and CLK_SEL_1 balls.

8.2 ENCODER/DECODERS

For the selected clock frequency, there is internal logic to derive the necessary clocks for the Manchester encoder and decoders. For all clock frequencies, the decoders sample the receiver outputs on both edges of the input clock. By in effect doubling the decoders' sampling frequency, this serves to widen the tolerance to zero-crossing distortion, and reduce the bit error rate.

8.3 TIME TAG

The PCI Total-ACE includes an internal read/writable Time Tag Register. This register is a CPU read/writable 16-bit counter with a programmable resolution of either 2, 4, 8, 16, 32, or 64 ms per LSB. In addition, this register can be incremented directly by the TAG_CLK input pin by writing all ones to the time tag resolution bits. Another option allows software controlled incrementing of the Time Tag Register. This supports self-test for the Time Tag Register. For each message processed, the value of the Time Tag Register is loaded into the second location of the respective descriptor stack entry ("TIME TAG WORD") for BC/RT/MT modes.

The functionality of the Time Tag Register is compatible with ACE/Mini-ACE (Plus) includes: the capability to issue an interrupt request and set a bit in the Interrupt Status Register when the Time Tag Register rolls over FFFF to 0000; for RT mode, the capability to automatically clear the Time Tag Register following reception of a Synchronize (without data) mode command, or to load the Time Tag Register following a Synchronize (with data) mode command.

Additional time tag features supported by the PCI Total-ACE include the capability for the BC to transmit the contents of the Time Tag Register as the data word for a Synchronize (with data) mode command; the capability for the RT to "filter" the data word for the Synchronize with data mode command, by only loading the Time Tag Register if the LSB of the received data word is "0"; an instruction enabling the BC Message Sequence Control engine to autonomously load the Time Tag Register with a specified value; and an instruction enabling the BC Message Sequence Control engine to write the value of the Time Tag Register to the General Purpose Queue.

8.4 INTERRUPTS

The PCI Total-ACE series terminals provide many programmable options for interrupt generation and handling. The interrupt output pin ($\overline{\text{INT}}$) has two software programmable modes of operation: a level output cleared under software control or a level output automatically cleared following a read of the Interrupt Status Register (#1 or #2).

Individual interrupts are enabled by the two Interrupt Mask Registers. The host processor may determine the cause of the interrupt by reading the two Interrupt Status Registers, which provide the current state of interrupt events and conditions. The Interrupt Status Registers may be updated in two ways. In one interrupt handling mode, a particular bit in Interrupt Status Register #1 or #2 will be updated only if the event occurs and the corresponding bit in Interrupt Mask Register #1 or #2 is enabled. In the enhanced interrupt handling mode, a particular bit in one of the Interrupt Status Registers will be updated if the event/condition occurs regardless of the value of the corresponding Interrupt Mask Register bit. In either case, the respective Interrupt Mask Register (#1 or #2) bit is used to enable an interrupt for a particular event/condition.

Individual interrupts are enabled by the two Interrupt Mask Registers. The host processor may determine the cause of the interrupt by reading the two Interrupt Status Registers, which provide the current state of interrupt events and conditions. The Interrupt Status Registers may be updated in two ways. In one interrupt handling mode, a particular bit in Interrupt Status Register #1 or #2 will be updated only if the event occurs and the corresponding bit in Interrupt Mask Register #1 or #2 is enabled. In the enhanced interrupt handling mode, a particular bit in one of the Interrupt Status Registers will be updated if the event/condition occurs regardless of the value of the corresponding Interrupt Mask Register bit. In either case, the respective Interrupt Mask Register (#1 or #2) bit is used to enable an interrupt for a particular event/condition.

The PCI Total-ACE supports all the interrupt events from ACE/Mini-ACE (Plus) and Enhanced Mini-ACE including RAM Parity Error, Transmitter Timeout, BC/RT Command Stack Rollover, MT Command Stack and Data Stack Rollover, Handshake Error, BC Retry, RT Address Parity Error, Time Tag Rollover, RT Circular Buffer Rollover, BC Message, RT Subaddress, BC End-of-Frame, Format Error, BC Status Set, RT Mode Code, MT Trigger, and End-of-Message.

For the PCI Total-ACE's Enhanced BC mode, there are four userdefined interrupt bits. The BC Message Sequence Control. Engine includes an instruction enabling it to issue these interrupts at any time.

For RT and Monitor modes, the PCI Total-ACE architecture includes an Interrupt Status Queue. This provides a mechanism for logging messages that result in interrupt requests. Entries to the Interrupt Status Queue may be filtered such that only valid and/or invalid messages will result in entries on the queue.

The PCI Total-ACE incorporates additional interrupt conditions beyond ACE/Mini-ACE (Plus), based on the addition of Interrupt Mask Register #2 and Interrupt Status Register #2. This is accomplished by chaining the two Interrupt Status Registers using the INTERRUPT CHAIN BIT (bit 0) in Interrupt Status Register #2 to indicate that an interrupt has occurred in Interrupt Status Register #1. Additional interrupts include "Self-Test Completed", masking bits for the Enhanced BC Control Interrupts, 50% Rollover interrupts for RT Command Stack, RT Circular Buffers, MT Command Stack, and MT Data Stack; BC Op Code Parity Error, (RT) Illegal Command, (BC) General Purpose Queue or (RT/MT) Interrupt Status Queue Rollover, Call Stack Pointer Register Error, BC Trap Op Code, and four User-Defined interrupts for the Enhanced BC mode.

8.5 RAM PARITY

The PCI Total-ACE is available with options of 4K or 64K words of internal RAM. For the 64K option, the RAM is 17 bits wide. The 64K X 17 internal RAM allows for parity generation for RAM write accesses, and parity checking for RAM read accesses. When the PCI Total-ACE detects a RAM parity error, it reports it to the host processor by means of an interrupt and a register bit. Also, for the RT and Selective Message Monitor modes, the RAM address(es) where a parity error(s) was detected will be stored on the Interrupt Status Queue (if enabled).

Figure 12 illustrates a generic connection diagram between a PCI "Initiator" and a PCI Total-ACE "Target."

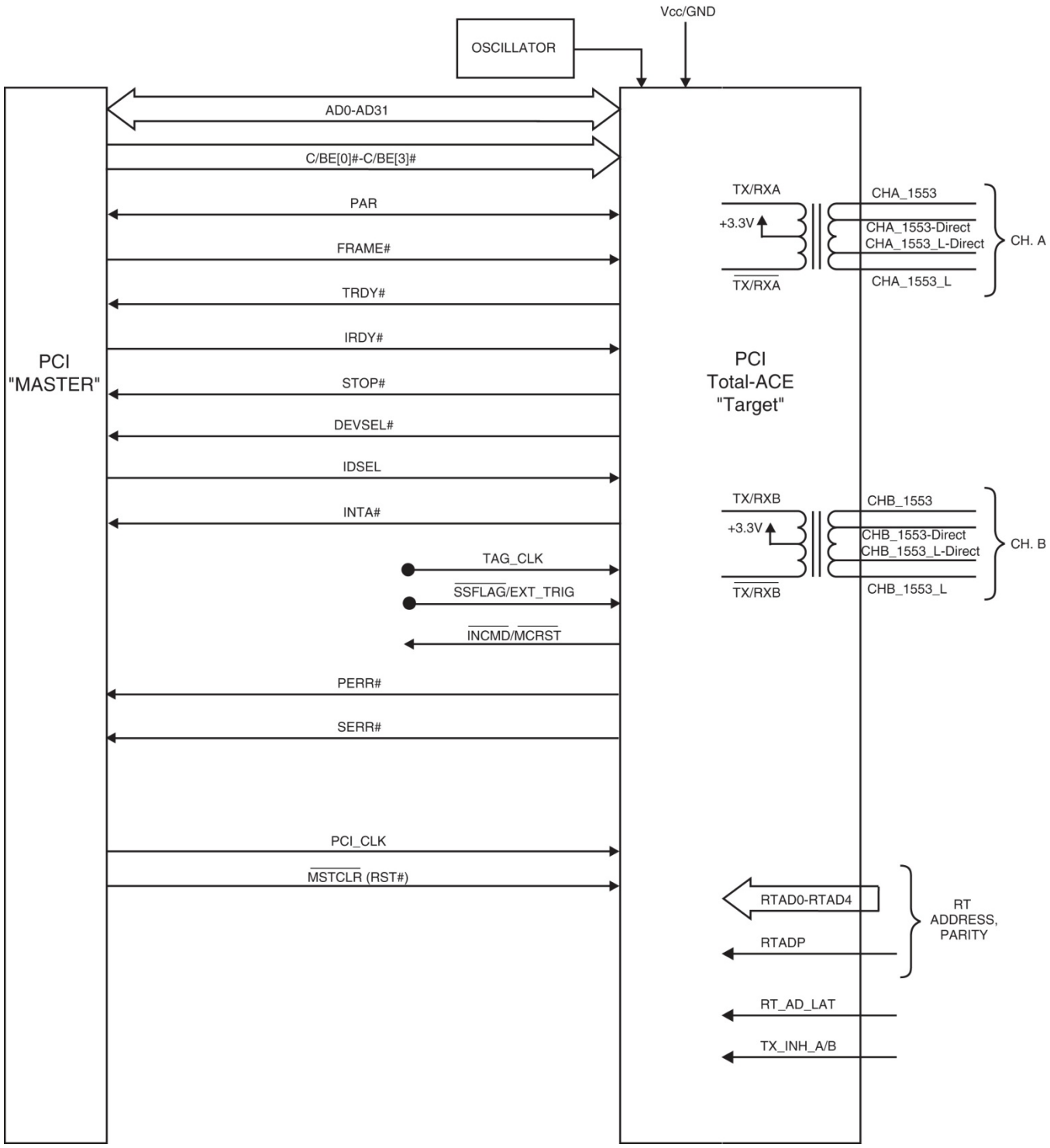


Figure 12. PCI Initiator to PCI Total-ACE Target Interface

The following timing diagrams illustrate the PCI commands that the PCI Total-ACE responds to. Note that these diagrams are meant to show the basic PCI bus operation of the PCI Total-ACE itself and do not show masters inserting wait states,

masters burst reading or writing past address boundaries, masters writing into a full FIFO, etc.

To help understand the following timing diagrams an explanation of the basic architecture of the PCI Total-ACE is helpful. The PCI Total-ACE can be thought of as the very successful Mini-ACE terminal family integrated with a 3.3V 33MHz PCI target interface. To simplify descriptions of the PCI Total-ACE architecture, the term ACE will be used as a substitute for "enhanced Mini-ACE" even though the 1553 terminal function is really an enhanced Mini-ACE. When reference is made to ACE memory (BAR0) or ACE registers (BAR1 00-FCh) these functions are part of the ACE portion of the die. These ACE functions are accessed via the write FIFO (for writes) and delayed read request logic (for reads). The "PCI interface registers" (BAR1 800-81Ch) are part of the PCI interface portion of the die and are written and read directly from the PCI bus, without use of the write FIFO or delayed read request logic.

The PCI Total-ACE's basic PCI transaction takes 3 PCI clocks, on top of the command phase. For example, a single write to any location within the PCI Total-ACE's memory space takes 4 PCI clocks, as shown in FIGURE 12. Note that this is a single write, not an attempted burst write: FRAME# is not held asserted by the master. Also note that a write to the ACE registers or ACE memory is actually a write into the write FIFO whereas a write to the PCI interface registers (BAR1 800-81Ch) is a write to the registers themselves.

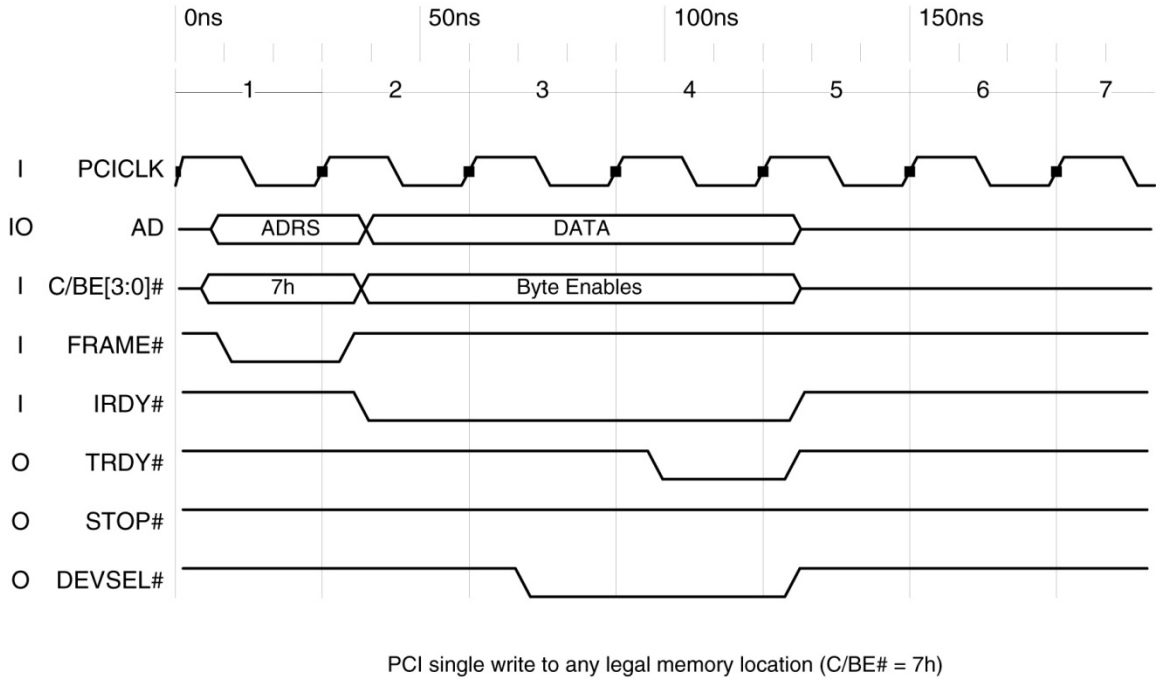


Figure 13. PCI Single Memory Write to PCI Total-ACE

Table 62 provides the timing parameters for 3.3V PCI signaling environments applicable to the PCI Total-ACE, and Figure 14shows the timing reference points. The timing parameters apply to the other timing diagrams, but are not illustrated. The PCI Total-ACE conforms to revision 2.2 of the PCI Local Bus specification. The timing parameters are provided here for ease of reference only.

Figure 14 illustrates a PCI read from the PCI Total-ACE's configuration space. The PCI Total-ACE only responds to Type Zero configuration access: AD[1:0] must be 00 during the command phase. The PCI Total-ACE will drive a full Dword on the AD lines independent of which byte enables are asserted during the configuration read.

Table 62. PCI InterfaceTimings

Symbol	Parameter	MIN	MAX	Units
tv	CLK to Signal Valid Delay	2	11	ns
tsu	Input Setuptime to CLK	7		ns
th	Input Hold Time from CLK	0		ns

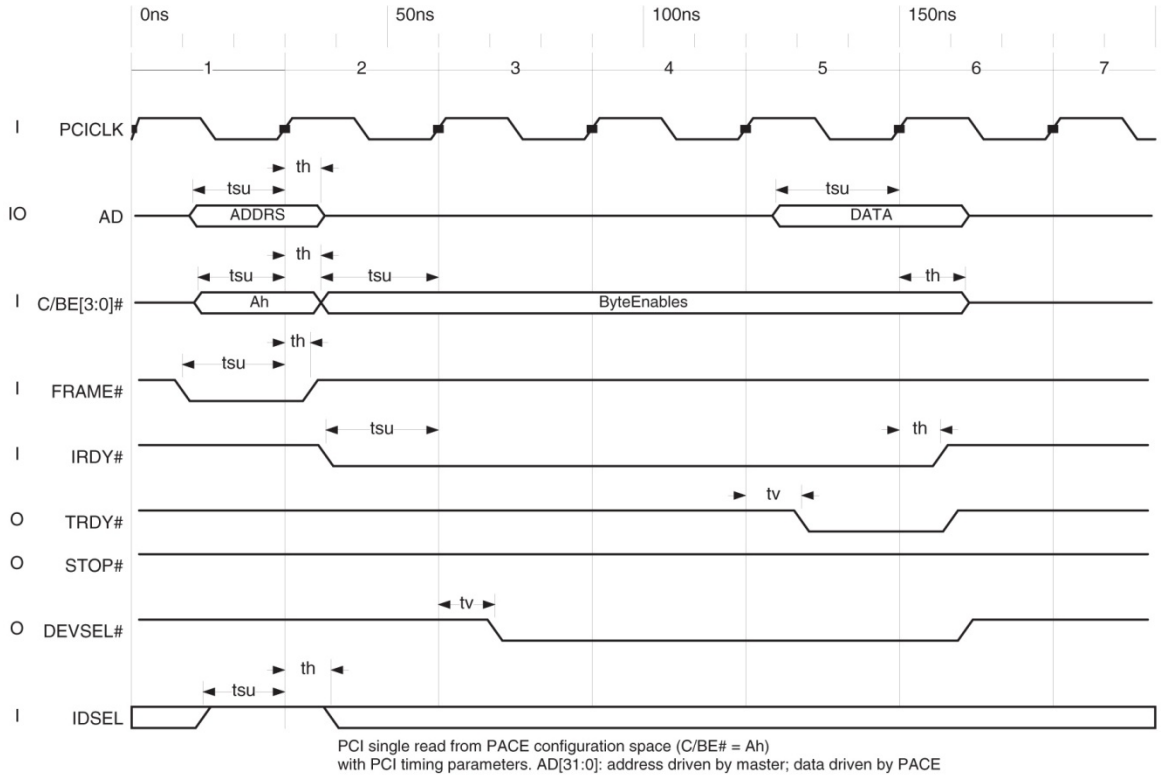


Figure 14. PCI Read of Configuration Space with Timing

Figure 15 illustrates a PCI single write to PCI Total-ACE configuration space. The PCI Total-ACE only responds to Type Zero configuration access: AD[1:0] must be 00 during the command phase. Note that all combinations of byte enables for configuration writes are supported. If no byte enables are asserted during a burst write to configuration space no internal write will occur, but the internal address will be incremented.

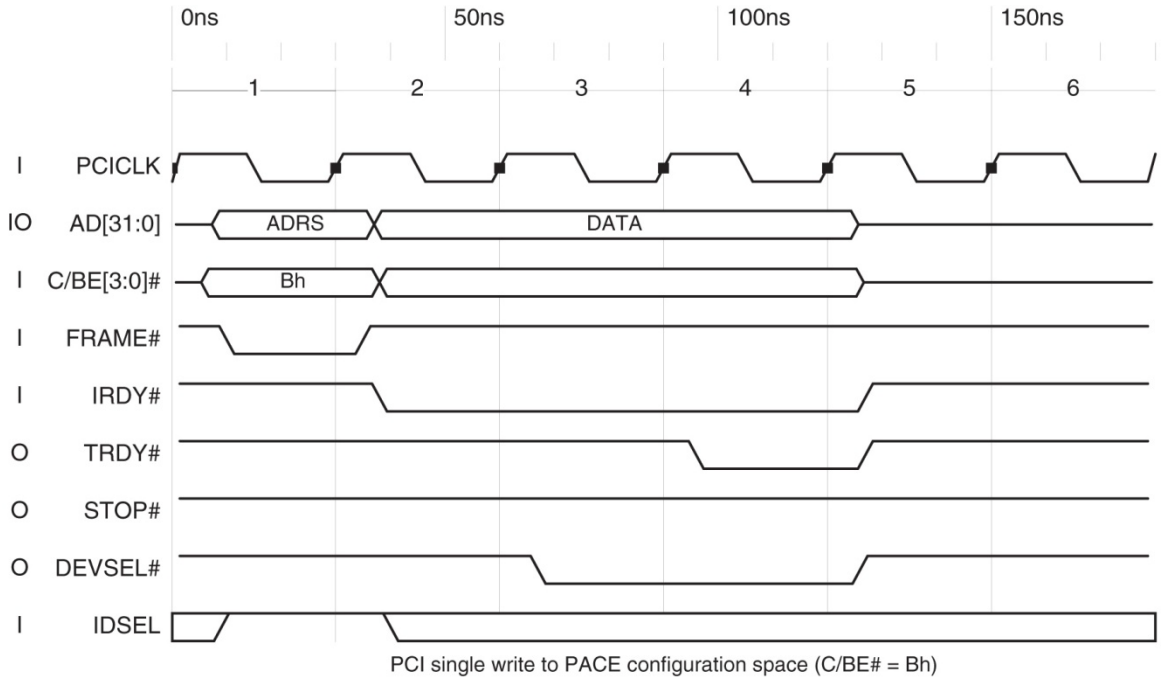


Figure 15. PCI Single Write to Configuration Space

Figure 16 shows the specific case of memory reads from the PCI-ACE interface registers at BAR1 800h-81Ch. Note that these registers are accessed quickly and without the Delayed Read Request mechanism required by reads from the other memory locations (see next section).

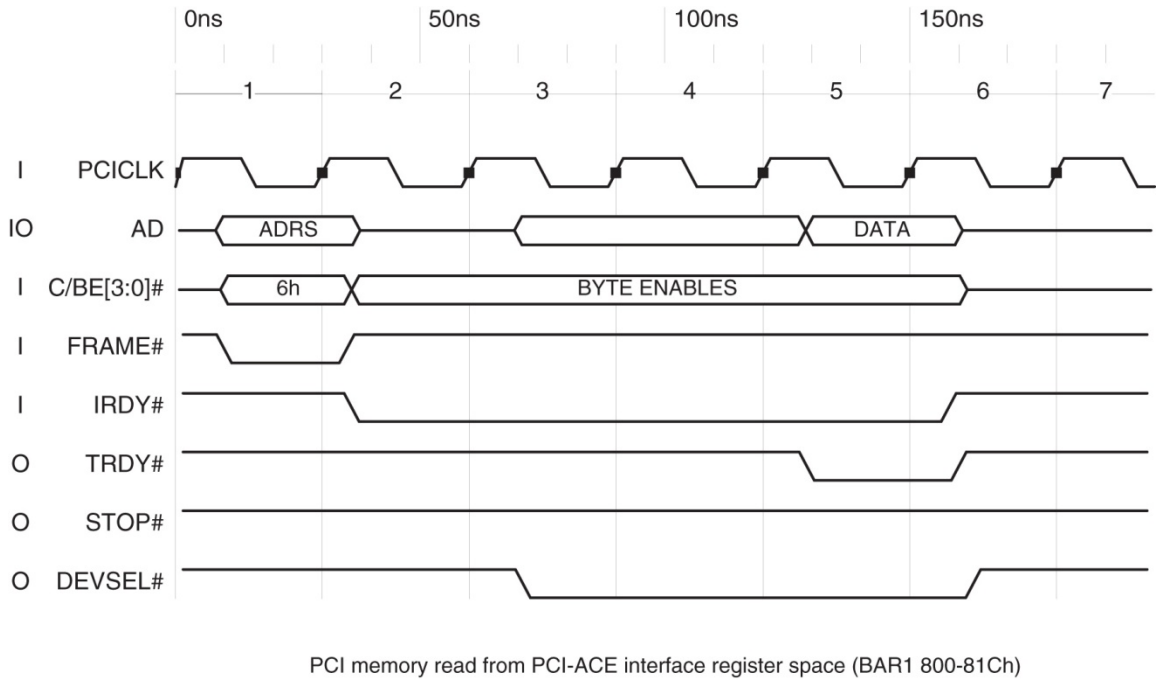


Figure 16. PCI Read of PCI-ACE If Registers (BAR1 800-81 CH)

Figure 17 illustrates the process of reading an ACE memory (BAR0) or ACE register (BAR1 00-FCh) location. The actual read shown is that of a single word read, due to the ~600 nS response time shown, see following text and timing formula tables. If the write FIFO is empty and there isn't a previous Delayed Read Request (DRR) pending, a read from these locations enques a DRR, which is then processed by the PCI Total-ACE. If either of these conditions is true, the PCI Total-ACE will respond with a Retry, but will not enque any new DRR.

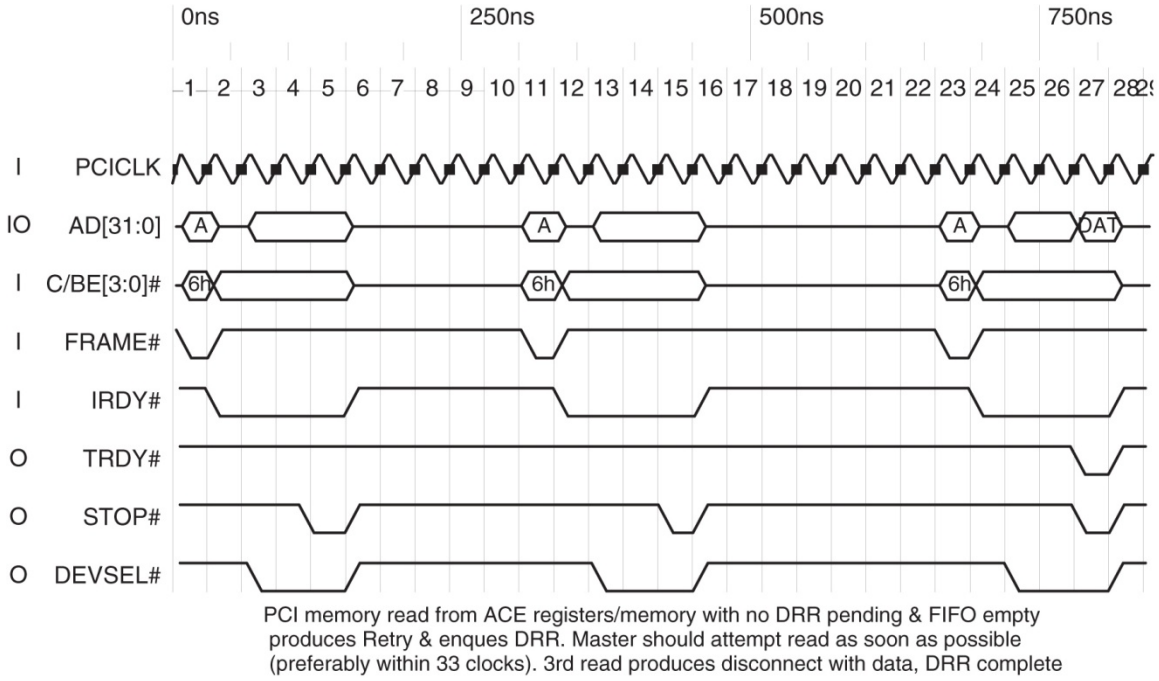


Figure 17. PCI Read of ACE Memory/Register

The PCI Total-ACE responds to the first read with a Retry. By PCI rules the master must repeat the same exact request until it completes. This is shown by the master's second read attempt, which also produces a Retry. Each repeated read request from the master will be target terminated with a Retry until the data from the enqued DRR is present in the PCI Total-ACE's PCI interface. The successful completion is shown at the third read request, which produces a Disconnect with Data.

This process applies to any memory read from legal address space **other** than the PCI-ACE interface registers at BAR1 offset 800-81Ch.

Note that one of the conditions for enquing a DRR is that the write FIFO must be empty. For efficient use of PCI bus bandwidth, the driver software should be written such that it checks the FIFO condition (BAR1 800-81CH registers are directly readable, bypassing the DRR mechanism) before reading from the other PCI Total-ACE locations. If the FIFO is not empty (BAR1 800h bit 30 is the FIFO not empty flag) and a read is attempted, the bus master will be using PCI bandwidth repeating the read request while the FIFO empties, BEFORE the read request is actually enqued as a DRR.

When reading ACE memory (BAR0), any combination of byte enables is supported, but the PCI Total-ACE will drive the entire word onto the AD lines when only a single byte enable in the word is asserted.

When reading ACE registers (BAR 00-FCh), byte enable combinations where only a single byte within a word is requested will cause the PCI Total-ACE to terminate the transaction with a target abort. The PCI Total-ACE will drive all zeros onto the AD lines if only the upper word byte enables or no byte enables are asserted.

With relation to actual timing, PCI double word reads of ACE memory (BAR0) will take longer to complete than single word ACE memory reads because the internal ACE memory data path is 16 bits wide. In addition, read cycles will take longer to complete with slower ACE clocks. See Table 63 for min/max formulas for calculating completion time for the various types of reads.

Table 63. MIN/MAX Delayed Read Formulas

Type of Read	MIN Time Formula	MAX Time Formula
ACE Memory (Bar0), Double Word	13 x PCI_CLK Period + 11 x ACE_CLK Period	16 x PCI_CLK Period + 14 x ACE_CLK Period
ACE Memory (Bar0), Single Word or ACE Register (Bar1), Double Word or Lower Word	8 x PCI_CLK Period + 5 x ACE_CLK Period	10 x PCI_CLK Period + 6 x ACE_CLK Period
No Cben# Asserted or ACE Register (Bar1) Upper Word	3 x PCI_CLK Period	3 x PCI_CLK Period

The third case returns all zeroes and is shown only for completeness.

The following examples have the same conditions: PCI clock = 33MHz, ACE clock = 16MHz, no ACE contention.

Single word read

Min time = 8 x 30 nS + 5 x 62.5 nS = 552.5 nS

Max time = 10 x 30nS + 6 x 62.5 nS = 675 nS

Double word read

Min time = 13 x 30 nS + 11 x 62.5 nS = 1077.5 nS

Max time = 16 x 30nS + 14 x 62.5 nS = 1167.5 nS

In addition, the following amount of ACE clocks should be added for maximum time if the ACE is active.

Table 64. Additional DRR Delay for Contested ACE RAM Access	
ACE Operating Mode	**Maximum Additional ACE Clocks**
Enhanced CPU Access Enabled, Single Word Transfer	3
Enhanced CP Access Enabled, Double Word Transfer	6
Enhanced CPU Access Disabled, Single Word Transfer	67
Enhanced DPU Access Disabled, Double Word Transfer	74
The Enhanced CPU Access is controlled by BIT 14 of Configuration Register #6	

Figure 18 illustrates a 16 Dword (32 word) PCI memory write burst, with the write FIFO empty (or with enough free space to absorb the 16 Dwords in the FIFO). The write FIFO accepts PCI memory writes to the ACE memory (BAR0) and ACE registers (BAR1 offset 00h - FCh). It does not accept writes to the PCI interface registers at BAR1 offset 800-81Ch. Writes to the BAR1 800-81Ch space go directly into the PCI interface registers. The 32 byte write shown could be an entire 1553 message being written to ACE memory.

Writes into the BAR 0 space must be word or Dword. If only one byte enable is asserted in a word, the PCI Total-ACE terminates the transaction with a Target-Abort. Writes into the BAR 1 00-FCh space must be word or Dword. If only one byte enable is asserted in a word, the PCI Total-ACE terminates the transaction with a Target-Abort. Since the ACE registers in this space are really 16 bit registers packed into the lower word of a 32-bit structure, only lower word or Dword writes transfer bits into these ACE registers.

In addition, as per PCI spec, a Memory Write and Invalidate (C/BE[3:0]# = Fh) command will be aliased to the basic Memory Write command and the timing diagram would look the same as Figure 18.

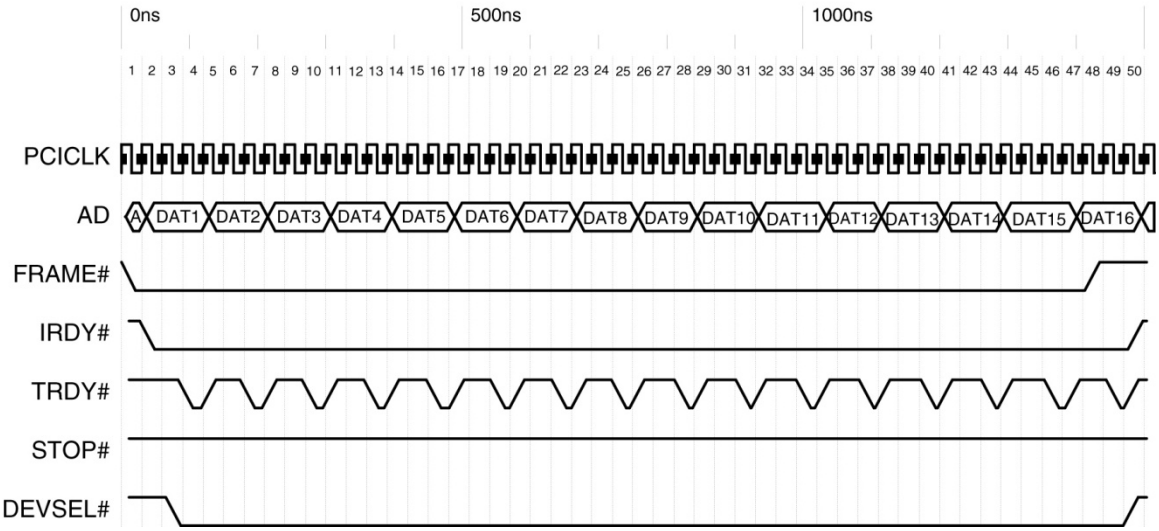


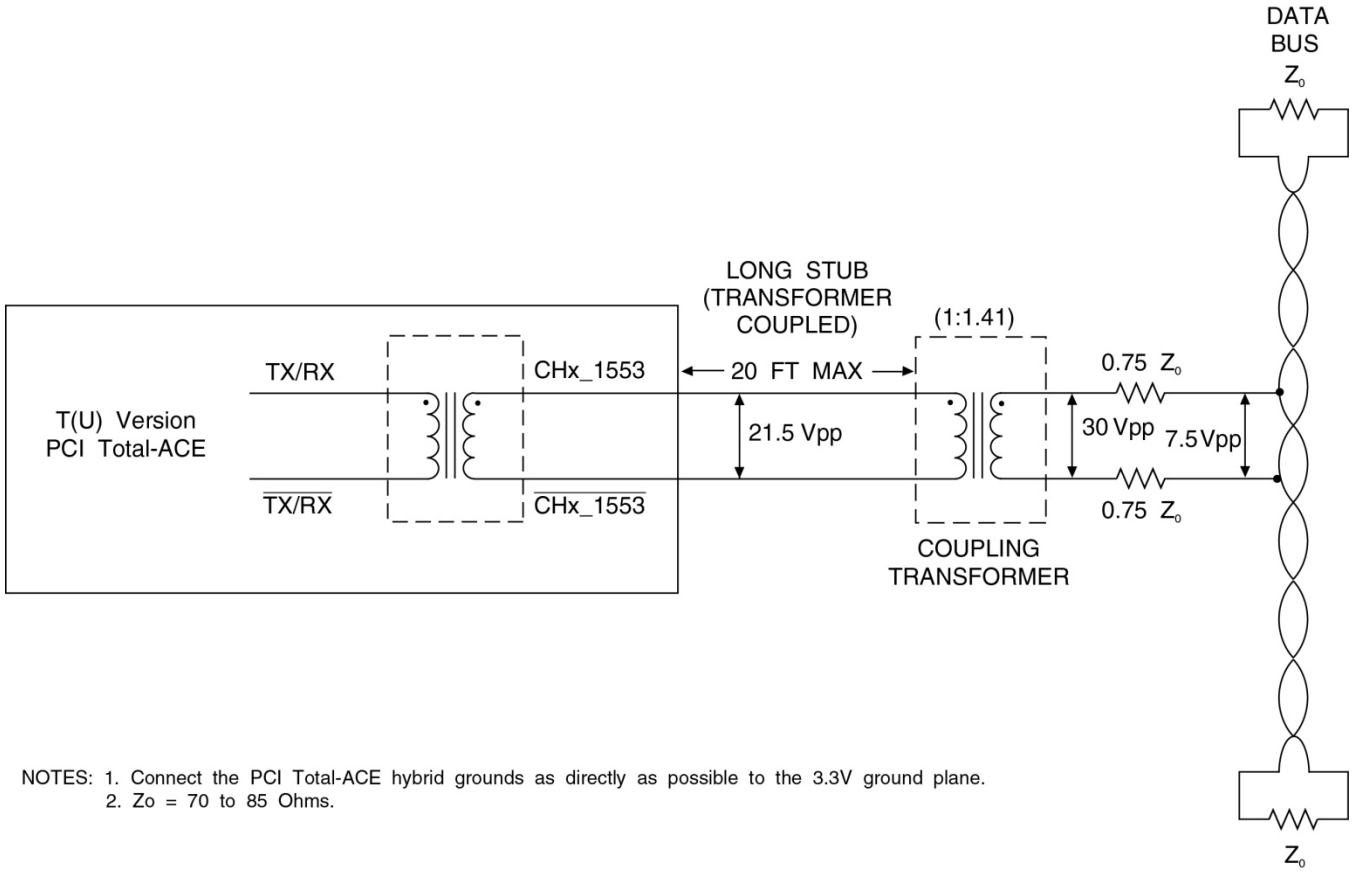
Figure 18. PCI Write Burst to ACE Memory with FIFO Empty

8.6 +3.3 VOLT INTERFACE TO MIL-STD-1553 BUS

The PCI Total-ACE is the world's first fully integrated PCI MILSTD- 1553 Terminal and Transformer solution.

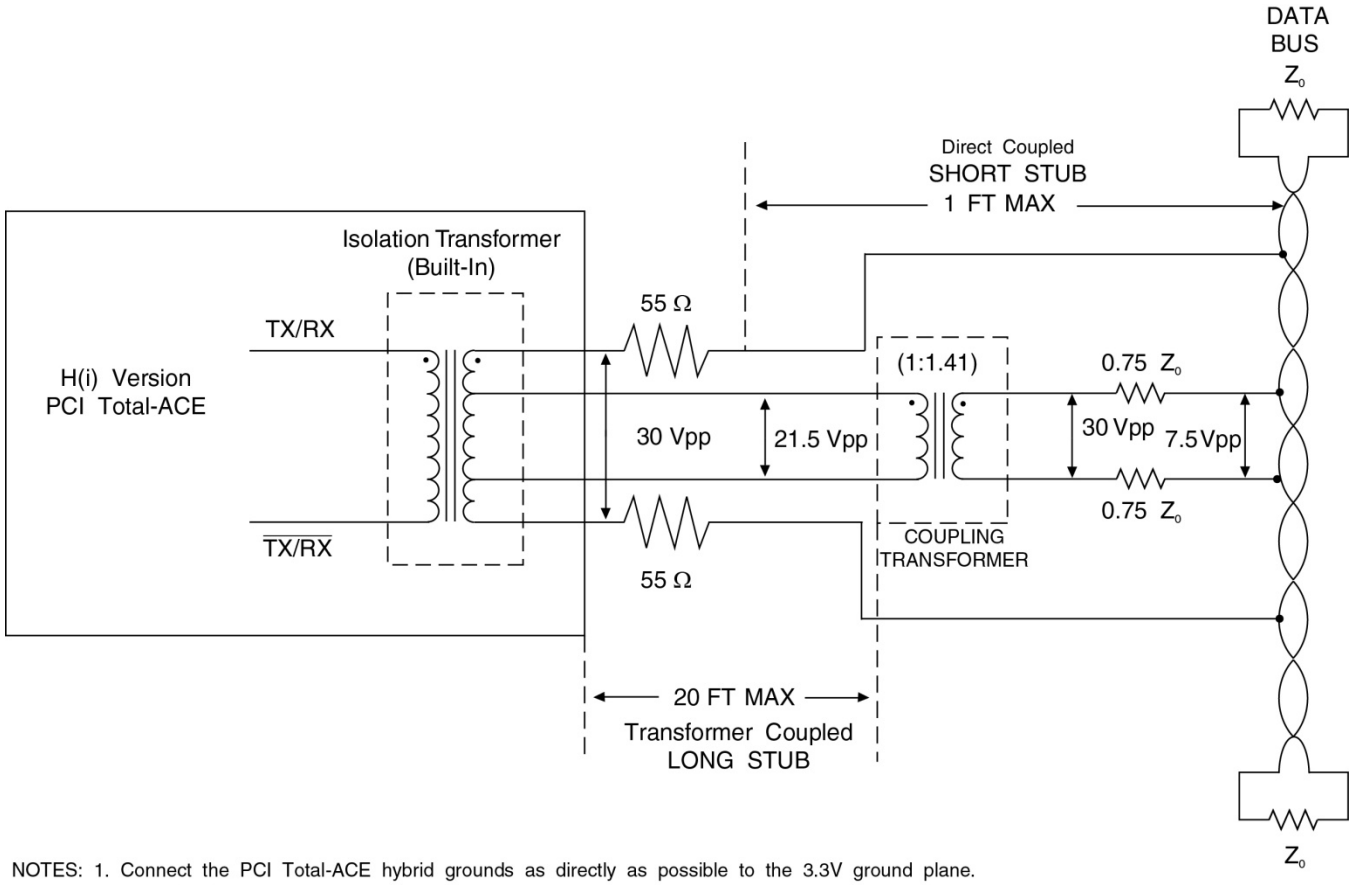
Figure 19 and Figure 20 illustrate the interface method between the PCI Total-Ace series and the MIL-STD-1553 bus. Depending on the version, connections for both transformer (long stub) and direct (short stub) coupling, as well as nominal peak-to-peak voltage levels at various points (when transmitting) are indicated in the diagram.

A 10µf, low inductance tantalum capacitor and a 0.01µf ceramic capacitor must be mounted as close as possible and with the shortest leads between +3.3V_XCVR Input and ground plane.



NOTES: 1. Connect the PCI Total-ACE hybrid grounds as directly as possible to the 3.3V ground plane.
2. Zo = 70 to 85 Ohms.

Figure 19. T(U) Version PCI Total-ACE Interface to MIL-STD-1553 Bus



NOTES: 1. Connect the PCI Total-ACE hybrid grounds as directly as possible to the 3.3V ground plane.
2. Zo = 70 to 85 Ohms.

Figure 20. H(I) Version PCI Total-ACE Interface to MIL-STD-1553 Bus

8.7 THERMAL MANAGEMENT FOR TOTAL-ACE (312-BALL BGA PACKAGE)

Ball Grid Array (BGA) components necessitate that thermal management issues be considered early in the design stage for MIL-STD-1553 terminals. This is especially true if high transmitter duty cycles are expected. The temperature range specified for DDC's Total-ACE device refers to the case temperature. Any duty cycle is acceptable as long as the case temperature is maintained within the industrial temperature range specified for the –Exx parts. See below for an explanation of thermal management requirements for high transmitter duty cycles with the military temperature range components.

All Total-ACE devices incorporate multiple package connections which perform the dual function of transceiver circuit ground and thermal heat sink. Refer to the pinout tables for thermal ball connection locations. It is mandatory that these thermal balls be directly soldered to a circuit ground/thermal plane (a circuit trace is insufficient).

Operation without an adequate ground/thermal plane is not recommended and extended exposure to these conditions may affect device reliability.

The purpose of this ground/thermal plane is to conduct the heat being generated by the transceivers within the package and conduct this heat away from the PCI Total-ACE. In general, the circuit ground and thermal (chassis) ground are not the same ground plane. It is acceptable for these balls to be directly soldered to a ground plane but it must be located in close physical and thermal proximity ("0.003" pre-preg layer recommended) to the thermal plane.

The temperature of each chip within the Total-Ace must be maintained below its respective maximum operating junction temperature as specified in Table 1. The simplest method to ensure this is to attribute all internal power dissipation to the transceiver, use the θ_{Jx} numbers also specified in Table 1 to calculate the temperature rise at the transceiver, and ensure that the temperature at the transceiver never exceeds the lowest maximum operating junction temperature allowed for any internal component (135°C for the protocol chip).

The general equation for the heat rise from ambient to the source of heat inside a component (typically the transistor junctions) is $\Delta T=P*\theta$, where P is the power dissipation of the component and θ is the thermal impedance from the junctions to ambient. Here there are two heat paths to the ambient, up through the top of the case, and down through the PCB, so we have a pair of equations:

$$\Delta T = P_C*(\theta_{JC}+\theta_{CA}) = P_B*(\theta_{JB}+\theta_{BA}) \text{ and } P = P_C+P_B.$$

Where P_C is the portion of the component power which flows through the top of the case to the ambient, θ_{JC} is the thermal impedance of the component from the junctions to the top of the case, and θ_{CA} is the thermal impedance of the system from the top of the case to ambient. Similarly, P_B is the portion of the component power which flows through the bottom of the case into the PCB, θ_{JB} is the thermal impedance of the component from the transistor junctions to the board, and θ_{BA} is the thermal impedance of the system from the board under the component to ambient.

For the case of a BU-65843H8-102 used as a monitor terminal, P=0.204W and θ_{JB}=26.5°C/W. This can be simplified by assuming that no heat flows out through the top of the case and only measuring the rise above package temperature without considering the whole path to ambient (ignoring θ_{BA}). The equation thus simplifies to:

$$\Delta T = P*(\theta_{JB}) = 0.204*(26.5+0) = 5.4°C$$

With a package temperature of 125°, this leaves the junction temperature below the maximum of 135°C.

The transmit duty cycle of a remote terminal is typically under 25%, with a few exceptions for high bandwidth devices like data loaders. Substituting the 25% duty cycle power (P=0.316W) into the equation above leads to a temperature rise of 8.4°C, which is still within acceptable limits as long as the board under the component is maintained at or below 125°C.

For a bus controller, higher duty cycles are common, so it may be necessary to add some form of heat sink to remove heat from the top of the component as well. For a BU-65863H8-102 with a duty cycle of 100%, P=0.655W. If the cooling paths from the top and bottom of the case to the ambient are assumed to be equally effective, ignoring θ_{CA} and θ_{BA} and setting the temperatures at both the top and bottom of the component to be the same, then the equations become:

$$\Delta T = P_C*(26.2) = P_B*(26.5)$$

And:

$$0.655 = P_C+P_B$$

Which turns into:

$$P_C = 0.655-P_B$$

Substituting for P_C and θ_{Jx} in the equation for ΔT, we get:

$$\Delta T = (0.655-P_B)*(26.2) = P_B*(26.5)$$
$$17.161-26.2 *P_B = 26.5*P_B$$
$$17.161 = 52.7*P_B$$
$$P_B = 0.3256$$

Substituting this result back into the ΔT equation, we get:

$$\Delta T = 0.3256*26.5 = 8.6°C$$

So as long as both the top and bottom of the case are maintained below 125°C, using heat sinks if necessary, the junction temperatures will remain within the acceptable limits.

For applications where high duty cycle operation is required at high ambient temperature, DDC also provides a thermal model that can be use with the FloTherm modeling tool from Mentor Graphics to assign power dissipation numbers to each internal component and determine the resulting operating junction temperature of

each, allowing the assurance of proper operation without requiring excessively conservative estimates that can hurt performance and increase costs.

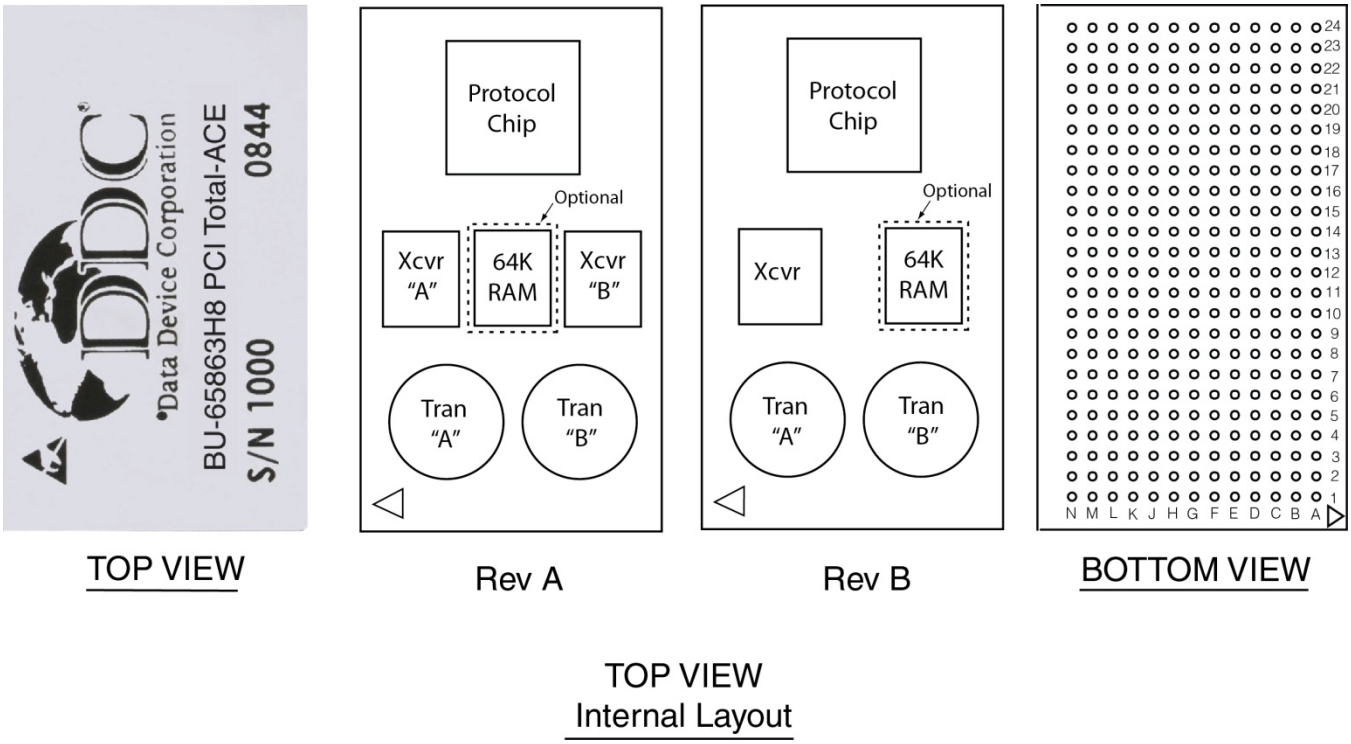


Figure 21. Ball Locations for PCI Total-ACE (312-Ball BGA Package)

8.8 Ball Grid Array Package - Signal Descriptions by Functional Groups

Table 65. Power and Ground		
Signal Name	**All Versions Ball**	**Description**
3V_Xcvr	B6, B7, B8, C6, C7, C12, D12, G6, G7, G8, G9, K12, L6, L7, L12, M6, M7, N9	+ 3.3 Volt Transceiver Power
3V_Logic	B16, B17, C16, C17, F13, F14, G13, G14, M16, M17, N19, N20	+3.3 V Logic Power
GND_Xcvr	A1, A2, A3, B1, B2, B3, H10, M1, M2, M3, N1, N2, N3	Transceiver Ground (thermal balls)
Gnd/Thermal	B9, B10, B11, C8, C9, C10, C11, D8, D9, D10, D11, E9, E10, E11, J9, J10, J11, K8, K9, K10, K11, L8, L9, L10, L11, M9, M10, M11	Transceiver Ground/Thermal connections. See Thermal Management Section for important user information.
Gnd	A1, A2, A3, A22, A23, A24, B1, B2, B3, B22, B23, B24, C22, C23, C24, E17, E18, E19, F17, F18, F19, G17, G18, G19, H17, H18, H19, H20, J17, J18, J19, J20, L14, L15, L22, L23, L24, M1, M14, M15, M2, M3, M22, M23, M24, N1, N2, N3, N22, N23, N24	Logic Ground

Note: *Logic ground and transceiver ground **are** tied together inside the package.*

Table 66. 1553 Stub Connection		
Signal Name	**All Versions Ball**	**Description**
CHA_1553 (I/O)	D1, D2, D3	1553 Transmit/Receive Input/Output. Connect directly to 1553 Long Stub.
CHA_1553_L (I/O)	F1, F2, F3	
CHB_1553 (I/O)	H1, H2, H3	
CHB_1553_L (I/O)	K1, K2, K3	
CHA_1553-Direct (I/O)	D4, E4, F4	1553 Transmit/Receive Input/Output. Connect directly to 1553, 55-Ohm Fault Isolation Resistors
CHA_1553-Direct_L (I/O)	E1, E2, E3	
CHB_1553-Direct (I/O)	H4, J4, K4	
CHB_1553-Direct_L (I/O)	J1, J2, J3	

Table 67. Mandatory Additional Connections & Interface to External Transceiver			
Signal Name	**Using Internal "Built-In" Transceivers**	**All Versions Ball**	**For Use with External Transceivers "Transceiverless"**
$\overline{\text{SNGL\_END}}$ (I)	No Connect "NC" if utilizing "Built-In" Transceivers	A21	If $\overline{\text{SNGL\_END}}$ is connected to logic "0" the Manchester decoder inputs will be configured to accept single-ended input signals (e.g.,MIL-STD-1773 fiber optic receiver outputs). If $\overline{\text{SNGL\_END}}$ is connected to logic "1," the decoder inputs will be configured to accept standard double-ended Manchester bi-phase input signals (i.e., MILSTD-1553 receiver outputs).
TXINH_IN_A (I)	These two signals MUST be directly connected for normal "Built-In" transceiver operation.	A12	Do NOT connect these two signals together. Connect TXINH_OUT (Digital transmit inhibit output) to the TX INH input of external MIL-STD-1553 transceivers. Asserted high to inhibit when not transmitting in the respective bus.
TXINH_OUT_A (O)		A13	
TXDATA_IN_A (I)	These two signals MUST be directly connected for normal "Built-In" transceiver operation.	A9	Do NOT connect these two signals. Connect TXDATA_OUT (Digital Manchester biphase transmit data output) directly to the corresponding input of a MIL-STD-1553 or MIL-STD-1773 (fiber optic) transceiver.
TXDATA_OUT_A (O)		A10	
$\overline{\text{TXDATA\_IN\_A}}$ (I)	These two signals MUST be directly connected for normal "Built-In" transceiver operation.	B14	Do NOT connect these two signals. Connect $\overline{\text{TXDATA\_OUT}}$ (Digital Manchester biphase transmit data output) directly to the corresponding input of a MIL-STD-1553 or MIL-STD-1773 (fiber optic) transceiver.
$\overline{\text{TXDATA\_OUT\_A}}$ (O)		C14	
$\overline{\text{RXDATA\_IN\_A}}$ (I)	These two signals MUST be directly connected for normal "Built-In" transceiver operation.	G12	Do NOT connect these two signals. Connect $\overline{\text{RXDATA\_IN}}$ (Digital Manchester biphase transmit data output) directly to the corresponding input of a MIL-STD-1553 or MIL-STD-1773 (fiber optic) transceiver.
$\overline{\text{RXDATA\_OUT\_A}}$ (O)		F12	
RXDATA_IN_A (I)	These two signals MUST be directly connected for normal "Built-In" transceiver operation.	G11	Do NOT connect these two signals. Connect RXDATA_IN (Digital Manchester biphase transmit data output) directly to the corresponding input of a MIL-STD-1553 or MIL-STD-1773 (fiber optic) transceiver.
RXDATA_OUT_A (O)		F11	
TXINH_IN_B (I)	These two signals MUST be directly connected for normal "Built-In" transceiver operation.	M20	Do NOT connect these two signals. Connect TXINH_OUT (Digital Manchester biphase transmit data output) directly to the corresponding input of a MIL-STD-1553 or MIL-STD-1773 (fiber optic) transceiver.
TXINH_OUT_B (O)		M19	
TXDATA_IN_B (I)	These two signals MUST be directly connected for normal "Built-In" transceiver operation.	J16	Do NOT connect these two signals. Connect TXDATA_OUT (Digital Manchester biphase transmit data output) directly to the corresponding input of a MIL-STD-1553 or MIL-STD-1773 (fiber optic) transceiver.
TXDATA_OUT_B (O)		K16	

Table 67. Mandatory Additional Connections & Interface to External Transceiver			
Signal Name	**Using Internal "Built-In" Transceivers**	**All Versions Ball**	**For Use with External Transceivers "Transceiverless"**
$\overline{\text{TXDATA\_IN\_B}}$ (I)	These two signals MUST be directly connected for normal "Built-In" transceiver operation.	K18	Do NOT connect these two signals. Connect $\overline{\text{TXDATA\_OUT}}$ (Digital Manchester biphase transmit data output) directly to the corresponding input of a MIL-STD-1553 or MIL-STD-1773 (fiber optic) transceiver.
$\overline{\text{TXDATA\_OUT\_B}}$ (O)		K19	
$\overline{\text{RXDATA\_IN\_B}}$ (I)	These two signals MUST be directly connected for normal "Built-In" transceiver operation.	M13	Do NOT connect these two signals. Connect $\overline{\text{RXDATA\_IN}}$ (Digital Manchester biphase receive data input) directly to the corresponding input of a MIL-STD-1553 or MIL-STD-1773 (fiber optic) transceiver.
$\overline{\text{RXDATA\_OUT\_B}}$ (O)		M12	
RXDATA_IN_B (I)	These two signals MUST be directly connected for normal "Built-In" transceiver operation.	N13	Do NOT connect these two signals. Connect RXDATA_IN (Digital Manchester biphase receive data input) directly to the corresponding input of a MIL-STD-1553 or MIL-STD-1773 (fiber optic) transceiver.
RXDATA_OUT_B (O)		N12	
Note: The device can be operated with either their internal transceivers or with external transceivers. When the devices are operated with their internal transceivers the customer must supply PCB traces that connect the device's "inputs to outputs" (within the correct column) as described in this table.			

Table 68. Processor Interface Control		
Signal Name	**All Versions Ball**	**Description**
$\overline{\text{SSFLAG}}$ (I) / EXT_TRIG (I)	L16	Subsystem Flag (RT) or External Trigger (BC/Word Monitor) input. In RT mode, if this input is asserted low, the Subsystem Flag bit will be set in the Total-ACE's RT Status Word. If the $\overline{\text{SSFLAG}}$ input is logic "0" while bit 8 of Configuration Register #1 has been programmed to logic "1" (cleared), the Subsystem Flag RT Status Word bit will become logic "1," but bit 8 of Configuration Register #1, $\overline{\text{SUBSYSTEM FLAG}}$, will return logic "1" when read. That is, the sense on the $\overline{\text{SSFLAG}}$ input has no effect on the SUBSYSTEM FLAG register bit. In the non-enhanced BC mode, this signal operates as an External Trigger input. In BC mode, if the external BC Start option is enabled (bit 7 of Configuration Register #1), a low to high transition on this input will issue a BC Start command, starting execution of the current BC frame. In the enhanced BC mode, during the execution of a Wait for External Trigger (WTG) instruction, the Total-ACE BC will wait for a low-to-high transition on EXT_TRIG before proceeding to the next instruction. In the Word Monitor mode, if the external trigger is enabled (bit 7 of Configuration Register #1), a low to high transition on this input will initiate a monitor start. This input has no effect in Message Monitor mode.

Table 69. RT Address		
Signal Name	**All Versions Ball**	**Description**
RTAD4 (MSB) (I)	A16	RT Address inputs (5V tolerant). If bit 5 of Configuration Register #6, RT ADDRESS SOURCE, is programmed to logic "0" (default), then the PCI Total-ACE's RT address is provided by means of these 5 input signals. In addition, if RT ADDRESS SOURCE is logic "0", the source of RT address parity is RTADP. There are many methods for using these input signals for designating the Total-ACE's RT address. For details, refer to the description of RT_AD_LAT. If RT ADDRESS SOURCE is programmed to logic "1", then the Total-ACE's source for its RT address and parity is under software control, via data lines D5-D0. In this case, the RTAD4-RTAD0 and RTADP signals are not used.
RTAD3 (I)	D14	
RTAD2 (I)	A15	
RTAD1 (I)	C15	
RTAD0 (LSB) (I)	C18	
RTADP (I)	E12	Remote Terminal Address Parity. This input signal must provide an odd parity sum with RTAD4-RTAD0 in order for the RT to respond to non-broadcast commands. That is, there must be an odd number of logic "1"s from among RTAD-4- RTAD0 and RTADP.
RT_AD_LAT (I)	B12	RT Address Latch. Input signal used to control the PCI Total-ACE's internal RT address latch. If RT_AD_LAT is connected to logic "0", then the PCI Total-ACE RT is configured to accept a hardwired (transparent) RT address from RTAD4-RTAD0 and RTADP. If RT_AD_LAT is initially logic "0", and then transitions to logic "1", the values presented on RTAD4- RTAD0 and RTADP will be latched internally on the rising edge of RT_AD_LAT. If RT_AD_LAT is connected to logic "1", then the PCI Total-ACE's RT address is latchable under host processor control. In this case, there are two possibilities: (1) If bit 5 of Configuration Register #6, RT ADDRESS SOURCE, is programmed to logic "0" (default), then the source of the RT Address is the RTAD4-RTAD0 and RTADP input signals. (2) If RT ADDRESS SOURCE is programmed to logic "1", then the source of the RT Address is the lower 6 bits of the processor data bus, D5-D1 (for RTAD4- 0) and D0 (for RTADP). In either of these two cases (with RT_AD_LAT = "1"), the processor will cause the RT address to be latched by: (1) Writing bit 15 of Configuration Register #3, ENHANCED Mode ENABLE, to logic "1". (2) Writing bit 3 of Configuration Register #4, LATCH RT ADDRESS WITH CONFIGURATION REGISTER #5, to logic "1". (3) Writing to Configuration Register #5. In the case of RT ADDRESS SOURCE = "1", then the values of RT address and RT address parity must be written to the lower 6 bits of Configuration Register #5, via D5-D0. In the case where RT ADDRESS SOURCE = "0", the bit values presented on D5-D0 become "don't care".

Table 70. Miscellaneous Signals

Signal Name	All Versions Ball	Description
$\overline{\text{INCMD}}$ (O) / $\overline{\text{MCRST}}$ (O)	F15	In-command or Mode Code Reset. The function of this pin is controlled by bit 0 of Configuration Register #7, $\overline{\text{MODE CODE RESET}}$ / $\overline{\text{INCMD}}$ SELECT. If this register bit is logic "0" (default), $\overline{\text{INCMD}}$ will be active on this pin. For BC, RT, or Selective Message Monitor modes, $\overline{\text{INCMD}}$ is asserted low whenever a message is being processed by the PCI Total-ACE. In Word Monitor mode, $\overline{\text{INCMD}}$ will be asserted low for as long as the monitor is online. For RT mode, if MODE CODE RESET/ $\overline{\text{INCMD}}$ SELECT is programmed to logic "1", $\overline{\text{MCRST}}$ will be active. In this case, $\overline{\text{MCRST}}$ will be asserted low for two clock cycles following receipt of a Reset remote terminal mode command. In BC or Monitor modes, if MODE CODE RESET/ $\overline{\text{INCMD}}$ SELECT is logic "1", this signal is inoperative; i.e., in this case, it will always output a value of logic "1".
TAG_CLK (I)	D23	Input (5V tolerant) for optional external tag clock. No connection needed if internal tag clock is used. Maximum TAG_CLK frequency is 1/44th of the 1553_CLK input.
1553_CLK (I)	E15	20 MHz, 16 MHz, 12 MHz, or 10 MHz clock input.
TX_INH A/B (I)	F16	Transmitter inhibit input (5V tolerant) for the Channel A and Channel B MIL-STD-1553 transmitters. For normal operation, this input should be connected to logic "0". To force a shutdown of Channel A and Channel B, a value of logic "1" should be applied to the TX_INH input.
$\overline{\text{MSTCLR}}$ (RST#) (I)	D18	Master Clear. Negative true Reset input, normally asserted low following power turn-on. This input conforms to PCI RST# convention.
$\overline{\text{RTBOOT}}$ (I)	A19	If $\overline{\text{RTBOOT}}$ is connected to Logic "0" the PCI Total-ACE will initialize in RT mode with the Busy status word bit set following power turn on. Received data will not be stored because the “BUSY RECEIVE TRANSFER DISABLE” bit will also be set following power turn on. In addition, CLK_SEL_0 and CLK_SEL_1 are enabled and they select the divider for the 1553 clock circuitry:

CLK_SEL1	CLK_SEL0	1553 Clock Frequency
0	0	10 MHz
0	1	20 MHz
1	0	12 MHz
1	1	16 MHz

CLOCK_SEL_0 (I)	K22	1553 CLOCK SELECT 0, ACTIVE ONLY WHEN $\overline{\text{RTBOOT}}$ = 0
CLOCK_SEL_1 (I)	B21	1553 CLOCK SELECT 1, ACTIVE ONLY WHEN $\overline{\text{RTBOOT}}$ = 0
BC_Disable	B20	Hardware lockout to disable BC operation and operate the part in RT-Only mode. Drive high to disable BC, low to enable all modes of operation. Note: For parts with Date Codes of 1111 or later. This ball must be grounded for parts with earlier Date Codes.

Table 71. PCI Bus Address and Data Signals		
Signal Name	**All Versions Ball**	**Description**
AD31 (I/O)	D15	32-Bit PCI Bus Address / Data lines. Address and Data are multiplexed on the same pins. Each bus operation consists of an address phase followed by one or more data phases. Address phases are identified when the control signal FRAME# is asserted. Data transfers occur during those clock cycles in which the control signals IRDY# and TRDY# are both asserted.
AD30 (I/O)	N16	
AD29 (I/O)	L17	
AD28 (I/O)	H21	
AD27 (I/O)	E14	
AD26 (I/O)	M18	
AD25 (I/O)	N17	
AD24 (I/O)	K24	
AD23 (I/O)	J24	
AD22 (I/O)	J21	
AS21 (I/O)	G23	
AS20 (I/O)	H22	
AD19 (I/O)	G24	
AD18 (I/O)	J23	
AD17 (I/O)	K23	
AD16 (I/O)	H24	
AD15 (I/O)	D21	
AD14 (I/O)	F24	
AD13 (I/O)	D22	
AD12 (I/O)	C21	
AD11 (I/O)	D24	
AD10 (I/O)	C20	
AD9 (I/O)	A20	
AD8 (I/O)	D20	
AD7 (I/O)	A18	
AD6 (I/O)	A17	
AD5 (I/O)	J14	
AD4 (I/O)	D17	
AD3 (I/O)	E13	
AD2 (I/O)	A14	
AD1 (I/O)	B15	
AD0 (I/O) (LSB)	D16	

Table 71. PCI Bus Address and Data Signals		
Signal Name	**All Versions Ball**	**Description**
C/BE[3]# (I)	K14	Bus Command and Byte Enables. These signals are multiplexed on the same pins. During the address phase of a bus operation, these pins identify the bus command, as shown in the table below. During the data phase of a bus operation, these pins are used as Byte Enables, with C/BE[0]# enabling byte 0 (LSB) and C/BE[3]# enabling byte 3 (MSB). The PCI Total-ACE responds to the following PCI commands **C/BE[3:0]#** — **Description (during address phase)** 0 1 1 0 — Memory Read 0 1 1 1 — Memory Write 1 0 1 0 — Configuration Read 1 0 1 1 — Configuration Write 1 1 0 0 — Memory Read Multiple 1 1 1 0 — Memory Read Line 1 1 1 1 — Memory Write and Invalidate Note that the last three memory commands are aliased to the basic memory commands: Memory Read and Memory Write.
C/BE[2]# (I)	H23	
C/BE[1]# (I)	E21	
C/BE[0]# (I)	B18	
PAR (I/O)	F22	Parity. This signal is even parity across the entire AD[31:0] field along with the C/BE[3:0]# field. The parity is stable in the clock following the address phase and is sourced by the Bus Master. During the data phase for write operations, the Bus Master sources this signal on the clock following IRDY# active. During the data phase for read operations, this signal is sourced by the Target and is valid on the clock following TRDY# active. The PAR signal therefore has the same timing as AD[31:0], delayed by one clock.
PCI_CLK (I)	N18	Clock input. The rising edge of this signal is the reference upon which all other clock signals are based, with the exception of RST# and INTA#. The maximum frequency accepted is 33 MHz and the minimum is 0 Hz.

Table 72. PCI Control Bus Data Signals (note that all signals listed, except INTA#, are sampled on the rising edge of PCI_CLK)		
Signal Name	**All Versions Ball**	**Description**
FRAME#(I)	G21	Frame. This signal is driven by the current bus master and identifies both the beginning and duration of a bus operation. When FRAME# is first asserted, it indicates that a bus transaction is beginning and that valid addresses and a corresponding bus command are present on the AD[31:0] and C/BE[3:0] lines, qualified by PCI _CLK. When FRAME# is deasserted the transaction is in the final data phase or has been completed.
IRDY#(I)	G22	Initiator Ready. This signal is sourced by the bus master and indicates that the bus master is able to complete the current data phase of a bus transaction. For write operations, it indicates that valid data is on the AD[31:0] pins. Wait states occur until both TRDY# and IRDY# are asserted together.
TRDY#(O)	F23	Target Ready. This signal is sourced by the selected target and indicates that the target is able to complete the current data phase of a bus transaction. For read

Table 72. PCI Control Bus Data Signals (note that all signals listed, except INTA#, are sampled on the rising edge of PCI_CLK)		
Signal Name	**All Versions Ball**	**Description**
		operations, it indicates that the target is providing valid data on the AD[31:0] pins. Wait states occur until both TRDY# and IRDY# are asserted together.
STOP#(O)	E22	Stop. The Stop signal is sourced by the selected target and conveys a request to the bus master to stop the current transaction.
IDSEL#(I)	K21	Initialization Device Select. This pin is used as a chip select during configuration read or write operations.
DEVSEL#(O)	F21	Device Select. This signal is sourced by an active target upon decoding that its address and bus commands are valid. For bus masters, it indicates whether any device has decoded the current bus cycle.
PERR#(O)	E23	Parity Error. This pin is used for reporting parity errors during the data portion of the bus transaction for all cycles except a Special Cycle. It is sourced by the agent receiving data and driven active two clocks following the detection of an error. This signal is driven inactive (high) two clocks prior to returning to the tri-state condition.
SERR#(O)	E24	System Error. This pin is used for reporting address parity errors, data parity errors on Special Cycle commands, or any other condition having a catastrophic system impact.
INTA#(O)	J22	Interrupt A. This pin is a level sensitive, active low interrupt to the host.

Table 73. No User Connections		
Signal Name	**H (I) Version Ball**	**Description**
NC	A11, A4, A5, A6, A7, A8, B13, B19, B4, B5, C1, C13, C19, C2, C3, C4, C5, D13, D19, D5, D6, D7, E16, E20, E5, E6, E7, E8, F10, F20, F5, F6, F7, F8, F9, G1, G10, G15, G16, G2, G20, G3, G4, G5, H11, H12, H13, H14, H15, H16, H5, H6, H7, H8, H9, J12, J13, J15, J5, J6, J7, J8, K13, K15, K17, K20, K5, K6, K7, L1, L13, L18, L19, L2, L20, L21, L3, L4, L5, M21, M4, M5, M8, N10, N11, N14, N15, N21, N4, N5, N6, N7, N8	No User Connections to these balls allowed.

Table 74. All Versions Pinout					
Ball	**Signal**	**Notes**	**Ball**	**Signal**	**Notes**
A1	GND_Xcvr		C1	NC	
A2	GND_Xcvr		C2	NC	
A3	GND_Xcvr		C3	NC	
A4	NC		C4	NC	
A5	NC		C5	NC	
A6	NC		C6	+3.3V_Xcvr	
A7	NC		C7	+3.3V_Xcvr	
A8	NC		C8	GND_Xcvr/Thermal***	
A9	TXDATA_IN_A	connect to ball A10	C9	GND_Xcvr/Thermal***	
A10	TXDATA_OUT_A	connect to ball A9	C10	GND_Xcvr/Thermal***	
A11	NC		C11	GND_Xcvr/Thermal***	
A12	TXINH_IN_A	connect to ball A13	C12	+3.3V_Xcvr	
A13	TXINH_OUT_A	connect to ball A12	C13	NC	
A14	AD02		C14	$\overline{\text{TXDATA\_OUT\_A}}$	connect to ball B14
A15	RTAD2		C15	RTAD1	
A16	RTAD4		C16	+3.3V_Logic	
A17	AD06		C17	+3.3V_Logic	
A18	AD07		C18	RTAD0	
A19	RTBOOT_L		C19	NC	
A20	AD09		C20	AD10	
A21	SNGL_END_L		C21	AD12	
A22	Gnd_Logic		C22	Gnd_Logic	
A23	Gnd_Logic		C23	Gnd_Logic	
A24	Gnd_Logic		C24	Gnd_Logic	
B1	GND_Xcvr		D1	CHA_1553	
B2	GND_Xcvr		D2	CHA_1553	
B3	GND_Xcvr		D3	CHA_1553	
B4	NC		D4	CHA_1553-Direct	
B5	NC		D5	NC	
B6	+3.3V_Xcvr		D6	NC	
B7	+3.3V_Xcvr		D7	NC	
B8	+3.3V_Xcvr		D8	GND_Xcvr/Thermal***	
B9	GND_Xcvr/Thermal***		D9	GND_Xcvr/Thermal***	
B10	GND_Xcvr/Thermal***		D10	GND_Xcvr/Thermal***	
B11	GND_Xcvr/Thermal***		D11	GND_Xcvr/Thermal***	
B12	RT_AD_LAT		D12	+3.3V_Xcvr	
B13	NC		D13	NC	
B14	$\overline{\text{TXDATA\_IN\_A}}$	connect to ball C14	D14	RTAD3	
B15	AD01		D15	AD31	
B16	+3.3V_Logic		D16	AD00	
B17	+3.3V_Logic		D17	AD04	
B18	C/BE[0]#		D18	$\overline{\text{MSTCLR}}$ (RST#)	
B19	NC		D19	NC	
B20	BC_Disable	this ball must be grounded for parts with a date code earlier than 1111.	D20	AD08	
B21	CLK_SEL_1		D21	AD15	
B22	Gnd_Logic		D22	AD13	
B23	Gnd_Logic		D23	TAG_CLK	
B24	Gnd_Logic		D24	AD11	

Table 74. All Versions Pinout					
Ball	**Signal**	**Notes**	**Ball**	**Signal**	**Notes**
E1	$\overline{\text{CHA\_1553}}$ -Direct		G1	NC	
E2	$\overline{\text{CHA\_1553}}$ -Direct		G2	NC	
E3	$\overline{\text{CHA\_1553}}$ -Direct		G3	NC	
E4	CHA_1553-Direct		G4	NC	
E5	NC		G5	NC	
E6	NC		G6	+3.3V_Xcvr	
E7	NC		G7	+3.3V_Xcvr	
E8	NC		G8	+3.3V_Xcvr	
E9	GND_Xcvr/Thermal***		G9	+3.3V_Xcvr	
E10	GND_Xcvr/Thermal***		G10	NC	
E11	GND_Xcvr/Thermal***		G11	RXDATA_IN_A	connect to ball F11
E12	RTADP		G12	$\overline{\text{RXDATA\_IN\_A}}$	connect to ball F12
E13	AD03		G13	+3.3V_Logic	
E14	AD27		G14	+3.3V_Logic	
E15	1553_CLK		G15	NC	
E16	NC		G16	NC	
E17	Gnd_Logic		G17	Gnd_Logic	
E18	Gnd_Logic		G18	Gnd_Logic	
E19	Gnd_Logic		G19	Gnd_Logic	
E20	NC		G20	NC	
E21	C/BE[1]#		G21	FRAME#	
E22	STOP#		G22	IRDY#	
E23	PERR#		G23	AD21	
E24	SERR#		G24	AD19	
F1	CHA_1553_L		H1	CHB_1553	
F2	CHA_1553_L		H2	CHB_1553	
F3	CHA_1553_L		H3	CHB_1553	
F4	CHA_1553-Direct		H4	CHB_1553-Direct	
F5	NC		H5	NC	
F6	NC		H6	NC	
F7	NC		H7	NC	
F8	NC		H8	NC	
F9	NC		H9	NC	
F10	NC		H10	GND_Xcvr	
F11	RXDATA_OUT_A	connect to ball G11	H11	NC	
F12	$\overline{\text{RXDATA\_OUT\_A}}$	connect to ball G12	H12	NC	
F13	+3.3V_Logic		H13	NC	
F14	+3.3V_Logic		H14	NC	
F15	$\overline{\text{INCMD}}$ / $\overline{\text{MCRST}}$		H15	NC	
F16	TX_INH_A/B		H16	NC	
F17	Gnd_Logic		H17	Gnd_Logic	
F18	Gnd_Logic		H18	Gnd_Logic	
F19	Gnd_Logic		H19	Gnd_Logic	
F20	NC		H20	Gnd_Logic	
F21	DEVSEL#		H21	AD28	
F22	PAR		H22	AD20	
F23	TRDY#		H23	C/BE[2]#	
F24	AD14		H24	AD16	

Table 74. All Versions Pinout					
Ball	**Signal**	**Notes**	**Ball**	**Signal**	**Notes**
J1	$\overline{\text{CHB\_1553}}$ -Direct		L1	NC	
J2	$\overline{\text{CHB\_1553}}$ -Direct		L2	NC	
J3	$\overline{\text{CHB\_1553}}$ -Direct		L3	NC	
J4	CHB_1553-Direct		L4	NC	
J5	NC		L5	NC	
J6	NC		L6	+3.3V_Xcvr	
J7	NC		L7	+3.3V_Xcvr	
J8	NC		L8	GND_Xcvr/Thermal***	
J9	GND_Xcvr/Thermal***		L9	GND_Xcvr/Thermal***	
J10	GND_Xcvr/Thermal***		L10	GND_Xcvr/Thermal***	
J11	GND_Xcvr/Thermal***		L11	GND_Xcvr/Thermal***	
J12	NC		L12	+3.3V_Xcvr	
J13	NC		L13	NC	
J14	AD05		L14	Gnd	
J15	NC		L15	Gnd	
J16	TXDATA_IN_B	connect to ball K16	L16	$\overline{\text{SSFLAG}}$ / EXT_TRIG	
J17	Gnd_Logic		L17	AD29	
J18	Gnd_Logic		L18	NC	
J19	Gnd_Logic		L19	NC	
J20	Gnd_Logic		L20	NC	
J21	AD22		L21	NC	
J22	INTA#		L22	Gnd_Logic	
J23	AD18		L23	Gnd_Logic	
J24	AD23		L24	Gnd_Logic	
K1	$\overline{\text{CHB\_1553}}$		M1	GND_Xcvr	
K2	$\overline{\text{CHB\_1553}}$		M2	GND_Xcvr	
K3	$\overline{\text{CHB\_1553}}$		M3	GND_Xcvr	
K4	$\overline{\text{CHB\_1553}}$ -Direct		M4	NC	
K5	NC		M5	NC	
K6	NC		M6	+3.3V_Xcvr	
K7	NC		M7	+3.3V_Xcvr	
K8	GND_Xcvr/Thermal***		M8	NC	
K9	GND_Xcvr/Thermal***		M9	GND_Xcvr/Thermal***	
K10	GND_Xcvr/Thermal***		M10	GND_Xcvr/Thermal***	
K11	GND_Xcvr/Thermal***		M11	GND_Xcvr/Thermal***	
K12	+3.3V_Xcvr		M12	$\overline{\text{RXDATA\_OUT\_B}}$	connect to ball M13
K13	NC		M13	$\overline{\text{RXDATA\_IN\_B}}$	connect to ball M12
K14	C/BE[3]#		M14	Gnd_Logic	
K15	NC		M15	Gnd_Logic	
K16	TXDATA_OUT_B	connect to ball J16	M16	+3.3V_Logic	
K17	NC		M17	+3.3V_Logic	
K18	$\overline{\text{TXDATA\_IN\_B}}$	connect to ball K19	M18	AD26	
K19	$\overline{\text{TXDATA\_OUT\_B}}$	connecto to ball K18	M19	TXINH_OUT_B	connect to ball M20
K20	NC		M20	TXINH_IN_B	connect to ball M19
K21	IDSEL#		M21	NC	
K22	CLK_SEL_0		M22	Gnd_Logic	
K23	AD17		M23	Gnd_Logic	
K24	AD24		M24	Gnd_Logic	

Table 74. All Versions Pinout		
Ball	**Signal**	**Notes**
N1	GND_Xcvr	
N2	GND_Xcvr	
N3	GND_Xcvr	
N4	NC	
N5	NC	
N6	NC	
N7	NC	
N8	NC	
N9	+3.3V_Xcvr	
N10	NC	
N11	NC	
N12	RXDATA_OUT_B	connect to ball N13
N13	RXDATA_IN_B	connect to ball N12
N14	NC	
N15	NC	
N16	AD30	
N17	AD25	
N18	PCI_CLK	
N19	+3.3V_Logic	
N20	+3.3V_Logic	
N21	NC	
N22	Gnd_Logic	
N23	Gnd_Logic	
N24	Gnd_Logic	

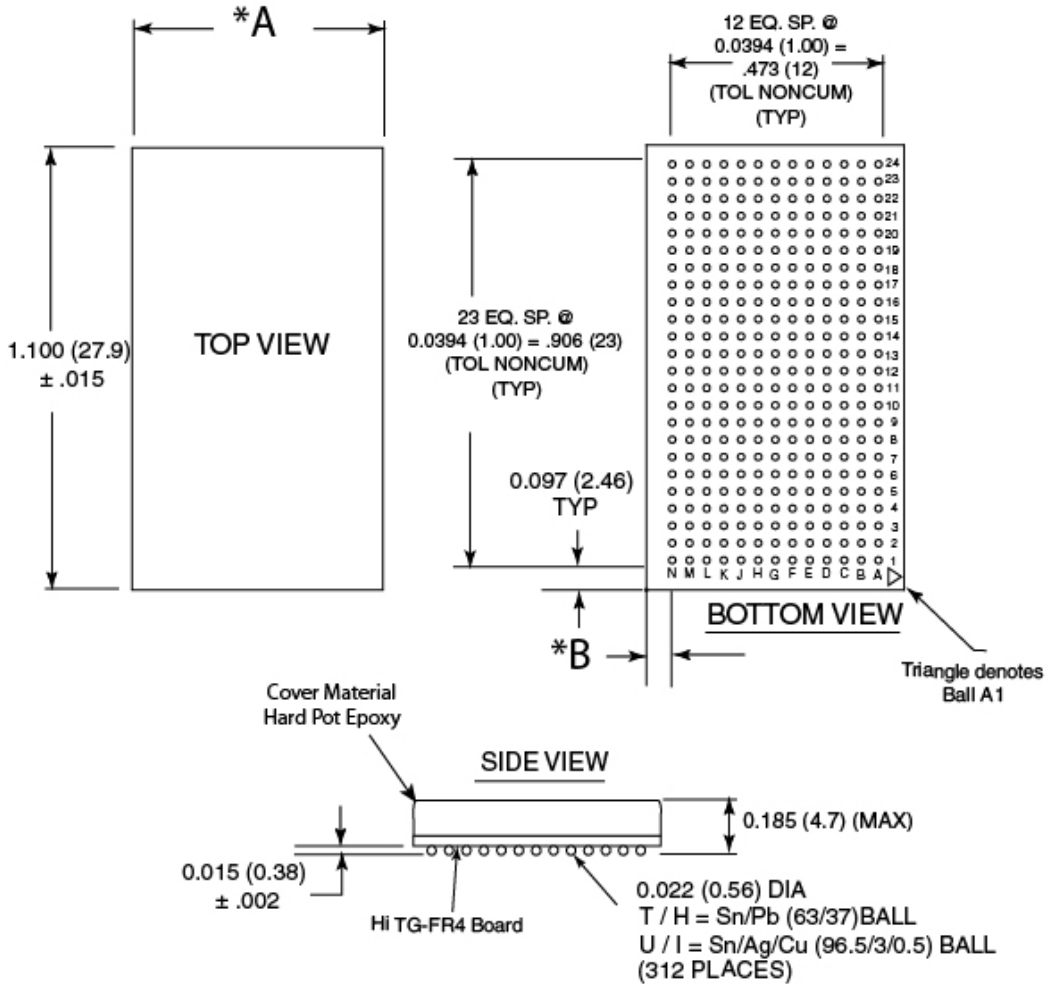
***See Thermal Management Section for important user information

NC = Do not connect – no user connections to these balls allowed

GND_Xcvr /Thermal = Thermal Ball – must be connected to PWB Thermal Plane

“Connect to ball XXX” = Logic Transceiver Interconnect Signals

Table 75. Total-ACE BU-65843T8-600 (BGA Package) "Daisy Chain" Mechanical Sample Connections				
Ball Pairs Wired Together	**Ball Pairs Wired Together**	**Ball Pairs Wired Together**	**Ball Pairs Wired Together**	**Ball Pairs Wired Together**
A1-A2	D1-D2	G1-G2	K1-K2	N1-N2
A3-A4	D3-D4	G3-G4	K3-K4	N3-N4
A5-A6	D5-D6	G5-G6	K5-K6	N5-N6
A7-A8	D7-D8	G7-G8	K7-K8	N7-N8
A9-A10	D9-D10	G9-G10	K9-K10	N9-N10
A11-A12	D11-D12	G11-G12	K11-K12	N11-N12
A13-A14	D13-D14	G13-G14	K13-K14	N13-N14
A15-A16	D15-D16	G15-G16	K15-K16	N15-N16
A17-A18	D17-D18	G17-G18	K17-K18	N17-N18
A19-A20	D19-D20	G19-G20	K19-K20	N19-N20
A21-A22	D21-D22	G21-G22	K21-K22	N21-N22
A23-A24	D23-D24	G23-G24	K23-K24	N23-N24
B1-B2	E1-E2	H1-H2	L1-L2	
B3-B4	E3-E4	H3-H4	L3-L4	
B5-B6	E5-E6	H5-H6	L5-L6	
B7-B8	E7-E8	H7-H8	L7-L8	
B9-B10	E9-E10	H9-H10	L9-L10	
B11-B12	E11-E12	H11-H12	L11-L10	
B13-B14	E13-E14	H13-H14	L13-L14	
B15-B16	E15-E16	H15-H16	L15-L16	
B17-B18	E17-E18	H17-H18	L17-L18	
B19-B20	E19-E20	H19-H20	L19-L20	
B21-B22	E21-E22	H21-H22	L21-L22	
B23-B24	E23-E24	H23-H24	L23-L24	
C1-C2	F1-F2	J1-J2	M1-M2	
C3-C4	F3-F4	J3-J4	M3-M4	
C5-C6	F5-F6	J5-J6	M5-M6	
C7-C8	F7-F8	J7-J8	M7-M8	
C9-C10	F9-F10	J9-J10	M9-M10	
C11-C12	F11-F12	J11-J12	M11-M12	
C13-C14	F13-F14	J13-J14	M13-M14	
C15-C16	F15-F16	J15-J16	M15-M16	
C17-C18	F17-F18	J17-J18	M17-M18	
C19-C20	F19-F20	J19-J20	M19-M20	
C21-C22	F21-F22	J21-J22	M21-M22	
C33-C24	F23-F24	J23-J24	M23-M24	



Notes:
1) Dimensions are in inches (mm)
2) Cover material: Hard Pot Epoxy
3) Base material: Substrate is Hi TG-FR4, Enig plated 1/2 oz copper
4) Solder Ball Cluster to be centralized within ±.010 of outline dimensions
5) Solder ball is 0.022". Substrate pads are 0.030" copper that are Solder mask defined to 0.022". Solder ball after reflow has a height of 0.015" and Diameter of 0.028".

*DIMENSIONAL INFORMATION		
PART NUMBER	A	B
BU-658x3T(U)8	0.600 (15.2) ± .015	0.064 (1.63) TYP
BU-658x3H(I)8	0.700 (17.8) ± .015	0.114 (2.89) TYP

Figure 22. Mechanical Outline Drawing for PCI Total-ACE BGA Packages

9 ORDERING INFORMATION

BU-658X 3 X 8-E 0 2

Test Criteria:
2 = MIL-STD-1760 Amplitude

Process Requirements:
0 = Standard DDC practices, no Burn-In

Environmental Temperature Options:
E = -40°C to +100°C (Note 1)
1 = -55°C to +125°C (Notes 1, 2)

Voltage/Transceiver Option:
8 = +3.3 Volts rise/fall times = 100 to 300 ns (1553B)

Package Type:
T = 63 Sn/ 37 Pb Solder Ball
(transformer coupled)
U = 96.5 Sn/ 3 Ag/ 0.5 Cu – Pb-Free Solder Ball
(transformer coupled)
H = 63 Sn/ 37 Pb Solder Ball
(transformer & direct coupled)
I = 96.5 Sn/ 3 Ag/ 0.5 Cu – Pb-Free Solder Ball
(transformer & direct coupled)

Logic / RAM Voltage:
3 = 3.3 Volt Logic/RAM

Product Type (see Product Matrix below):
BU-6584 = BC/RT/MT PCI with 4K x 16 RAM
BU-6586 = BC/RT/MT PCI with 64K x 17 RAM

Notes:
1. Temperature Range applies to case temperature
2. See section 8.7 for thermal management requirements at high transmit duty cycles.
3. See PCI Total-ACE Product Matrix below for valid ordering options
4. Unless otherwise specified, thes products contain tin lead solder

ORDERING INFORMATION FOR TOTAL-ACE MECHANICAL SAMPLE

BU-64843T8-600

Total-ACE (312 Ball BGA) Mechanical Sample, with "daisy chain" connections of alternating balls, for use in environmental (mechanical/thermal) integrity testing.

Standard DDC Processing for BGA Products		
Test	**MIL-STD-883**	
	Method(s)	**Condition(s)**
Inspection	2010, 2017, and 2032	—
Temperature Cycle	1010	B

PCI Total-ACE Product Matrix						
Part Number	**Transformer Coupled**	**Transformer & Direct Coupled**	**Logic Voltage**	**Memory**	**Ram Voltage**	**Transceiver Voltage**
BU-65843T(U)8-E02	✔		3.3V	4K x 16	3.3V	3.3V
BU-65863T(U)8-E02	✔		3.3V	64K x 17	3.3V	3.3V
BU-65843H(I)8-E02		✔	3.3V	4K x 16	3.3V	3.3V
BU-65863H(I)8-E02		✔	3.3V	64K x 17	3.3V	3.3V
BU-65843T(U)8-102	✔		3.3V	4K x 16	3.3V	3.3V
BU-65863T(U)8-102	✔		3.3V	64K x 17	3.3V	3.3V
BU-65843H(I)8-102		✔	3.3V	4K x 16	3.3V	3.3V
BU-65863H(I)8-102		✔	3.3V	64K x 17	3.3V	3.3V

Data Device Corporation

Leadership Built on Over 45 Years of Innovation

Military | Commercial Aerospace | Space | Industrial

Data Device Corporation (DDC) is the world leader in the design and manufacture of high-reliability data bus products, motion control, and solid-state power controllers for aerospace, defense, and industrial automation applications. For more than 45 years, DDC has continuously advanced the state of high-reliability data communications and control technology for MIL-STD-1553, ARINC 429, Synchro/Resolver interface, and Solid-State Power Controllers with innovations that have minimized component size and weight while increasing performance. DDC offers a broad product line consisting of advanced data bus technology for Fibre Channel networks; MIL-STD-1553 and ARINC 429 Data Networking cards, components, and software; Synchro/Resolver interface components; and Solid-State Power Controllers and Motor Drives.

Product Families

Data Bus | Synchro/Resolver | Power Controllers | Motor Drives

DDC is a leader in the development, design, and manufacture of highly reliable and innovative military data bus solutions. DDC's Data Networking Solutions include MIL-STD-1553, ARINC 429, and Fibre Channel. Each Interface is supported by a complete line of quality MIL-STD-1553 and ARINC 429 commercial, military, and COTS grade cards and components, as well as software that maintain compatibility between product generations. The Data Bus product line has been field proven for the military, commercial and aerospace markets.

DDC is also a global leader in Synchro/Resolver Solutions. We offer a broad line of Synchro/Resolver instrument-grade cards, including angle position indicators and simulators. Our Synchro/Resolver-to-Digital and Digital-to-Synchro/Resolver microelectronic components are the smallest, most accurate converters, and also serve as the building block for our card-level products. All of our Synchro/Resolver line is supported by software, designed to meet today's COTS/MOTS needs. The Synchro/Resolver line has been field proven for military and industrial applications, including radar, IR, and navigation systems, fire control, flight instrumentation/simulators, motor/motion feedback controls and drivers, and robotic systems.

As the world's largest supplier of Solid-State Power Controllers (SSPCs) and Remote Power Controllers (RPCs), DDC was the first to offer commercial and fully-qualified MIL-PRF-38534 and Class K Space-level screening for these products. DDC's complete line of SSPC and RPC boards and components support real-time digital status reporting and computer control, and are equipped with instant trip, and true I^2T wire protection. The SSPC and RPC product line has been field proven for military markets, and are used in the Bradley fighting vehicles and M1A2 tank.

DDC is the premier manufacturer of hybrid motor drives and controllers for brush, 3-phase brushless, and induction motors operating from 28 Vdc to 270 Vdc requiring up to 18 kilowatts of power. Applications range from aircraft actuators for primary and secondary flight controls, jet or rocket engine thrust vector control, missile flight controls, to pumps, fans, solar arrays and momentum wheel control for space and satellite systems.

Certifications

Data Device Corporation is ISO 9001: 2008 and AS 9100, Rev. C certified.

DDC has also been granted certification by the Defense Supply Center Columbus (DSCC) for manufacturing Class D, G, H, and K hybrid products in accordance with MIL-PRF-38534, as well as ESA and NASA approved.

Industry documents used to support DDC's certifications and Quality system are: AS9001 OEM Certification, MIL-STD-883, ANSI/NCSL Z540-1, IPC-A-610, MIL-STD-202, JESD-22, and J-STD-020.

DATA DEVICE CORPORATION
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ISO 9001:2008, AS9100C:2009-01
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