Enhanced Miniature Advanced Communications Engine (Enhanced Mini-ACE® Series) Users Guide

MN-6186X-001

Volume 1 - Architectural Reference

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RECORD OF CHANGE

Revision	Date	Pages	Description
A	3/2003	All	Reformatted
B	8/2004	All	Major Revision, See MarCom for Markup
C	8/2005	All	Major Revision
D	1/2007 6/2007	All 255	Major Revision Added note and warning under Figure 19
E	7/2007	127	Change in Table 86
F	12/2007	222, various	Added double buffering support note, modified Tables 61 and 155, misc typographical edits.
G	2/2008	Various	Removed tables 1 and 2, edited former table 4, renumbered all tables.
H	5/2008	180	Changed minor typo
J	8/2008	13, 34, 68	Edits to tables 6 and 40. Changed note on page 68.
K	1/2009	Various	Addition of the Total-ACE product line
L	5/2009	85, 114	Edit to Table 69 and Table 85
M	4/2010	94, 96	Edits to Table 75 and corresponding Equal and Less Than Flag descriptions on page 96, edits to Table 111
N	2/2012	101, 290	Update to section 4.31 and 6.45
P	11/2012	290, 313	Changed “0x8B90” to “0X8B80” on page 290. Removed redundant RT_AD_LAT text on page 313.
R	2/2018	44	Updated “Important Note” section.

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1 PREFACE

This User's Guide employs typographical conventions to assist the reader in identifying content.

1.1 Text Usage

BOLD–indicates important information and table, figure, and chapter references.

BOLD ITALIC–designates DDC Part Numbers.

`Courier New`–indicates code examples.

<…> - indicates user-entered text or commands.

1.2 Special Handling and Cautions

The ***Enhanced Mini-ACE Series*** uses state-of-the-art components, and proper care should be used to ensure that the device will not be damaged by Electrical Static Discharge (ESD), physical shock, or improper power surges and that precautions are taken to avoid electrocution.

Cautionary Notice

Turn off power to the PC and unplug from wall.

NEVER insert or remove card with power turned on.

Ensure that standard ESD precautions are followed. As a minimum, one hand should be grounded to the power supply in order to equalize the static potential.

Do not store disks in environments exposed to excessive heat, magnetic fields or radiation.

1.3 Trademarks

All trademarks are the property of their respective owners.

2 INTRODUCTION

All references throughout this document to the “Enhanced Mini-ACE” shall be interpreted to include Enhanced Mini-ACE, Micro-ACE, Mini-ACE Mark3, Micro-ACE TE, and Total-ACE products. Any specific references to a unique series of components (i.e. Micro-ACE only) will utilize the component part number (i.e. BU-61740B, BU-61840B/61860B etc.).

The Enhanced Mini-ACE family (Enhanced Mini-ACE, Micro-ACE, Mini-ACE Mark 3, Micro-ACE TE, Total-ACE) of MIL-STD-1553 terminals provides complete interfaces between a host processor and a 1553 bus. All these terminals integrate dual transceiver, protocol logic, and 4K words or 64K words of RAM. Additionally, the Total-ACE integrates the isolation transformer(s) as well. The BC/RT/MT versions with 64K words of RAM include built-in RAM parity checking.

The Enhanced Mini-ACE is packaged in a choice of a 1.0-inch square Flat Pack or Gull Wing package, or a 0.815-inch square BGA package (Micro-ACE). The Mini-ACE Mark 3 is packaged in a choice of a 0.890-inch Flat Pack or Gull Wing package, or a 0.815-inch square BGA package (Micro-ACE-TE). The Total-ACE is packaged in a 1.100-inch x 0.600-inch rectangular, plastic BGA.

The Flat Pack or Gull Wing packaged Enhanced Mini-ACE provides footprint compatibility with the previous generation Mini-ACE (Plus) terminal.

All members of the Enhanced Mini-ACE series (Enhanced Mini-ACE, Micro-ACE, Mini-ACE Mark3, Micro-ACE-TE, and Total-ACE) provide software compatibility with the previous generation Mini-ACE (Plus) terminals, and the older ACE series.

The Enhanced Mini-ACE and Micro-ACE are powered by a choice 5V, or 5V/3.3V (3.3V logic). Multiprotocol support of MIL-STD-1553A/B and STANAG 3838, including versions incorporating McAir compatible transmitters, is provided. There is a choice of 10, 12, 16, or 20 MHz clocks.

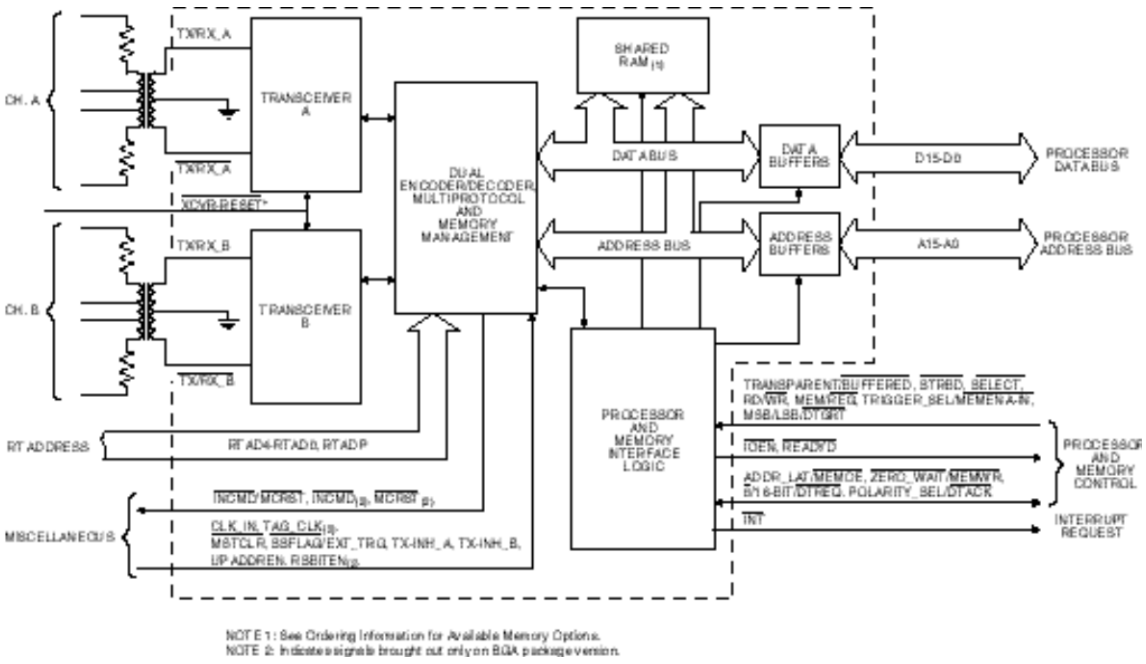
The Mini-ACE Mark3 and Micro-ACE-TE are powered by a choice of 3.3V/5V (logic), and 3.3V/5V (transceivers). (Certain combination restrictions apply. See datasheet for full ordering information). Multiprotocol support of MIL-STD-1553A/B and STANAG 3838, including versions incorporating McAir compatible transmitters, is provided. There is a choice of 10, 12, 16, or 20 MHz clocks.

The Total-ACE is an all 3.3V device (logic & transceivers) with integrated isolation transformers. (Certain combination restrictions apply. See datasheet for full ordering information). Multiprotocol support of MIL-STD-1553A/B and STANAG 3838, is provided. There is a choice of 10, 12, 16, or 20 MHz clocks.

BC features include a built-in engine, with a set of 20 instructions. This provides an autonomous means of implementing multi-frame message scheduling, message retry schemes, data double buffering, asynchronous message insertion, and reporting to the host CPU. The Enhanced Mini-ACE incorporates a fully autonomous built-in selftest, which provides comprehensive testing of the internal protocol logic and/or RAM.

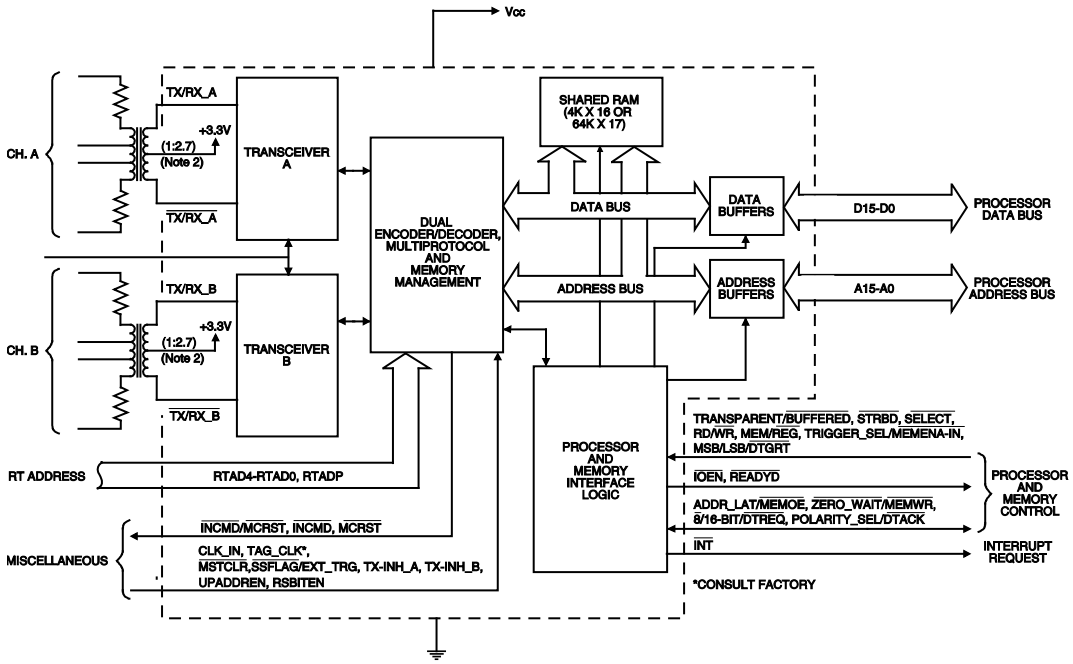
The Enhanced Mini-ACE RT offers the same choices of subaddress buffering as ACE and Mini-ACE (Plus), along with a global circular buffering option, 50% rollover interrupt for circular buffers, an interrupt status queue, and an “Auto-boot” option to support MIL-STD-1760.

The Enhanced Mini-ACE terminals provide the same flexibility in host interface configurations as the Mini-ACE (Plus) terminals, and the older ACE series along with a reduction in the host processor’s worst-case holdoff time.



NOTE 1: See Ordering Information for Available Memory Options.
NOTE 2: Indicates signals brought out only on BGA package version.

Figure 1. Enhanced Mini-ACE / Micro-ACE Series Block Diagram



Note 1: See Ordering Information for Available Memory Options.
Note 2: Transformer-Coupled configuration and ratio shown.

Figure 2. Mini-ACE Mark3 and Micro-ACE-TE Series Block Diagram (Shown with +3.3V Transceivers)

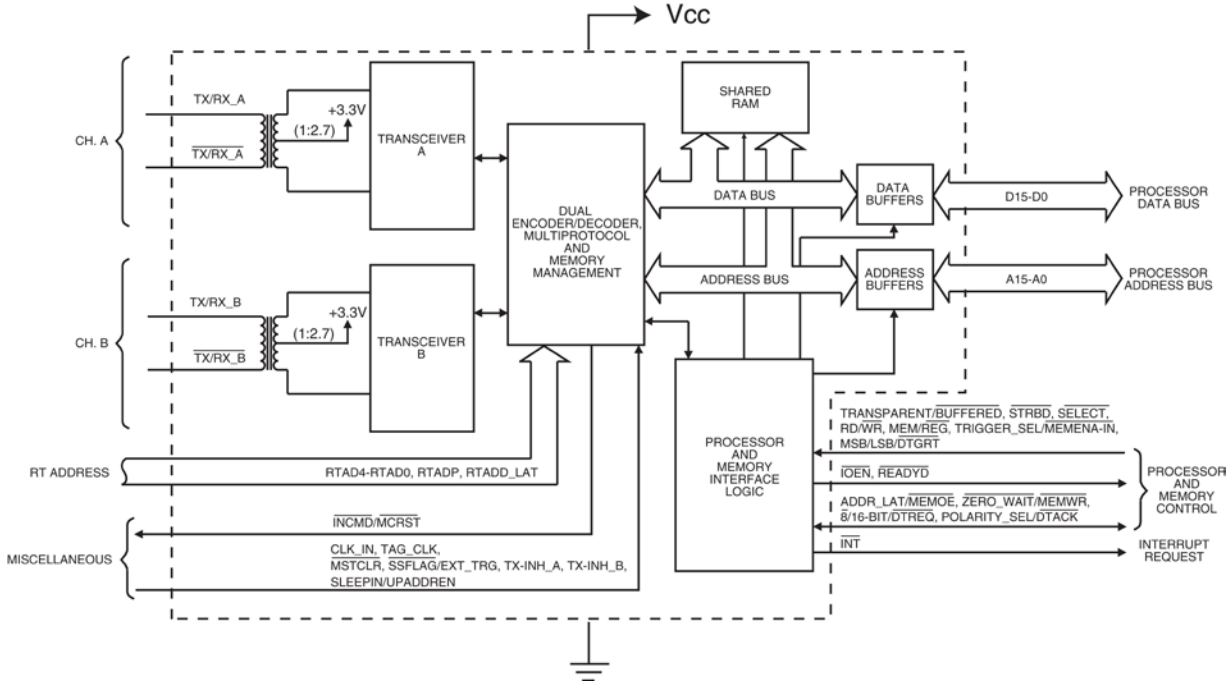


Figure 3. Total-ACE Block Diagram

2.1 Device Specifications

The Latest Device Specifications for the Enhanced Mini-Ace/ Micro-Ace and Mini-ACE Mark3/ Micro-ACE TE, and Total-ACE are available at http://www.ddc-web.com:

For the latest Enhanced Mini-ACE/Micro-ACE information, see the BU-6174X/6184X/1686X Data Sheet.

For the latest Mini-ACE/Micro-ACE information, see the BU-6474X/6484X/6486X Data Sheet.

For the latest Total-ACE information, see the BU-64843T Data Sheet.

3 FUNCTIONAL OVERVIEW

The BU-61743/61745 RT, and BU-61843/61845/61864/61865 BC/RT/MT Enhanced Mini-ACE (BU-61740B RT, and BU-61840B/61860B BC/RT/MT Micro-ACE), BU-64743/64745 RT, and BU-64843/64845/64863 BC/RT/MT Mini-ACE Mark3 (BU-64840B/64843B/64860B/64863B BC/RT/MT Micro-ACE-TE), and the BU-64843T Total-ACE family of MIL-STD-1553 terminals comprise a complete integrated interface between a host processor and a MIL-STD-1553 bus.

The BU-61743/61745 RT, and BU-61843/61845/61864/61865 BC/RT/MT Enhanced Mini-ACE are packaged in a 1.0-inch square ceramic flatpack package providing footprint (with four pin differences) compatibility with previous generation Mini-ACE terminals.

The BU-64743/64745 RT, and BU-64843/64845/64863 BC/RT/MT Mini-ACE Mark3 are packaged in a 0.890-inch square ceramic flatpack package. The BU-61740B RT, and BU-61840B/61860B BC/RT/MT Micro-ACE and BU-64840B/64843B/64860B/64863B BC/RT/MT Micro-ACE-TE are packaged in a 0.815-inch square BGA package.

The BU-64843T BC/RT/MT Total-ACE (with integrated isolation transformers) is packaged in a 1.100-inch x 0.600-inch rectangular, plastic BGA.

The Enhanced Mini-ACE series of hybrids provides software compatibility with the previous generation Mini-ACE terminals, as well as software compatibility with the older ACE series.

The Enhanced Mini-ACE RT provides complete multi-protocol support of MIL-STD-1553A/B/McAir and STANAG 3838. All versions integrate dual transceiver; along with protocol, host interface, memory management logic; and a minimum of 4K words of RAM. In addition, the BU-61864/BU-61865/61860B/64863/64860B/64863B BC/RT/MT terminals include 64K words of internal RAM, with built-in parity checking.The Enhanced Mini-ACE series includes 5V or 3.3V, voltage source transceivers for improved line driving capability, with options for MIL-STD-1760 and McAir compatibility. As a means of reducing power consumption, there are versions for which the logic is powered by 3.3V, rather than 5V. To provide further flexibility, the Enhanced Mini-ACE may operate with a choice of 10, 12, 16, or 20 MHz clock inputs.

One of the salient new features of the Enhanced Mini-ACE is its enhanced bus controller architecture. The Enhanced BC's highly autonomous message sequence control engine provides a means for offloading the host processor for implementing minor and major frame timing control; asynchronous message insertion; data block double buffering; bulk data transfers; and retry and bus switching strategy. For the purpose of performing messaging to the host processor, the Enhanced BC mode includes a General Purpose Queue, along with user-defined interrupts.

The Enhanced Mini-ACE is the latest device group in the ACE family. The term “enhanced” has also been used in earlier versions of the family to describe new features introduced at each stage. For backward compatibility reasons, the same terms and options have been maintained in the Enhanced Mini-ACE. The user will be aware of Enhanced Mode, set by bit 15 of Configuration Register (CR) # 3 along with the following optional features from earlier families:

Enhanced RT Memory Management	CR#2 Bit #1
Enhanced RT Interrupt Handling	CR#2 Bit #15
Enhanced Mode Code Handling	CR#3 Bit #0
Enhanced Mode Enable	CR#3 Bit #15
Expanded BC Control Word Enable	CR#4 Bit #12

Plus for the latest devices:

Enhanced BC	CR#6 Bit #15
Enhanced Time Tag Synchronization	CR#7 Bit #2
Enhanced BC Watchdog Timer Enable	CR#7 Bit #1

In many cases, the user may wish to enable most of these bits at initialization to have all available features active.

A second major new feature of the Enhanced Mini-ACE is the incorporation of a fully autonomous built-in self-test. This test provides comprehensive testing of the internal protocol logic. A separate test verifies the operation of the internal RAM. Since the self-tests are fully autonomous, they eliminate the need for the host to write and read stimulus and response vectors.

The Enhanced Mini-ACE RT offers the same choices of single, double, and circular buffering for individual subaddresses as the ACE and Mini-ACE (Plus). New enhancements to the RT architecture include a global circular buffering option for multiple (or all) receive subaddresses, a 50% rollover interrupt for circular buffers, an interrupt status queue for logging up to 32 interrupt events, and an option to automatically initialize to RT mode with the busy bit set. The interrupt status queue and 50% rollover interrupt features are also included as improvements to the Enhanced Mini-ACE’s monitor architecture.

To minimize board space and "glue" logic, the Enhanced Mini-ACE terminals provide the same wide choice of host interface configurations as the ACE and Mini-ACE (Plus). This includes support of shared RAM interfaces to 16-bit or 8-bit processors, memory or port type interfaces, and multiplexed or non-multiplexed address/data buses; plus a DMA interface configuration.

Hermetic, ceramic packaged, Enhanced Mini-ACE series terminals are available in versions operating over the full military temperature range of -55 to +125°C. Available screened to MIL-PRF-38534C, these terminals are ideal for military and industrial processor-to-1553 applications.

3.1 Transceivers

The transceivers in the Enhanced Mini-ACE series of terminals are fully monolithic, requiring only a +5 or 3.3 volt power input. The transmitters are voltage sources, which provide improved line driving capability over current sources. This serves to improve performance on long buses with many taps. The transmitters also offer an option that satisfies the MIL-STD-1760 requirement for a minimum of 20 volts peak-to-peak, transformer coupled output.

Besides eliminating the demand for an additional power supply, the use of a +5V or 3.3V -only transceivers requires the use of a step-up, rather than a step-down, isolation transformer. This provides the advantage of higher terminal input impedance than is possible for a 15 volt or 12 volt transmitter. As a result, there is a greater margin for the input impedance test, mandated for the 1553 validation test. This characteristic allows for longer cable lengths between a system connector and the isolation transformers of an embedded 1553 terminal. To provide compatibility to McAir specs, the Enhanced Mini-ACE is available with an option for transmitters with increased rise and fall times.

The receiver sections of the Enhanced Mini-ACE are fully compliant with MIL-STD-1553B Notice 2 in terms of front end over voltage protection, threshold, common mode rejection, and word error rate.

4 REGISTERS

4.1 Power Turn-On / Initialization State

The Enhanced Mini-ACE reverts to its power turn-on, or initialization state, following either a hardware or software reset. A hardware reset, which generally occurs following power turn-on, is caused by asserting the $\overline{\text{MSTCLR}}$ input to logic "0" for at least 100 ns, and then transitioning $\overline{\text{MSTCLR}}$ from logic “0” to logic “1.”

Note that in order to ensure correct initialization of the Enhanced Mini-ACE transceivers, the rise time of $\overline{\text{MSTCLR}}$ MUST be less than 10 µs.

The Enhanced Mini-ACE will **automatically** perform its built-in protocol self-test following power turn-on. That is, the test will be initiated following a hardware reset; i.e., after the MSTCLR (reset) input transitions from logic "0" to logic "1.” There exists a ball programmable option “RSTBITEN” on BU-61740B RT, and BU-61840B/61860B BC/RT/MT Micro-ACE and BU-64840B/64843B/64860B/64863B BC/RT/MT Micro-ACE-TE, and BU-64843T Total-ACE components which is used to disable both the automatic, power-up built-in protocol self-test and manually initiated protocol self-test. Note that the self-test will **not** automatically be performed following a software reset; that is, after the host writes a value of logic "1" to bit 0 of the Start/Reset Register (Write 03H). If the host attempts a **write access** to the Enhanced Mini-ACE registers or internal RAM (e.g., to perform initialization) while the self-test is being performed, the register or RAM transfer will **not** be completed correctly. Table 1 illustrates the time for performing the power turn-on protocol self-test, in milliseconds.

Table 1. Protocol Self-Test Times (in ms)

		10 MHz	12 MHz	16 MHz	20 MHz
Protocol Self-Test		3.2	2.7	2.0	1.6
RAM Self-Test	4K RAM	4.1	3.4	2.6	2.0
	64K RAM	65.5	54.6	42.0	32.8

Therefore, when porting software that was used for a previous ACE or Mini-ACE (Plus) application to the Enhanced Mini-ACE, it is recommended that software initialization be delayed until after the completion of the power-on self-test.

A software reset occurs when the host CPU writes a logic "1" to RESET, bit 0 of the Start/Reset Register. In addition, the Enhanced Mini-ACE's RT protocol logic will be reset approximately 2 µs following the mid-parity bit zero crossing of a received Reset remote terminal mode code Command Word. Note that the Enhanced Mini-ACE will not perform its protocol self-test following software reset.

The state of the Enhanced Mini-ACE's internal logic following a hardware, software, or "Reset RT" (mode code) reset is summarized in Table 2.

Table 2. Reset Conditions			
	Following Hardware Reset ($\overline{\text{MSTCLR}}$ input)	**Following Software Reset (bit 0 of Start/Reset Register)**	**Following Reception of a 1553B Reset Remote Terminal Mode Command**
Protocol Self-Test	**Will be** performed.	**Will not be** performed.	If RT HALT ENABLE (bit 4 of Configuration Register #7) is logic "1," the Enhanced Mini-ACE RT will automatically go to an offline (BC or idle) state, but the protocol self-test will **not** automatically be performed. Self-test must then be initiated by the host.
Protocol Self-Test with device strapped for RTBOOT* (4K RAM version only)	**Will be** performed. Device initializes as RT with Busy status word bit set (Config. Reg. #1, bit #10 = Zero).	**Will not be** performed. Device initializes as RT with Busy status word bit set (Config. Reg. #1, bit #10 = Zero).	Protocol self-test will **not** be performed. Self-test must be initiated by the host. Device remains in RT mode with Busy status word bit set (Config. Reg. #1, bit #10 = Zero).
1553 Message Activity in Progress	Message Activity Aborted	Message Activity Aborted	Message Activity Continues
Interrupt Mask Register	Cleared to 0000	Cleared to 0000	No change
Configuration Registers	All cleared to 0000	All cleared to 0000	No change
Transmitter Inhibited Conditions (from mode command), Terminal Flag Inhibited Condition, and Message Error and Broadcast Command Received bits (if 1553A MODE CODES are not enabled).	Transmitters are re-enabled (if inhibited); Terminal Flag bit re-enabled (if inhibited); Message Error and Broadcast Command Received RT Status Word bits are cleared to logic "0."	Transmitters are re-enabled (if inhibited); Terminal Flag bit re-enabled (if inhibited); Message Error and Broadcast Command Received RT Status Word bits are cleared to logic "0."	Transmitters are re-enabled (if inhibited); Terminal Flag bit re-enabled (if inhibited); Message Error bit cleared to logic "0," unless Reset RT mode command is illegalized; Broadcast Command Received bit cleared to "0," unless the Reset RT mode command is received to address 11111. Bits 15 through 9 in the RT BIT Word are cleared to logic "0."
Transmitter Inhibited Condition (from mode command), Terminal Flag Inhibited Condition, and Message Error and Broadcast Command Received bits (if 1553A MODE CODES are enabled).	Transmitters are re-enabled (if inhibited); Terminal Flag bit re-enabled (if inhibited); Message Error and Broadcast Command Received RT Status Word bits are cleared to logic "0."	Transmitters are re-enabled (if inhibited); Terminal Flag bit re-enabled (if inhibited); Message Error and Broadcast Command Received RT Status Word bits are cleared to logic "0."	No change
Address and Data uses	Revert to High impedance state Immediately	No change	No change
RT Address Parity	Clears to 00000 0	No change	No change
BIT Test Status Register	Clears to 0800. This register is updated as the result of protocol self-test. During protocol self-test, this register should return a value of 4800h, Assuming that the self-test passes, this register will return a value of A800h.	No change.	No change. If the host then initiates protocol self-test, this register should return a value of 4800h; Assuming that the self-test passes, this register will return a value of A800h.

4.2 Overall Address Mapping: Words vs. Bytes

It is important to note that with respect to the Enhanced Mini-ACE's address bus, A15 through A0, all of the Enhanced Mini-ACE's internal address mapping (i.e., pointers) is word-oriented, rather than byte-oriented. Although there are a few exceptions (e.g., the MIL-STD-1750A instruction set architecture), the inherent address mapping for most standard 8-, 16-, and 32-bit microprocessors is byte-oriented. This difference in mapping convention must be taken into account when assigning pointer values and making CPU accesses to the Enhanced Mini-ACE's internal data structures (stack, lookup tables, data tables, etc.) in the Enhanced Mini-ACE's shared RAM address space. That is, in terms of the host processor's memory map, the address offset of these data structures, relative to the Enhanced Mini-ACE's base memory address, will be double the value of the pointer that is stored in the Enhanced Mini-ACE's shared RAM.

For interfacing to most 16-bit microprocessors, the processor's A1 signal connects to the Enhanced Mini-ACE's A0 pin, processor A2 connects to the Enhanced Mini-ACE's A1 pin, processor A16 connects to the Enhanced Mini-ACE's A15 pin. For interfacing to an 8-bit microprocessor, the processor's A0 output connects to the Enhanced Mini-ACE's MSB/LSB input, the processor's A1 output connects to the Enhanced Mini-ACE's A0 pin, processor A2 connects to the Enhanced Mini-ACE's A1 pin, etc.

While the Enhanced Mini-ACE's internal shared RAM is intended primarily for the buffering of 1553 messages and related pointer data, it is important to note that there is no restriction prohibiting the use of this RAM for general purpose program memory or data memory.

4.3 Software Interface: Internal RAM and Registers

The Enhanced Mini-ACE series presents a memory mapped software interface to its host microprocessor. The maximum size of the Enhanced Mini-ACE memory address space is 64K words of RAM. The minimum size of the Enhanced Mini-ACE memory address space is 4K words of internal RAM. For the BU-61743/5 and BU-61843/5, there are 4K of internal RAM. In the Enhanced Mini-ACE's transparent/DMA processor interface configuration, additional external RAM may be added, up to the 64K-word limit.

For devices with 64K of internal RAM, the "X 17" option may be activated by programming RAM PARITY ENABLE, Bit 14 of CR#2, to logic "1." This provides the capability for the Enhanced Mini-ACE to perform parity generation and checking on all RAM accesses. Setting RAM PARITY ERROR, Bit 14 of Interrupt Mask Register #1, to logic "1," allows interrupt reporting of the error.

The Enhanced Mini-ACE's internal register space is either 32 or 64 address locations. To provide compatibility with the previous ACE and Mini-ACE generations, the default size of the register space is 32 words. However, the Enhanced Mini-ACE (Plus) includes an additional 32-word area of address space, to accommodate additional test registers. As shown in Table 3, these upper 32 registers may be made accessible by programming 64-WORD REGISTER SPACE, bit 2 of Configuration Register #6, to logic "1."

Table 3. Register Offset Addresses		
ADDRESS OFFSET (hex)	**REGISTERS**	**NOTES**
00-0F	Operational Registers	Always accessible (by default)
10-17	Test Registers	
18-1F	Operational Registers	
20-3F	Additional Test Registers	Only accessible if 64-WORD REGISTER SPACE (bit 2 of Configuration Register #6) is logic "1"

4.4 Internal Registers Address and Bit Mapping

The software interface of the Enhanced Mini-ACE to the host processor consists of 24 internal operational registers for normal operation, an additional 40 test registers, plus 64K words of shared memory address space. The Enhanced Mini-ACE's 4K X 16 or 64K X 17 internal RAM resides in this address space.

For normal operation, the host processor only needs to access the lower 32 register address locations (00-1F). The next 32 locations (20-3F) should be reserved, since many of these are used for factory test.

The address mapping for the Enhanced Mini-ACE registers is illustrated in Table 4.

Table 4. Register Address Mapping					
ADDRESS LINES					Register Description/Accessibility
A4	A3	A2	A1	A0	
0	0	0	0	0	Interrupt Mask Register #1 (RD/WR)
0	0	0	0	1	Configuration Register #1 (RD/WR)
0	0	0	1	0	Configuration Register #2 (RD/WR)
0	0	0	1	1	Start/Reset Register (WR)
0	0	0	1	1	Non-Enhanced BC or RT Command Stack Pointer/Enhanced BC Instruction List Pointer Register (RD)
0	0	1	0	0	BC Control Word/ RT Subaddress Control Word Register (RD/WR)
0	0	1	0	1	Time Tag Register (RD/WR)
0	0	1	1	0	Interrupt Status Register #1(RD)
0	0	1	1	1	Configuration Register #3 (RD/WR)
0	1	0	0	0	Configuration Register #4 (RD/WR)
0	1	0	0	1	Configuration Register #5 (RD/WR)
0	1	0	1	0	RT/Monitor Data Stack Address Register (RD/WR)
0	1	0	1	1	BC Frame Time Remaining Register (RD)
0	1	1	0	0	BC Time Remaining to Next Message Register (RD)
0	1	1	0	1	Non-Enhanced BC Frame Time/Enhanced BC Initial Instruction Pointer /RT Last Command/MT Trigger Word Register (RD/WR)
0	1	1	1	0	RT Status Word Register (RD)
0	1	1	1	1	RT BIT Word Register (RD)
1	0	0	0	0	Test Mode Register 0
1	0	0	0	1	Test Mode Register 1
1	0	0	1	0	Test Mode Register 2
1	0	0	1	1	Test Mode Register 3
1	0	1	0	0	Test Mode Register 4
1	0	1	0	1	Test Mode Register 5
1	0	1	1	0	Test Mode Register 6
1	0	1	1	1	Test Mode Register 7
1	1	0	0	0	Configuration Register #6 (RD/WR)
1	1	0	0	1	Configuration Register #7 (RD/WR)
1	1	0	1	0	RESERVED
1	1	0	1	1	BC Condition Code Register (RD)
1	1	0	1	1	BC General Purpose Flag Register (WR)
1	1	1	0	0	BIT Test Status Register (RD)
1	1	1	0	1	Interrupt Mask Register #2 (RD/WR)
1	1	1	1	0	Interrupt Status Register #2 (RD)
1	1	1	1	1	BC General Purpose Queue Pointer/ RT-MT Interrupt Status Queue Pointer Register (RD/WR)

Table 5. Interrupt Mask Register #1 (Read/Write 00h)	
BIT	**DESCRIPTION**
15(MSB)	RESERVED
14	RAM PARITY ERROR *
13	BC/RT TRANSMITTER TIMEOUT
12	BC/RT COMMAND STACK ROLLOVER
11	MT COMMAND STACK ROLLOVER
10	MT DATA STACK ROLLOVER
9	HANDSHAKE FAILURE
8	BC RETRY
7	RT ADDRESS PARITY ERROR *
6	TIME TAG ROLLOVER *
5	RT CIRCULAR BUFFER ROLLOVER
4	BC CONTROL WORD/RT SUBADDRESS CONTROL WORD EOM
3	BC END OF FRAME
2	FORMAT ERROR
1	BC STATUS SET/RT MODE CODE/MT PATTERN TRIGGER
0(LSB)	END OF MESSAGE

* Note: See Appendix "F" for important information **IF** any of these bits are enabled (logic "1") **AND** terminal is operating in RT Mode **AND** Interrupt Status Queue is enabled (i.e., bit 6 of Configuration Register #6 is logic "1").

Table 6. Configuration Register #1 (Read/Write 01h)				
BIT	**BC FUNCTION (Bits 11-0 Enhanced Mode Only)**	**RT WITHOUT ALTERNATE STATUS**	**RT WITH ALTERNATE STATUS (Enhanced Mode Only)**	**MONITOR FUNCTION (Enhanced Mode Only, bits 12-0)**
15 (MSB)	RT/$\overline{BC - MT}$ (Logic 0)	(Logic "1")	(Logic "1")	(Logic 0)
14	**MT/$\overline{BC - RT}$ (Logic 0)**	(Logic 0)	(Logic 0)	(Logic "1")
13	CURRENT AREA B/ $\overline{A}$	CURRENT AREA B/ $\overline{A}$	CURRENT AREA B/ $\overline{A}$	CURRENT AREA B/ $\overline{A}$
12	MESSAGE STOP-ON-ERROR	MESSAGE MONITOR ENABLED (MMT)	MESSAGE MONITOR ENABLED	MESSAGE MONITOR ENABLED
11	FRAME STOP-ON-ERROR	$\overline{\text{DYNAMIC BUS CONTROL}}$ $\overline{\text{ACCEPTANCE}}$	S10	TRIGGER WORD ENABLED
10	STATUS SET STOP-ON-MESSAGE	$\overline{\text{BUSY}}$	S09	START-ON-TRIGGER
9	STATUS SET STOP-ON-FRAME	$\overline{\text{SERVICE REQUEST}}$	S08	STOP-ON-TRIGGER
8	FRAME AUTO-REPEAT	$\overline{\text{SSFLAG}}$	S07	NOT USED
7	EXTERNAL TRIGGER ENABLED	$\overline{\text{RTFLAG}}$ (Enhanced Mode Only)	S06	EXTERNAL TRIGGER ENABLED
6	INTERNAL TRIGGER ENABLED	NOT USED	S05	NOT USED
5	INTERMESSAGE GAP TIMER ENABLED	NOT USED	S04	NOT USED
4	RETRY ENABLED	NOT USED	S03	NOT USED
3	DOUBLE/SINGLE* RETRY	NOT USED	S02	NOT USED
2	BC ENABLED (Read Only)	NOT USED	S01	MONITOR ENABLED (Read Only)
1	BC FRAME IN PROGRESS (Read Only)	NOT USED	S00	MONITOR TRIGGERED (Read Only)
0(LSB)	**BC MESSAGE IN PROGRESS (Read Only)**	RT MESSAGE IN PROGRESS (Enhanced mode only, Read only)	RT MESSAGE IN PROGRESS (Read Only)	MONITOR ACTIVE (Read Only)

Table 7. Configuration Register #2 (Read/Write 02h)	
BIT	**DESCRIPTION**
15(MSB)	ENHANCED INTERRUPTS
14	RAM PARITY ENABLE (64K RAM Devices ONLY)
13	BUSY LOOK UP TABLE ENABLE
12	RX SA DOUBLE BUFFER ENABLE
11	OVERWRITE INVALID DATA
10	256-WORD BOUNDARY DISABLE
9	TIME TAG RESOLUTION 2
8	TIME TAG RESOLUTION 1
7	TIME TAG RESOLUTION 0
6	CLEAR TIME TAG ON SYNCHRONIZE *
5	LOAD/TRANSMIT TIME TAG ON SYNCHRONIZE
4	INTERRUPT STATUS AUTO CLEAR
3	LEVEL/PULSE* INTERRUPT REQUEST
2	CLEAR SERVICE REQUEST *
1	ENHANCED RT MEMORY MANAGEMENT
0(LSB)	SEPARATE BROADCAST DATA

* See Appendix "F" for important information IF any of these bits are enabled (Logic "1") AND terminal is operating in RT Mode AND Interrupt Status Queue is enabled (i.e., bit 6 of Configuration Register #6 is Logic "1") AND bits 6, 7 or 14 (Time Tag Rollover, RT Address Parity Error, or RAM Parity Error respectively) of Interrupt Mask Register #1 are enabled (Logic "1").

Table 8. Start/Reset Register (Write 03h)	
BIT	**DESCRIPTION**
15(MSB)	RESERVED
14	RESERVED
13	RESERVED
12	RESERVED
11	CLEAR RT HALT
10	CLEAR SELF-TEST REGISTER
9	INITIATE RAM SELF-TEST
8	RESERVED
7	INITIATE PROTOCOL SELF-TEST
6	BC/MT STOP-ON-MESSAGE
5	BC STOP-ON-FRAME
4	TIME TAG TEST CLOCK
3	TIME TAG RESET
2	INTERRUPT RESET
1	BC/MT START
0(LSB)	RESET

Table 9. BC/RT Command Stack Pointer (Register 03h)	
BIT	**DESCRIPTION**
15(MSB)	COMMAND STACK POINTER 15
•	•
•	•
•	•
0(LSB)	COMMAND STACK POINTER 0

Table 10. BC Control Word Register (Read/Write 04h)	
BIT	**DESCRIPTION**
15(MSB)	TRANSMIT TIMETAG FOR SYNCHRONIZE MODE COMMAND
14	MESSAGE ERROR MASK
13	SERVICE REQUEST BIT MASK
12	BUSY BIT MASK
11	SUBSYSTEM FLAG BIT MASK
10	TERMINAL FLAG BIT MASK
9	RESERVED BITS MASK
8	RETRY ENABLED
7	BUS CHANNEL A/B*
6	OFF-LINE SELF-TEST
5	MASK BROADCAST BIT
4	EOM INTERRUPT ENABLE
3	1553A/B SELECT
2	MODE CODE FORMAT
1	BROADCAST FORMAT
0(LSB)	RT-TO-RT FORMAT

Table 11. RT Subaddress Control Word (Read/Write 04h)	
BIT	**DESCRIPTION**
15 (MSB)	RX: DOUBLE BUFFER ENABLE
14	TX: EOM INT
13	TX: CIRC BUF INT
12	TX: MEMORY MANAGEMENT 2 (MM2)
11	TX: MEMORY MANAGEMENT 1 (MM1)
10	TX: MEMORY MANAGEMENT 0 (MM0)
9	RX: EOM INT
8	RX: CIRC BUF INT
7	RX: MEMORY MANAGEMENT 2 (MM2)
6	RX: MEMORY MANAGEMENT 1 (MM1)
5	RX: MEMORY MANAGEMENT 0 (MM0)
4	BCST: EOM INT
3	BCST: CIRC BUF INT
2	BCST: MEMORY MANAGEMENT 2 (MM2)
1	BCST: MEMORY MANAGEMENT 1 (MM1)
0(LSB)	BCST: MEMORY MANAGEMENT 0 (MM0)

Table 12. Time Tag Register (Read/Write 05h)	
BIT	**DESCRIPTION**
15(MSB)	TIME TAG 15
•	•
•	•
•	•
D0(LSB)	TIME TAG 0

Table 13. Interrupt Register #1 (Read/Write 06h)	
BIT	**DESCRIPTION**
15(MSB)	MASTER INTERRUPT
14	RAM PARITY ERROR
13	TRANSMITTER TIMEOUT
12	BC/RT COMMAND STACK ROLLOVER
11	MT COMMAND STACK ROLLOVER
10	MT DATA STACK ROLLOVER
9	HANDSHAKE FAILURE
8	BC RETRY
7	RT ADDRESS PARITY ERROR
6	TIME TAG ROLLOVER *
5	RT CIRCULAR BUFFER ROLLOVER
4	BC CONTROL WORD/RT SUBADDRESS CONTROL WORD EOM
3	BC END OF FRAME
2	FORMAT ERROR
1	BC STATUS SET/RT MODE CODE/ MT PATTERN TRIGGER
0(LSB)	END OF MESSAGE

***See Appendix "F"** for important information regarding Time Tag Rollover (i.e., bit 6 of Interrupt Register #1 is Logic "1") used in conjunction with Interrupt Status Queue (i.e., bit 6 of Configuration Register #6 is Logic "1")

Table 14. Configuration Register #3 (Read/Write 07h)

BIT	DESCRIPTION
15(MSB)	ENHANCED MODE ENABLE
14	BC/RT COMMAND STACK SIZE 1
13	BC/RT COMMAND STACK SIZE 0
12	MT COMMAND STACK SIZE 1
11	MT COMMAND STACK SIZE 0
10	MT DATA STACK SIZE 2
9	MT DATA STACK SIZE 1
8	MT DATA STACK SIZE 0
7	ILLEGALIZATION DISABLED
6	OVERRIDE MODE T/$\overline{R}$ ERROR
5	ALTERNATE STATUS WORD ENABLE
4	ILLEGAL RX TRANSFER DISABLE
3	BUSY RX TRANSFER DISABLE
2	$\overline{\text{RTFAIL}}$/$\overline{\text{RTFLAG}}$ WRAP ENABLE
1	1553A MODE CODES ENABLE
0(LSB)	ENHANCED MODE CODE HANDLING

Table 15. Configuration Register #4 (Read/Write 08h)

BIT	DESCRIPTION
15(MSB)	EXTERNAL BIT WORD ENABLE
14	INHIBIT BIT WORD IF BUSY
13	MODE COMMAND OVERRIDE BUSY
12	EXPANDED BC CONTROL WORD ENABLE
11	BROADCAST MASK ENA/ $\overline{\text{XOR}}$
10	RETRY IF -A AND M.E.
9	RETRY IF STATUS SET
8	1ST RETRY ALT/$\overline{\text{SAME}}$ BUS
7	2ND RETRY ALT/ $\overline{\text{SAME}}$ BUS
6	VALID M.E./NO DATA
5	VALID BUSY/NO DATA
4	MT TAG GAP OPTION
3	LATCH RT ADDR WITH CONFIG. REG. #5
2	TEST MODE 2
1	TEST MODE 1
0(LSB)	TEST MODE 0

Table 16. Configuration Register #5 (Read/Write 09h)

BIT	DESCRIPTION
15(MSB)	12/$\overline{16}$ MHZ CLOCK SELECT
14	SINGLE-ENDED SELECT
13	EXTERNAL TX INHIBIT A
12	EXTERNAL TX INHIBIT B
11	EXPANDED CROSSING ENABLED
10	RESPONSE TIMEOUT SELECT 1
9	RESPONSE TIMEOUT SELECT 0
8	GAP CHECK ENABLED
7	BROADCAST DISABLED
6	RT ADDRESS LATCH/ $\overline{\text{TRANSPARENT}}$
5	RT ADDRESS 4
4	RT ADDRESS 3
3	RT ADDRESS 2
2	RT ADDRESS 1
1	RT ADDRESS 0
0	RT ADDRESS PARITY

Table 17. RT/Monitor Data Stack Address Register (Read/Write 0Ah)

BIT	DESCRIPTION
15 (MSB)	RT/MONITOR DATA STACK ADDRESS 15
•	•
•	•
•	•
0(LSB)	RT/MONITOR DATA STACK ADDRESS 0

Table 18. BC Frame Time Remaining Register (Read/Write 0Bh)

BIT	DESCRIPTION
15(MSB)	BC FRAME TIME REMAINING 15
•	•
•	•
•	•
0(LSB)	BC FRAME TIME REMAINING 0

NOTE: Resolution = 100 μs per LSB

Table 19. BC Message Time Remaining Register (Read0Ch)

BIT	DESCRIPTION
15(MSB)	BC MESSAGE TIME REMAINING 15
•	•
•	•
•	•
0(LSB)	BC MESSAGE TIME REMAINING 0

Table 20. Non-Enhanced BC Frame Time/Enhanced BC Initial Instruction Pointer/RT Last Command/MT Trigger Register (Read/Write 0Dh)

BIT	DESCRIPTION
15(MSB)	BIT 15
•	•
•	•
•	•
0(LSB)	BIT 0

Table 21. RT Status Word Register (Read 0Eh)

BIT	DESCRIPTION
15(MSB)	LOGIC “0”
14	LOGIC “0”
13	LOGIC “0”
12	LOGIC “0”
11	LOGIC “0”
10	MESSAGE ERROR
9	INSTRUMENTATION
8	SERVICE REQUEST
7	RESERVED
6	RESERVED
5	RESERVED
4	BROADCAST COMMAND RECEIVED
3	BUSY
2	SUBSYSTEM FLAG
1	DYNAMIC BUS CONTROL ACCEPT
0(LSB)	TERMINAL FLAG

Table 22. RT BIT Word Register (Read 0Fh)

BIT	DESCRIPTION
15(MSB)	TRANSMITTER TIMEOUT
14	LOOP TEST FAILURE B
13	LOOP TEST FAILURE A
12	HANDSHAKE FAILURE
11	TRANSMITTER SHUTDOWN B
10	TRANSMITTER SHUTDOWN A
9	TERMINAL FLAG INHIBITED
8	BIT TEST FAIL
7	HIGH WORD COUNT
6	LOW WORD COUNT
5	INCORRECT SYNC RECEIVED
4	PARITY/MANCHESTER ERROR RECEIVED
3	RT-RT GAP/SYNC/ADDRESS ERROR
2	RT-RT NO RESPONSE ERROR
1	RT-RT 2ND COMMAND WORD ERROR
0(LSB)	COMMAND WORD CONTENTS ERROR

Table 23. Configuration Register #6 (Read/Write 18h)	
BIT	**DESCRIPTION**
15(MSB)	ENHANCED BUS CONTROLLER
14	ENHANCED CPU ACCESS
13	COMMAND STACK POINTER INCREMENT ON EOM (RT, MT)
12	GLOBAL CIRCULAR BUFFER
11	GLOBAL CIRCULAR BUFFER SIZE 2
10	GLOBAL CIRCULAR BUFFER SIZE 1
9	GLOBAL CIRCULAR BUFFER SIZE 0
8	DISABLE INVALID MESSAGES TO INTERRUPT STATUS QUEUE
7	DISABLE VALID MESSAGES TO INTERRUPT STATUS QUEUE
6	INTERRUPT STATUS QUEUE ENABLE *
5	RT ADDRESS SOURCE
4	ENHANCED MESSAGE MONITOR
3	RESERVED
2	64-WORD REGISTER SPACE
1	CLOCK SELECT 1
0(LSB)	CLOCK SELECT 0

*Note: See Appendix "F" for important information **IF** this bit is enabled (logic "1") **AND** terminal is operating in RT Mode **AND** bits 6, 7 or 14 (Time Tag Rollover, RT Address Parity Error, or RAM Parity Error respectively) of Interrupt Mask Register #1 are enabled (logic "1").

Table 24. Configuration Register #7 (Read/Write 19h)	
BIT	**DESCRIPTION**
15(MSB)	MEMORY MANAGEMENT BASE ADDRESS 15
14	MEMORY MANAGEMENT BASE ADDRESS 14
13	MEMORY MANAGEMENT BASE ADDRESS 13
12	MEMORY MANAGEMENT BASE ADDRESS 12
11	MEMORY MANAGEMENT BASE ADDRESS 11
10	MEMORY MANAGEMENT BASE ADDRESS 10
9	RESERVED
8	RESERVED
7	RESERVED
6	RESERVED
5	RESERVED
4	RT HALT ENABLE
3	1553B RESPONSE TIME
2	ENHANCED TIME TAG SYNCHRONIZE
1	ENHANCED BC WATCHDOG TIMER ENABLED
0 (LSB)	MODE CODE RESET/INCMD* SELECT

Table 25. BC Condition Code Register (Read 1Bh)	
BIT	**DESCRIPTION**
15(MSB)	ALWAYS
14	RETRY 1
13	RETRY 0
12	BAD MESSAGE
11	MESSAGE STATUS SET
10	GOOD BLOCK TRANSFER
9	FORMAT ERROR
8	NO RESPONSE
7	GENERAL PURPOSE FLAG 7
6	GENERAL PURPOSE FLAG 6
5	GENERAL PURPOSE FLAG 5
4	GENERAL PURPOSE FLAG 4
3	GENERAL PURPOSE FLAG 3
2	GENERAL PURPOSE FLAG 2
1	EQUAL FLAG/GENERAL PURPOSE FLAG 1
0 (LSB)	LESS THAN FLAG/GENERAL PURPOSE FLAG 1

Table 26. BC General Purpose Flag Register (Write 1Bh)	
BIT	**DESCRIPTION**
15 (MSB)	CLEAR GENERAL PURPOSE FLAG 7
14	CLEAR GENERAL PURPOSE FLAG 6
13	CLEAR GENERAL PURPOSE FLAG 5
12	CLEAR GENERAL PURPOSE FLAG 4
11	CLEAR GENERAL PURPOSE FLAG 3
10	CLEAR GENERAL PURPOSE FLAG 2
9	CLEAR GENERAL PURPOSE FLAG 1
8	CLEAR GENERAL PURPOSE FLAG 0
7	SET GENERAL PURPOSE FLAG 7
6	SET GENERAL PURPOSE FLAG 6
4	SET GENERAL PURPOSE FLAG 4
3	SET GENERAL PURPOSE FLAG 3
2	SET GENERAL PURPOSE FLAG 2
1	SET GENERAL PURPOSE FLAG 1
0 (LSB)	SET GENERAL PURPOSE FLAG 0

Table 27. Bit Test Status Register (Read 1Ch)	
BIT	**DESCRIPTION**
15 (MSB)	PROTOCOL BUILT-IN TEST COMPLETE
14	PROTOCOL BUILT-IN TEST IN PROGRESS
13	PROTOCOL BUILT-IN-TEST PASSED
12	PROTOCOL BUILT-IN-TEST ABORT
11	PROTOCOL BUILT-IN TEST PROGRESS OR COMPLETE
10	LOGIC “0”
9	LOGIC “0”
8	LOGIC “0”
7	RAM BUILT-IN TEST COMPLETE
6	RAM BUILT-IN TEST IN PROGRESS
5	RAM BUILT-IN TEST PASSED
4	LOGIC “0”
3	LOGIC “0”
2	LOGIC “0”
1	LOGIC “0”
0(LSB)	LOGIC “0”

Note for TABLE 26: If the Enhanced Mini-ACE is not online (i.e., processing instructions) in enhanced BC Mode, the BC Condition Code Register will always return a value of 0000.

Table 28. Interrupt Mask Register #2 (Read/Write 1Dh)	
BIT	**DESCRIPTION**
15 (MSB)	NOT USED
14	BC OP CODE PARITY ERROR
13	RT ILLEGAL COMMAND/MESSAGE MONITOR MESSAGE RECEIVED
12	GENERAL PURPOSE QUEUE/ INTERRUPT STATUS QUEUE ROLLOVER
11	CALL STACK POINTER REGISTER ERROR
10	BC TRAP OP CODE
9	RT COMMAND STACK 50% ROLLOVER
8	RT CIRCULAR BUFFER 50% ROLLOVER
7	MONITOR COMMAND STACK 50% ROLLOVER
6	MONITOR DATA STACK 50% ROLLOVER
5	ENHANCED BC IRQ3
4	ENHANCED BC IRQ2
3	ENHANCED BC IRQ1
2	ENHANCED BC IRQ0
1	BIT TEST COMPLETE
0 (LSB)	NOT USED

Table 29. Interrupt Status Register #2 (Read 1Eh)	
BIT	**DESCRIPTION**
15 (MSB)	MASTER INTERRUPT
14	BC OP CODE PARITY ERROR
13	RT ILLEGAL COMMAND/MESSAGE MONITOR MESSAGE RECEIVED
12	GENERAL PURPOSE QUEUE/INTERRUPT STATUS QUEUE ROLLOVER
11	CALL STACK POINTER REGISTER ERROR
10	BC TRAP OP CODE
9	RT COMMAND STACK 50% ROLLOVER
8	RT CIRCULAR BUFFER 50% ROLLOVER
7	MONITOR COMMAND STACK 50% ROLLOVER
6	MONITOR DATA STACK 50% ROLLOVER
5	ENHANCED BC IRQ3
4	ENHANCED BC IRQ2
3	ENHANCED BC IRQ1
2	ENHANCED BC IRQ0
1	BIT TEST COMPLETE
0(LSB)	INTERRUPT CHAIN BIT

Table 30. BC General Purpose Queue Pointer Register RT, MT Interrupt Status Queue Pointer Register (Read/Write 1Fh)	
BIT	**DESCRIPTION**
15 (MSB)	QUEUE POINTER BASE ADDRESS 15
14	QUEUE POINTER BASE ADDRESS 14
13	QUEUE POINTER BASE ADDRESS 13
12	QUEUE POINTER BASE ADDRESS 12
11	QUEUE POINTER BASE ADDRESS 11
10	QUEUE POINTER BASE ADDRESS 10
9	QUEUE POINTER BASE ADDRESS 9
8	QUEUE POINTER BASE ADDRESS 8
7	QUEUE POINTER BASE ADDRESS 7
6	QUEUE POINTER BASE ADDRESS 6
5	QUEUE POINTER BASE ADDRESS 5
4	QUEUE POINTER BASE ADDRESS 4
3	QUEUE POINTER BASE ADDRESS 3
2	QUEUE POINTER BASE ADDRESS 2
1	QUEUE POINTER BASE ADDRESS 1
0 (LSB)	QUEUE POINTER BASE ADDRESS 0

Note: Addresses 20(H) – 3F(H) are reserved for Factory Testing

Table 31. BC Mode Block Status Word	
BIT	**DESCRIPTION**
15(MSB)	EOM
14	SOM
13	CHANNEL B/ $\overline{A}$
12	ERROR FLAG
11	STATUS SET
10	FORMAT ERROR
9	NO RESPONSE TIMEOUT
8	LOOP TEST FAIL
7	MASKED STATUS SET
6	RETRY COUNT 1
5	RETRY COUNT 0
4	GOOD DATA BLOCK TRANSFER
3	WRONG STATUS ADDRESS/NO GAP
2	WORD COUNT ERROR
1	INCORRECT SYNC TYPE
0(LSB)	INVALID WORD

Note: Tables 32 to 38 are not registers, but are words stored in various RAM locations.

Table 32. RT Mode Block Status Word	
BIT	**DESCRIPTION**
15(MSB)	EOM
14	SOM
13	CHANNEL B/ $\overline{A}$
12	ERROR FLAG
11	RT-RT FORMAT
10	FORMAT ERROR
9	NO RESPONSE TIMEOUT
8	LOOP TEST FAIL
7	DATA STACK ROLLOVER
6	ILLEGAL COMMAND WORD
5	WORD COUNT ERROR
4	INCORRECT DATA SYNC
3	INVALID WORD
2	RT-RT GAP/SYNCH/ADDRESS ERROR
1	RT-RT 2ND COMMAND ERROR
0(LSB)	COMMAND WORD CONTENTS ERROR

Table 33. MIL-STD-1553 Command Word	
BIT	**DESCRIPTION**
15(MSB)	REMOTE TERMINAL ADDRESS BIT 4
14	REMOTE TERMINAL ADDRESS BIT 3
13	REMOTE TERMINAL ADDRESS BIT 2
12	REMOTE TERMINAL ADDRESS BIT 1
11	REMOTE TERMINAL ADDRESS BIT 0
10	TRANSMIT/$\overline{\text{RECEIVE}}$
9	SUBADDRESS/MODE CODE BIT 4
8	SUBADDRESS/MODE CODE BIT 3
7	SUBADDRESS/MODE CODE BIT 2
6	SUBADDRESS/MODE CODE BIT 1
5	SUBADDRESS/MODE CODE BIT 0
4	DATA WORD COUNT/MODE CODE BIT 4
3	DATA WORD COUNT/MODE CODE BIT 3
2	DATA WORD COUNT/MODE CODE BIT 2
1	DATA WORD COUNT/MODE CODE BIT 1
0(LSB)	DATA WORD COUNT/MODE CODE BIT 0

Table 34. Word Monitor Identification Word	
BIT	**DESCRIPTION**
15(MSB)	GAP TIME (MSB)
•	•
•	•
•	•
8	GAP TIME 0 (LSB)
7	WORD FLAG
6	$\overline{\text{THIS RT}}$
5	$\overline{\text{BROADCAST}}$
4	ERROR
3	COMMAND/$\overline{\text{DATA}}$
2	CHANNEL B/$\overline{\text{A}}$
1	CONTIGUOUS DATA/$\overline{\text{GAP}}$
0(LSB)	$\overline{\text{MODE\_CODE}}$

Table 35. Selective Message Monitor Mode Block Status Word	
BIT	**DESCRIPTION**
15(MSB)	EOM
14	SOM
13	CHANNEL $\overline{\text{B/A}}$
12	ERROR FLAG
11	RT-RT TRANSFER
10	FORMAT ERROR
9	NO RESPONSE TIMEOUT
8	GOOD DATA BLOCK TRANSFER
7	DATA STACK ROLLOVER
6	RESERVED (logic “0”)
5	WORD COUNT ERROR
4	INCORRECT DATA SYNC
3	INVALID WORD
2	RT-RT GAP/SYNC/ADDRESS ERROR
1	RT-RT 2ND COMMAND ERROR
0	COMMAND WORD CONTENTS ERROR

Table 36. RT Status Word	
BIT	**DESCRIPTION**
15(MSB)	REMOTE TERMINAL ADDRESS BIT 4
14	REMOTE TERMINAL ADDRESS BIT 3
13	REMOTE TERMINAL ADDRESS BIT 2
12	REMOTE TERMINAL ADDRESS BIT 1
11	REMOTE TERMINAL ADDRESS BIT 0
10	MESSAGE ERROR
9	INSTRUMENTATION
8	SERVICE REQUEST
7	RESERVED
6	RESERVED
5	RESERVED
4	BROADCAST COMMAND RECEIVED
3	BUSY
2	SUBSYSTEM FLAG
1	DYNAMIC BUS CONTROL ACCEPTANCE
0(LSB)	TERMINAL FLAG

Table 37. RT/Monitor Interrupt Status Word (for Interrupt Status Word)		
BIT	**DEFINITION FOR MESSAGE INTERRUPT EVENT**	**DEFINITION FOR NON-MESSAGE INTERRUPT EVENT**
15	TRANSMITTER TIMEOUT	NOT USED
14	ILLEGAL COMMAND	NOT USED
13	MONITOR DATA STACK 50% ROLLOVER	NOT USED
12	MONITOR DATA STACK ROLLOVER	NOT USED
11	RT CIRCULAR BUFFER 50% ROLLOVER	NOT USED
10	RT CIRCULAR BUFFER ROLLOVER	NOT USED
9	MONITOR COMMAND (DESCRIPTOR) STACK 50% ROLLOVER	NOT USED
8	MONITOR COMMAND (DESCRIPTOR) STACK ROLLOVER	NOT USED
7	RT COMMAND (DESCRIPTOR) STACK 50% ROLLOVER	NOT USED
6	RT COMMAND (DESCRIPTOR) STACK ROLLOVER	NOT USED
5	HANDSHAKE FAIL	NOT USED
4	FORMAT ERROR	TIME TAG ROLLOVER
3	MODE CODE INTERRUPT	RT ADDRESS PARITY ERROR
2	SUBADDRESS CONTROL WORD EOM	PROTOCOL SELF-TEST COMPLETE
1	END-OF-MESSAGE (EOM)	RAM PARITY ERROR
0	“1” FOR MESSAGE INTERRUPT EVENT; “0” FOR NON-MESSAGE INTERRUPT EVENT	

4.5 Register Function Summary

A summary of the Enhanced Mini-ACE's 24 non-test registers is as follows:

Interrupt Mask Registers #1 and #2 are used to enable and disable interrupt requests for various events and conditions.

Configuration Registers #1 and #2 are used to select the Enhanced Mini-ACE's mode of operation, and for software control of RT Status Word bits, Active Memory Area, BC Stop-On-Error, RT Memory Management mode selection, and control of the Time Tag operation.

Start/Reset Register is used for "command" type functions such as software reset, BC/MT Start, Interrupt reset, Time Tag Reset, Time Tag Register Test, Initiate protocol self-test, Initiate RAM self-test, Clear self-test register, and Clear RT Halt. The Start/Reset Register also includes provisions for stopping the BC in its auto-repeat mode, either at the end of the current message or at the end of the current BC frame.

BC/RT Command Stack Register allows the host processor to determine the pointer location for the current or most recent message.

BC Instruction List Pointer Register may be read to determine the current location of the Instruction List Pointer for the Enhanced BC mode.

BC Control Word/RT Subaddress Control Word Register: In BC mode, allows host access to the current word or most recent BC Control Word. The BC Control Word contains bits that select the active bus and message format, enable off-line self-test, masking of Status Word bits, enable retires and interrupts, and specify MIL-STD-1553A or -1553B error handling. In RT mode, this register allows host access to the current or most recent Subaddress Control Word. The Subaddress Control Word is used to select the memory management scheme and enable interrupts for the current message.

Time Tag Register maintains the value of a real-time clock. The resolution of this register is programmable from among 2, 4, 8, 16, 32, and 64 μs/LSB. The Start-of-Message (SOM) and End-of-Message (EOM) sequences in BC, RT, and Message Monitor modes cause a write of the current value of the Time Tag Register to the stack area of the RAM.

Interrupt Status Register #1 and #2 allow the host processor to determine the cause of an interrupt request by means of one or two read accesses. The interrupt events of the two Interrupt Status Registers are mapped to correspond to the respective bit positions in the two Interrupt Mask Registers. Interrupt Status Register #2 contains an INTERRUPT CHAIN bit, used to indicate an interrupt event from Interrupt Status Register #1.

Configuration Registers #3, #4, and #5 are used to enable many of the Enhanced Mini-ACE's advanced features that were implemented by the prior generation products, the ACE and Mini-ACE (Plus). For BC, RT, and MT modes, use of the

ENHANCED MODE enables the various read-only bits in Configuration Register #1. For BC mode, ENHANCED mode features include the expanded BC Control Word and BC Block Status Word, additional Stop-On-Error and Stop-On-Status Set functions, frame auto-repeat, programmable intermessage gap times, automatic retires, expanded Status Word Masking, and the capability to generate interrupts following the completion of any selected message. For RT mode, the enhanced mode features include the expanded RT Block Status Word, combined RT/Selective Message Monitor mode, internal wrapping of the $\overline{\text{RTFAIL}}$ output signal to the $\overline{\text{RTFAIL}}$ RT Status Word bit; the double buffering scheme for individual receive (broadcast) subaddresses, and the alternate (fully software programmable) RT Status Word. For MT mode, use of the enhanced mode enables the Selective Message Monitor, the combined RT/Selective Monitor modes, and the monitor triggering capability.

RT/Monitor Data Stack Address Register provides a read/writable indication of the last data word stored for RT or Monitor modes.

BC Frame Time Remaining Register provides a read-only indication of the time remaining in the current BC frame. In the enhanced BC mode, this timer may be used for minor or major frame control, or as a watchdog timer for the BC message sequence control processor. The resolution of this register is 100 μs/LSB.

BC Time Remaining to Next Message Register provides a read-only indication of the time remaining before the start of the next message in a BC frame. In the Enhanced BC mode, this timer may be also be used for the BC message sequence control processor's Delay (DLY) instruction, or for minor or major frame control. The resolution of this register is 1 μs/LSB.

BC Frame Time/RT Last Command/MT Trigger Word Register. In the non-enhanced BC mode, this register is used to program the BC frame time, for use in the frame auto-repeat mode. In Enhanced BC mode, frame time is a parameter that may be programmed by means of the BC Message Sequence Control Engine instruction set. The resolution of this register is 100 μs/LSB, with a range up to 6.55 seconds. In RT mode, this register stores the current (or most previous) 1553 Command Word processed by the Enhanced Mini-ACE RT. In the Word Monitor mode, this register is used to specify a 16-bit Trigger (Command) Word. The Trigger Word may be used to start or stop the monitor, or to generate interrupts.

BC Initial Instruction List Pointer Register enables the host to assign the starting address for the enhanced BC Instruction List.

RT Status Word Register and BIT Word Registers provide read-only indications of the RT Status and BIT Words.

Test Mode Registers 0-7. These registers are included for factory test. In normal operation, these registers do not need to be accessed by the host processor.

Configuration Registers #6 and #7 are used to enable the Enhanced Mini-ACE features that extend beyond the architecture of the Enhanced Mode of the Mini-ACE (Plus). These include the Enhanced BC mode; RT Global Circular Buffer (including buffer size); the RT/MT Interrupt Status Queue, including valid/invalid message filtering; enabling a software-assigned RT address; clock frequency selection; a base

address for the “non-data” portion of Enhanced Mini-ACE memory; LSB filtering for the Synchronize (with data) time tag operations; and enabling a watchdog timer for the Enhanced BC message sequence control engine.

BC Condition Code Register is used to enable the host processor to read the current value of the Enhanced BC Message Sequence Control Engine’s condition flags.

BC General Purpose Flag Register allows the host processor to be able to set, clear, or toggle any of the Enhanced BC Message Sequence Control Engine’s General Purpose condition flags.

BIT Test Status Register is used to provide read-only access of the status of the protocol and RAM built-in self-tests (BIT).

BC General Purpose Queue Pointer provides a means for initializing the pointer for the General Purpose Queue, for the Enhanced BC mode. In addition, this register enables the host to determine the current location of the General Purpose Queue pointer, which is incremented internally by the Enhanced BC message sequence control engine.

RT/MT Interrupt Status Queue Pointer Register provides a means for initializing the pointer for the Interrupt Status Queue, for RT, MT, and RT/MT modes. In addition, this register enables the host to determine the current location of the Interrupt Status Queue pointer, which is incremented internally by the RT/MT message processor.

4.6 Register Bit Maps and Bit Descriptions

4.7 Interrupt Mask Register #1

(Register Address 00000; READ/WRITE

Table 38. Interrupt Mask Register (Read/Write 00H)

BIT	DESCRIPTION
15	RESERVED
14	RAM PARITY ERROR *
13	BC/RT TRANSMITTER TIMEOUT
12	BC/RT COMMAND STACK ROLLOVER
11	MT COMMAND STACK ROLLOVER
10	MT DATA STACK ROLLOVER
9	HANDSHAKE FAILURE
8	BC RETRY
7	RT ADDRESS PARITY ERROR *
6	TIME TAG ROLLOVER *
5	RT CIRCULAR BUFFER ROLLOVER
4	BC CONTROL WORD/RT SUBADDRESS CONTROL WORD EOM
3	BC END OF FRAME
2	FORMAT ERROR
1	BC STATUS SET/RT MODE CODE/MT PATTERN TRIGGER
0(LSB)	END OF MESSAGE

* Note: **See Appendix "F"** for important information **IF** any of these bits are enabled (logic "1") **AND** terminal is operating in RT Mode **AND** Interrupt Status Queue is enabled (i.e., bit 6 of Configuration Register #6 is logic "1").

An interrupt request will be issued (either a pulse or level, as determined by bit 3 of Configuration Register #2) whenever one (or more) of the interrupt request conditions in either Interrupt Status Register #1 and/or Interrupt Status Register #2 occurs and the respective bit of the Interrupt Mask Register is set to logic "1." For a level type of request output, $\overline{\text{INT}}$ will be cleared high after the Interrupt Status Register has been read, if bit 4 of Configuration Register #2 (INTERRUPT STATUS AUTO CLEAR) is set. Otherwise, $\overline{\text{INT}}$ the level may be reset by writing logic "1" to bit 2 (INTERRUPT RESET) of the Start/Reset Register. Note: Interrupt Status Register #2 must also be read if it contains active masked bits before $\overline{\text{INT}}$ will be cleared. Refer to text describing Interrupt Mask # 2.

The respective bit(s) in Interrupt Status Register#1 and/or Interrupt Status Register #2 will be set under either of the following two conditions:

1. The Enhanced Mini-ACE is in its non-ENHANCED mode (ENHANCED MODE ENABLED, bit 15 of Configuration Register #3 is logic "0") **or** ENHANCED INTERRUPTS are not enabled (bit 15 of Configuration Register #2 is logic "0")) **and** the respective bit in the Interrupt Mask Register is logic "1" **and** the condition occurs.

2. The Enhanced Mini-ACE is in its ENHANCED mode (ENHANCED MODE ENABLED, bit 15 of Configuration Register #3 is logic "1") and ENHANCED INTERRUPTS are enabled (bit 15 of Configuration Register #2 is logic "1") and the condition occurs, regardless of whether or not the respective bit in the Interrupt Mask Register is set to logic "1."

In the non-ENHANCED mode (ENHANCED MODE ENABLE, bit 15 of Configuration Register #3, set to logic "0"), bits 7 through 0 of Interrupt Mask Register #1 are used to both enable interrupts for the various events/conditions and to enable the respective bits of the Interrupt Status Register to be set. That is, the various bits of the Interrupt Status Register will not become set if the corresponding bits of the Interrupt Mask Register are not set. Bits 14 through 8 are not used in the non-ENHANCED mode.

In the ENHANCED mode with Enhanced Interrupts Enabled (bit 15 of Configuration Register #2 set to logic "1"), all 29 interrupt events/conditions (indicated by bits 14 through 0 of Interrupt Status Register #1, and bits 14 through 1 of Interrupt Status Register #2) are applicable and the value of the Interrupt Mask Registers has no effect on the operation of the two Interrupt Status Registers. If Enhanced Interrupts are enabled, the bits of the Interrupt Status Registers do not need to be enabled by the corresponding bits in the Interrupt Mask Register. In the Enhanced Interrupt mode, these bits become set following the occurrence of the respective event/condition, regardless of the programming of the corresponding Interrupt Mask Register bit. In either mode, an interrupt for any of the 29 event/conditions (8 in non-ENHANCED mode) is only enabled if the respective bit of the appropriate Interrupt Mask Register (for the event/condition) has been programmed to logic "1."

Table 39 summarizes the effect of the ENHANCED mode and the ENABLE INTERRUPTS bit on the operation of the Interrupt Request output $\overline{\text{INT}}$ and the Interrupt Mask and Interrupt Status Registers.

Table 39. Enhanced Mode Interrupts				
ENHANCED MODE/ NON-ENHANCED	**ENHANCED INTERRUPTS ENABLED BIT (bit 15 of configuration Register #2)**	**INTERRUPT REQUEST ENABLED**	**INTERRUPT STATUS REGISTER BIT ENABLED**	**ACTIVE INTERRUPT MASK AND INTERRUPT STATUS BITS**
NON-ENHANCED	X	If condition enabled by corresponding Interrupt Mask Register bit	If condition enabled by corresponding Interrupt Mask Register bit	Bits 7-0 of Interrupt Status Register #1 only.
ENHANCED	1	If condition enabled by corresponding Interrupt Mask Register bit	**Always Enabled**	Bits 14-0 of Interrupt Status Register #1, and bits 14 through 1 of Interrupt Status Register #2.
ENHANCED	0	If condition enabled by corresponding Interrupt Mask Register bit	**If condition enabled by corresponding Interrupt Mask Register bit**	Bits 7-0 of Interrupt Status Register #1 only

RAM PARITY ERROR (bit 14): This bit is applicable only in the ENHANCED mode (ENHANCED MODE ENABLE, bit 15 of Configuration Register #3, set to logic "1") and if RAM PARITY ENABLE, bit 14 of Configuration Register #2, is logic "1." RAM PARITY ERROR allows an interrupt request to be issued as the result of a RAM parity error during a read access.

IMPORTANT NOTE: For the BU-61743/5 and BU-61843/5 (4K RAM) versions of the Enhanced Mini-ACE, there is **no** 17-bit RAM. Therefore, for these products, RAM parity is NOT implemented. RAM PARITY ERROR **must** be set to logic "0" for 4K RAM versions of the Enhanced Mini-ACE.

For (64K X 17 RAM) version of the Enhanced Mini-ACE, setting RAM PARITY ERROR to logic "1" enables an interrupt request to occur following a RAM parity error.

See Appendix "F" for important information **IF** this bit is enabled (logic "1") **AND** terminal is operating in RT Mode **AND** Interrupt Status Queue is enabled (i.e., bit 6 of Configuration Register #6 is logic "1").

BC/RT TRANSMITTER TIMEOUT (bit 13) : If set, enables an interrupt following a timeout of the Enhanced Mini-ACE's transmitter watchdog timer. This occurs if the Enhanced Mini-ACE's encoder attempts to transmit for longer than 660.5 μs. This interrupt only occurs in the BC or the RT mode.

BC/RT COMMAND STACK ROLLOVER (bit 12) : If set, enables an interrupt following a rollover of the BC or RT stack (Command Stack 1). The size of Command Stack 1 is programmable from among 256 (64 messages), 512, 1024, and 2048 words (512 messages) by means of bits 14 and 13 of Configuration Register #3. This

interrupt only occurs in the ENHANCED mode (bit 15 of Configuration Register #3 programmed to logic "1").

MT COMMAND STACK ROLLOVER (bit 11) : If set, enables an interrupt following a rollover of the Message Monitor Command Stack (Command Stack 2). This is applicable for both the Message Monitor as well as the combined RT/Message Monitor modes. The size of Command Stack 2 is programmable from among 256 (64 messages), 1024, 4096, and 16,384 words (4096 messages) by means of bits 12 and 11 of Configuration Register #3. This interrupt only occurs in the ENHANCED mode (bit 15 of Configuration Register #3 programmed to logic "1").

MT DATA STACK ROLLOVER (bit 10) : If set, enables an interrupt following a rollover of the Word Monitor or Message Monitor Data Stack. The size of the Data Stack is programmable from among 512, 1024, 2048, 4096, 8192, 16,384, 32,768, or 65,536 words by means of bits 10, 9, and 8 of Configuration Register #3. This interrupt only occurs in the ENHANCED mode (bit 15 of Configuration Register #3 programmed to logic "1").

HANDSHAKE FAILURE (bit 9): If set, enables an interrupt following a handshake timeout during a transfer between the 1553 protocol section and the RAM. A Handshake Failure can only occur in the transparent configuration of the Enhanced Mini-ACE host interface. There are two conditions that can cause a Handshake Failure. For both conditions, the maximum allotted time is 10.5 μs for a 20 MHz clock input, 10.0 μs for a 16 MHz clock input, 9.0 μs for a 12 MHz clock input, and 8.5 μs for a 10 MHz clock input:

When the Data Transfer Grant $\overline{(DTGRT)}$ input is not asserted within the allotted time after the Enhanced Mini-ACE's Data Transfer Request $\overline{(DTREQ)}$ output has been asserted.

When the $\overline{(STRBD)}$ input signal is held low too long at the end of a processor transfer cycle (as indicated by the falling edge of READYD*). Note that STRBD* asserted low for too long will **not** result in a HANDSHAKE-FAILURE condition in the buffered mode configuration.

BC RETRY (bit 8): If set, enables an interrupt following the occurrence of a retried message in BC mode. If enabled, the interrupt will occur regardless of whether the retry attempt was successful or unsuccessful.

RT ADDRESS PARITY ERROR (bit 7) : If set, enables an interrupt if an RT Address parity error condition is sensed. That is, if RTAD4-RTAD0 plus RTADP, or, assuming that RT_AD_LAT is connected to logic “1” and RT ADDRESS SOURCE, bit 5 of Configuration Register #6 is logic “1,” if the software-programmed RT address and parity fail to have an odd parity sum.

See Appendix “F” for important information **IF** this bit is enabled (logic “1”) **AND** terminal is operating in RT Mode **AND** Interrupt Status Queue is enabled (i.e., bit 6 of Configuration Register #6 is logic “1”).

TIME TAG ROLLOVER (bit 6) : If set, enables an interrupt if the 16-bit Time Tag Register rolls over from FFFF to 0000.

See Appendix "F" for important information **IF** this bit is enabled (logic "1") **AND** terminal is operating in RT Mode **AND** Interrupt Status Queue is enabled (i.e., bit 6 of Configuration Register #6 is logic "1").

RT CIRCULAR BUFFER ROLLOVER (bit 5) : If this bit is set and the Enhanced Mini-ACE is in the Enhanced Memory Management RT mode (bit 1 of Configuration Register #2 is set to logic "1") and the "Interrupt at Rollover" bit is set in the Subaddress Control Word for the respective Tx/Rx/Bcst subaddress, an interrupt request will be issued when the respective data lookup address pointer crosses the lower boundary of its circular buffer, resulting in a rollover. This interrupt is applicable for both subaddress-specific circular buffers, as well as the global circular buffer.

If bit 11 of Configuration Register #2 (OVERWRITE INVALID DATA) is logic "0," the RT Subaddress Circular Buffer Rollover interrupt request will be issued immediately after the last word at the bottom boundary of the circular buffer in the shared RAM address space (address XXXX...1111) has been read or written.

However, if OVERWRITE INVALID DATA is logic "1," the interrupt request will occur at the end of a transmit message or a valid receive message in which the word at the bottom boundary of the circular buffer in the shared RAM address space has been read or written. For a receive message, an interrupt request will not be issued if bit 11 is set and there is an error in the message, even if the last word of the buffer was accessed during the message.

BC MSG/RT Subaddress CONTROL WORD EOM (bit 4) : For BC mode, if this bit is logic "1" and the EXPANDED BC CONTROL WORD bit (bit 12 of Configuration Register #4) is logic "1" and the EOM_INTERRUPT ENABLE bit (bit 4) of the respective BC Control Word is logic "1," an interrupt request will be issued at the end of the current message. For RT mode, if this bit is set and the Enhanced Mini-ACE is in the Enhanced Memory Management RT mode and the "Interrupt at EOM" bit is set in the Subaddress Control Word for the respective Tx/Rx/Bcst subaddress, an interrupt will occur at the end of the current message.

BC END OF FRAME (bit 3) : For the non-enhanced BC mode; it is not applicable for the Enhanced BC mode, if enabled, this bit enables an interrupt after an entire programmed BC message frame has been processed. That is, following the end of a message that resulted in the active area Message Count RAM location to have been incremented to FFFF (hex). Note that if BC STOP-ON-ERROR is enabled and a BC frame is aborted before the Message Count has incremented to FFFF (hex), the BC_EOM interrupt will not occur.

When in enhanced BC mode, with bit 1 of Configuration Register #7 (ENH BC WATCHDOG TIMER EN) set to logic "1," this bit enables an interrupt when frame timer decrements to zero.

FORMAT ERROR (bit 2) : If enabled, will result in an interrupt request for any of the following conditions:

Loop Test Failure: A loopback test is performed on every word transmitted by the Enhanced Mini-ACE BC or RT for each message. If the received version of one or more words is decoded as invalid and/or the received version of the last transmitted word does not match the transmitted version, the loopback test is considered to have failed.

Message Error: A Received Message contained a violation of the 1553 message validation criteria (encoding, parity, bit count, word count, etc.). For RT mode, this does not include an error in the received Command Word. If an invalid Command Word is detected, the entire message is ignored.

Response Timeout: In BC or Message Monitor modes, an RT has either not responded or has responded later than the programmed value of the BC No Response Timeout time. This time is programmable for values of Approximately 18.5, 22.5, 50.5, or 130μs by means of bits 10 and 9 of Configuration Register #5. In RT mode, a response timeout occurs if the Enhanced Mini-ACE is the receiving RT in an RT-to-RT transfer and the transmitting RT has not responded with its Status Word within the RT-to-RT No Response Timeout time. The RT-to-RT timeout time is programmable with the same choice of values as the BC No Response Timeout.

BC STATUS SET/RT MODE CODE/MT PATTERN TRIGGER (bit 1): For BC mode, this bit involves a message in which the RT Status Word received from a responding RT either contained an incorrect RT address field or one of the 8 non-RESERVED Status bits contained an unexpected bit value. The expected value for these 8 bits is normally zero (0), with one exception: If (the Enhanced Mini-ACE is in its non-ENHANCED mode (ENHANCED MODE ENABLED, bit 15 of Configuration Register #3 is logic "0") or BROADCAST MASK ENABLE/$\overline{\text{XOR}}$, bit 11 of Configuration Register #4 is logic "0") and if the Mask Broadcast bit of the message's BC Control Word is set, the expected value of the Broadcast Command Received bit becomes 1, rather than 0.

In RT mode, this interrupt can only occur in the ENHANCED mode (bit 15 of Configuration Register #3 is set to logic "1") and if Enhanced Mode Code Handling is enabled (bit 0 of Configuration Register #3 is set to logic "1"). If these two bits are set, mode code interrupts for individual broadcast-T/R bit-mode codes may be enabled by setting the appropriate bit(s) in address locations 0108-010F in shared RAM. Reception of an enabled mode code message will then cause a mode code interrupt to occur at the end of the message.

In the Word Monitor mode, a Pattern Trigger interrupt will occur in the ENHANCED mode (bit 15 of Configuration Register #3 is set to logic "1") following the reception of a valid Command Word that matches the bit pattern programmed in the Monitor Trigger Register.

END OF MESSAGE (bit 0): End of Message. If enabled, will result in an interrupt in BC, RT, and Selective Monitor modes at the completion of every message (regardless of validity).

4.8 Configuration Register #1

Table 40. Configuration Register #1 (Read/Write01H)				
BIT	**BC FUNCTION (Bits 11-0 Enhanced Mode Only)**	**RT WITHOUT ALTERNATE STATUS**	**RT WITH ALTERNATE STATUS (Enhanced Mode Only)**	**MONITOR FUNCTION (Enhanced Mode Only, bits 12-0)**
15(MSB)	RT/BC-MT* (Logic 0)	(Logic "1")	(Logic "1")	(Logic 0)
14	MT/BC-RT* (Logic 0)	(Logic 0)	(Logic 0)	(Logic "1")
13	CURRENT AREA B/A*	CURRENT AREA B/A*	CURRENT AREA B/A*	CURRENT AREA B/A*
12	MESSAGE STOP-ON-ERROR	MESSAGE MONITOR ENABLED (MMT)	MESSAGE MONITOR ENABLED	MESSAGE MONITOR ENABLED
11	FRAME-STOP-ON-ERROR	DYNAMIC BUS CONTROL ACCEPTANCE*	S10	TRIGGER WORD ENABLED
10	STATUS SET STOP-ON-MESSAGE	$\overline{\text{BUSY}}$	S09	START-ON-TRIGGER
9	STATUS SET STOP-ON-FRAME	$\overline{\text{SERVICE REQUEST}}$	S08	STOP-ON-TRIGGER
8	FRAME AUTO-REPEAT	$\overline{\text{SUBSYSTEM FLAG}}$	S07	NOT USED
7	EXTERNAL TRIGGER ENABLED	$\overline{\text{RTFLAG}}$ (ENHANCED MODE ONLY)	S06	EXTERNAL TRIGGER ENABLED
6	INTERNAL TRIGGER ENABLED	NOT USED	S05	NOT USED
5	INTERMESSAGE GAP TIMER ENABLED	NOT USED	S04	NOT USED
4	RETRY ENABLED	NOT USED	S03	NOT USED
3	DOUBLE/SINGLE* RETRY	NOT USED	S02	NOT USED
2	BC ENABLED (READ ONLY)	NOT USED	S01	MONITOR ENABLED (READ ONLY)
1	BC FRAME IN PROGRESS (READ ONLY)	NOT USED	S00	MONITOR TRIGGERED (READ ONLY)
0(LSB)	BC MESSAGE IN PROGRESS (READ ONLY)	RT MESSAGE IN PROGRESS (Enhanced mode only, read only)	RT MESSAGE IN PROGRESS (Read Only)	MONITOR ACTIVE (Read Only)

Notes

1. The combined RT/Message Monitor mode uses the RT WITHOUT ALTERNATE STATUS or the RT WITH ALTERNATE STATUS bit definitions not the MONITOR FUNCTION bit definitions.
2. In the alternate RT Status Word mode, bit 10 (Message Error) may also be set for an illegalized message (Broadcast-T/R* bitsubaddress-word count/mode code).
3. Refer to RT Status Word section in the RT operation chapter on the use of RT status word bits.

RT/BC-MT*, MT/BC-RT*, and MMT (bit 15,14) : Selects the Enhanced Mini-ACE's mode of operation as follows:

Table 41. Configuration Register #1. Mode Assignments

Configuration #1			Conflg #3	Mode
Bit 15	Bit 14	Bit 12	Bit 15	
0	0	X	0	Non-ENHANCED BC (See Note)
0	0	X	1	ENHANCED BC
0	1	0	X	Word Monitor
0	1	1	0	Word Monitor
0	1	1	1	Message Monitor
1	0	X	0	Non-ENHANCED RT
1	0	0	1	ENHANCED RT
1	0	1	1	Enhanced RT/Message Monitor
1	1	X	X	Idle

Notes

1. Following hardware reset ($\overline{\text{MSTCLR}}$ asserted) or software reset (by means of the Start/Reset Register), BC/RT/MT versions of the Enhanced Mini-ACE will initialize to (non-transmitting) BC mode, while RT only versions will initialize to Idle mode. In both cases, the values of bits 15 and 14 will initialize to logic "0."
2. Notes 2 thru 6 are only applicable to the BC/RT/MT versions of Enhanced Mini-ACE:
   If the Enhanced Mini-ACE is switched from RT to combined RT/Monitor mode in the middle of an RT message, the message will be completed.
3. If the Enhanced Mini-ACE is switched from combined RT/Monitor mode to RT mode in the middle of an RT message or Monitor message, the message will be completed.
4. If the Enhanced Mini-ACE is switched from either RT mode or Monitor mode to either BC mode or "Idle" mode in the middle of an RT message, the message will be aborted.
5. If the Enhanced Mini-ACE is switched from non-enhanced RT mode to "Idle" mode, there is no effect.
6. If the Enhanced Mini-ACE is switched from (enhanced or non-enhanced) BC mode to "Idle" mode in the middle of a message, the message will be aborted.

   It should be noted that ENHANCED MODE ENABLED, bit 15 of Configuration Register #3, must be set to logic "1," prior to activating the ENHANCED BC or RT modes, or the Message Monitor or RT/Message Monitor modes. In addition, the Enhanced Mini-ACE must be programmed for its ENHANCED mode PRIOR to setting bit 5 of Configuration Register #3 in order to activate RT with Alternate Status. In this instance, Configuration Register #3 must be written twice.

CURRENT AREA B/A* (bit 13): Selects Current Area Pointers. Note that if bit 13 is updated during the processing of a BC frame, or while an RT or Selective Message Monitor message is in progress, the value that will be returned to the host processor will continue to be the old value until the BC frame or RT/MT message in progress has been completed. After the current BC frame or RT/MT message has been completed, bit 13 as read by the host CPU will toggle to its new value. If the Enhanced Mini-ACE is already on-line in the Word Monitor mode, toggling this bit will have no effect. It should be noted that Active Area selection is NOT related to the selection or operation of the bus channels on a dual redundant 1553 bus (Bus A vs. Bus B). For BC mode, bits 12 through 0 are defined **as follows:**

MESSAGE STOP-ON-ERROR (bit 12): If this bit is set, the Enhanced Mini-ACE will abort the processing of messages following the end of the current message if it encounters either a word error (gap, sync, encoding, or parity error), message format error (incorrect RT Address in Status Word, high or low word count), a response timeout condition, or a loop test failure.

If retries are enabled for a particular message, the retry will be attempted even if MESSAGE STOP-ON-ERROR is programmed to logic "1." It should be noted that the processing of subsequent BC messages in the frame would continue if a failed message were successfully retried.

For BC mode, bits 11 through 0 are defined in the ENHANCED BC Mode (bit 15 of Configuration Register #3 set to logic "1") as follows:

FRAME STOP-ON-ERROR (bit 11) : This bit is only applicable in the ENHANCED mode (ENHANCED MODE ENABLE, bit 15 of Configuration Register #3, set to logic "1"). This mode is invoked if bit 8 of this register, FRAME AUTO REPEAT, is programmed to logic "1." If FRAME STOP-ON-ERROR is set, the Enhanced Mini-ACE will abort the processing of messages following the end of the current BC frame if it encounters either a word error (gap, sync, encoding, or parity error) or message format error (incorrect RT Address in Status Word, high or low word count), a response timeout condition, or a loop-test failure.

If retries are enabled for a particular message, the retry will be attempted even if FRAME STOP-ON-ERROR is programmed to logic "1." It should be noted that the processing of subsequent BC frames would continue if a failed message were successfully retried.

STATUS SET STOP-ON-MESSAGE (bit 10) : This bit is only applicable in the ENHANCED mode (ENHANCED MODE ENABLE, bit 15 of Configuration Register #3, set to logic "1"). If this bit is set, the Enhanced Mini-ACE will abort the processing of messages following the end of the current message if it encounters a "Status Set" condition in the message. A "Status Set" condition is defined as an unexpected value for one of the 8 non-reserved Status Word bits.

If bit 12 of Configuration Register #4, EXPANDED BC CONTROL WORD, is programmed to logic "0," Status Set encompasses all 8 of the non-reserved Status Word bits. The expected value for the 8 non-reserved Status Word bits is normally zero (0), with one exception: if bit 11 of Configuration Register #4, BROADCAST MASK ENA/XOR*, is logic "0" and the MASK BROADCAST bit of the message's BC Control Word is logic "1," the expected value of the Broadcast Command Received bit becomes 1, rather than 0. If BROADCAST MASK ENA/XOR* is programmed to logic "1," the MASK BROADCAST bit of the BC Control Word is used as a mask bit, rather than performing an "XOR" operation with the Broadcast Received Status Word bit. In this instance, a Status Set condition arising from the Broadcast Command Received RT Status bit occurs when the MASK BROADCAST BC Control Word bit is logic "0" and the Broadcast Command Received RT Status Word bit is logic "1."

If EXPANDED BC CONTROL WORD is programmed to logic "1," the RT Status Word is masked by bits 14 through 9 of the BC Control Word. In this instance, the corresponding BC Control Word bit must be programmed to logic "0" in order for a "Status Set" condition to arise from the corresponding bit in the received RT Status Word. In this instance, Status Set conditions will not occur from Status Mask bits in the BC Control Word that are programmed to logic "1."

If a "STATUS SET" retry is enabled for a particular message, the retry will be attempted, even if STATUS SET STOP-ON-MESSAGE is programmed to logic "1." It should be noted that the processing of subsequent BC messages will continue if a message containing a STATUS SET condition is retried and the STATUS SET condition does not occur on the retry.

STATUS SET STOP-ON-FRAME (bit 9) : This bit is only applicable in the ENHANCED mode (ENHANCED MODE ENABLE, bit 15 of Configuration Register #3, set to logic "1"). If this bit is set, the Enhanced Mini-ACE will abort the processing of the current BC frame following the end of the frame if it encounters a "Status Set" condition in one or more messages in the frame. A "Status Set" condition is defined as described in the preceding paragraph.

If a "STATUS SET" retry is enabled for a particular message, the retry will be attempted, even if STATUS SET STOP-ON-MESSAGE is programmed to logic "1." It should be noted that the processing of subsequent BC frames will continue if a message containing a STATUS SET condition is retried and the STATUS SET condition does not occur on the retry.

FRAME AUTO-REPEAT (bit 8) : This bit is applicable only in the ENHANCED mode (ENHANCED MODE ENABLE, bit 15 of Configuration Register #3, set to logic "1"). If this bit is programmed to logic "0," the Enhanced Mini-ACE will process its programmed BC frame one time and then halt. In this instance, the BC Stack Pointer and BC Message Count are maintained at shared RAM locations 0100 and 0101, respectively, for Area A and locations 0104 and 0105, respectively, for Area B.

If FRAME AUTO-REPEAT is programmed to logic "1," the Enhanced Mini-ACE's BC frame will repeat indefinitely until either: a RESET, STOP-ON-MESSAGE, or STOP-ON-FRAME software command is invoked via the Start/Reset Register; or an enabled (MESSAGE or FRAME) STOP-ON-ERROR or STOP-ON-STATUS SET condition has occurred. In the Frame Auto-Repeat mode, just as in the "single frame" mode, the current values of the BC Stack Pointer and BC Message Count are maintained at shared RAM locations 0100 and 0101, respectively, for Area A and locations 0104 and 0105, respectively, for Area B. In addition, for the AUTO-REPEAT mode, the "initial" values which are, the values of the Stack Pointer and Message Count at the start of each frame, must also be loaded in the shared RAM to support the frame repetition: addresses 102 and 103, respectively for area A and locations 106 and 107, respectively for area B.

If the INTERNAL TRIGGER ENABLE bit of this register is set to logic "1," the BC frame will repeat with a fixed frame time as specified in the BC Frame Time Register (100 μs to 6.55 seconds). Alternatively, if the EXTERNAL TRIGGER ENABLE bit of this register is set to logic "1," each repetitive BC frame may be initiated by means of an external pulse delivered to the Enhanced Mini-ACE's EXT_TRIG input. If both the INTERNAL TRIGGER ENABLE and the EXTERNAL TRIGGER ENABLE bits are set, the initial frame will be initiated by the EXT_TRIG input and all subsequent frames will be initiated by the internal frame timer.

EXTERNAL TRIGGER ENABLED (bit 7) : This bit is applicable only in the ENHANCED mode (ENHANCED MODE ENABLE, bit 15 of Configuration Register #3, set to logic "1"). If this bit is logic "0," the Enhanced Mini-ACE BC may only be started by means of a "START" software command to the Start/Reset Register. If this bit is set to logic "1," the Enhanced Mini-ACE BC frame may be initiated by an external signal delivered to the EXT_TRIG input as well as by means of a software command via the Start/Reset Register. If the FRAME AUTO-REPEAT and INTERNAL TRIGGER ENABLE, and EXTERNAL TRIGGER ENABLE bits are set, the initial frame will be initiated by the EXT_TRIG input and all subsequent frames will be initiated by the internal frame timer.

INTERNAL TRIGGER ENABLED (bit 6) : This bit is applicable only in the ENHANCED mode (ENHANCED MODE ENABLE, bit 15 of Configuration Register #3, set to logic "1"). This bit is used in conjunction with the FRAME AUTO-REPEAT bit to enable automatic frame repetition. If FRAME AUTO-REPEAT is set to logic "1" and INTERNAL TRIGGER ENABLED is set to logic "0," the Enhanced Mini-ACE BC will halt the processing of messages after a single frame; in this scenario, a repetitive frame may still be re-triggered by means of an external signal delivered to EXT_TRIG, provided that EXTERNAL TRIGGER ENABLE has been programmed to logic "1." If INTERNAL TRIGGER ENABLE is set to logic "1," the BC frame will repeat with a fixed frame time as specified in the BC Frame Time Register (100 μs to 6.55 seconds). If both the INTERNAL TRIGGER ENABLE and the EXTERNAL TRIGGER ENABLE bits are set, the initial frame will be initiated by the EXT_TRIG input and the internal frame timer will initiate all subsequent frames.

MESSAGE GAP TIMER ENABLED (bit 5) : This bit is applicable only in the ENHANCED mode (ENHANCED MODE ENABLE, bit 15 of Configuration Register #3, set to logic "1"). If this bit is programmed to logic "0," the Enhanced Mini-ACE's intermessage gap will assume a fixed minimum value of approximately 8 to 11 μs. If this bit is programmed to logic "1," the message gap for each message will be specified by means of the third word in the respective BC message block descriptor. This time value, which specifies the time from the start of the current message to the time of the start of the subsequent message, is programmable from the minimum value (approximately 8 to 11 μs) up to 65.535 ms, in steps of 1 μs. If the programmed value of the message gap time is less than the time required to process the current message, the current message will be processed to completion before the subsequent message is started. In this case, the gap time between messages will assume the minimum value of approximately 8 to 11 μs.

RETRY ENABLED (bit 4) : This bit is applicable only in the ENHANCED mode (ENHANCED MODE ENABLE, bit 15 of Configuration Register #3, set to logic "1"). If this bit is programmed to logic "0," BC retries are disabled for all messages. If this bit is programmed to logic "1," automatic retry may be enabled on a message-by-message basis by setting bit 8 of the BC Control Word to logic "1" for all messages to be retried.

DOUBLE/SINGLE* RETRY (bit 3) : This bit is applicable only in the ENHANCED mode (ENHANCED MODE ENABLE, bit Register #3, set to logic "1"). If retries are enabled (RETRY ENABLED, bit 4 of Configuration Register #1, set to logic "1"), this bit is used to program the number of retries that will be performed (when enabled). A logic "0" will cause the Enhanced Mini-ACE to perform a single retry, while a logic "1" will cause the Enhanced Mini-ACE to perform up to two retries.

BC ENABLED (READ ONLY) (bit 2) : This bit is applicable only in the ENHANCED mode (ENHANCED MODE ENABLE, bit 15 of Configuration Register #3, set to logic "1"). This bit will return a value of logic "1" after the Enhanced Mini-ACE BC has been started by means of either the Start/Reset Register or a signal delivered to EXT_TRIG. This bit will continue to return a logic "1" until either: a single message frame completes, if not in FRAME AUTO-REPEAT mode; a RESET, STOP-ON-MESSAGE, or STOP-ON-FRAME software command is invoked via the Start/Reset Register; or an enabled (MESSAGE or FRAME) STOP-ON-ERROR or STOP-ON-STATUS SET condition occurs.

BC FRAME-IN-PROGRESS (READ ONLY) (bit 1) : This bit is applicable only in the ENHANCED mode (ENHANCED MODE ENABLE, bit 15 of Configuration Register #3, set to logic "1"). This bit will return a value of logic "1" between the time of the BC Start-of-Message (SOM) sequence for the first message of a programmed BC frame, until the completion of the BC End-of-Message (EOM) sequence for the last programmed message of the frame. In the FRAME AUTO-REPEAT mode, BC FRAME-IN-PROGRESS will automatically return to a value of logic "1" just prior to the start of the first SOM sequence for the new frame.

BC MESSAGE-IN-PROGRESS (READ ONLY) (bit 0) : This bit is applicable only in the ENHANCED mode (ENHANCED MODE ENABLE, bit 15 of Configuration Register #3, set to logic "1"). This bit will return a value of logic "1" during the processing of all BC messages. This bit will transition from logic "0" to logic "1" just prior to each BC Start-of-Message (SOM) sequence and return to logic "0" following the completion of each BC End-of-Message (EOM) sequence.

For RT mode WITHOUT ALTERNATE STATUS WORD ENABLE, i.e., bit 5 of Configuration Register #3, set to logic "0," the Enhanced Mini-ACE's RT Status Word will comply with MIL-STD-1553B. In this mode, bits 11 through 7 and bit 0 are defined as follows:

Accept Dynamic Bus Control* (bit 11) : If this bit is logic "0," it enables the Enhanced Mini-ACE RT to respond with the DYNAMIC BUS CONTROL ACCEPTANCE bit set in its RT Status Word in response to a Dynamic Bus Control mode code command (but not in response to other commands). If this register bit is logic "1," the DYNAMIC BUS CONTROL ACCEPTANCE Status Word bit will always be low.

Busy* (bit 10) : If this bit is logic "0," the BUSY bit in the RT Status Word will be set (logic "1"). The Enhanced Mini-ACE will not transmit any Data Words in response to a transmit command if its BUSY bit is set. If the BUSY Status Word bit is set and BUSY RECEIVE TRANSFER DISABLE, bit 3 of Configuration Register #3, is programmed to logic "0," the Enhanced Mini-ACE will store received Data Words in the shared RAM. However, if the BUSY bit in the RT Status Word is set and BUSY RECEIVE TRANSFER DISABLE has been programmed to logic "1," received Data Words will not be transferred to the Enhanced Mini-ACE shared RAM.

If BUSY* is logic "1," the BUSY bit in the transmitted RT Status Word will be logic "0," unless: ENHANCED MODE is enabled (bit 15 of Configuration Register #3 is logic "1") and BUSY LOOKUP TABLE ENABLED (bit 13 of Configuration Register #2 is logic "1") and the bit corresponding to the Broadcast-T/R* bit-Subaddress fields of the current Command Word has been programmed to logic "1" in the Busy Lookup Table (address locations 0240-0247 in shared RAM).

Service Request* (bit 9) : If this bit is logic "0," the SERVICE REQUEST bit in the RT Status Word will be set. If the CLEAR SERVICE REQUEST BIT (bit 2) of Configuration Register #2 is set, the value of SERVICE REQUEST* will be automatically toggled from logic 0 to Logic “1” after the Enhanced Mini-ACE has responded to a Transmit Vector Word mode command.

Subsystem Flag* (bit 8) : If this bit is logic "0," the SUBSYSTEM FLAG bit in the RT Status Word will be set. The Subsystem Flag Status Word bit will also be set whenever the SSFLAG* input Signal to the Enhanced Mini-ACE is asserted low. It should be noted that the sense of the SSFLAG* input pin does not effect the status of the SUBSYSTEM FLAG* register bit.

RT Flag* (bit 7) : This bit is only applicable in the ENHANCED mode (ENHANCED MODE ENABLE, bit 15 of Configuration Register #3, set to logic "1"). If programmed to logic "0," it causes the Terminal Flag bit in the Enhanced Mini-ACE's RT Status Word to be set. The Terminal Flag bit transmitted in the RT Status Word will also become set if RTFAIL-RTFLAG AUTO WRAP ENABLE, bit 2 of Configuration Register #3, is programmed to logic "1" and either a transmitter timeout (668 µs) condition had occurred or the Enhanced Mini-ACE RT had failed its loopback test on the previous non-broadcast message. The loopback test verifies validity (sync, encoding, bit count, parity) for the received version of every word transmitted by the Enhanced Mini-ACE RT and verifies that the received version of the last transmitted word matches the transmitted version.

RT Message-in-progress (Read Only) (bit 0) : This bit is only applicable in the ENHANCED mode (ENHANCED MODE ENABLE, bit 15 of Configuration Register #3, set to logic "1"). If this bit returns a logic "1," it indicates that the Enhanced Mini-ACE RT is currently processing a message. The RT MESSAGE IN PROGRESS bit is asserted to logic "1" just prior to the RT Start-of-Message (SOM) sequence, and returns to logic "0" just following the completion of the RT End-of-Message (EOM) sequence.

For RT mode WITH ALTERNATE STATUS WORD ENABLE, bit 5 of Configuration Register #3, set to logic "1," all 11 bits of the Enhanced Mini-ACE's RT Status Word are programmable by the host processor. The alternate Status Word may only be used in the ENHANCED mode (ENHANCED MODE ENABLE, bit 15 of Configuration Register #3, set to logic "1"). In this mode, bits 11 through 0 are defined as follows:

S10 through S0 (bit 11-bit 1) : For 1553A and McAir applications, direct software control over the eleven (11) lower RT Status Word bits is allowed. S10 controls the bit in bit time 9 (the first bit after the RT Address field)...S0 controls the bit in bit time 19 (LSB). Note that the logic sense of S10-S0 is the same (no inversion) as that of the respective transmitted RT Status Word bits. It should be noted that the Message Error Status Word bit, controlled by S10, will also be set if a particular command (broadcast-T/R* bit-subaddress-word count/mode code) has been illegalized.

RT Message-in-progress (Read Only) (bit 0) : If this bit returns a logic "1," it indicates that the Enhanced Mini-ACE RT is currently processing a message. The RT-MESSAGE-IN-PROGRESS bit is asserted to logic "1" just prior to the RT Start-of-Message (SOM) sequence, and returns to logic "0" following the completion of the RT End-of-Message (EOM) sequence.

For Monitor (MT) mode with ENHANCED MODE ENABLE, bit 15 of Configuration Register #3, set to logic "1," bits 11 through 0 are defined as indicated below. Note these bits have no effect in Monitor mode if ENHANCED MODE ENABLE is programmed to logic "0."

Trigger Enabled (bit 11) : This bit must be set to logic "1" in order to activate the MT trigger logic. The Monitor Trigger capability is applicable only for the Word Monitor mode. It is not applicable for the Message Monitor mode. The trigger event is either a pattern match of a valid, received 1553 Command Word with the contents of the Monitor Trigger Register or an external pulse presented to the Enhanced Mini-ACE's EXT_TRIG input. EXTERNAL TRIGGER ENABLED must also be programmed to logic "1" to allow use of the EXT_TRIG input signal. The MT trigger may be used to start monitoring, stop monitoring, set a register bit, and/or result in an interrupt request.

Start-on-trigger (bit 10) : If this bit is set, the Enhanced Mini-ACE will start storing words following reception of a valid 1553 Command (or Status) Word that matches the word programmed in the Monitor Trigger Register. The word that resulted in the trigger condition will be the first word stored.

Stop-on-trigger (bit 9) : If this bit is set, the Enhanced Mini-ACE will stop storing words following reception of a valid 1553 Command Word that matches the word programmed in the Monitor Trigger Register. The Command Word that resulted in the trigger condition will be the last word stored.

External Trigger Enable (bit 7) : If this bit is set to logic "1," it allows an external signal delivered to the Enhanced Mini-ACE's EXT_TRIG input pin to serve as a monitor trigger.

Monitor Enabled (Read Only) (bit 2) : This bit will return a value of logic "1" whenever the Enhanced Mini-ACE's monitor is in its on-line state. The Enhanced Mini-ACE's MT is considered to be "on-line" after it has been started by a MT Start Command (writing a logic "1" to bit 1 of the Start/Reset Register), even if a trigger condition (if enabled) has not yet occurred.

Monitor Triggered (Read Only) (bit 1) : This bit is applicable for the Word Monitor mode only. It is not applicable (will always return logic "0") in the Message Monitor mode. This bit reverts to logic "0" following a Word Monitor START command (writing logic "1" to bit 1 of the Start/Reset Register). This bit gets set to logic "1" after an enabled trigger condition has occurred. The two trigger conditions, which are enabled by means of bits 11 and 7 of Configuration Register #1, are reception of a valid Command Word to the Monitor Trigger Register (bit 11) or receipt of an EXT_TRIG signal, if enabled. Once asserted, MONITOR TRIGGERED will remain logic "1" until either the Enhanced Mini-ACE is reset or the Monitor is stopped. If the Monitor is stopped by a trigger condition (enabled by bit 9 of Configuration Register #9 set to logic "1"), MONITOR TRIGGERED will remain logic "1" until the Monitor is restarted.

Monitor Active (Read Only) (bit 0) : In the Word Monitor mode, this bit will return a logic "1" after the Word Monitor has been started. That is, after the Word Monitor has been started by a MT Start Command (writing a logic "1" to bit 1 of the Start/Reset Register), even if a trigger condition (if enabled) has not yet occurred. In the Message Monitor mode, MONITOR ACTIVE will return logic "1" only when the Message Monitor is currently storing the words of a selected message. MONITOR ACTIVE will return logic "0" when the monitor is in its off-line state.

4.9 Configuration Register #2

(Register Address 0010; READ/WRITE)

Table 42. Configuration Register #2 (Read/Write 02H)

BIT	DESCRIPTION
15(MSB)	ENHANCED INTERRUPTS
14	RAM PARITY ENABLE
13	BUSY LOOK UP TABLE ENABLE
12	RX SA DOUBLE BUFFER ENABLE
11	OVERWRITE INVALID DATA
10	256-WORD BOUNDR DISBL
9	TIME TAG RESOLUTION 2 (TTR2)
8	TIME TAG RESOLUTION 1 (TTR1)
7	TIME TAG RESOLUTION 0 (TTR0)
6	CLEAR TIME TAG ON SYNCHRONIZE *
5	LOAD/TRANSMIT TIME TAG ON SYNCHRONIZE
4	INTERRUPT STATUS AUTO CLEAR
3	LEVEL/PULSE INTERRUPT REQUEST
2	CLEAR SERVICE REQUEST *
1	ENHANCED RT MEMORY MANAGEMENT
0(LSB)	SEPARATE BROADCAST DATA

* Note: See Appendix “F” for important information IF any of these bits are enabled (Logic “1”) AND terminal is operating in RT Mode AND Interrupt Status Queue is enabled (i.e., bit 6 of Configuration Register #6 is Logic “1”) AND bits 6, 7 or 14 (Time Tag Rollover, RT Address Parity Error, or RAM Parity Error respectively) of Interrupt Mask Register #1 are enabled (Logic “1”).

ENHANCED INTERRUPTS ENABLE (bit 15) : This bit is applicable only in the ENHANCED mode (ENHANCED MODE ENABLE, bit 15 of Configuration Register #3, set to logic "1"). This bit controls the operation of the interrupt mask registers and interrupts status registers. If this bit is programmed to logic "0," the only interrupt conditions that may be enabled are those that are enabled by bits 7-0 in Interrupt Mask Register #1. In addition, if ENHANCED INTERRUPTS ENABLED is logic "0," the respective bit(s) in the Interrupt Status Register will only become set if the corresponding bit(s) is (are) set in the Interrupt Mask Register.

If this bit is set to logic "1" (enabled), all 15 possible interrupt conditions of Interrupt Mask (and Status) Register #1, along with all 14 interrupt conditions of Interrupt Mask (and Status) Register #2 may be enabled by means of bits 14-0 of the Interrupt Mask Register. In addition, if ENHANCED INTERRUPT ENABLE is logic "1," the various bits in the Interrupt Status Register may become set regardless of the value of the corresponding Interrupt Mask Register bits.

RAM PARITY ENABLE (bit 14) : This bit is applicable only in the ENHANCED mode (ENHANCED MODE ENABLE, bit 15 of Configuration Register #3, set to logic "1"). RAM PARITY ENABLE, when set to logic "1," enables parity checking for 17-bit buffered RAM. This entails internal hardware generation of a 17th bit (parity bit) for ALL (processor and 1553) RAM write accesses and parity checking for ALL RAM read accesses. If the parity check fails for any read access, an interrupt request may be issued (if enabled) and a bit set in the Interrupt Status Register.

IMPORTANT NOTE:

For the (4K RAM) versions of Enhanced Mini-ACE, there is **no** 17-bit buffered RAM. For these products, RAM parity is not implemented. Therefore, RAM PARITY ENABLE **must** be set to logic "0" for these products.

The RAM parity feature may be utilized with (64K RAM) version of the Enhanced Mini-ACE as these contains an internal 64K x 17 RAM which supports RAM parity generation and checking.

BUSY BIT LOOKUP TABLE ENABLE (bit 13) : This bit is applicable only in the ENHANCED RT mode (ENHANCED MODE ENABLE, bit 15 of Configuration Register #3, set to logic "1"). This bit allows the host processor to optionally set the busy bit in the RT status response, based on broadcast, and the T/R*, and subaddress fields of received Command Words. Setting this bit to logic "1" enables a lookup table in a fixed area of the RAM (address range 0240-0247). Placing a logic "1" in the proper bit location in the Busy table will cause the Enhanced Mini-ACE RT to respond to the selected command with the BUSY bit set. Programming BUSY BIT LOOKUP TABLE ENABLE to logic "0" disables the busy bit lookup table and frees up the fixed area of RAM.

RECEIVE SUDADDRESS DOUBLE BUFFERING ENABLE (bit 12) : This bit is applicable only in the ENHANCED mode (ENHANCED MODE ENABLE, bit 15 of Configuration Register #3, set to logic "1"). The receive subaddress double buffering feature supports double buffering either globally, or on a subaddress basis for individual receive (and broadcast receive) subaddresses. If RECEIVE Subaddress DOUBLE BUFFERING ENABLE is programmed to a value of logic "0," the subaddress double buffering feature is disabled for all receive and broadcast receive subaddresses.

If RECEIVE SUBADDRESS DOUBLE BUFFERING ENABLE is programmed to a value of logic "1" and ENHANCED RT MEMORY MANAGEMENT, bit 1 of this register, is programmed to logic "0," the subaddress double buffering feature will be invoked for all receive (and broadcast receive) subaddresses. If both ENHANCED RT MEMORY MANAGEMENT and RECEIVE Subaddress DOUBLE BUFFERING ENABLE are programmed to logic "1," the subaddress double buffering feature may be invoked for individual receive (and broadcast receive) subaddresses by setting bit 15 of the respective Subaddress Control Word(s) to logic "1" and programming the appropriate "memory management" bits (MM2, MM1, MM0) to values of 000.

OVERWRITE INVALID DATA (bit 11) : This bit affects the operation of the RT subaddress circular buffer memory management mode. If this bit is logic 0, the Enhanced Mini-ACE will update the value of the Lookup Table pointer address for the respective Tx/Rx-Bcst-subaddress following transmit messages as well as following both valid and invalid receive messages. In addition, if the bit is logic 0, an interrupt request for a subaddress or global circular buffer rollover condition (if enabled) will be issued immediately after the word at the lower address boundary of the respective circular buffer has been accessed.

If OVERWRITE INVALID DATA is Logic “1,” the Lookup Table address pointer will only be updated following a transmit message or following a valid receive or broadcast message to the respective Rx/Bcst subaddress. If the bit is Logic “1,” the Lookup Table pointer will not be updated following an invalid receive or broadcast message. In addition, if the bit is Logic “1,” an interrupt request for a circular buffer rollover condition (if enabled) will only occur following the end of a transmit message during which the last location in the circular buffer has been read or following the end of a valid receive or Broadcast message in which the last location in the circular buffer has been written to.

256-WORD BOUNDARY DISABLE (bit 10) : This bit controls the Enhanced Mini-ACE's memory management scheme for BC message blocks and for RT data blocks for both the default (global single message) mode as well as for any individual subaddresses in the ENHANCED mode for which the "single message" or "double buffered" options are selected. If this bit is logic "0," the rollover at 256-word boundaries is enabled. That is, when the 1553 memory management logic is processing a message, its memory address will roll over from XXFF (hex) to XX00, rather than increment to (XX+1)00. If this bit is logic "1," the memory management logic will enable 256-Word boundaries to be crossed for BC Message Blocks as well as for RT Data Blocks in both the Default (bit 1 of this register = 0) and Enhanced Memory Management/Single Buffer modes. In this instance, the address will increment from XXFF to (XX+1)00, when a 256-word boundary is encountered in the shared RAM address space. It should be noted that 256-WORD BOUNDARY DISABLE has no effect on the BC or RT Command Stack. That is, for the stack area of RAM in both BC and RT modes, the rollover at 256-(or 512-, 1024-, 2048-) word boundaries is always enforced.

IMPORTANT NOTE:

For RT mode, if 256-WORD BOUNDARY DISABLE is “0”, then subaddress circular buffering will operate in accordance with the programming of the respective subaddress control word. This includes the programmed size of the respective circular buffers. However, If 256-WORD BOUNDARY DISABLE is programmed to logic "1" in RT mode, the size for all subaddress circular buffers becomes 65,536 words, regardless of the programming of the respective Subaddress Control Word bits. The operation of global circular buffering is not affected by the programming of 256-WORD BOUNDARY DISABLE.

It is therefore recommended that 256-WORD BOUNDARY DISABLE be programmed to logic “1” for BC mode, and to logic “0” for RT mode.

TIME TAG RESOLUTION 2,1,0 (bit 9,8,7) : These bits allow the resolution of the time tag register to be selected by means of software control. The choices are 64 µs (default), 32 µs, 16 µs, 8 µs, 4 µs, and 2 µs/LSB. There is also a test mode for the Time Tag register. It is also possible for the time tag counter to be clocked from an external source (consult factory). Time tag resolution is programmed as described in Table 43.

Table 43. Time Tag Resolution			
BIT 9 TTR2	**BIT 8 TTR1**	**BIT 7 TTR0**	**TIME TAG RESOLUTION**
0	0	0	64 µs
0	0	1	32 µs
0	1	0	16 µs
0	1	1	8 µs
1	0	0	4 µs
1	0	1	2 µs
1	1	0	TEST MODE (NOTE 1)
1	1	1	EXTERNAL CLOCK (NOTE 2)

Notes

1. In the Time Tag TEST MODE, the Time Tag Register only increments when the CPU writes a logic "1" to bit 4 of the Start/Reset Register (TIME TAG TEST CLOCK).
2. The time tag external clock feature “TAG_CLK” input is not included in all Enhanced Mini-Ace series products. Certain Enhanced Mini-ACE based products include this input as a standard feature.

CLEAR TIME TAG ON SYNCHRONIZE (bit 6) : If this bit is set, reception of a Synchronize (without data) mode command, in RT mode, will cause the value of the internal Time Tag Register to clear to 0000.

See Appendix “F” for important information **IF** this bit is enabled (Logic “1”) **AND** terminal is operating in RT Mode **AND** Interrupt Status Queue is enabled (i.e., bit 6 of Configuration Register #6 is Logic “1”) **AND** bits 6, 7 or 14 (Time Tag Rollover, RT Address Parity Error, or RAM Parity Error respectively) of Interrupt Mask Register #1 are enabled (Logic “1”).

LOAD/TRANSMIT TIME TAG ON SYNCHRONIZE (bit 5) : In RT mode, if this bit is set, reception of a Synchronize (with data) mode command will cause the Data Word from the Synchronize message to be loaded into the Time Tag Register.

In BC mode, if this bit is set, the Enhanced Mini-ACE BC will be enabled to transmit the value of its Time Tag Register as the data word for a Synchronize (with data) mode code. When the ENHANCED TIME TAG SYNCHRONIZE (bit 2 of Configuration Register #7) is programmed to logic “1,” the transmitted data word will contain current 16-bit Time Tag value.

INTERRUPT STATUS AUTO CLEAR (bit 4) : If this bit is logic "1," the value of Interrupt Status Registers #1 and #2 will clear to 0000 after the respective register has been read by the host processor. Note that there are bits set in both interrupt status registers; it will be necessary to read both interrupt status registers in order to clear both of them.

Also, if both the INTERRUPT STATUS AUTO CLEAR and LEVEL/PULSE Interrupt Request (bit 3) are logic "1," the Enhanced Mini-ACE's Interrupt Request output INT* will be cleared (high) after all active Interrupt Status Registers have been read.

LEVEL/PULSE* INTERRUPT REQUEST (bit 3) : If this bit is logic "0," the Interrupt Request output, INT*, will be a negative pulse of approximately 500 ns width. If this register bit is logic "1," an interrupt will be requested by asserting INT* as a low level. If the level option is selected, INT* will be reset high after the Interrupt Status Register(s) has been read (provided that the INTERRUPT STATUS AUTO CLEAR [bit 4] is set), or when a "1" is written to the INTERRUPT RESET bit (bit 2) of the Start/Reset Register.

CLEAR SERVICE REQUEST (bit 2): If this bit is logic "0," the Service Request RT Status word bit may be controlled only by the host processor software. If the bit is logic "1," the Service Request bit may still be set and cleared under software (register) control. In addition, the SERVICE REQUEST* Configuration Register (#1) bit will automatically clear (go to Logic "1") after the Enhanced Mini-ACE RT has responded to a Transmit Vector Word mode code command. That is, if the CLEAR SERVICE REQUEST bit is set to 1 while SERVICE REQUEST* is set to 0, the Enhanced Mini-ACE RT will respond with the Service Request Status bit set for all commands until the RT responds to a Transmit Vector Word command. In this instance, the ACE will respond with the Service Request still set in the Status Word for this message. Following this message, SERVICE REQUEST* in the Configuration Register automatically clears to a logic "1." It stays logic "1" (cleared) for subsequent messages until it is reasserted to a logic "0" by the host processor.

See **Appendix "F"** for important information **IF** this bit is enabled (Logic "1") **AND** terminal is operating in RT Mode **AND** Interrupt Status Queue is enabled (i.e., bit 6 of Configuration Register #6 is Logic "1") **AND** bits 6, 7 or 14 (Time Tag Rollover, RT Address Parity Error, or RAM Parity Error respectively) of Interrupt Mask Register #1 are enabled (Logic "1").

ENHANCED RT MEMORY MANAGEMENT (bit 1) : If this bit is logic "0," the Enhanced Mini-ACE RT memory management defaults to either a global single Data Word buffer or double Data Word buffer for each transmit, receive, and (optionally) broadcast subaddress: single message, for all transmit subaddresses; single message, for all receive (and broadcast receive) subaddresses if RX Subaddress DOUBLE BUFFER ENABLE (bit 12 of this register) is logic programmed to "0."

If ENHANCED MODE (bit 15 of Configuration Register #3 is logic "1") and RX Subaddress DOUBLE BUFFER ENABLE are logic "1," double buffering is provided for all receive/broadcast subaddresses. In the single message mode, each data block is repeatedly overread or overwritten. If ENHANCED RT MEMORY MANAGEMENT is logic "1," the Enhanced Mini-ACE RT memory management capability is expanded to allow for either the "single-buffer" mode, the "double buffer" (redundant mailbox) mode, or for a variable-sized circular buffer (128 to 8192 words) to be programmed on an individual basis for each transmit, receive and broadcast subaddress. Note that subaddress double buffering is applicable for receive (and broadcast) subaddresses, but not for transmit subaddresses.

If ENHANCED RT MEMORY MANAGEMENT and GLOBAL CIRCULAR BUFFER, bit 12 of Configuration Register #6, are both logic “1,” this enables the RT global circular buffer to be specified for individual Rx(/Bcst) and/or broadcast subaddresses. This may be done by means of the individual subaddress control words.

SEPARATE BROADCAST DATA (bit 0) : If this bit is logic "0," the data pointers for both broadcast as well as non-broadcast receive messages are stored in a common portion (the "receive" portion) of the RT Lookup Table. If this bit is logic "1," broadcast data is separated from non-broadcast receive data by means of separate areas of the RT Lookup Tables provided for broadcast messages.

4.10 Start/Reset Register

(Register Address 0011; WRITE ONLY)

The Start/Reset Register is a write only register. The protocol and RAM built-in self-test specific bits in this register should only be written to one at a time. It provides command functions for resetting the entire ACE terminal, for initiating BC or Monitor operation, for resetting the Interrupt Status Register and Interrupt Request Output, for resetting the value of the Time Tag Register, and for initiating the protocol and RAM built-in self-tests. It also contains bits to facilitate testing of the Time Tag Register and to stop the ACE BC at the end of the current message or the current frame.

Table 44. Start/Reset Register (Write 03H)

BIT	DESCRIPTION
15(MSB)	RESERVED
14	RESERVED
13	RESERVED
12	RESERVED
11	CLEAR RT HALT
10	CLEAR SELF-TEST REGISTER
9	INITIATE RAM SELF-TEST
8	RESERVED
7	INITIATE PROTOCOL SELF-TEST
6	BC/MT STOP-ON-MESSAGE
5	BC STOP-ON-FRAME
4	TIME TAG TEST CLOCK
3	TIME TAG RESET
2	INTERRUPT RESET
1	BC/MT START
0(LSB)	RESET

CLEAR RT HALT (bit 11): If bit 4 of Configuration Register #7, RT HALT ENABLE, has been programmed to logic "1" and the Enhanced Mini-ACE RT receives an Initiate self-test mode code command, the RT will go to an offline state; i.e., it will not receive or respond to messages from the 1553 bus. With the BU-61743/5 (RT-only) version, the Enhanced Mini-ACE's "offline RT" state is, in effect, an "Idle" mode, with bits 15 and 14 of Configuration Register #1 both assuming values of "0" (in RT mode, bit 15 is "1," while bit 14 is "0"). With the BU-61843/5 and BU-61864/5 (BC/RT/MT) versions, the Enhanced Mini-ACE's "offline RT" state is, inactive BC mode, with bits 15 and 14 of Configuration Register #1 both assuming values of "0."

It is then up to the host to initiate protocol and/or RAM self-test, via bits 9 and/or 7 of the Start/Reset Register. Once the self-test completes, the RT will automatically go back online. However, if the user/host elects to **not** run self-test, it may then write a value of logic "1" to CLEAR RT HALT. Following this write transfer, the Enhanced Mini-ACE will revert back to its online RT state, and resume receiving and responding to messages from the 1553 bus. When this occurs, the value of bit 15 of Configuration Register #1 will change from "0" to "1."

CLEAR SELF-TEST REGISTER (bit 10): Writing logic "1" to this bit will clear the value of the BIT TEST STATUS REGISTER (register address 1Ch) to a value of 0000h.

INITIATE RAM SELF-TEST (bit 9): Writing logic "1" to this bit will initiate the self-test of the Enhanced Mini-ACE's internal 4K X 16 (and 64K X 16 if present) internal RAM. The RAM self-test consists of a walking pattern of "data = address," followed by a walking pattern of "data = address inverted." (See Table 1 for timing).

INITIATE PROTOCOL SELF-TEST (bit 7): Writing logic "1" to this bit will initiate the autonomous self-test of the Enhanced Mini-ACE's protocol logic. This test exercises the internal registers, encoder, decoder, and protocol logic. (See Table 1 for timing).

BC/SELECTIVE MONITOR STOP-ON-MESSAGE (bit 6) : Writing a value of logic "1" to this bit causes the Enhanced Mini-ACE to assume its off-line BC or Selected Monitor mode following the completion of the current message. If there is no message currently being processed, the Enhanced Mini-ACE halts operation immediately.

BC STOP-ON-FRAME (bit 5) : Writing a value of logic "1" to this bit causes the Enhanced Mini-ACE to assume its off-line BC mode following the completion of the current BC frame. If the Enhanced Mini-ACE is currently waiting to start the next BC frame when BC STOP-ON-FRAME is written to as logic "1," the Enhanced Mini-ACE will halt its BC operation immediately.

TIME TAG TEST CLOCK (bit 4) : When the TIME TAG RESOLUTION bits are programmed for the Time Tag Test Mode (bits 9, 8 and 7 of Configuration Register #2 are programmed to 1 1 0), writing a logic "1" to this bit will cause the value of the Time Tag register to increment by 1 LSB. In the Time Tag Test Mode, the Time Tag Register will only increment when a logic "1" is written to TIME TAG TEST CLOCK.

TIME TAG RESET (bit 3) : Writing a logic "1" to this bit causes the value of the Time Tag Register to Reset to zero (0000).

INTERRUPT RESET (bit 2) : Writing a "1" to this bit resets the value of the Interrupt Status Registers 1 and 2 to 0000 (except for the RT ADDRESS PARITY ERROR bit, if the condition persists). In addition, if the PULSE*/LEVEL Configuration Register bit is set to a "1," writing a "1" to this bit clears the INT* output to logic "1."

BC/MT START (bit 1) : When a logic "1" is written to this bit in either non-enhanced or enhanced BC mode, the Enhanced Mini-ACE starts processing its programmed frame of BC messages. When a logic "1" is written to this bit in MT mode, the Enhanced Mini-ACE Monitor goes on-line and starts storing received words to the shared RAM. It should be noted that an MT START command is required to start either the Word Monitor or the Selective Message Monitor, in the Monitor (only) mode. However, in the combined RT/Selective Monitor mode, an MT START command is not required. That is, assuming that the Enhanced Mini-ACE is in the ENHANCED mode, the RT and MT will go on-line immediately after Configuration Register #1 has been programmed for the RT/Selective Monitor mode.

RESET (bit 0) : This bit provides software-reset capability for the Enhanced Mini-ACE. When a logic "1" is written to this bit, any message in progress in BC or RT modes is immediately aborted. In Monitor mode, the ACE goes off-line immediately and stops storing received words. Built-in Self-test is not performed; the BIT Test Status Registers will revert to its default value of 0800 (hex). All other registers are reset to 0000 (hex). All other internal states are reinitialized to their default (power turn-on) conditions.

When writing to the Start/Reset Register, all RESERVED bits must be written with a value of "0."

4.11 Command Stack Pointer Register/Enhanced BC Instruction List Register.

(Register Address 0011; Read Only)

This register provides the host processor read access to the current value of the Stack Pointer for non-enhanced BC mode, as well for RT and MT modes. In these modes, the value of this register is loaded to the value of the pointer to the start of the command stack descriptor for the current message during the message's SOM (Start-of-Message) sequence.

In non-enhanced BC mode, RT mode, and Selective Monitor Mode, the value of the stack pointer is incremented by four for each message processed. In non-enhanced BC mode, the value of the Active Area Stack Pointer shared RAM location will be incremented by four – to the value of the descriptor address for the next BC message – during the message's EOM (End-of-Message) sequence.

In enhanced BC mode, this register reflects the current (running) value of the BC instruction list pointer. The value of this pointer is incremented by two following the execution of the current instruction. Note that in general this value is different from that stored in the Initial Instruction List Pointer, which is programmed by means of read/write register 0D.

For RT and Selective Monitor modes, if COMMAND STACK POINTER INCREMENT ON EOM, bit 13 of Configuration Register #6, is programmed to logic "0" (default, Enhanced Mini-ACE compatible), then the value of the Active Area Command Stack Pointer RAM location will be incremented by four (4) during the message's SOM (start-of-message) sequence; that is, it is updated from the value of the descriptor pointer for the current message to the value of the descriptor pointer for the next message.

However (for RT and Monitor modes), if COMMAND STACK POINTER INCREMENT ON EOM is programmed to logic "1," the value of the Active Area Command Stack Pointer RAM location will be incremented by four during the message's EOM (end-of-message) sequence. That is, it will be updated from the value of the descriptor pointer for the current message to the value of the descriptor pointer for the next message. For the case of a superceded message (where there is no EOM sequence), the value will be updated during the SOM sequence for the next message.

The Stack Pointer Register is not used in the Word Monitor mode.

It should be noted that the BC/RT Command Stack size defaults to 256 in the non-ENHANCED mode. In the ENHANCED mode (ENHANCED MODE ENABLE, bit 15 of Configuration Register #3, set to logic "1"), the stack size is programmable for 256, 512, 1024, and 2048 words by means of bits 14 and 13 of Configuration Register #3.

The operation of the Command Stack Pointer Register and the Active Area Stack Pointer is summarized in Table 45. This table illustrates the bit mapping of the Command Stack Pointer Register.

Table 45. Incrementing of Command Stack Pointer RAM Register and Active Area Stack Pointer RAM Location

MODE	COMMAND STACK POINTER REGISTER	ACTIVE AREA RAM LOCATION
Non-Enhanced BC	Updated from the value of the descriptor pointer for the previous message to the value of the current message during SOM.	Updated from the value of the descriptor pointer for the current message to the value of the descriptor pointer for the next message during EOM.
Enhanced BC	Reflects the current value of the BC Instruction List pointer. The value of this pointer is incremented by two following the execution of the current instruction.	Not applicable.
RT or Selective Message Monitor, with COMMAND STACK POINTER INCREMENT ON EOM = "0"	Updated from the value of the descriptor pointer for the previous message to the value of the current message during SOM.	Updated from the value of the descriptor pointer for the current message to the value of the descriptor pointer for the next message during SOM.
RT or Selective Message Monitor, with COMMAND STACK POINTER INCREMENT ON EOM = "1"	Updated from the value of the descriptor pointer for the previous message to the value of the current message during SOM.	Updated from the value of the descriptor pointer for the current message to the value of the descriptor pointer for the next message during EOM. In the case of a superceded message (where there is no EOM sequence), the value will be updated during the SOM sequence for the next message.
Word Monitor	Not applicable.	

Table 46. BC/RT Command Stack Pointer Register (Read 03H)

BIT	DESCRIPTION
15(MSB)	COMMAND STACK POINTER 15
• • •	• • •
0(LSB)	COMMAND STACK POINTER 0

4.12 BC Control Word/RT Subaddress Control Word Register

(Register Address 0100; Read/Write)

This register provides read/write accessibility for the current BC Control Word or RT Subaddress Control Word. While the host CPU can always read this register, it should be noted that the host processor couldn't write it:

When the Enhanced Mini-ACE is programmed for RT or Monitor mode, or, during the processing of a frame of messages when in BC mode. The BC CONTROL WORD/RT Subaddress REGISTER may be written when the Enhanced Mini-ACE is in "Idle" BC mode, that is, when it is programmed for BC mode (via bits 15 and 14 of Configuration Register #1) but not currently processing a frame of messages.

The bit mapping of this register is provided by Table 47 and Table 48.

Table 47. BC Control Word Register (Read/Write 04H)

BIT	DESCRIPTION
15(MSB)	TRANSMIT TIME TAG FOR SYNCHRONIZE MODE COMMAND
14	M. E. MASK
13	SERVICE REQUEST BIT MASK
12	SUBSYS BUSY BIT MASK
11	SUBSYS FLAG BIT MASK
10	TERMINAL FLAG BIT MASK
9	RESERVED BITS MASK
8	RETRY ENABLED
7	BUS CHANNEL A/B*
6	OFF LINE SELF TEST
5	MASK BROADCAST BIT
4	EOM INTERRUPT ENABLE
3	1553A/B SELECT
2	MODE CODE FORMAT
1	BROADCAST FORMAT
0(LSB)	RT-TO-RT FORMAT

Table 48. RT Subaddress Control Word (Read/Write 04H)	
BIT	**DESCRIPTION**
15(MSB)	RX: DOUBLE BUFFER ENABLE
14	TX: EOM INT
13	TX: CIRC BUF INT
12	TX: MEMORY MANAGEMENT 2 (MM2)
11	TX: MEMORY MANAGEMENT 1 (MM1)
10	TX: MEMORY MANAGEMENT 0 (MM0)
9	RX: EOM INT
8	RX: CIRC BUF INT
7	RX: MEMORY MANAGEMENT 2 (MM2)
6	RX: MEMORY MANAGEMENT 1 (MM1)
5	RX: MEMORY MANAGEMENT 0 (MM0)
4	BCST: EOM INT
3	BCST: CIRC BUF INT
2	BCST: MEMORY MANAGEMENT 2 (MM2)
1	BCST: MEMORY MANAGEMENT 1 (MM1)
0(LSB)	BCST MEMORY MANAGEMENT 0 (MM0)

4.13 Time Tag Register

(Register Address 0101; READ/WRITE)

Table 49. Time Tag Register (Read/Write 05H)	
BIT	**DESCRIPTION**
15(MSB)	TIME TAG 15
• • •	• • •
0(LSB)	TIME TAG 0

See Appendix "F" for important information Time Tag Register may not clear **IF** terminal is operating in RT Mode **AND** Interrupt Status Queue is enabled (i.e., bit 6 of Configuration Register #6 is Logic "1") **AND** bits 6, 7 or 14 (Time Tag Rollover, RT Address Parity Error, or RAM Parity Error respectively) of Interrupt Mask Register #1 are enabled (Logic "1").

As illustrated in Table 50, the resolution (µs/LSB) of the Time Tag Register is programmable by means of bits 9, 8, and 7 of Configuration Register #2.

Table 50. Time Tag Register Resolution				
CONFIGURATION REGISTER #2			TIME TAG RESOLUTION	ROLLOVER TIME (MODULUS)
BIT 9 TTR2	BIT 8 TTR1	BIT 7 TTR0		
0	0	0	64 μs	4.194 sec
0	0	1	32 μs	2.097 sec
0	1	0	16 μs	1.048 sec
0	1	1	8 μs	524 ms
1	0	0	4 μs	262 ms
1	0	1	2 μs	131 ms
1	1	0	TEST MODE	N/A
1	1	1	EXTERNAL CLOCK (See NOTE)	N/A

NOTE: The time tag external clock feature “TAG_CLK” input is not included in all Enhanced Mini-Ace series products. Certain Enhanced Mini-ACE based products include this input as a standard feature.

The Time Tag Register provides the output of a free-running counter. The resolution of the counter is programmable by means of bits 9, 8, and 7 of Configuration Register #2 from among 64, 32, 16, 8, 4 and 2 μs/LSB. There is also a test mode in which the Time Tag register may be incremented one LSB at a time under software control for the purpose of self-test.

The time tag external clock feature “TAG_CLK” input is not included in all Enhanced Mini-Ace series products. Certain Enhanced Mini-ACE based products include this input as a standard feature.

The Time Tag Register is reset to zero following hardware or software reset, a TIME TAG RESET (bit 3 of the Start/Rest Register), or after the Enhanced Mini-ACE has received a Synchronize (without data) mode code and bit 6 of Configuration Register #2 is logic "1." The Time Tag Register is loaded by the received Data Word following reception of a Synchronize (with data) mode code, provided that bit 5 of Configuration Register #2 is logic "1." If ENHANCED MODE CODE SYNCHRONIZE, bit 2 of Configuration Register #7, is logic “1,” then the data word will only be stored to the time tag counter if its LSB is logic “0.”

In BC mode, if TRANSMIT TIME TAG FOR SYNCHRONIZE (bit 5 of Configuration Register #2) is programmed to logic “1,” the Enhanced Mini-ACE BC will transmit the value of its Time Tag Register as the data word for a Synchronize (with data) mode code. When the ENHANCED TIME TAG SYNCHRONIZE (bit 2 of Configuration Register #7) is programmed to logic “1,” the transmitted data word will contain current 16-bit Time Tag value.

4.14 Interrupt Status Register #1

(Register Address 0110; Read Only)

Interrupt Status Register #1 and Interrupt Status Register #2 allow the host processor to determine the cause of an interrupt request by means of a pair of READ operations. Either of these registers will be cleared after that Interrupt Status Register (but not the other one) has been read, provided that CLEAR INTERRUPT STATUS AUTO CLEAR, bit 4 of Configuration Register #2 ,is logic "1." Also, both interrupt status registers will be cleared by writing logic "1" to INTERRUPT RESET, bit 2 of the Start/Reset Register.

It should be noted that for non-ENHANCED mode (ENHANCED MODE ENABLE, bit 15 of Configuration Register #3 programmed to logic "0"), only bits 7-0 of Interrupt Status Register #1 are active. In ENHANCED MODE (bit 15 of Configuration Register #3 set to logic "1"), with ENHANCED INTERRUPTS enabled (bit 15 of Configuration Register logic #2 is logic "1"), all 15 bits (14-0) of Interrupt Status Register #1 as well as bits 14-1 of Interrupt Status Register #2 may become set.

It should also be noted that in the non-ENHANCED mode, bits 7 through 0 of Interrupt Mask Register #1 are used to both enable interrupts for the various events/conditions and to enable the respective bits of Interrupt Status Register #1 to be set. That is, the various bits of Interrupt Status Register #1 will not become set if the corresponding bits of Interrupt Mask Register #1 are not set. Bits 14-8 of Interrupt Mask (and Status) Register #1, as well as all of the bits of Interrupt Mask (and Status) Register #2 are not used in non-ENHANCED mode.

ENHANCED mode, with ENHANCED INTERRUPTS ENABLED (bit 15 of Configuration Register #2 programmed to logic "1"), supports polling (non-interrupting) applications. In this mode, the value of the Interrupt Mask Register (#1 and #2) bits has no effect on the operation of the respective Interrupt Status Register (#1 and #2) bits. If ENHANCED INTERRUPTS are enabled, the bits of the Interrupt Status Registers do not need to be enabled by the corresponding bits in the Interrupt Mask Registers. In the ENHANCED INTERRUPT mode, these bits become set following the occurrence of the respective event/condition, regardless of the status of the corresponding Interrupt Mask Register bit. In either case, an interrupt for any of the 29 event/conditions defined by Interrupt Mask/Status Registers #1 and #2 (8 in non-ENHANCED mode) is only enabled if the respective bit of the Interrupt Mask Register (for the event/condition) has been programmed to logic "1."

Table 51 provides the bit mapping of Interrupt Status Register #1.

Table 51. Interrupt Status Register #1 (Read Only 05H)	
BIT	**DESCRIPTION**
15(MSB)	MASTER INTERRUPT
14	RAM PARITY ERROR
13	TRANSMITTER TIMEOUT
12	BC/RT COMMAND STACK ROLLOVER
11	MT COMMAND STACK ROLLOVER
10	MT DATA STACK ROLLOVER
9	HANDSHAKE FAILURE
8	BC RETRY
7	RT ADDRESS PARITY ERROR
6	TIME TAG ROLLOVER *
5	RT CIRCULAR BUFFER ROLLOVER
4	BC CONTROL WORD/RT SUBADDRESS CONTROL WORD EOM
3	BC END OF FRAME
2	FORMAT ERROR
1	BC STATUS SET/RT MODE CODE/MT PATTERN TRIGGER
0(LSB)	END OF MESSAGE

* **See Appendix "F"** for important information regarding Time Tag Rollover (i.e., bit 6 of Interrupt Register #1 is Logic "1") used in conjunction with Interrupt Status Queue (i.e., bit 6 of Configuration Register #6 is Logic "1").

MASTER INTERRUPT (bit 15) : In order for the MASTER INTERRUPT bit to be set, the Enhanced Mini-ACE must be programmed for ENHANCED mode (bit 15 of Configuration Register #3 = logic "1") and ENHANCED INTERRUPTS must be enabled, by setting bit 15 of Configuration Register #2. In this case, MASTER INTERRUPT will be set if one or more of bits 14-0 of Interrupt Status Register #1 or any of bits 14-1 of Interrupt Status Register #2 have been set to logic "1" and the respective bit of the corresponding Interrupt Mask Register bit(s) has been set. That is, this bit reflects the state of the Enhanced Mini-ACE's interrupt request output (INT*). A logic "1" indicates that an interrupt request has been issued.

Note that the INTERRUPT CHAIN BIT, bit 0 of Interrupt Status Register #2, indicates that one or more bits are set in Interrupt Status Register #1, denoting interrupt event(s). If ENHANCED INTERRUPTS are enabled (bit 15 of Configuration Register #2 = logic "1"), and there are one or more bits set in Interrupt Status Register #1 that do not result in an interrupt request (because these requests have been disabled by means of Interrupt Mask Register #1), note that these bits **will not** result in the setting of either MASTER INTERRUPT or the INTERRUPT CHAIN BIT.

It is recommended that Interrupt Status Register #2 be read prior to reading Interrupt Status Register #1. That is, it will only be necessary to read Interrupt Status Register #1 if the INTERRUPT CHAIN BIT in Interrupt Status Register #2 has been set.

Note that if INTERRUPT STATUS AUTO-CLEAR, bit 4 of Configuration Register #1, is logic "1," that each of the two Interrupt Status Registers will only be auto-cleared by the reading of **that specific** interrupt status register. That is, if both Interrupt Status Register #1 and Interrupt Status Register #2 have issued **enabled** interrupts, that Interrupt Status Register #2 will be cleared immediately following being read, independent of whether or not Interrupt Status Register #1 has been read. Likewise, Interrupt Status Register #1 will be cleared immediately following being read, independent of whether or not Interrupt Status Register #2 has been read.

If the Enhanced Mini-ACE's INT* output has been configured for "level" mode (i.e., bit 3 of Configuration Register #2, LEVEL/PULSE* INTERRUPT REQUEST, is logic "1"), then it will only be necessary to read the Interrupt Status Register (#1 and/or #2) that is requesting an interrupt that has been enabled by the corresponding Interrupt Mask Register. However, for the case where both Interrupt Status Register #1 and Interrupt Status Register #2 have bits set reflecting interrupt events, it will be necessary to read both interrupt status registers in order to clear INT*.

RAM PARITY ERROR (bit 14) : Applicable only in the ENHANCED mode (ENHANCED MODE ENABLE, bit 15 of Configuration Register #3 set to logic "1") and ENHANCED INTERRUPTS ENABLED (bit 15 of Configuration Register #2 set to logic "1"). If set to logic "1," this indicates a RAM parity error. This bit is only applicable for 64K X 17 RAM versions of Enhanced Mini-ACE. It is not applicable for 4K X 16 RAM versions. By programming RAM PARITY ENABLE, bit 14 of Configuration Register #2 to logic "1," the 64K X 17 RAM versions of the Enhanced Mini-ACE can be programmed to generate a parity bit on all write accesses to 17-bit RAM. A parity check is then performed on all read accesses to the 17-bit RAM. A RAM PARITY ERROR interrupt indicates a failure of this parity check.

TRANSMITTER TIMEOUT (bit 13) : Applicable only in the ENHANCED mode (ENHANCED MODE ENABLE, bit 15 of Configuration Register #3 set to logic "1") and ENHANCED INTERRUPTS ENABLED (bit 15 of Configuration Register #2 set to logic "1"). If this bit is set to logic "1," this indicates that the Enhanced Mini-ACE's transmitter watchdog timer has timed out. This occurs if the Enhanced Mini-ACE's encoder attempts to transmit for longer than 660.5 µs.

BC/RT COMMAND STACK ROLLOVER (bit 12) : Applicable only in the ENHANCED mode (ENHANCED MODE ENABLE, bit 15 of Configuration Register #3 set to logic "1") and ENHANCED INTERRUPTS ENABLED (bit 15 of Configuration Register #2 set to logic "1"). If this bit returns a value of logic "1," it indicates a rollover of the BC/RT Command Stack. The size of the BC/RT Command Stack 1 is programmable from among 256 words (64 messages), 512, 1024, and 2048 words (512 messages) by means of bits 14 and 13 of Configuration Register #3.

MESSAGE MONITOR COMMAND STACK ROLLOVER (bit 11) : Applicable only in the ENHANCED mode (ENHANCED MODE ENABLE, bit 15 of Configuration Register #3 set to logic "1") and ENHANCED INTERRUPTS ENABLED (bit 15 of Configuration Register #2 set to logic "1"). If this bit returns a value of logic "1," it indicates an interrupt following a rollover of the Message Monitor Command Stack. This is applicable for both the Message Monitor as well as the combined RT/Message Monitor modes. The size of the MT Command Stack is programmable from among 256 (64 messages), 1024, 4096, and 16,384 words (4096 messages) by means of bits 12 and 11 of Configuration Register #3.

MONITOR DATA STACK ROLLOVER (bit 10) : Applicable only in the ENHANCED mode (ENHANCED MODE ENABLE, bit 15 of Configuration Register #3 set to logic "1") and ENHANCED INTERRUPTS ENABLED (bit 15 of Configuration Register #2 set to logic "1"). If this bit returns a value of logic "1," it indicates a rollover of the Word Monitor or Message Monitor Data Stack. The size of the Data Stack is programmable from among 512, 1024, 2048, 4096, 8192, 16,384, 32,768, or 65,536 words by means of bits 10, 9, and 8 of Configuration Register #3.

HANDSHAKE FAILURE (bit 9) : Applicable only in the ENHANCED mode (ENHANCED MODE ENABLE, bit 15 of Configuration Register #3 set to logic "1") and ENHANCED INTERRUPTS ENABLED (bit 15 of Configuration Register #2 set to logic "1"). If set, enables an interrupt following a handshake timeout during a transfer between the 1553 protocol section and the RAM. A Handshake Failure can only occur in the transparent mode; it cannot occur in buffered mode. There are two conditions that can cause a Handshake Failure. For both conditions, the allotted time is 10.5 µs for 20 MHz clock input, 10.0 µs for a 16 MHz clock, 9.0 µs for a 12 MHz clock, and 8.5 µs for 10 MHz clock input.

The two conditions are:

When the Data Transfer Grant (DTGRT) input is not asserted within the allotted time after the Data Transfer Request (DTREQ) output is asserted.

When the STRBD* input signal is held at logic "0" for longer than the allotted time after the Enhanced Mini-ACE's READYD* output is asserted low at the end of a CPU transfer cycle.

BC RETRY (bit 8) : Applicable only in the ENHANCED mode (ENHANCED MODE ENABLE, bit 15 of Configuration Register #3 set to logic "1") and ENHANCED INTERRUPTS ENABLED (bit 15 of Configuration Register #2 set to logic "1"). A value of logic "1" indicates the occurrence of a retried message in BC mode. If enabled, the interrupt will occur regardless of whether the retry attempt was successful or unsuccessful. The interrupt will occur after the failed message has been retried (either once or twice, successfully or unsuccessfully).

RT ADDRESS PARITY ERROR (bit 7) : Indicates that the parity sum of the internal RTAD4-RTAD0 and RTADP signals is even, rather than odd, as required for the Enhanced Mini-ACE to respond to messages directed to its own address in RT mode. If the input signal RT_AD_LAT is connected to logic “0,” or if RT_AD_LAT is connected to logic “1” and RT ADDRESS SOURCE (bit 5 of Configuration Register #6) has been programmed to logic “0,” then the internal RTAD4-RTAD0 and RTADP logic levels are derived directly from the RTAD4-RTAD0 and RTADP input signals. However, if the input signal RT_AD_LAT is connected to logic “1” and RT_AD_LAT is connected to logic “1” and RT ADDRESS SOURCE (bit 5 of Configuration Register #6) has been programmed to logic “1,” then the internal RTAD4-RTAD0 and RTADP logic levels are programmed by the host processor, by means of Configuration Register #5.

It should be noted that if an RT ADDRESS PARITY ERROR condition occurs, the respective Interrupt Status Register bit will clear to logic "0" after the Interrupt Status Register has been read (if AUTO CLEAR is enabled) or after INTERRUPT RESET, bit 2 of the Start/Reset Register, has been written as logic "1." The RT ADDRESS PARITY ERROR bit will remain at logic "0" and will not return to logic "1" until either of the following two sequences has occurred: (1) the RT Address parity error condition goes away and then re-occurs, or (2) the RT ADDRESS PARITY ERROR bit in Interrupt Mask Register #1 is cleared (either by writing "0" to the register bit or by means of either a hardware or software reset to the Enhanced Mini-ACE) and is then set back to logic "1," assuming that the address parity error condition persists.

TIME TAG ROLLOVER (bit 6) : Indicates that the Time Tag Register has rolled over from FFFF to 0000.

See Appendix “F” for important information regardingTime Tag Rollover (i.e., bit 6 of Interrupt Register #1 is Logic “1”) used in conjunction with Interrupt Status Queue (i.e., bit 6 of Configuration Register #6 is Logic “1”).

RT CIRCULAR BUFFER ROLLOVER (bit 5) : This bit will be set at the end of a message in RT mode, provided that the Enhanced Mini-ACE is in the ENHANCED RT Memory Management mode (bit 2 of Configuration Register #2 = logic “1”) and the "Interrupt at Rollover" bit is set in the Subaddress Control Word for the Tx/Rx/Bcst subaddress of the just completed message and the current message caused the data block Lookup Table address pointer to cross the lower boundary of the respective circular buffer, resulting in a rollover. This interrupt is applicable for rollovers of either a subaddress-specific circular buffer, or the global circular buffer.

NOTE: If OVERWRITE INVALID DATA (bit 11 of Configuration Register #2) is logic "0, "this interrupt request will occur immediately when the address location at the upper boundary of a circular buffer is accessed. If OVERWRITE INVALID DATA is logic "1," the interrupt request will occur at the end of a valid message in which the last location in the circular buffer was accessed. If OVERWRITE INVALID DATA is

logic "1," an RT CIRCULAR BUFFER ROLLOVER will not occur following an invalid received message.

RT SUBADDRESS CONTROL WORD EOM/BC SELECTIVE EOM (bit 4) : In RT mode, this bit will be set at the end of a message, provided that the Enhanced Mini-ACE is in the Enhanced Memory Management RT mode (bit 2 of Configuration Register #2 = logic “1”) and the "Interrupt at EOM" bit is set in the Subaddress Control Word for the Tx/Rx/Bcst-subaddress of the just completed message.

In BC mode, this bit will also be set at the end of a message, provided that the Enhanced Mini-ACE is in the ENHANCED mode (bit 15 of Configuration Register #3 = logic “1”) and EXPANDED BC CONTROL WORD is enabled (bit 12 of Configuration Register #4 is logic "1") and the EOM INTERRUPT ENABLE bit (bit 4) in the current BC Control Word is set to logic "1.”

BC END-OF-FRAME (bit 3) : For non-Enhanced Bus Controller End-of-Frame indicates that an entire programmed BC message frame has been completed. That is, following the end of the last message processed, the Message Count RAM location incremented to FFFF (hex). Note that if BC STOP-ON-ERROR is enabled and a BC frame is aborted before the Message Count has incremented to FFFF (hex), the BC END-OF-FRAME condition will not occur.

In Enhanced BC mode, with bit 1 of Configuration Register #7 (ENH BC WATCHDOG TIMER EN) set to logic “1,” this bit indicates that frame timer has decremented to zero.

FORMAT ERROR (bit 2) : Indicates that a completed message, in BC, RT, or Selective Message Monitor Mode, contained one or more of the following errors:

Loop Test Failure: A loopback test is performed on all messages transmitted by the BC or RT (except broadcast messages in RT mode). The received version of all transmitted words is checked for validity and correct sync type. In addition, a 16-bit comparison is performed on the last word transmitted by the BC or RT. If **any** of these checks or comparisons do not verify, the loopback test is considered to have failed. Loop Test Failure is not applicable in Monitor mode.

Message Error: A received message contained a violation of the 1553 message validation criteria (encoding, parity, bit count, word count, etc.).

Response Timeout: In BC mode, an RT has either not responded, or has responded later than the programmed value of the BC No Response Timeout time. In RT mode, if the Enhanced Mini-ACE is the receiving RT in an RT-to-RT transfer and the transmitting RT has not responded with its Status Word within the programmed value of the RT-to-RT Response Timeout time after the Transmit Command Word.

BC STATUS SET/RT SELECTED MODE CODE INTERRUPT/MT PATTERN TRIGGER (bit 1) : In BC mode, the RT Status Word received from a responding RT either contained an incorrect RT address field or one of the 8 non-RESERVED Status bits contained an unexpected bit value. The expected value for these 8 bits is normally zero (0), with one exception: If BROADCAST MASK ENABLED/XOR* (bit 11 of Configuration Register #4) is logic "0" and the MASK BROADCAST bit (bit 5) of the message's BC Control Word is logic "1," the expected value of the Broadcast Command Received bit becomes "1," rather than "0."

In RT mode, this interrupt can only occur in the ENHANCED mode (bit 15 of Configuration Register #3 is set to logic "1") and if Enhanced Mode Code Handling is enabled (bit 0 of Configuration Register #3 is set to logic "1"). If these two bits are set, mode code interrupts for individual broadcast-T/R bit-mode codes may be enabled by setting the appropriate bit(s) in address locations 0108-010F in the shared RAM. Reception of an enabled mode code message will then cause a MODE CODE interrupt to occur at the end of the message.

In the Word Monitor mode, a Pattern Trigger interrupt will occur in the ENHANCED mode (bit 15 of Configuration Register #3 is set to logic "1") following the reception of a valid Command Word that matches the bit pattern programmed in the Monitor Trigger Register.

END OF MESSAGE (bit 0) : End of Message. In BC, RT, or Selective Message Monitor mode, indicates the completion of a message (regardless of validity).

4.15 Configuration Register #3

(Register Address 0111; READ/WRITE)

Table 52. Configuration Register #3 (Read/Write 07H)

BIT	DESCRIPTION
15 (MSB)	ENHANCED MODE ENABLE
14	BC/RT COMMAND STACK SIZE 1
13	BC/RT COMMAND STACK SIZE 0
12	MT COMMAND STACK SIZE 1
11	MT COMMAND STACK SIZE 0
10	MT DATA STACK SIZE 2
9	MT DATA STACK SIZE 1
8	MT DATA STACK SIZE 0
7	ILLEGALIZATION DISABLED
6	OVERRIDE MODE T/$\overline{R}$ ERROR
5	ALTERNATE STATUS WORD ENABLE
4	ILLEGAL RX TRANSFER DISABLE
3	BUSY RX TRANSFER DISABLE
2	$\overline{RTFAIL}$/$\overline{RTFLAG}$ WRAP ENABLE
1	1553A MODE CODES ENABLE
0 (LSB)	ENHANCED MODE CODE HANDLING

ENHANCED MODE ENABLE (bit 15) : If this bit in programmed to logic "0," the functionality of the Enhanced Mini-ACE defaults to that of the BUS-61559 Advanced Integrated Mux Hybrid with ENHANCED RT Features (AIM-HY'er). Programming this bit to logic "1" allows many of the Enhanced Mini-ACE's advanced features to be enabled by means of the Interrupt Mask Register, the various Configuration Registers, as well as by the BC Control Word and RT Subaddress Control Word.

These features include **all** of the functions enabled by the various bits of Configuration Registers #3, 4, 5, 6, and 7. If ENHANCED MODE ENABLE is programmed to logic "0," the operation of these register functions defaults to that indicated by their logic "0" state.

It should be noted that in order to enable any of the ENHANCED features, ENHANCED MODE ENABLED must be set to logic "1" PRIOR TO setting any of the other Configuration Register bits to enable the ENHANCED features. THIS INCLUDES ANY OF THE FEATURES ENABLED BY THE LOWER 15 bits (14-0) OF CONFIGURATION REGISTER #3, as well as features enabled by other registers.
Specifically, bit 15 must first be set by writing 8000 (hex) to Configuration Register #3 BEFORE proceeding to set any of bits 14-0. When these bits are set, ENHANCED MODE ENABLE must continue to be programmed to logic "1."

In the non-ENHANCED mode, functions activated by the following register bits are active:

- Interrupt Mask Register #1 and Interrupt Status Register #1, bits 7-0
- Configuration Register #1: for BC mode, bits 15-12; for RT mode (without Alternate Status only), bits 15-13 and 11-8; for Word Monitor mode, bits 15-13
- Configuration Register #2, bits 11-0
- Start/Reset Register, bits 4-0
- BC/RT Command Stack Pointer
- RT Subaddress Control Word Register
- Time Tag Register
- Interrupt Status Register bits 15 and 7-0

In the ENHANCED mode, in addition to all of the non-ENHANCED mode functions, those enabled by the following registers (or register bits) may also be activated:

- Interrupt Mask Register #1 and Interrupt Status Register #1, bits 14-8, and Interrupt Mask Register #2 and Interrupt Status Register #2

- Configuration Register #1: BC mode, bits 11-0; RT mode, bits 12 and 7-0, and the RT With Alternate Status mode; Monitor, bits 12-9, 7, 2-0; and the Message Monitor and RT/Message Monitor modes
- Configuration Register #2, bits 15-12
- Start/Reset Register, bits 11, 10, 9, 7, 6 and 5
- BC Control Word Register
- Configuration Registers #3, #4, #5, #6, and #7
- RT/Monitor Data Stack Address Register
- BC Frame Time Remaining Register
- BC Time to Next Message Remaining Register
- BC Frame Time /RT Last Command/Monitor Trigger Word Register
- RT Status Word Register
- RT BIT Word Register
- BC Condition Code Register and BC General Purpose Flag Register
- BIT Test Status Register
- BC General Purpose Queue Pointer Register/RT-MT Interrupt Status Queue Pointer Register
- Test Mode Registers 0-7, and the test registers in the register address range from 32 to 63 (20h to 3Fh)

For all three modes, use of the ENHANCED Mode enables the various read-only bits (bits 2-0) in Configuration Register #1.

The Enhanced Mini-ACE must be in the ENHANCED mode in order to enable ENHANCED INTERRUPTS (by setting bit 15 of Configuration Register #2 to logic "1").

The Enhanced Mini-ACE must be in ENHANCED mode in order for the host to be able to initiate a protocol and/or RAM built-in self-test.

For BC mode, the features that require ENHANCED MODE ENABLE programmed to logic "1" include the expanded BC Control Word and BC Block Status Word, additional STOP-ON-ERROR and STOP-ON-STATUS SET functions, frame auto-repeat, programmable intermessage gap times, automatic retries, expanded Status Word Masking, and the capability to generate interrupts following the completion of any selected message. ENHANCED MODE ENABLE must also be logic “1” in order to invoke the Enhanced Mini-ACE’s enhanced BC mode, including use of the general-purpose queue.

For RT mode, the features that require ENHANCED MODE ENABLE programmed to logic "1" include the expanded RT Block Status Word, the combined RT/Selective Message Monitor mode, internal wrapping of the "RTFAIL*" output signal to the "RTFLAG*" input signal, the double buffering scheme for individual receive (broadcast) subaddresses, and the alternate (fully software programmable) RT Status Word, and the busy bit lookup table option. ENHANCED MODE ENABLE must also be “1” in order to invoke any of the host programmable RT features introduced in the Enhanced Mini-ACE generation, including global circular buffer for received messages, 50% rollover interrupts, and the interrupt status queue.

For MT mode, use of the ENHANCED Mode enables use of both the Selective Message Monitor and the combined RT/Selective Monitor modes, as well as use of the monitor triggering capability. ENHANCED MODE ENABLE must also be “1” in order to invoke any of the Monitor mode features introduced in the Enhanced Mini-ACE generation, including 50% rollover interrupts and the interrupt status queue.

BC/RT COMMAND STACK SIZE 1,0 (bits 14,13) : These two bits select the size of the BC/RT Command Stack. The default value for both bits is logic "0," which specifies a stack size of 256 words (64 messages). Table 53 illustrates the BC/RT Command Stack Sizes.

Table 53. BC/RT Command Stack Size

BIT 14 BC/RT CMD STACK SIZE 1	BIT 13 BC/RT CMD STACK SIZE 0	BC/RT STACK SIZE (WORDS)
0	0	256 (64 messages)
0	1	512 (128 messages)
1	0	1024 (256 messages)
1	1	2048 (512 messages)

NOTE: The default size is 256 words (64 messages).

MONITOR COMMAND STACK SIZE 1,0 (bits 12,11) : These two bits select the size of the Monitor Command Stack. The default value for these two bits is logic "00," which specifies a stack size of 256 words. Table 54 illustrates the MT Command Stack Sizes.

Table 54. Monitor Command Stack Size

BIT 12 MT CMD STACK SIZE 1	BIT 11 MT CMD STACK SIZE 0	MONITOR STACK SIZE (WORDS)
0	0	256 (64 messages)
0	1	1024 (256 messages)
1	0	4096 (1024 messages)
1	1	16384 (4096 messages)

NOTE: The default size is 256 words (64 messages).

MONITOR DATA STACK SIZE 2,1,0 (bits 10,9,8) : These three bits select the size of the Monitor Data Stack. This stack is used in both the Word Monitor and Message Monitor modes. The default value for these three bits is logic "000," which specifies a stack size of 65,536 words. Table 55 illustrates the MT Data Stack Sizes.

Table 55. Monitor Data Stack Size

BIT 10 MT DATA STACK SIZE 2	BIT 9 MT DATA STACK SIZE 1	BIT 8 MT DATA STACK SIZE 0	MONITOR DATA STACK SIZE (WORDS)
0	0	0	65,536 (default)
0	0	1	32768
0	1	0	16384
0	1	1	8192
1	0	0	4096
1	0	1	2048
1	1	0	1024
1	1	1	512

NOTE: The default monitor data stack size is 65,536 words.

ILLEGALIZATION DISABLED (bit 7) : For RT mode. If this bit is programmed to logic "0," the Enhanced Mini-ACE's internal RT Command illegalization feature is enabled. That is, shared RAM address locations 0300 to 03FF (hex) are dedicated to the illegalization function. If this bit is programmed to logic "1," the illegalization function is disabled. In this configuration, addresses 0300 through 03FF may be used for the storage of Stack or message data. This bit has no effect for BC or MT modes.

OVERRIDE MODE CODE T/R* BIT ERROR (bit 6) : For RT mode. If this bit is programmed to logic "0," a mode code Command Word with a T/R* bit of logic "0" and an MSB of the mode code field of "0" (receive mode codes 0 to 15) is considered an undefined Command Word. In this configuration, the Enhanced Mini-ACE RT will not respond to such a command and the Message Error bit will be set. If this bit is programmed to logic "1," a mode code Command Word with a T/R* bit of 0 and an MSB of the mode code field of 0 will be considered a defined (reserved) mode Command Word. In this configuration, the Enhanced Mini-ACE will respond to such a command and the Message Error bit will not become set.

ALTERNATE RT STATUS WORD ENABLED (bit 5) : For RT mode. If this bit is programmed to logic "0," only the Dynamic Bus Control Acceptance, Busy, Service Request, Subsystem Flag, and Terminal Flag RT Status Word bits are under control of the host processor, by means of bits 11 through 7 of Configuration Register #1. If this bit is programmed to logic "1," all 11 RT Status Word bits are under control of the host processor, by means of bits 11 through 1 of Configuration Register #1.

ILLEGAL RECEIVE TRANSFER DISABLE (bit 4) : If this bit is programmed to logic "0" (default) and the Enhanced Mini-ACE receives a receive command that has been illegalized, the Enhanced Mini-ACE will store the received Data Words to the shared RAM. If this bit is programmed to logic "1" and the Enhanced Mini-ACE receives a receive command that has been illegalized, the Enhanced Mini-ACE will not store the received Data Words to the shared RAM.

BUSY RECEIVE TRANSFER DISABLE (bit 3) : If this bit is programmed to logic "0" (default), and the host processor has programmed BUSY* (bit 10 of Configuration Register #1 is logic "0") or the particular command word (broadcast, T/R* bit, subaddress) has been programmed to be busy by means of the busy lookup table and the Enhanced Mini-ACE RT receives a receive command, the Enhanced Mini-ACE will respond with its Status Word with the Busy bit set and will store the received Data Words to the shared RAM.

Note: BUSY RECEIVE TRANSFER DISABLE (bit 3) feature is not supported on PCI-Enhanced Mini-ACE, PCI Mini-ACE Mark3, or PCI-Micro-ACE-TE. BUSY RECEIVE TRANSFER DISABLE (bit 3) is RESERVED and should be set to zero on PCI-Enhanced Mini-ACE, PCI Mini-ACE Mark3, or PCI-Micro-ACE-TE.

If this bit is programmed to logic "1," the host processor has programmed BUSY* to logic "0" or the particular Command Word (broadcast, T/R* bit, subaddress) has been programmed to be busy by means of the Busy lookup table and the Enhanced Mini-ACE RT receives a receive command, the Enhanced Mini-ACE will respond with its Status Word with the Busy bit set and will not store the received Data Words to the shared RAM.

RTFAIL*/RTFLAG* WRAP ENABLE (bit 2) : Affects RT mode only. If this bit is programmed to logic "0" (default), the Terminal flag status word bit is controlled entirely by the host processor, via Configuration Register #1. However, if this bit is programmed to logic "1," the Terminal flag status word bit will also become set if either a transmitter timeout (660.5 µs) condition had occurred or the Enhanced Mini-ACE RT had failed its loopback test for the previous non-broadcast message. The loopback test is performed on all non-broadcast messages processed by the Enhanced Mini-ACE RT. The received version of all transmitted words is checked for validity (sync and data encoding, bit count, parity) and correct sync type. In addition, a 16-bit comparison is performed on the received version of the last word transmitted by the Enhanced Mini-ACE RT. If any of these checks or comparisons do not verify, the loopback test is considered to have failed.

1553A MODE CODES ENABLED (bit 1) : Affects both RT and Message Monitor modes. If this bit is programmed to logic "0" (default), the Enhanced Mini-ACE considers both subaddresses 0 and 31 to be mode code subaddresses. In this configuration, the Enhanced Mini-ACE RT recognizes and responds to all MIL-STD-1553B mode codes, including those with or without data words. In addition, if this bit is logic "0," the Enhanced Mini-ACE will decode for the MIL-STD-1553B "Transmit Status" and "Transmit Last Command" mode codes and will not update its internal RT Status Word Register as a result of these commands, with the exception of setting the Message Error bit if the command is illegalized.

If this bit is programmed to logic "1," the Enhanced Mini-ACE RT or Message Monitor considers only subaddress 0 to be a mode code subaddress. Subaddress 31 is treated as a standard non-mode code subaddress. In this configuration, the Enhanced Mini-ACE will consider valid and respond only to mode code commands containing no data words. In this configuration, the Enhanced Mini-ACE RT will consider all mode commands followed by data words to be invalid and will not respond. In addition, if this bit is logic "1," the Enhanced Mini-ACE will not decode for the MIL-STD-1553B "Transmit Status" and "Transmit Last Command" mode codes. As a result, the internal RT Status Word Register will be updated as a result of these commands.

ENHANCED MODE CODE HANDLING (bit 0) : Affects RT mode. If this bit is logic "0" (default), there is no capability to request interrupts to indicate the reception of specific mode code commands. If the bit is logic "0," mode code interrupts may be still enabled globally for transmit and/or receive mode codes, for subaddresses 0 and/or 31. In addition, if ENHANCED MODE CODE HANDLING is logic "0," the Data Words for individual mode codes are all mapped to the same address locations in the shared RAM, for transmit and receive (and broadcast -- optionally separated) subaddresses 0 and 31. Two exceptions involve the Transmit Last Command and Transmit BIT Word mode codes, in which the Data Words are accessed from internal registers.

If ENHANCED MODE CODE HANDLING is logic "1," there is capability to request interrupts to follow the reception of messages containing specific, individual mode commands. Interrupts may be enabled for selected mode codes, as a function of broadcast/own address and the T/R* bit and mode code fields of received mode code messages. This is implemented by means of the mode code selective interrupt table, address locations 0108 through 010F in the shared RAM.

In addition, if ENHANCED MODE CODE HANDLING is logic "1," the Data Words for individual mode codes are mapped as a function of receive/transmit/broadcast and the lower four bits of the mode code field (bit 4 of the mode code field is assumed to be logic "1" for a mode code command with data). If ENHANCED MODE CODE HANDLING is logic "1," address locations 0110 through 013F are allocated to the storage of Data Words for mode code messages.

If ENHANCED MODE CODE HANDLING is logic "0," the RT lookup table pointer to the (single word) Data Word block will be stored in the third word of the RT message descriptor in the RT Command Stack for mode code messages. If ENHANCED MODE CODE HANDLING is logic "1," the received or transmitted data word associated with a mode code message, rather than the pointer to the data word, will be stored in the third location of the message descriptor in the stack. If ENHANCED MODE CODE HANDLING is logic "1," there will be no word stored in the third word of the RT message descriptor for mode code messages with no Data Word.

It should be noted that ENHANCED MODE CODE HANDLING has no effect on the Data Word transmitted in response to a Transmit Last Command mode code. The Data Word in response to this command, representing the previous Command Word received by the RT, is always accessed from an internal register in the Enhanced Mini-ACE and not from a RAM location.

4.16 Configuration Register #4

(Register Address 1000; READ/WRITE)

Table 56. Configuration Register #4 (Read/Write 08H)

BIT	DESCRIPTION
15(MSB)	EXTERNAL BIT WORD ENABLE
14	INHIBIT BIT WORD IF BUSY
13	MODE COMMAND OVERRIDE BUSY
12	EXPANDED BC CONTROL WORD ENABLE
11	BROADCAST MASK ENABLED/XOR*
10	RETRY IF 1553A AND MESSAGE ERROR
9	RETRY IF STATUS SET
8	FIRST RETRY ALT/SAME* BUS
7	SECOND RETRY ALT/SAME* BUS
6	VALID IF MESSAGE ERROR BIT/NO DATA
5	VALID BUSY BIT/NO DATA
4	MONITOR TIME GAP OPTION
3	LATCH RT ADDRESS WITH CFG REG #5
2	TEST MODE 2
1	TEST MODE 1
0(LSB)	TEST MODE 0

NOTE: The Enhanced Mini-ACE must be programmed for its ENHANCED mode (ENHANCED MODE ENABLED, bit 15 of Configuration Register #3 must be logic "1") PRIOR to being able to activate any of the functions enabled by Configuration Register #4.

EXTERNAL BIT WORD ENABLE (bit 15) : Affects RT operation only. If programmed to logic "0," the Enhanced Mini-ACE RT will respond to a Transmit BIT word mode command with the contents of the Enhanced Mini-ACE's internal BIT Word Register as the data word. If programmed to logic "1," the Enhanced Mini-ACE will access the BIT data word from a location in the shared RAM. In the latter instance, the BIT Word must be written to RAM by the host processor.

The location of the BIT Word RAM address location is as follows: if ENHANCED MODE CODE HANDLING, bit 0 of Configuration Register #3, is programmed to logic "0," the BIT Word will be read from the location referenced by the active area lookup table pointer for transmit subaddress 0 or 31. In this configuration, it should be noted that the Data Word in response to a Transmit vector word mode command will be read from the same pair of address locations in which the external BIT Word is stored.

However, if EXTERNAL BIT WORD ENABLE and ENHANCED MODE CODE HANDLING are both programmed to logic "1," the BIT Word will be read from the fixed shared RAM address location 0123.

INHIBIT BIT WORD TRANSMIT IF BUSY (bit 14) : Affects RT operation only. If programmed to logic "0" and either BUSY* (bit 10 of Configuration Register #1) is programmed to logic "0" or if BUSY LOOKUP TABLE (bit 13 of Configuration Register #2) is logic "1" and the respective bit(s) in the Busy lookup table (bit 0 of location 0242 and/or bit 15 of location 0243) is programmed to logic "1," the Enhanced Mini-ACE will respond to a Transmit BIT Word mode command with its RT Status Word with the BUSY bit set, followed by its internal or external Built-in-Test (BIT) Word. If INHIBIT BIT WORD TRANSMIT IF BUSY is programmed to logic "1" and BUSY* is programmed to logic "0" or the appropriate bit in the Busy lookup table is logic "1," the Enhanced Mini-ACE will respond with its RT Status Word with the BUSY bit set, but no Data Word (BIT Word) will be transmitted.

MODE CODE OVERRIDE BUSY (bit 13) : Affects RT operation only. If MODE CODE OVERRIDE BUSY is programmed to logic "0," and BUSY* (bit 10 of Configuration Register #1) is programmed to logic "0" or if BUSY LOOKUP TABLE (bit 13 of Configuration Register #2) is logic "1" and the respective bit(s) in the Busy Lookup Table (bit 0 of location 0242 and/or bit 15 of location 0243) is programmed to logic "1," the Enhanced Mini-ACE will transmit only its Status Word with its BUSY bit set. It will not transmit a following Data Word; in response to either a Transmit Vector Word mode command or a Reserved transmit mode command with data (transmit mode codes 10110 through 11111).

However, if MODE CODE OVERRIDE BUSY is programmed to logic "1," and BUSY* is programmed to logic "0" or if BUSY LOOKUP TABLE (bit 13 of Configuration Register #2) is logic "1" and the respective bit(s) in the Busy Lookup Table (bit 0 of location 0242 and/or bit 15 of location 0243) is programmed to logic "1," the Enhanced Mini-ACE will transmit its Status Word with its BUSY bit set, followed by a single Data Word, in response to either a Transmit Vector Word mode command or a Reserved transmit mode command with data (transmit mode codes 10110 through 11111).

EXPANDED BC CONTROL WORD ENABLE (bit 12) : Affects BC operation only. If either ENHANCED MODE (bit 15 of Configuration Register #3) or EXPANDED BC CONTROL WORD ENABLE is programmed to logic "0," the Enhanced Mini-ACE BC Control Word defaults to that of the BUS-61559 AIM-HY'er. That is, only bits 7, 6, 5, 2, 1, and 0 are active; in this configuration, the functions of the other bits cannot be activated. If both ENHANCED MODE and EXPANDED BC CONTROL WORD ENABLE are programmed to logic "1," then all 15 bits (bits 14 through 0) of the BC Control Word are enabled (may be activated).

BROADCAST MASK ENABLED/XOR* (bit 11) : Affects BC operation only. This bit affects the operation of bit 5 of the BC Control Word, MASK BROADCAST. If BROADCAST MASK ENABLED/XOR* is logic 0 and the MASK BROADCAST bit of the message's BC Control Word is logic "1," the expected value of the Broadcast Command Received Status Word bit becomes "1," rather than "0."

However, if BROADCAST MASK ENA/XOR* is programmed to logic "1," the MASK BROADCAST bit of the BC Control Word is used as a mask bit, rather than performing an "XOR" operation with the Broadcast Received Status Word bit. In this case, a Status Set condition arising from the Broadcast Command Received bit occurs when MASK BROADCAST is logic "0" and the Broadcast Command Received RT Status Word bit is logic "1."

RETRY IF 1553A AND MESSAGE ERROR (bit 10) : This bit affects the operation of BC retries. If programmed to logic "0," BC retries will result from the following conditions: no response timeout, format errors such as incorrect status word address, invalid word, incorrect sync type, low and high word count.

If programmed to logic "1," the BC will also retry as a result of any of the conditions listed above. In addition, a message will also be retried if the 1553A/1553B* bit (bit 3) of the BC Control Word is programmed to logic "1" and the Message Error bit in the RT Status Word is logic "1."

RETRY IF STATUS SET (bit 9) : This bit affects the operation of BC retries. If programmed to logic "0," the BC will not retry a message as a result of one or more bits being set in an RT Status Word; the only exception being that if RETRY IF 1553A AND MESSAGE ERROR (bit 10 of this register) is logic "1," a message will be retried if the 1553A/1553B* bit of the BC Control Word (bit 3) is programmed to logic "1" and the Message Error bit in the RT Status Word is logic "1."

If RETRY IF STATUS SET is programmed to logic "1," the BC will retry a message in which a STATUS SET condition was detected. A STATUS SET condition is defined as follows: If bit 12 of Configuration Register #4, EXPANDED BC CONTROL WORD, is programmed to logic "0," STATUS SET encompasses all 8 of the non-reserved Status Word bits. The expected value for the 8 non-reserved Status Word bits is LOGIC "0," with one exception: If bit 11 of Configuration Register #4, BROADCAST MASK ENA/XOR*, is logic “0” and the MASK BROADCAST bit of the message's BC Control Word is LOGIC "1," the expected value of the Broadcast Command Received bit becomes 1, rather than 0. If BROADCAST MASK ENA/XOR* is programmed to logic "1," the MASK BROADCAST bit of the BC Control Word is used as a mask bit, rather than performing an "XOR" operation with the Broadcast Received Status Word bit; in this instance, a Status Set condition arising from the Broadcast Command Received RT Status bit occurs when the MASK BROADCAST BC Control Word bit is logic "0" and the Broadcast Command Received RT Status Word bit is logic "1."

If EXPANDED BC CONTROL WORD is programmed to logic "1," a STATUS SET condition is defined such that the only bits that can result in a STATUS SET condition are those for which the corresponding bits in the message's BC Control Word have been programmed to logic "0." Status word bits for which the respective mask bits has have been programmed to logic “1” will not result in a status set condition.

FIRST RETRY, SECOND RETRY ALT/SAME* BUS (bits 8,7) : These two bits affect the operation of BC retries. Bit 8 selects the bus on which the first message retry (following the failed initial message) will take place. If bit 8 is logic "0," the first retry will take place on the same bus as the original message. If bit 8 is logic "1," the first retry will take place on the alternate bus from where the message was originally transmitted.

Similarly, bit 7 selects the bus for the second retry attempt. A second retry will be attempted only if DOUBLE/SINGLE* RETRY, bit 3 of Configuration Register #1, has been programmed to logic "1." The second retry will only take place after a first retry has failed. If bit 7 is logic "0," the second retry takes place on the same bus as the original message. If bit 7 is logic "1," the second retry will take place on the alternate bus from where the message was originally transmitted.

VALID IF MESSAGE ERROR BIT/NO DATA (bit 6) : This bit affects the BC validation criteria for RT responses. When this bit is programmed to logic "0," if an RT responds to a transmit command with the Message Error bit set in its Status Word, the response is considered valid only if the Status Word is followed by the requested number of Data Words. In this scenario, a response of Status Word only with Message Error bit set, followed by no Data Words is considered to be a format error.

If programmed to logic "1," an RT response to a transmit command of Status Word with the Message Error bit set followed by the requested number of Data Words is considered a valid response. In addition, in this mode, a response of Status Word with the Message Error bit set followed by no Data Words is also considered a valid response, rather than a format error.

VALID BUSY BIT/NO DATA (bit 5) : This bit affects the BC validation criteria for RT responses. When this bit is programmed to logic "0," if an RT responds to a transmit command with the BUSY bit set in its Status Word, the response is considered valid only if the Status Word is followed by the requested number of Data Words. In this scenario, a response of Status Word only with the BUSY bit set, followed by no Data Words is considered to be a format error.

If programmed to logic "1," an RT response to a transmit command of Status Word with the BUSY bit set followed by the requested number of Data Words is considered a valid response. In addition, in this configuration, a response of Status Word with the BUSY bit set followed by no Data Words is also considered a valid response, rather than a format error.

MONITOR TAG GAP OPTION (bit 4) : This bit affects the operation of the Monitor Identification Word in the Word Monitor mode. Specifically, it affects the operation of the CONTIGUOUS DATA/GAP* bit, the 8-bit GAP TIME field, and the MODE CODE* bit. If programmed to logic "0" and a word is received on the alternate bus from the previous command, the CONTIGUOUS DATA/GAP* bit will be logic "0" (even if the time frame of the current word overlapped that of the previous word) and the GAP TIME field will assume a value of 20 µs greater than the actual time gap (if any) between the end of the previous word on the alternate bus and the start of the current word on the current bus. The operation of the MODE CODE* bit in the tag word will remain unchanged from the older AIM-HY and AIM-HY'ER components, i.e., a Logic "1" indicates that the word is not a mode code while a logic 0 indicates that the word is a mode command.

If MONITOR TAG GAP OPTION is programmed to logic "1" and a word is received on the alternate bus from the previous command within a time frame overlapping that of the previous word, the CONTIGUOUS DATA/GAP* bit will be logic "1" and the GAP TIME field will assume a value of 0. If there is a gap in time between the end of the previous word on the alternate bus and the start of the current word on the same bus, CONTIGUOUS DATA/GAP* will assume a value of logic "0" and the 8-bit GAP TIME field will reflect the correct time between the previous and current words. In this case, it will not be offset (high) by 20 µs.

In addition, if MONITOR TAG GAP OPTION is programmed to logic "1," the MODE CODE* bit in the monitor tag word will change function to signify the occurrence of a DMA Handshake failure. A handshake failure occurs in the transparent/DMA mode when an external arbitration circuit withholds the data transfer grant signal beyond the specified timeout period. When a timeout occurs, the monitored 1553 word and tag word will be lost and the Enhanced Mini-ACE will assert the MODE CODE* bit in the tag word of the next monitored word to indicate that a timeout occurred and a word was lost.

LATCH RT ADDRESS WITH CONFIGURATION REGISTER 5 (bit 3) : This bit, which affects RT mode only, is only applicable if the input signal RT_AD_LAT is connected to logic "1."

This bit affects the capability of the Enhanced Mini-ACE to latch the RT address. The RT address is latched from one of two sources:

1) If RT ADDRESS SOURCE, bit 5 of Configuration Register #6, is programmed to logic "0" (default), then the RT address is latched from the pins RTAD4-RTAD0 and RTADP, by the host processor performing a write cycle to Configuration Register #5. Note that for this write operation, the value of data bus lines D5-D0 is essentially "don't care." That is, the RT address is latched from RTAD4-RTAD0 and RTADP, and not from D5-D0.

2) If RT ADDRESS SOURCE, bit 5 of Configuration Register #6, is programmed to logic “1” then the RT address is latched from the processor data bus signals D5-D0 by writing to Configuration Register #5, and not from the RTAD4-RTAD0 and RTADP pins.

If LATCH RT ADDRESS WITH CONFIG REG 5 is logic "0," writing to Configuration Register #5 has no effect on the value of the internal latched RT address and parity. However, if RT_AD_LAT is logic "1" and the Enhanced Mini-ACE is in ENHANCED mode (bit 15 of Configuration Register #3 = logic “1”) and LATCH RT ADDRESS WITH CONFIG REG 5 is programmed to logic "1," then the RT Address is in the latched mode. In the latched mode, the logic values presented on the inputs RTAD4-RTAD0 and RTADP or D5-D0 (depending on the programmed value of RT ADDRESS SOURCE) will be latched internally when the host processor performs a write operation to Configuration Register #5. It should also be noted that:

If the signal RT_AD_LAT is logic "0," the Enhanced Mini-ACE's RT Address will continuously track the inputs RTAD4-RTAD0 and RTADP.

The signals presented on RTAD4-RTAD0 and RTADP may also be latched on the rising edge of the RT_AD_LAT input.

In ENHANCED mode (bit 15 of Configuration Register #3 = logic “1”), then the current latched values of the Enhanced Mini-ACE's RT Address and RT Address parity (from whatever source) may always be read from bits 5 through 0 of Configuration Register #5.

TEST MODE 2, 1, 0 (bits 2,1,0) : Used for test purposes only. Must be programmed to logic "000" for normal operation. The different test modes are defined as follows for reference only:

Table 57. Test Mode Selection

Configuration Register #4			MODE
Bit 2: TEST MODE 2	Bit 1: TEST MODE 1	Bit 0: TEST MODE 0	
0	0	0	Normal Operation
0	0	1	Decoder Test
0	1	0	Encoder Test
0	1	1	Protocol Test
1	0	0	Failsafe Timer Test
1	0	1	Register Test
1	1	0	RESERVED
1	1	1	Test Mode

4.17 Configuration Register #5

(Register Address 1001; READ/WRITE)

Table 58. Configuration Register #5 (Read/Write 09H)	
BIT	**DESCRIPTION**
15(MSB)	RESERVED
14	SINGLE-ENDED SELECT (read-only)
13	EXTERNAL TX INHIBIT A
12	EXTERNAL TX INHIBIT B
11	EXPANDED CROSSING ENABLED
10	RESPONSE TIMEOUT SELECT 1
9	RESPONSE TIMEOUT SELECT 0
8	GAP CHECK ENABLED
7	BROADCAST DISABLED
6	RT ADDR LATCH/TRANSPARENT*
5	RT ADDRESS 4
4	RT ADDRESS 3
3	RT ADDRESS 2
2	RT ADDRESS 1
1	RT ADDRESS 0
0(LSB)	RT ADDRESS PARITY

Note : The Enhanced Mini-ACE must be programmed for its ENHANCED mode (ENHANCED MODE ENABLED, bit 15 of Configuration Register #3 must be logic "1") PRIOR to being able to activate any of the functions enabled by Configuration Register #5.

RESERVED (bit 15) : No Description

Table 59 illustrates the Enhanced Mini-ACE's methods for clock frequency selection.

Table 59. Clock Frequency Selection

PRODUCT Containing	INPUT SIGNALS			CONFIGURATION REGISTER #6		CLOCK FREQUENCY
	UPADDREN	A15/ CLK_SEL_1	A14/ CLK_SEL_0	CLOCK SELECT 1 (bit 1)	CLOCK SELECT 0 (bit 0)	
64K x 17 RAM	N/A	N/A	N/A	0	0	16 MHz
				0	1	12 MHz
				1	0	20 MHz
				1	1	10 MHz
4K x 16 RAM	0	0	0	X	X	10 MHz
	0	0	1	X	X	20 MHz
	0	1	0	X	X	12 MHz
	0	1	1	X	X	16 MHz
	1	X	X	0	0	16 MHz
	1	X	X	0	1	12 MHz
	1	X	X	1	0	20 MHz
	1	X	X	1	1	10 MHz

NOTE: "N/A" = Not Applicable, "X" = Don't Care.

SINGLE-ENDED SELECT (READ-ONLY) (bit 14) : The Manchester decoders for the BU-61743/61745 RT, and BU-61843/61845/61864/61865 BC/RT/MT Enhanced Mini-ACE (BU-61740B RT, and BU-61840B/61860B BC/RT/MT Micro-ACE), BU-64743/64745 RT, and BU-64843/64845/64863 BC/RT/MT Mini-ACE Mark3 are factory configured for double-ended (MIL-STD-1553 receiver) type of inputs. For these products, SINGLE-ENDED SELECT is a read-only bit, and will always return a value of logic "0."

The Manchester decoders within the BU-64840B/64843B/64860B/64863B BC/RT/MT Micro-ACE-TE and BU-64843T BC/RT/MT Total-ACE are user programmable via input signal "SNGL_END*."

If SNGL_END* is connected to logic "0" the Manchester decoder inputs are configured to accept single-ended input signals (e.g.,MIL-STD-1773 fiber optic receiver outputs). Under this condition, SINGLE-ENDED SELECT is a read-only bit, and will always return a value of logic "1."

If SNGL_END* is connected to logic "1," the decoder inputs will be configured to accept standard double-ended Manchester bi-phase input signals (i.e., MIL-STD-1553 receiver outputs). Under this condition, SINGLE-ENDED SELECT is a read-only bit, and will always return a value of logic "0."

EXTERNAL TX A INHIBIT (READ-ONLY) (bit 13): If this bit is logic "0," this indicates that the input signal TX_INH_A is connected to logic "0" and, therefore, the channel A transceiver is enabled and not externally inhibited. If this bit is logic "1," indicates that TX_INH_A is connected to logic "1." In this instance, the Channel A transmitter is being externally inhibited. There will be no output from the Enhanced Mini-ACE on Bus A if the Channel A transmitter is inhibited. In addition, the Enhanced Mini-ACE will fail its BC off-line self-test if the TX_INH input for the respective channel is connected to logic "1."

EXTERNAL TX B INHIBIT (READ-ONLY) (bit 12) : If this bit is logic "0," this indicates that the input signal TX_INH_B is connected to logic "0" and, therefore, the channel A transceiver is enabled and not externally inhibited. If this bit is logic "1," indicates that TX_INH_B is connected to logic "1." In this instance, the Channel B transmitter is being externally inhibited. There will be no output from the Enhanced Mini-ACE on Bus B if the Channel B transmitter is inhibited. In addition, the Enhanced Mini-ACE will fail its BC off-line self-test if the TX_INH input for the respective channel is connected to logic "1."

EXPANDED ZERO-CROSSING ENABLED (READ/WRITE) (bit 11) : This read/writable bit provides legacy compatibility to the ACE and Mini-ACE (Plus) generations. It defaults to a value of logic “0” and will update to logic “1” if programmed so by the host.

However, it is important to note that the Enhanced Mini-ACE’s Manchester decoders are **always** configured to sample using **both** edges of the clock input CLK_IN. That is, depending on the input clock frequency, the decoder sampling frequency doubles to either 20 (for a 10 MHz clock), 24 (for 12 MHz), 32 (for 16 MHz), or 40 MHz (for 20 MHz). The higher sampling frequency provides improved tolerance (about 30 to 40 ns) to input zero crossing distortion.

RESPONSE TIMEOUT SELECT 1, 0 (READ/WRITE) (bits 10,9) : These two bits are used to select the value of the Enhanced Mini-ACE's response timeout timer. This timer is used in BC mode, for RT mode (for messages in which the Enhanced Mini-ACE is the receiving RT in an RT-to-RT transfer), and in the Message Monitor mode. The four programmable choices (approximate timeout values) are shown in Table 60.

Table 60. Response Timeout Select

BIT 10 RESPONSE TIMEOUT SELECT 1	BIT 9 RESPONSE TIMEOUT SELECT 0	RESPONSE TIMEOUT TIME VALUE (µs)
0	0	18.5
0	1	22.5
1	0	50.5
1	1	130

NOTE: Default value for non-ENHANCED mode is 18.5 µs.

GAP CHECK ENABLED (READ/WRITE) (bit 8) : For MIL-STD-1553B applications it is strongly recommended that this bit be programmed for a value of Logic “0.” If programmed to logic "0," the Enhanced Mini-ACE does not check for a minimum of dead bus time prior the start of transmission by another terminal on the 1553 bus. If programmed to logic "1," the Enhanced Mini-ACE does verify for a minimum of 2 µs of dead bus time prior to the transmission by an external BC or RT on the 1553 bus. If this minimum gap time is violated, the Enhanced Mini-ACE will determine that the BC Command Word or the RT Response (Status Word) is invalid, representing a message format error.

BROADCAST DISABLED (READ/WRITE) (bit 7) : Applicable to RT and Monitor modes. If the BROADCAST DISABLED bit is programmed to logic "0," the Enhanced Mini-ACE will recognize RT Address 31 as the broadcast address. In this configuration, RT Address 31 cannot be used as the Enhanced Mini-ACE's discrete RT Address. If BROADCAST DISABLED is programmed to logic "1," the Enhanced Mini-ACE will not recognize RT Address 31 as the broadcast address. In this instance, RT Address 31 may be used as a discrete RT address.

In Word Monitor mode, bit 5 of the Monitor Identification Word, BROADCAST*, will always return logic "1" (even for a Command Word to RT Address 31) if BROADCAST DISABLED has been programmed to logic "1."

RT ADDRESS LATCH/TRANSPARENT* (READ ONLY) (bit 6) : This bit reflects the logic sense of the input signal RT_AD_LAT. If this bit is logic "0," this indicates that the Enhanced Mini-ACE's internal RT Address signal will continuously track the inputs RTAD4-RTAD0 and RTADP. When a logic "1" level is applied to the RT_AD_LAT input, the Enhanced Mini-ACE’s internal RT address may be optionally latched under software control. In addition, if RT_AD_LAT transitions from logic “0” to logic “1” while MSTCLR* is high, the Enhanced Mini-ACE’s RT address will be latched from the input signals RTAD4-RTAD0 and RTADP on this rising edge.

If LATCH RT ADDRESS WITH CONFIG REG 5 (bit 3 of Configuration Register #4) is set to logic "0,” writing to Configuration Register #5 has no effect on the value of the Enhanced Mini-ACE's RT address and parity. However, if RT_AD_LAT is logic "1,” and both ENHANCED MODE (bit 15 of Configuration Register #3) and LATCH RT ADDRESS WITH CONFIG REG 5 have been programmed to logic "1,” the RT address will be latched internally when the host processor performs a write operation to Configuration Register #5. In this instance, the source of the RT address for this write cycle will be RTAD4-RTAD0 and RTADP pins if RT ADDRESS SOURCE (bit 5 of Configuration Register #6) is logic “0,” or the signals D5-D0 from the host processor data bus if RT ADDRESS SOURCE is logic “1.”

RT ADDRESS 4-0 and RTADP (READ-ONLY; OPTIONALLY READ-WRITE) (bits 5,4,3,2,1,0) : When read, these six bits return the values of the Enhanced Mini-ACE's five internal RT address signals and RT address parity signal. If the parity sum of the internal RTAD4-0 and RTADP signals is even rather than odd, the Enhanced Mini-ACE will not recognize, and therefore not respond to, a Command Word directed to its specific RT address. It will, however, receive messages to the broadcast address (address 31), unless broadcast has been disabled.

If the signal RT_AD_LAT is logic "0," the Enhanced Mini-ACE's internal RT address and RT address parity will continuously track the inputs RTAD4-RTAD0 and RTADP. In this case, the RTAD4 through RTAD0 and RTADP register bits are read-only. That is, if the RT_AD_LAT signal is logic "0," or either of the ENHANCED MODE ENABLE (bit 15 of Configuration Register #3) or LATCH RT ADDRESS WITH CONFIG REG 5 (bit 3 of Configuration Register #4) register bits are logic "0," writing to Configuration Register #5 will have no effect on the value of the internal latched RT Address and address parity.

However, if RT_AD_LAT is logic "1," and both ENHANCED MODE and LATCH RT ADDRESS WITH CONFIG REG 5 have been programmed to logic "1," the Enhanced Mini-ACE's RT address and RT address parity will be latched internally when the host processor performs a write operation to Configuration Register #5. In this case, the source of the RT address for this

Write cycle will be RTAD4-RTAD0 and RTADP if RT ADDRESS SOURCE (bit 5 of Configuration Register #6) is logic "0," or the signals D5-D0 from the host processor data bus if RT ADDRESS SOURCE is logic "1."

4.18 RT/Monitor Data Stack Address

(Register Address 1010; READ/WRITE)

Table 61. RT Monitor Data Stack Address Register (Read/Write0AH)

BIT	DESCRIPTION
15(MSB)	RT/MONITOR DATA STACK ADDRESS 15
• • •	• • •
0(LSB)	RT/MONITOR DATA STACK ADDRESS 0

In RT mode, the pointer word read from the lookup table during the Start-of-Message (SOM) sequence is initially loaded into the Data Stack Address Register. The value of the register is then incremented by one after each successive Data Word accessed to/from the respective Data Word table. If 256-WORD BOUNDARY DISABLE, bit 10 of Configuration Register #2 is logic "0," then the data stack address will roll over at 256-word address boundaries.

In the Word Monitor mode, the Monitor Data Stack Address contains the current value of the Data Stack Pointer. The value of this register is incremented by one after each word written to shared RAM.

In Selective Message Monitor or combined RT/Monitor modes, this register contains the current value of the Monitor Data Stack Pointer. The value of this register is incremented by one (modulo the monitor data stack size) after each word written to the monitor data stack.

4.19 BC Frame Time Remaining

(Register Address 1011; READ ONLY)

In both non-enhanced and enhanced BC modes, the resolution of the BC Frame Time Remaining register is 100ms/LSB, with a maximum value of 6.55 ms.

In the non-enhanced BC mode, this read only register contains the value of the time remaining in the BC frame. In this mode, the frame time is programmed by means of the Non-Enhanced BC Frame Time Register, register address 0D.

In enhanced BC mode, this register contains the value remaining in the BC frame timer. In this mode, the BC frame timer may be loaded by means of the BC Message Sequence Control Engine's Load Frame Counter Register (LFT) instruction, and caused to start running (decrementing) by means of the Start Frame Timer (SFT) instruction.

Table 62 shows the bit mapping of the BC Frame Time Remaining Register.

Table 62. BC Frame Time Remaining Register (Read-Only 0BH)

BIT	DESCRIPTION
15(MSB)	BC FRAME TIME REMAINING 15
• • •	• • •
0(LSB)	BC FRAME TIME REMAINING 0

4.20 BC Message Time Remaining

(Register Address 1100; READ ONLY)

In both non-enhanced and enhanced BC modes, the BC message time remaining register reflects the current value of the time-to-next message timer. In non-enhanced BC mode, this word is programmable as the third word of the message descriptor in the BC stack. In enhanced BC mode, this word is programmable as the fourth word of the BC Control/Status Block.

This timer is programmable with a resolution of 1μs/LSB, and a maximum range of 65.535 ms.

Table 63. BC Message Remaining Register (Read-Only 0CH)	
BIT	**DESCRIPTION**
15(MSB)	BC MESSAGE TIME REMAINING 15
•	•
•	•
•	•
0(LSB)	BC MESSAGE TIME REMAINING 0

4.21 Non-Enhanced BC Frame Time/Enhanced BC Initial Instruction Pointer/RT Last Command/MT Trigger Register

(Register Address 1101; READ/WRITE)

Table 64. BC Frame Time/RT Last Command/Mt Trigger Register (Read/Write 0DH)	
BIT	**DESCRIPTION**
15(MSB)	BIT 15
•	•
•	•
•	•
0(LSB)	BIT 0

In non-enhanced BC mode, the BC frame time, used in the BC AUTO-REPEAT mode, is programmable by means of this register. The value of the BC FRAME TIME is programmable in increments of 100 µs/LSB, up to a maximum of 6.55 seconds. Note that the value of this register does **not** decrement during the processing of a BC frame. Note that the decrementing Or "running" value of remaining BC frame time may be determined by reading register address 0B.

In enhanced BC mode, this register is used for the host to program the initial value of the BC instruction list pointer. Note that the "running" value of the BC instruction list by reading register address 03.

In RT mode, this register stores the Command Word for the current or last message processed by the Enhanced Mini-ACE RT. This register is updated at the beginning of each message processed by the Enhanced Mini-ACE RT.

In Word Monitor mode, this register stores the contents of the Monitor Trigger Word. The host processor must supply this word. When the Enhanced Mini-ACE Word Monitor is on-line, it compares the contents of this register to all valid, received Command Words. The Monitor Trigger mechanism may be used to start the Word Monitor, stop the Word Monitor, or generate interrupt requests. The trigger feature is NOT applicable for the Message Monitor and RT/Message Monitor modes.

4.22 RT Status Word Register

(Register Address 1110; READ ONLY)

Table 65. RT Status Word Register (Shown for MIL-STD-1553B) (Read-Only 0EH)	
BIT	**DESCRIPTION**
15 (MSB)	LOGIC “0”
14	LOGIC “0”
13	LOGIC “0”
12	LOGIC “0”
11	LOGIC “0”
10	MESSAGE ERROR
9	INSTRUMENTATION
8	SERVICE REQUEST
7	RESERVED
6	RESERVED
5	RESERVED
4	BROADCAST COMMAND RECEIVED
3	BUSY
2	SUBSYSTEM FLAG
1	DYNAMIC BUS CONTROL ACCEPT
0 (LSB)	TERMINAL FLAG

4.23 RT Bit Word Register

Table 66. RT BIT Word Register (Read-Only 0FH)	
BIT	**DESCRIPTION**
15(MSB)	TRANSMITTER TIMEOUT
14	LOOP TEST FAILURE B
13	LOOP TEST FAILURE A
12	HANDSHAKE FAILURE
11	TRANSMITTER SHUTDOWN B
10	TRANSMITTER SHUTDOWN A
9	TERMINAL FLAG INHIBITED
8	BIT TEST FAIL
7	HIGH WORD COUNT
6	LOW WORD COUNT
5	INCORRECT SYNC RECEIVED
4	PARITY/MANCHESTER ERROR RECEIVED
3	RT-RT GAP/SYNC/ADDRESS ERROR
2	RT-RT NO RESPONSE ERROR
1	RT-RT 2ND COMMAND WORD ERROR
0(LSB)	COMMAND WORD CONTENTS ERROR

4.24 Block Status Word

In non-enhanced BC, RT, Selective Monitor, and RT/Selective Monitor modes, the Block Status Word is stored in the first location of the Message Block descriptor in the Command Stack. In enhanced BC mode, the block status word is stored in the sixth location of the Control/Status Block. There are two Command Stacks maintained for the RT/Selective Monitor mode: one for the RT, one for the Monitor. There is no Command Stack in the Word Monitor mode. For all modes except Word Monitor, the Block Status Word is updated by the Enhanced Mini-ACE's 1553 memory management logic at both the beginning and at the end of the respective message. It contains information relating to whether the message is in progress or has been completed, what channel it was processed on, and whether or not there were any errors in the message table.

Table 67. BC Mode Block Status Word

BIT	DESCRIPTION
15(MSB)	EOM
14	SOM
13	CHANNEL B/A*
12	ERROR FLAG
11	STATUS SET
10	FORMAT ERROR
9	NO RESPONSE TIMEOUT
8	LOOP TEST FAIL
7	MASKED STATUS SET
6	RETRY COUNT 1
5	RETRY COUNT 0
4	GOOD DATA BLOCK TRANSFER
3	WRONG STATUS ADDRESS/NO GAP
2	WORD COUNT ERROR
1	INCORRECT SYNC TYPE
0(LSB)	INVALID WORD

Note: If a message is retried in BC mode, the bits of the Block Status Word reflect the result of the latest message retry.

Table 68. RT Mode Block Status Word

BIT	DESCRIPTION
15 (MSB)	EOM
14	SOM
13	CHANNEL B/A*
12	ERROR FLAG
11	RT-RT FORMAT
10	FORMAT ERROR
9	NO RESPONSE TIMEOUT
8	LOOP TEST FAIL
7	DATA STACK ROLLOVER
6	ILLEGAL COMMAND WORD
5	WORD COUNT ERROR
4	INCORRECT DATA SYNC
3	INVALID WORD
2	RT-RT GAP/SYNCH/ADDRESS ERROR
1	RT-RT 2ND COMMAND ERROR
0 (LSB)	COMMAND WORD CONTENTS ERROR

Table 69. Message Monitor Mode Block Status Word	
BIT	**DESCRIPTION**
15 (MSB)	EOM
14	SOM
13	CHANNEL B/A*
12	ERROR FLAG
11	RT-RT TRANSFER
10	FORMAT ERROR
9	NO RESPONSE TIMEOUT
8	GOOD DATA BLOCK TRANSFER
7	DATA STACK ROLLOVER
6	RESERVED
5	WORD COUNT ERROR
4	INCORRECT DATA SYNC
3	INVALID WORD
2	RT-RT GAP/SYNCH/ADDRESS ERROR
1	RT-RT 2ND COMMAND ERROR
0 (LSB)	COMMAND WORD CONTENTS ERROR

4.25 Configuration Register #6

(Register Address 11000; READ/WRITE)

Table 70. Configuration Register #6 (Read/Write 18H)	
BIT	**DESCRIPTION**
15 (MSB)	ENHANCED BUS CONTROLLER
14	ENHANCED CPU ACCESS
13	COMMAND STACK POINTER INCREMENT ON EOM (RT, MT)
12	GLOBAL CIRCULAR BUFFER
11	GLOBAL CIRCULAR BUFFER SIZE 2
10	GLOBAL CIRCULAR BUFFER SIZE 1
9	GLOBAL CIRCULAR BUFFER SIZE 0
8	DISABLE INVALID MESSAGES TO INTERRUPT STATUS QUEUE
7	DISABLE VALID MESSAGES TO INTERRUPT STATUS QUEUE
6	INTERRUPT STATUS QUEUE ENABLE *
5	RT ADDRESS SOURCE
4	ENHANCED MESSAGE MONITOR
3	RESERVED
2	64-WORD REGISTER SPACE
1	CLOCK SELECT 1
0(LSB)	CLOCK SELECT 0

Note: **See Appendix "F"** for important information **IF** this bit is enabled (logic "1") **AND** terminal is operating in RT Mode **AND** bits 6, 7 or 14 (Time Tag Rollover, RT Address Parity Error, or RAM Parity Error respectively) of Interrupt Mask Register #1 are enabled (logic "1").

ENHANCED BUS CONTROLLER (bit 15) : If this bit is logic "0" (default), the Enhanced Mini-ACE bus controller operates in its legacy ACE/Mini-ACE(Plus) compatible mode. That is, each message descriptor on the BC stack is four words, and the messages are processed sequentially, in the order of the BC stack descriptors. In the non-enhanced BC mode, the Enhanced Mini-ACE op codes, condition codes, and BC user-defined interrupts are **not** used.

If ENHANCED BUS CONTROLLER is programmed to logic "1," the Enhanced Mini-ACE BC mode is enabled. In this mode, the BC message sequence control processor executes instructions from the BC instruction list. The instruction list consists of pairs of words, including an instruction/op code word, followed by a parameter word. In the enhanced BC mode, BC control/status blocks replace the non-enhanced BC's 4-word stack descriptors. The control/status blocks are comprised of either eight words or, for RT-to-RT transfer messages, ten words. In enhanced BC mode, messages are processed in the order resulting from the execution of the op codes, in accordance with the parameters in the BC Message Sequence Control Block. In the Enhanced BC mode, the condition codes, BC user-defined interrupts, and general-purpose queue **may be** used. **In RT MONITOR MODE this bit must be programmed to a value of logic "0."**

NOTE: For RT and Monitor modes, ENHANCED BUS CONTROLLER MUST be programmed to a value of logic "0."

ENHANCED CPU ACCESS (bit 14) : This bit affects the operation of logic that arbitrates between the host processor and the Enhanced Mini-ACE's internal logic for accessing internal registers and shared RAM. Specifically, it affects the worst case contention (wait state) time for the host processor's access during the Enhanced Mini-ACE's SOM (start-of-message) and EOM (end-of-message) internal transfer sequences; i.e., the time between the host asserting STRBD* low to the Enhanced Mini-ACE asserting IOEN* and READYD* low.

If this bit is logic "0" (default), the arbitration circuitry operates as in the ACE/Mini-ACE. In this configuration, the host must wait for the completion of an entire SOM or EOM sequence before it can complete its access cycle. That is, the host's worst case delay (STRBD* low to IOEN* low), waiting for completion of an internal SOM or EOM sequence, is approximately 74 clock cycles, or 4.6 µs for a 16 MHz clock input.

If this bit is programmed to logic "1," the Enhanced Mini-ACE will allow the host processor to access shared RAM or registers on an interleaving basis, **within** the internal SOM (start-of-message) and/or EOM (end-of-message) transfer sequences. The effect of this is to reduce the worst-case contention time to approximately 9 clock cycles **plus** input setup and output delay times. For a 16 MHz clock, this reduces the maximum value the delay from STRBD*/SELECT* low to IOEN* low to approximately 635 ns.

The worst case STRBD*/SELECT* (low) to READYD* (low) contention delays are shown in Table 71:

Table 71. Worst Case Contention Times			
Clock Input Frequency	**Worst case contention delay for ENHANCED CPU ACCESS = "0"**	**Worst case contention delay for read accesses, with ENHANCED CPU ACCESS = "1"**	**Worst case contention delay for write accesses, with ENHANCED CPU ACCESS = "1"**
16 MHz	4.6 µs	635 ns	570 ns
12 MHz	6.0 µs	820 ns	737 ns
10 MHz	7.2 µs	970 ns	870 ns
20 MHz	3.6 µs	520 ns	470 ns

COMMAND STACK POINTER INCREMENT ON EOM (RT, MT) (bit 13) : This bit is applicable for the Enhanced Mini-ACE's RT, Message Monitor, and combined RT/Monitor modes. It is **not** applicable for BC or Word Monitor modes.

If this bit is programmed to logic "0" (default, Mini-ACE (Plus) compatible), the value of the Command Stack Pointer RAM location will be incremented by four (4) during the message's **SOM** (start-of-message) sequence. If this bit is programmed to logic "1," the value of the Command Stack Pointer will be incremented by four (4) during the message's **EOM** (end-of-message) sequence.

NOTE: For new Enhanced Mini-ACE RT or Message Monitor applications, it is recommended that ENHANCED CPU ACCESS and COMMAND STACK POINTER INCREMENT ON EOM (RT, MT) both be programmed to values of logic "1."

GLOBAL CIRCULAR BUFFER (bit 12) : This bit is applicable for the Enhanced Mini-ACE's RT mode. It is not applicable for the BC and/or Monitor modes. If programmed to logic "1," the RT global circular buffer will be enabled.

If GLOBAL CIRCULAR BUFFER is enabled, the size of the RT global circular buffer is programmed by means of bits 11, 10, and 9 of Configuration Register #6. The use of the global circular buffer may be activated for individual receive (/broadcast) and/or receive subaddresses by means of the respective subaddress control word.

In order to activate the global circular buffer for storage of received data words for a particular Receive(/Broadcast) subaddress, it is necessary to program bit 15 and bits 7, 6, and 5 of the respective Receive (/Broadcast) Subaddress Control Word. If data for broadcast messages is to be separated from non-broadcast received data, it is necessary to program bit 15 and bits 2, 1, and 0 of the respective Broadcast Subaddress Control Word to logic "1."

The pointer for the global circular buffer is located at memory location 101 or 105. If CURRENT AREA B/A* (bit 13 of Configuration Register #1) is logic "0," then the global circular buffer is at location 101. If CURRENT AREA B/A is programmed to logic "1," then the global circular buffer is at location 105.

GLOBAL CIRCULAR BUFFER SIZE 2, 1, and 0 (bits 11,10,9) : If GLOBAL CIRCULAR BUFFER is enabled; the size of the global circular is enabled by bits 11, 10, and 9 of Configuration Register #6, as follows:

Table 72. Global Circular Buffer Size

GLOBAL CIRCULAR BUFFER SIZE 2 (bit 11 of C.R. 6)	GLOBAL CIRCULAR BUFFER SIZE 1 (bit 10 of C.R. 6)	GLOBAL CIRCULAR BUFFER SIZE 0 (bit 9 of C.R. 6)	Global Buffering Scheme	
0	0	0	Single or double message buffer (**not** circular)	
0	0	1	128-Word	Global Circular Buffered of Specified Size (for both Area A and Area B)
0	1	0	256-Word	
0	1	1	512-Word	
1	0	0	1024-Word	
1	0	1	2048-Word	
1	1	0	4096-Word	
1	1	1	8192-Word	

DISABLE INVALID MESSAGES TO INTERRUPT STATUS QUEUE (bit 8) : This bit is only applicable for RT and Message Monitor modes. If INTERRUPT STATUS QUEUE, bit 6 of Configuration Register #6 is programmed to logic "1" **and** INVALID MESSAGES TO INTERRUPT STATUS QUEUE are programmed to logic "0" (default), then invalid received messages that generate interrupt requests **will** result in 2-word entries being stored on the Interrupt Status Queue. If this bit is programmed to logic "1," then there will be **no** queue entries for invalid messages. The Interrupt Status Queue is a 64-word circular buffer. The pointer to this buffer is stored in Interrupt Status Queue Pointer Register (register address 1Fh).

DISABLE VALID MESSAGES TO INTERRUPT STATUS QUEUE (bit 7) : This bit is only applicable for RT and Message Monitor modes. If INTERRUPT STATUS QUEUE, bit 6 of Configuration Register #6 is programmed to logic "1" **and** VALID MESSAGES TO INTERRUPT STATUS QUEUE are programmed to logic "0" (default), then valid received messages that generate interrupt requests **will** result in 2-word entries being stored on the Interrupt Status Queue. If this bit is programmed to logic "1," then there will be **no** queue entries for valid messages. The Interrupt Status Queue is a 64-word circular buffer. The pointer to this buffer is stored in Interrupt Status Queue Pointer Register (register address 1Fh).

INTERRUPT STATUS QUEUE ENABLE (bit 6) : This bit is only applicable for RT and Message Monitor modes. If this bit is logic "1," it enables received messages that generate interrupt requests to result in 2-word entries being stored on the Interrupt Status Queue. The Interrupt Status Queue is a 64-word circular buffer. The pointer to this buffer is stored in the Interrupt Status Queue Pointer Register (register address 1Fh).

See Appendix "F" for important information **IF** this bit is enabled (logic "1") **AND** terminal is operating in RT Mode **AND** bits 6, 7 or 14 (Time Tag Rollover, RT Address Parity Error, or RAM Parity Error respectively) of Interrupt Mask Register #1 are enabled (logic "1").

RT ADDRESS SOURCE (bit 5) : This bit selects the source of the Mini-ACE's RT address. If RT ADDRESS SOURCE is logic "0," the Enhanced Mini-ACE's RT Address is provided by means of the RTAD4-RTAD0 and RTADP input signals. In this configuration, the options for designating RT address are the same as for Enhanced Mini-ACE. That is, the RT address may be either (1) hardwired, if RT_AD_LAT is logic "0"; (2) latched by the "0" to "1" transition of RT_AD_LAT; or (3) if RT_AD_LAT is connected to logic "1" and assuming ENHANCED MODE (bit 15 of Configuration Register #3 set to logic "1"), the RT Address may be latched under software control from the RTAD4-RTAD0 and RADP signals by setting bit 3 of Configuration Register #4, LATCH RT ADDRESS WITH CFG REG #5, to logic "1," and then writing to Configuration Register #5. In this configuration, the RT Address and RT Address Parity may be read from bits 5-1 and bit 0 respectively of Configuration Register #5.

Note : *If the input signal RT_ADDR_LAT is logic "0," then "RT ADDRESS SOURCE (bit 5)" will always be logic "0" (RTAD4-RTAD0 and RTADP inputs, rather than D5-D0, are the source of the RT address) even if the host attempts to program it to logic "1." Thus if RT_ADDR_LAT = "0," then RT ADDRESS SOURCE = "0." Also, if RT_ADDR_LAT = "1" and then RT ADDRESS SOURCE is programmed to "1," RT ADDRESS SOURCE will become "1"…however, if RT_ADDR_LAT subsequently goes to "0," then RT ADDRESS SOURCE will also go to "0" and remain "0." It will only go back to "1" if RT_AD_LAT is brought to "1" and then RT ADDRESS SOURCE is programmed to "1."*

If RT ADDRESS SOURCE is set to logic "1" **and** RT_AD_LAT is connected to logic "1," then the Enhanced Mini-ACE's RT address may be programmed by means of the data bus, with the RT address programmed by means of the processor data bus D5-D1, and RT Address Parity programmed by D0 (rather than RTAD4-RTAD0 and RTADP). In this configuration, the RT address is software programmable by: (1) setting ENHANCED MODE, bit 15 of Configuration Register #3 to logic "1"; then, (2) setting bit 3 of Configuration Register #4, LATCH RT ADDRESS WITH CFG REG #5, to logic "1," and then (3) writing the value of the RT address (bits 5-1) and RT address parity (bit 0) to the lower six bits of Configuration Register #5. The RT address may also be read and verified by means of Configuration Register #5 at any time.

ENHANCED MESSAGE MONITOR (bit 4) : For the combined RT/Monitor mode, if this bit is logic "0," then receipt of the RT's status word will prompt the monitor logic to access the Selective Monitor lookup table, to determine whether the word represents the command word for a message that the selective monitor will store. Since the RT status word contains the RT's own address, normally the corresponding entry in the Selective Monitor Lookup Table will be programmed to logic "0," in which case the monitor will **not** attempt to store such a "command word" and any accompanying data words.

However, if this lookup table bit has been programmed to logic "1," then the Message Monitor will interpret the RT's status word as a command word. In this case, it will create a new entry on the Command Stack (including the "command" (status) word); in addition, any accompanying data words will be stored on the Monitor Data Stack. If the Enhanced Mini-ACE then receives a new command to its own RT address within 14 μs after the status word (or the last accompanying data word), this will be interpreted as the "status" word for the new message.

If ENHANCED MESSAGE MONITOR is logic "1," then receipt of the RT's status word will **not** prompt the monitor logic to access the Selective Monitor lookup table, to determine whether the word represents a command word for a message that the monitor will store. Therefore, the RT's own status word will **never** be considered a "command word" that could potentially result in the monitor storing (part of) a message sent by the Enhanced Mini-ACE RT.

For new applications of the RT/MT mode, it is recommended that ENHANCED MESSAGE MONITOR be programmed for a value of logic "1."

RESERVED (bit 3)

64-WORD REGISTER SPACE (bit 2) : If this bit is logic "0," then only register addresses 00h through 1Fh will be decoded as valid registers by the Enhance Mini-ACE. In terms of register address mapping, this configuration is compatible to Mini-ACE (Plus).

If 64-WORD ADDRESS SPACE is programmed to logic "1," then the Enhanced Mini-ACE decodes register addresses 20h through 3Fh as valid internal register addresses (many of the Enhanced Mini-ACE test registers are located above register address 1Fh).

In general, there is no user need to access the test registers. Therefore, this bit should normally be programmed to a value of logic "0."

CLOCK SELECT 1, CLOCK SELECT 0 (bits 1,0) : These two bits are used to specify the frequency of the Enhanced Mini-ACE's clock input. Note that for versions of the Enhanced Mini-ACE with 4K of internal RAM, the clock frequency may be designated by means of hardwired input signals. That is, if the input signal UPADDREN is connected to logic "0," the address signal A15 becomes CLK_SEL_1, and the address signal A14 becomes CLK_SEL_0. In this configuration, the clock frequency is designated by the hardwiring of CLK_SEL_1 and CLK_SEL_0. Note that for this hardwired configuration, it is necessary to connect CLK_SEL_1 and CLK_SEL_0 to the **inverse** of the values indicated in **Error! Reference source not found.**. The values indicated in **Error! Reference source not found.** are only applicable for specifying the clock frequency via Configuration Register 6.

For Enhanced Mini-ACE devices with 64K x 17 RAM, or for Enhanced Mini-ACE devices with 4K x 16 RAM with UPADDREN connected to logic "1," the clock frequency is designated by software, according to **Error! Reference source not found.**.

Table 73. Clock Frequency Selection

Configuration Register #6		Clock Frequency
Clock Select 1 (bit 1)	Clock Select 0 (bit 0)	
0	0	16 MHz (default, see **NOTE**)
0	1	12 MHz
1	0	20 MHz
1	1	10 MHz

NOTE: Programming CLOCK SELECT1 = CLOCK SELECT0 = "0" provides compatibility to Mini-ACE (Plus), by allowing the clock frequency to be designated as either 16 MHz or 12 MHz, by means of bit 15 of Configuration Register #5. In this case, a logic "0" (default) for Configuration Register 5 bit 15 specifies 16 MHz, while a logic "1" specifies 12 MHz.

4.26 Configuration Register #7

(Register Address 11001; READ/WRITE)

Table 74. Configuration Register #7 (Read/Write 19H)

BIT	DESCRIPTION
15(MSB)	MEMORY MANAGEMENT BASE ADDRESS 15
14	MEMORY MANAGEMENT BASE ADDRESS 14
13	MEMORY MANAGEMENT BASE ADDRESS 13
12	MEMORY MANAGEMENT BASE ADDRESS 12
11	MEMORY MANAGEMENT BASE ADDRESS 11
10	MEMORY MANAGEMENT BASE ADDRESS 10
9	RESERVED
8	RESERVED
7	RESERVED
6	RESERVED
5	RESERVED
4	RT HALT ENABLE
3	1553B RESPONSE TIME
2	ENHANCED TIME TAG SYNCHRONIZE
1	ENHANCED BC WATCHDOG TIMER ENABLED
0 (LSB)	MODE CODE RESET/INCMD* SELECT

MEMORY MANAGEMENT BASE ADDRESS 15-10 (bits 15,14,13,12,11,10) : These bits provide a mechanism for relocating the area of the shared RAM addresses that are allocated for storage of the BC's or RT's pointers, counters, tables, and other "non-message" data structures. This provides a means for multiple Enhanced Mini-ACEs that are connected using the DMA host processor interface configuration to be able to share a common 64K word area of host RAM. To provide backwards compatibility to ACE and Mini-ACE (Plus), the default for the "non-data" area of memory remains 0000h-03FFh.; that is, these 6 register bits default to a value of 000000. To relocate the "non-data" area of RAM for a specific Enhanced Mini-ACE, it is necessary to program a different set of different values for MEMORY MANAGEMENT BASE ADDRESS 15-10.

RESERVED (bits 9,8,7,6,5) : These bits must be programmed to logic "0," to allow for future use.

RT HALT ENABLE (bit 4) : This bit provides a software mechanism for enabling the Enhanced Mini-ACE RT to be automatically taken offline, for the purpose of running the autonomous built-in protocol self-test. If this bit has been programmed to a value of logic "1," then receipt of an Initiate self-test mode command will result in the RT going "offline"; that is, the RT will revert to either BC mode for BC/RT/MT devices or "Idle" mode for RT only devices and will **not** respond to any messages received. At this time, the host may initiate the built-in protocol self-test, by writing logic "1" to bit 7 (INITIATE PROTOCOL SELF-TEST) of the Start/Reset Register. When the protocol self-test completes, the RT will automatically revert back to its online state, and resume responding to commands received on the 1553 bus.

Following receipt of an Initiate self-test mode code, resulting in the RT going offline, the host processor has the option of bringing the RT back online ***without*** **running the self-test** by programming a value of logic "1" to bit 11 (CLEAR RT HALT) of the

Start/Reset Register. Note that if this action is taken, the value of RT HALT will **not** be affected; i.e., it will remain as logic "1."

1553B RESPONSE TIME* (bit 3) : For the DMA host processor configuration, this bit controls the maximum DMA request-to-grant time. If 1553B RESPONSE TIME is logic "0" (default), the maximum request-to-grant time is 8 µs. If 1553B RESPONSE TIME is programmed to logic "1," the maximum request-to-grant time increases to 10 µs. For a MIL-STD-1553A RT application, in order to ensure that the Enhanced Mini-ACE meets the maximum response time requirement for -1553A of 5 µs (dead time), it is necessary to program 1553B RESPONSE TIME for a value of logic "0."

ENHANCED TIME TAG SYNCHRONIZE (bit 2) : This feature provides flexibility for using the 1553 Synchronize (with data) mode code. For RT mode, the data word received for a Synchronize (with data) mode command will be loaded to the Time Tag Register, if LOAD TIME TAG ON SYNCHRONIZE (bit 5 of Configuration Register #2) is programmed to logic "1." In this case, if ENHANCED TIME TAG SYNCHRONIZE is also programmed to logic "1," the Enhanced Mini-ACE RT will load the received data word for a received Synchronize (with data) mode code **only** if the LSB of the received data word is logic "0."

In BC mode, if ENHANCED TIME TAG SYNCHRONIZE is programmed to logic "1" and LOAD TIME TAG FOR SYNCHRONIZE (bit 5 of Configuration Register #2) **and** TRANSMIT TIMETAG FOR SYNCHRONIZE MODE COMMAND, Bit 15 of the BC Control Word, are programmed to logic "1," the Enhanced Mini-ACE BC will be enabled to transmit the value of its Time Tag Register as the data word for a Synchronize (with data) mode code.

ENHANCED BC WATCHDOG TIMER ENABLED (bit 1) : For the Enhanced BC mode, if this bit is programmed to logic "1," the BC will set BC EOF (bit 3) of Interrupt Status Reg. #1 and generate interrupt if bit 3 of Interrupt Mask register is set, following an expiration of the BC Frame Timer.

In order to use this feature, it is necessary to periodically reload the Frame Time Register by means of a Load Frame Time Register (LFT) instruction in the message sequence control block. The value programmed for the Frame Timer must be sufficient to allow for the worst-case BC frame time, allowing for message retries. The watchdog timer provides a failsafe mechanism for such faults as the message sequence control block getting stuck in a loop without re-loading the frame timer, or branching to an incorrect thread.

MODE CODE RESET/INCMD* SELECT (bit 0) : The pin INCMD*/MCRST* may be programmed to function as either of two output signals: INCMD* (In-command) or MCRST* (mode code reset). If this register bit is logic "0" (default), INCMD* will be active on this pin; if the bit is logic "1," MCRST* will be active. INCMD* is asserted low to frame the time that a message is being processed by the Enhanced Mini-ACE BC, RT, or Monitor. In RT mode, MCRST* is asserted low for two clock cycles following receipt of a Reset remote terminal mode command.

4.27 BC Condition Code Register

(Register Address 11011; READ-ONLY)

Table 75. BC Condition Code Register (Read-Only 1BH)	
BIT	**DESCRIPTION**
15 (MSB)	LOGIC "1"
14	RETRY 1
13	RETRY 0
12	BAD MESSAGE
11	MASKED STATUS SET
10	GOOD BLOCK TRANSFER
9	FORMAT ERROR
8	NO RESPONSE
7	GENERAL PURPOSE FLAG 7
6	GENERAL PURPOSE FLAG 6
5	GENERAL PURPOSE FLAG 5
4	GENERAL PURPOSE FLAG 4
3	GENERAL PURPOSE FLAG 3
2	GENERAL PURPOSE FLAG 2
1	EQUAL FLAG/GENERAL PURPOSE FLAG 1
0 (LSB)	LESS THAN/GENERAL PURPOSE FLAG 0

Note: If the Enhanced Mini-ACE is not online (i.e., processing instructions) in enhanced BC Mode, the BC Condition Code Register will always return a value of 0000.

The BC Condition Code Register is a read-only register, which is only applicable in the enhanced BC mode. With the exception of bit 15, which when the enhanced BC is running, will always return a logic "1" when read, the upper 8 bits reflect the result of the last message processed by the BC. The lower 8 bits of this register are general-purpose flag bits, which may be set, cleared, or toggled by the host, by means of the BC General Purpose Flag Register; **or** by the BC Message Sequence Processor, by means of the GP Flag Bits (FLG) instruction. In addition, the lower two bits (bits 1 and 0) may also be set or cleared by the BC Message Sequence Control Processor, by means of the Compare to Frame Timer (CFT) or Compare to Message Timer (CMT) instructions.

LOGIC "1" (bit 15) : This bit will always return a value of logic "1" when the enhanced BC is running. Will return a value of logic "0" if BC is not running.

RETRY1 and RETRY0 (bits 14,13) : These two bits reflect the retry status of the most recent message. The number of times that the message was retried is delineated by these two bits as shown in Table 76 :

Table 76. Number Of Message Retries		
RETRY COUNT 1 (bit 14)	**RETRY COUNT 0 (bit 13)**	**Number of Message Retries**
0	0	0
0	1	1
1	0	N/A
1	1	2

BAD MESSAGE (bit 12) : If this bit is high, this indicates either a format error, loop test fail, or no response error for the most recent message.

MASKED STATUS SET (bit 11) : This bit will be set if one or both of the following conditions have occurred on the most recent message: (1) If one (or more) of the Status Mask bits (14 through 9) in the BC Control Word is logic **"0" and** the corresponding bit(s) is (are) set (logic "1") in the received RT Status Word. In the case of the RESERVED BITS MASK (bit 9) set to logic "0," any or all of the 3 Reserved status word bits being set will result in a MASKED STATUS SET condition; **and/or** (2) If BROADCAST MASK ENABLED/XOR* (bit 11 of Configuration Register #4) is logic "0" **and** the logic sense of the MASK BROADCAST bit of the message's BC Control Word and the BROADCAST COMMAND RECEIVED bit in the received RT Status Word are **opposite**; **or** (3) If BROADCAST MASK ENABLED/XOR* (bit 11 of Configuration Register #4) is logic "1" **and** the MASK BROADCAST bit of the message's BC Control Word is logic "0" **and** the BROADCAST COMMAND RECEIVED bit in the received RT Status Word is logic "1."

Table 77 summarizes the operation of the MASKED STATUS SET bit.

Table 77. Operation Of Masked Status Set Condition

BROADCAST MASK ENABLED/XOR* (bit 11 of Configuration Register #4)	Respective "MASK" bit (bits 14-9) in BC Control Word (see Note (1))	MASK BROADCAST bit (bit 5) in BC Control Word	RT Status Word Bit	Will this status word bit contribute to a MASKED STATUS SET condition?
X	0	X	0	No
X	0	X	1	Yes
X	1	X	X	No
0	X	0	0	No
0	X	0	1	Yes
0	X	1	0	Yes
0	X	1	1	No
1	X	0	0	No
1	X	0	1	Yes
1	X	1	X	No

NOTES:

(1) This column is applicable to the MESSAGE ERROR, SERVICE REQUEST, BUSY, SUBSYSTEM FLAG, 3 RESERVED, and TERMINAL FLAG mask bits and status word bits, but not to the BROADCAST COMMAND RECEIVED bit.

(2) "X" = don't care.

GOOD BLOCK TRANSFER (bit 10) : For the most recent message, this bit will be set to logic "1" following completion of a valid (error-free) RT-to-BC transfer, RT-to-RT transfer, or transmit mode code with data message. This bit is set to logic "0" following an invalid message. GOOD DATA BLOCK TRANSFER is always logic "0" following a BC-to-RT transfer, a mode code message with data, or a mode code message without data. The Loop Test has no effect on GOOD DATA BLOCK TRANSFER. The GOOD DATA BLOCK TRANSFER bit may be used to determine if the transmitting portion of an RT-to-RT transfer was error free. An RT-to-RT transfer with both the ERROR FLAG and GOOD BLOCK TRANSFER bits set in Block Status Word indicates that the transmitting RT responded correctly, but there was an error detected in the receiving portion of the message.

FORMAT ERROR (bit 9) : If this bit is logic “1,” this indicates that the received portion of the most recent message contained one or more violations of the 1553 message validation criteria (sync, encoding, parity, bit count, word count, etc.), or the status word received from a responding RT contained an incorrect RT address field.

NO RESPONSE (bit 8) : If this bit is logic “1,” this indicates that an RT has either not responded or has responded later than the BC No Response Timeout time. The Enhanced Mini-ACE's No Response Timeout Time is defined per MIL-STD-1553B as the time from the mid-bit crossing of the parity bit to the mid-sync crossing of the RT Status Word. The value of the No Response Timeout value is programmable from among the values 18.5, 22.5, 50.5, and 130 μs (±1 μs) by means of bits 10 and 9 of Configuration Register #5.

GENERAL PURPOSE FLAGS 7-2 (bits 7,6,5,4,3,2) : The interpretation of these flag bits is user-defined. These bits are set, cleared, or toggled autonomously by the BC, by means of the FLG (Set/Clear bits) instruction; and/or by host processor, by means of the BC General Purpose Flag Register.

EQUAL FLAG/GENERAL PURPOSE FLAG 1 (bit 1) : This bit may be set or cleared by means of the BC, following execution of a CFT (Compare to Frame Time Counter) or CMT (Compare to Message Time Counter) operation. In addition, this bit may be set, cleared, or toggled autonomously by the BC, by means of the FLG (Set/Clear bits) instruction; and/or by host processor, by means of the BC General Purpose Flag Register.

LESS THAN FLAG/GENERAL PURPOSE FLAG 0 (bit 0) : This bit may be set or cleared by means of the BC, following execution of a CFT (Compare to Frame Time Counter) or CMT (Compare to Message Time Counter) operation. In addition, this bit may be set, cleared, or toggled autonomously by the BC, by means of the FLG (Set/Clear bits) instruction; and/or by host processor, by means of the BC General Purpose Flag Register.

4.28 BC General Purpose Flag Register

(Register Address 11011; READ/WRITE)

Table 78. BC General Purpose Flag Register (Write-Only 1BH)	
BIT	**DESCRIPTION**
15 (MSB)	CLEAR GENERAL PURPOSE FLAG 7
14	CLEAR GENERAL PURPOSE FLAG 6
13	CLEAR GENERAL PURPOSE FLAG 5
12	CLEAR GENERAL PURPOSE FLAG 4
11	CLEAR GENERAL PURPOSE FLAG 3
10	CLEAR GENERAL PURPOSE FLAG 2
9	CLEAR GENERAL PURPOSE FLAG 1
8	CLEAR GENERAL PURPOSE FLAG 0
7	SET GENERAL PURPOSE FLAG 7
6	SET GENERAL PURPOSE FLAG 6
5	SET GENERAL PURPOSE FLAG 5
4	SET GENERAL PURPOSE FLAG 4
3	SET GENERAL PURPOSE FLAG 3
2	SET GENERAL PURPOSE FLAG 2
1	SET GENERAL PURPOSE FLAG 1
0 (LSB)	SET GENERAL PURPOSE FLAG 0

In the Enhanced Mini-ACE's enhanced BC mode, the BC General Purpose Flag Register may be used to set, clear, or toggle any of the eight general-purpose flags. Table 79 illustrates the use of the General Purpose Flag Register for the case of GP0 (General Purpose Flag 0):

Table 79. Control Of General Purpose Flag Bits		
BIT 8	**BIT 0**	**EFFECT ON GP0**
0	0	NO CHANGE
0	1	SET FLAG
1	0	CLEAR FLAG
1	1	TOGGLE FLAG

4.29 Bit Test Status Register

(Register Address 11100; READ ONLY)

Table 80. BIT Test Status Register (Read-Only 1CH)	
BIT	**DESCRIPTION**
15 (MSB)	PROTOCOL BUILT-IN TEST COMPLETE
14	PROTOCOL BUILT-IN TEST IN PROGRESS
13	PROTOCOL BUILT-IN TEST PASSED
12	PROTOCOL BUILT IN TEST ABORT
11	PROTOCOL BUILT-IN TEST IN PROGRESS OR COMPLETE
10	LOGIC “0”
9	LOGIC “0”
8	LOGIC “0”
7	RAM BUILT-IN TEST COMPLETE
6	RAM BUILT-IN TEST IN PROGRESS
5	RAM BUILT-IN TEST PASSED
4	LOGIC “0”
3	LOGIC “0”
2	LOGIC “0”
1	LOGIC “0”
0 (LSB)	LOGIC “0”

The BIT Test Status Register may be read during or after protocol or RAM self-test to determine the status and results of the test. The Enhanced Mini-ACE will automatically perform its protocol self-test after MSTCLR* goes high following power turn-on. Note that after the host has initiated the protocol or RAM self-test and the test is still running, that the host may read any RAM or register location (including the BIT Test Status Register), and this will have **no effect** on the self-test. However, if the host writes any RAM or register location during self-test, this will cause the self-test to abort, and result in a software reset of the Enhanced Mini-ACE.

PROTOCOL BUILT-IN TEST COMPLETE (bit 15) : Following power turn-on and MSTCLR* going high, this bit initializes to a value of logic “0.” Normally, it will change to logic “1” after the Enhanced Mini-ACE completes its power turn-on protocol self-test. It will remain at logic “1” until a value of logic “1” is written to CLEAR SELF-TEST REGISTER, bit 10 of the Start/Reset register, or until the host initiates a subsequent protocol self-test. PROTOCOL SELF-TEST COMPLETE will clear to a value of logic “0” at the start of the new self-test.

PROTOCOL BUILT-IN-TEST IN PROGRESS (bit 14) : If this bit is logic “1,” it indicates that the Enhanced Mini-ACE is currently running its protocol self-test. This bit will clear to logic “0” upon completion of the test. If this bit persists in returning a value of logic “1” after the time that the test should have been completed (e.g., after more than 2.0 ms following the initiation of the test, assuming a 16 MHz clock input - reference Table 1), then the test has probably hung. This indicates a likely problem in the Enhanced Mini-ACE’s internal self-test logic.

PROTOCOL BUILT-IN TEST PASSED (bit 13) : If this bit is logic "1," this indicates that the built-in protocol self-test has passed. This bit will remain logic "1" until a value of logic "1" has been written to CLEAR SELF-TEST REGISTER, or the host initiates a subsequent protocol self-test. The start of a subsequent protocol self-test clears PROTOCOL BUILT-IN TEST PASSED to "0."

PROTOCOL BUILT-IN TEST ABORT (bit 12) : This bit indicates that the protocol self-test has been terminated. The self-test will immediately abort if the host processor writes to any Enhanced Mini-ACE registers or RAM while the protocol self-test is being performed.

PROTOCOL BUILT-IN TEST PROGRESS OR COMPLETE (bit 11) : Following hardware reset (MSTCLR* low), this bit initializes to logic "0." However, when the power turn-on protocol self-test begins, PROTOCOL BUILT-IN TEST IN PROGRESS OR COMPLETE transitions to logic "1," and remains at logic "1" after the test completes. It **is** cleared to logic "0" by clearing the BIT Test Status Register, by means of CLEAR SELF-TEST REGISTER. Otherwise, it will stay at logic "1." If cleared to "0," it will go back to "1" after another protocol self-test is initiated. PROTOCOL BUILT-IN TEST IN PROGRESS OR COMPLETE is **not** cleared to "0" by software reset.

RAM BUILT-IN TEST COMPLETED (bit 7) : If this bit is logic "1," this indicates that the RAM self-test has completed. Following power turn-on and MSTCLR* going high, this bit initializes to a value of logic "0." It will return a value of "0" while a RAM self-test is being performed, and will only return logic "1" following completion of the RAM self-test. The host may clear this bit by writing logic "1" to CLEAR SELF-TEST REGISTER, or by initiating a subsequent RAM self-test.

RAM BUILT-IN-TEST IN PROGRESS (bit 6) : If this bit is logic "1," it indicates that the Enhanced Mini-ACE is currently running its built-in RAM self-test. This bit will clear to logic "0" upon completion of the test. If this bit persists in returning a value of logic "1" after the time that the test should have been completed (e.g., after more than 2.6 ms following the initiation of the test, assuming a 4K RAM Enhanced Mini-ACE and a 16 MHz clock input - reference Table 1), then the test has probably hung. This indicates a likely problem in the Enhanced Mini-ACE's internal self-test logic.

RAM BUILT-IN TEST PASSED (bit 5) : If this bit is logic "1," this indicates that the built-in RAM self-test has completed and passed. This bit will remain logic "1" until a value of logic "1" has been written to CLEAR SELF-TEST REGISTER, or the host initiates a subsequent RAM self-test. The start of a subsequent RAM self-test clears RAM BUILT-IN TEST PASSED to "0."

4.30 Interrupt Mask Register #2

(Register Address 11101; READ/WRITE)

Table 81. Interrupt Mask Register #2 (Read/Write 1DH)

BIT	DESCRIPTION
15 (MSB)	NOT USED
14	BC OP CODE PARITY ERROR
13	RT ILLEGAL COMMAND/MESSAGE MONITOR MESSAGE RECEIVED
12	GENERAL PURPOSE QUEUE/INTERRUPT STATUS QUEUE ROLLOVER
11	CALL STACK POINTER REGISTER ERROR
10	BC TRAP OP CODE
9	RT COMMAND STACK 50% ROLLOVER
8	RT CIRCULAR BUFFER 50% ROLLOVER
7	MONITOR COMMAND STACK 50% ROLLOVER
6	MONITOR DATA STACK 50% ROLLOVER
5	ENHANCED BC IRQ3
4	ENHANCED BC IRQ2
3	ENHANCED BC IRQ1
2	ENHANCED BC IRQ0
1	BIT TEST COMPLETE
0 (LSB)	NOT USED

4.31 Interrupt Status Register #2

(Register Address 11110; READ ONLY)

Table 82. Interrupt Status Register #2 (Read-Only 1EH)

BIT	DESCRIPTION
15 (MSB)	MASTER INTERRUPT
14	BC OP CODE PARITY ERROR
13	RT ILLEGAL COMMAND/MESSAGE MONITOR MESSAGE RECEIVED
12	GENERAL PURPOSE QUEUE/INTERRUPT STATUS QUEUE ROLLOVER
11	CALL STACK POINTER REGISTER ERROR
10	BC TRAP OP CODE
9	BC/RT COMMAND STACK 50% ROLLOVER (applicable for non-Enhanced BC only)
8	RT CIRCULAR BUFFER 50% ROLLOVER
7	MONITOR COMMAND STACK 50% ROLLOVER
6	MONITOR DATA STACK 50% ROLLOVER
5	ENHANCED BC IRQ3
4	ENHANCED BC IRQ2
3	ENHANCED BC IRQ1
2	ENHANCED BC IRQ0
1	BIT TEST COMPLETE
0 (LSB)	INTERRUPT CHAIN BIT

Master Interrupt (bit 15) : For Interrupt Status Register #2, this bit indicates that one or more if the interrupt events indicated by bits 14 through 0 (including bit 0, INTERRUPT CHAIN BIT) of Interrupt Request Register #2, has occurred. Note that for Interrupt Mask Register #2, this bit is not used.

BC OP CODE PARITY ERROR (bit 14) : For the enhanced BC mode, this bit indicates that the op code word for a BC instruction failed its parity check. The parity check verifies that there is an odd number of logic “1”s among the parity bit (bit 15) and bits 14-0. Note that if this interrupt event occurs, that a BC TRAP OP CODE event will also have occurred.

RT ILLEGAL COMMAND/MESSAGE MONITOR MESSAGE RECEIVED (bit 13) : For RT mode, this bit indicates that a message containing a command word that has been illegalized by means of the illegalizing table has been received. For Message Monitor Mode, this bit indicates that a message has been received and stored by the selective monitor. This bit has no function for BC or Word Monitor Modes.

GENERAL PURPOSE QUEUE/INTERRUPT STATUS QUEUE ROLLOVER(bit 12) : In enhanced BC mode, this bit indicates that the General Purpose Queue has rolled over. The General Purpose Queue rolls over at address boundaries of modulo 64. This bit has no function in the non-enhanced BC mode.

In RT or Message Monitor modes, this bit indicates that the Interrupt Status Queue has rolled over. The Interrupt Status Queue rolls over at address boundaries, which have an exact modulo of 64.

CALL STACK POINTER REGISTER ERROR (bit 11) : For the enhanced BC mode, this bit indicates that there has been a violation of the BC's subroutine stack depth. This occurs for either: (1) a call stack overflow condition; or (2) a call stack underflow condition.

The call stack depth increases by one each time the BC invokes a CAL (Subroutine Call) instruction, and decreases by one each time the BC invokes a RTN (Subroutine Return) instruction. The minimum call depth is zero, while maximum call stack depth is four. If the call stack depth is already four, a subsequent CAL instruction will result in a Call Stack Pointer Register Error. Similarly, if the call stack depth is zero, a subsequent RTN instruction will also result in a Call Stack Register Error.

BC TRAP (bit 10) : For the enhanced bus controller mode, this bit indicates that the BC has fetched an illegal op code. This halts the BC's operation following the completion of the current message.

An illegal op code is one that is not defined, fails its parity check (bit 15), and/or has an incorrect value for one or more of bits 9 through 5.

A BC watchdog timeout occurs when bit 1 of Configuration Register #7, ENHANCED BC WATCHDOG TIMER ENABLED, is logic "1" and the BC frame timer, which is under control of the BC Message Sequence Processor, has timed out.

RT COMMAND STACK 50% ROLLOVER (bit 9) : For RT mode, this bit indicates that the RT descriptor stack (command stack) pointer has crossed an address boundary which is an exact multiple of half of the programmed value of the Command Stack size. If the stack pointer was initialized at an address that is an exact multiple of its programmed size, then this interrupt will indicate that the stack is half full.

The timing for this interrupt request depends on the programming of COMMAND STACK POINTER INCREMENT ON EOM, bit 13 of Configuration Register #6. If COMMAND STACK POINTER INCREMENT ON EOM is logic "0" (default), then the command stack 50% rollover interrupt will occur during the SOM (start-of-message) sequence for the message in which the 50% rollover occurred, which occurs following receipt of the command word. However, if COMMAND STACK POINTER INCREMENT ON EOM has been programmed to logic "1," then the command stack 50% rollover interrupt will occur at the end of the EOM (END-of-message) sequence, for the message in which the value of the stack pointer incremented past the 50% point of the command stack. The "50% rollover" address will be an exact multiple of half of the programmed stack size.

RT CIRCULAR BUFFER 50% ROLLOVER (bit 8) : For RT mode, this bit indicates that an RT circular buffer – either for an individual transmit, receive (/broadcast), or broadcast subaddress, or the global circular buffer - has crossed an address boundary which is an exact multiple of half of the programmed value of the circular buffer size. If the circular buffer lookup table pointer was initialized at an address that is an exact multiple of its programmed size, then this interrupt will indicate that the stack is half full. Note that this interrupt will occur at the end of the message in which the 50% rollover occurred.

MONITOR COMMAND STACK 50% ROLLOVER (bit 7) : For Selective Monitor mode, this bit indicates that the Monitor descriptor stack (command stack) pointer has crossed an address boundary which is an exact multiple of half of the programmed value of the Monitor Command Stack size. If the command stack pointer was initialized at an address, which is an exact multiple of its programmed size, then this interrupt will indicate that the command stack is half full.

The timing for this interrupt request depends on the programming of COMMAND STACK POINTER INCREMENT ON EOM, bit 13 of Configuration Register #6. If COMMAND STACK POINTER INCREMENT ON EOM is logic "0" (default), then the command stack 50% rollover interrupt will occur during the SOM (start-of-message) sequence for the message in which the 50% rollover occurred, which occurs following receipt of the command word. However, if COMMAND STACK POINTER INCREMENT ON EOM has been programmed to logic "1," then the command stack 50% rollover interrupt will occur at the end of the EOM (END-of-message) sequence, for the message in which the value of the stack pointer incremented past the 50% point of the command stack. The “50% rollover” address will be an exact multiple of half of the programmed stack size.

MONITOR DATA STACK 50% ROLLOVER (bit 6) : For Selective Monitor mode, this bit indicates that the Monitor data stack pointer has crossed an address boundary which is an exact multiple of half of the programmed value of the Monitor Data Stack size. If the data stack pointer was initialized at an address, which is an exact multiple of its programmed size, then this interrupt will indicate that the data stack is half full. Note that this interrupt will occur at the end of the message in which the 50% rollover occurred.

ENHANCED BC INTERRUPT REQUEST 3-0 (bits 5,4,3,2) : These four interrupts are only applicable for the Enhanced Bus Controller mode. They are issued as the result of an IRQ (Generate Interrupt) instruction by the Enhanced BC. The bit pattern of these four bits will be equal to the value of the lower 4 bits of the parameter associated with the IRQ instruction. The interpretation of this bit pattern is user defined.

BIT TEST COMPLETE (bit 1) : This bit indicates that the protocol built-in self-test or the RAM built-in self-test has been completed. The result of the test may be determined by reading the BIT Test Status Register.

INTERRUPT CHAIN BIT (bit 0) : This bit indicates that one or more bits are set in Interrupt Status Register #1, indicating interrupt conditions and/or event(s). If ENHANCED INTERRUPTS are enabled (bit 15 of Configuration Register #2 = logic “1”), and there are one or more bits set in Interrupt Status Register #1 that do not result in an interrupt request (because these requests have been disabled by means of Interrupt Mask Register #1), note that these bits will not result in the setting of the INTERRUPT CHAIN BIT.

Note that for Interrupt Mask Register #2, this bit is not used.

It is recommended that Interrupt Status Register #2 be read prior to reading Interrupt Status Register #1. That is, it will only be necessary to read Interrupt Status Register #1 if the INTERRUPT CHAIN BIT in Interrupt Status Register #2 has been set.

Note that if INTERRUPT STATUS AUTO-CLEAR, bit 4 of Configuration Register #1 is logic "1," that each of the two Interrupt Status Registers will only be cleared by the reading of that specific interrupt status register. That is, if both Interrupt Status Register #1 and Interrupt Status Register #2 have issued enabled interrupts, that Interrupt Status Register #2 will be cleared immediately following being read, independent of whether or not Interrupt Status Register #1 has been read. Likewise, Interrupt Status Register #1 will be cleared immediately following being read, independent of whether or not Interrupt Status Register #2 has been read.

If the Enhanced Mini-ACE's INT* output has been configured for "level" mode (i.e., bit 3 of Configuration Register #2, LEVEL/PULSE* INTERRUPT REQUEST, is logic "1"), then it will only be necessary to read the Interrupt Status Register (#1 and/or #2) that is requesting an interrupt that has been enabled by the corresponding Interrupt Mask Register. However, for the case where both Interrupt Status Register #1 and Interrupt Status Register #2 have bits set reflecting interrupt events, it will be necessary to read both interrupt status registers in order to clear INT*.

4.32 BC General Purpose Queue Pointer Register/RT, MT Interrupt Status Queue Pointer Register

(Register Address 11111; READ/WRITE)

**Table 83. General Purpose Pointer Register (RD/WR 1FH)
RT, MT Interrupt Status Queue Pointer Register (RD/WR 1FH)**

BIT	DESCRIPTION
15 (MSB)	QUEUE POINTER BASE ADDRESS 15
. . .	. . .
6	QUEUE POINTER BASE ADDRESS 15
5	QUEUE POINTER ADDRESS 5
. . .	. . .
0 (LSB)	QUEUE POINTER ADDRESS 0

For Enhanced BC mode, this register serves as a pointer for the General Purpose Queue. In RT and Message Monitor modes, assuming that INTERRUPT STATUS QUEUE ENABLE, bit 6 of Configuration Register #6 is logic “1,” this register serves as a pointer for the Interrupt Status Queue.

The host processor should initialize this register. Bits 15 through 6 serve as a base address register for the General Purpose Queue or Interrupt Status Queue, and are not modified by the Enhanced Mini-ACE’s internal logic. Bits 5-0 are incremented by the internal logic, and roll over from a value of 3F to a value of 00.

5 BC OPERATION

5.1 Definitions

ENHANCED MODE - means that bit 15 of Configuration Register #3 = logic “1.”

ENHANCED MODE DISABLED - means that bit 15 of Configuration Register #3, is logic "0.”

EXPANDED BC CONTROL WORD ENABLE - means that bit 12 of Configuration Register #4 is logic "1.”

EXPANDED BC CONTROL WORD DISABLE - means that bit 12 of Configuration Register #4 is logic "0.”

5.2 Introduction

The BC functionality for the Enhanced Mini-ACE includes two separate architectures: (1) the legacy non-Enhanced mode, which provides complete compatibility with the previous ACE and Mini-ACE (Plus) generation products; and (2) the newer, enhanced BC mode. The enhanced BC mode offers several new powerful architectural features. These include the incorporation of a highly autonomous BC message sequence control engine, which greatly serves to offload the operation of the host CPU.

The first part of the BC section of the user’s guide focuses on the legacy BC architecture. The second part of the BC section focuses on the enhanced BC architecture. Note that a number of constructs introduced in the legacy BC portion are also applicable to the enhanced BC architecture. These include:

- BC Control Word
- Time-to-Next Message
- Block Status Word
- Time Tag
- BC Control Word
- Automatic Retries
- BC Response Timeout
- Status Word Masking

- The lower three (read-only) bits of Configuration Register #1.

IMPORTANT NOTE: *There is a distinction between the Enhanced Mini-ACE's ENHANCED mode, and the Enhanced BC mode. ENHANCED MODE is enabled by setting bit 15 of Configuration #3, to logic "1," while the Enhanced BC mode is enabled by setting ENHANCED BC MODE, bit 15 of Configuration Register #6 (as well as ENHANCED MODE ENABLED) to logic "1."*

Note that ENHANCED MODE (bit 15 of Configuration Register #3) is applicable for enabling a number of functions in the Enhanced Mini-ACE's ***legacy*** *BC mode. These include Configuration Register #1 bits 11-0; Configuration Register #2 bits 15-12; Configuration Registers #3, #4, and #5; BC Control Word Register; BC Frame Time Remaining Register; BC Time-to-Next Message Remaining Register; and the BC frame Time Register.*

5.3 Legacy BC Mode

The legacy BC mode provides backward software compatibility for ACE and Mini-ACE (Plus) BC applications. For new applications, it is not recommended that the legacy BC mode be used because the Enhanced BC provides much more powerful control. In order to configure the Enhanced Mini-ACE for the legacy BC mode, bit 15 (RT/BC-MT*) and 14 (MT/BC-RT*) of Configuration Register #1, along with bit 15 of Configuration Register #6 (ENHANCED BUS CONTROLLER) must be programmed to logic "0."

The BC protocol of the Enhanced Mini-ACE implements all MIL-STD-1553B message formats. Message format is programmable on a message-by-message basis by means of individual BC control words and the T/R* bit of the 1553 command word to be transmitted. In addition to message format, the BC control word allows bus channel, self-test, retries, interrupts, and RT status word masking to be specified on an individual message basis. The BC performs all error checking required by MIL-STD-1553B. This includes validation of sync type and encoding, Manchester II encoding, parity, bit count, word count, and Status Word RT Address field. RT response time is verified to be less than the Enhanced Mini-ACE 's programmable response timeout value (17.5 to 19.5 µs default).

5.4 BC Memory Organization

Table 84 illustrates a typical memory map for the Mini-ACE/ACE legacy Bus Controller. Note that there are eight (8) fixed memory locations within the BC memory map. For each of the two global "areas" (A and B), these are the Stack Pointer and Message Counter, and the Initial Stack Pointer and Message Counter. The host processor must initialize the Stack Pointer and Message Counter before starting single message frames. For the frame auto-repeat mode, the host processor must initialize the Initial Stack Pointer and Initial Message Count locations before initializing a repetitive frame of BC messages.

Table 84. Typical Legacy BC Memory Map (Shown For 4K RAM)	
ADDRESS HEX	**DESCRIPTION**
0000-00FF	STACK A
100	STACK POINTER A (FIXED LOCATION)
101	MESSAGE COUNT A (FIXED LOCATION)
102	INITIAL STACK POINTER A (AUTO-FRAME REPEAT MODE)1
103	INITIAL MESSAGE COUNT A (AUTO-FRAME REPEAT MODE)1
104	STACK POINTER B (FIXED LOCATION)
105	MESSAGE COUNT B (FIXED LOCATION)
106	INITIAL STACK POINTER B (AUTO-FRAME REPEAT MODE)1
107	INITIAL MESSAGE COUNT B (AUTO-FRAME REPEAT MODE)1
0108-012D	MESSAGE BLOCK 0
012E-0153	MESSAGE BLOCK 1
• • •	• • •
0ED6-0EFB	MESSAGE BLOCK 93
0EFC-0EFF	NOT USED
0F00-0FFF	STACK B

Notes

1. Used only if ENHANCED MODE and Frame Auto-Repeat is enabled.
2. The user is free to locate the BC stack and BC message blocks anywhere within the Enhanced Mini ACE 's 4K word or 64K word address space.

5.5 256-Word Boundaries

It should be noted that the BC (as well as RT) stack area of RAM will roll over at a boundary in the Enhanced Mini-ACE shared RAM address space, as specified by bits 14 and 13 of Configuration Register #3 (default is 256 words). The BC/RT Stack size is programmable with choices of 256 words (64 messages), 512, 1024, and 2048 words (512 messages). The default is 256 words (64 messages). That is, the value of the Stack Pointer will increment from XXFF to XX00, not to (XX+1)00. If bit 10 of Configuration Register #2, 256-WORD BOUNDARY DISABLE, is logic 0, the 256-word boundaries will also be enforced for BC message blocks.

However, if 256-WORD BOUNDARY DISABLE is programmed to logic "1," the address for BC message blocks **will not** roll over at 256-word boundaries. This allows for more efficient allocation of the shared RAM address space for storing BC message blocks.

IMPORTANT NOTE: For BC mode, it is strongly recommended that 256-WORD BOUNDARY DISABLE be programmed to logic "1."

For simplicity of illustration, the maximum message size is allocated for each BC message block in the typical BC memory map of Table 84. Note, that the maximum size of a BC message block is 38 words, for an RT-to-RT transfer of 32 Data Words (Control + 2 Commands + Loopback + 2 Status Words + 32 Data Words). This requires that 256-word boundaries are disabled.

5.5.1 Active Areas Double Buffering

For the legacy BC mode, the Active Area feature provides a global mechanism for dividing the shared RAM into *active* and *non-active* areas using current area bit 13 of CR# 1. At any point in time, only the various data structures within the "active" area are accessed by the internal 1553 memory management logic. It should be noted, however, that at any point in time, both the *active* and *non-active* areas are accessible by the host processor. It should be noted that if the host CPU changes the active area while a BC frame is being processed (by toggling bit 13 of Configuration Register #1), the active area will **not** actually switch until the current BC frame has been completed.

5.6 Programming BC Message Frames

5.6.1 BC Memory Management

An overview of the Enhanced Mini-ACE memory management scheme for legacy BC mode is illustrated in Figure 4. The BC may be programmed to transmit multi-message frames of up to 512 unique messages. The number of messages to be processed is programmable by means of the fixed Message Count location in the shared RAM. In addition, the host processor must initialize a second fixed location as the Stack Pointer. This RAM location contains a pointer that references the four-word message block descriptor (in the Stack area of shared RAM) for each message to be processed. Each message resides in a designated message block area of the shared RAM. The starting location for each message block is specified by a pointer that is stored in the fourth location of the block descriptor for the respective message. The host processor must load this pointer before the message is processed. The first word of each BC message block is the BC control word. Referring to Figure 4 the CPU may select between global Area A and global Area B by means of bit 13 of Configuration Register #1. In the figure, it is assumed that Area A is delineated by the non-shaded area and is the current "active" area; it can be assumed that Area B is the "non-active" (shaded) area.

The Enhanced Mini-ACE's global double buffering feature provides a relatively simple mechanism for ensuring data consistency. The host processor designates the current active area by means of bit 13 of Configuration Register #1 (ACTIVE AREA B/A*). A common practice is for the host to access the "non-active" area, while allowing the Enhanced Mini-ACE 's 1553 protocol logic to access the "active" area. After the current message frame has been completed for the current "active" area, the host should switch ("ping-pong") the "active" and "non-active" areas by means of ACTIVE AREA B/A*.

The use of the Enhanced Mini-ACE 's global double buffering feature eliminates the possibility of data inconsistency by precluding the possibility that the BC will transmit or that the CPU will read a mixture of old and new Data Words for any particular message. In addition, this technique eliminates the possibility of a contended CPU access to the Enhanced Mini-ACE 's shared RAM.

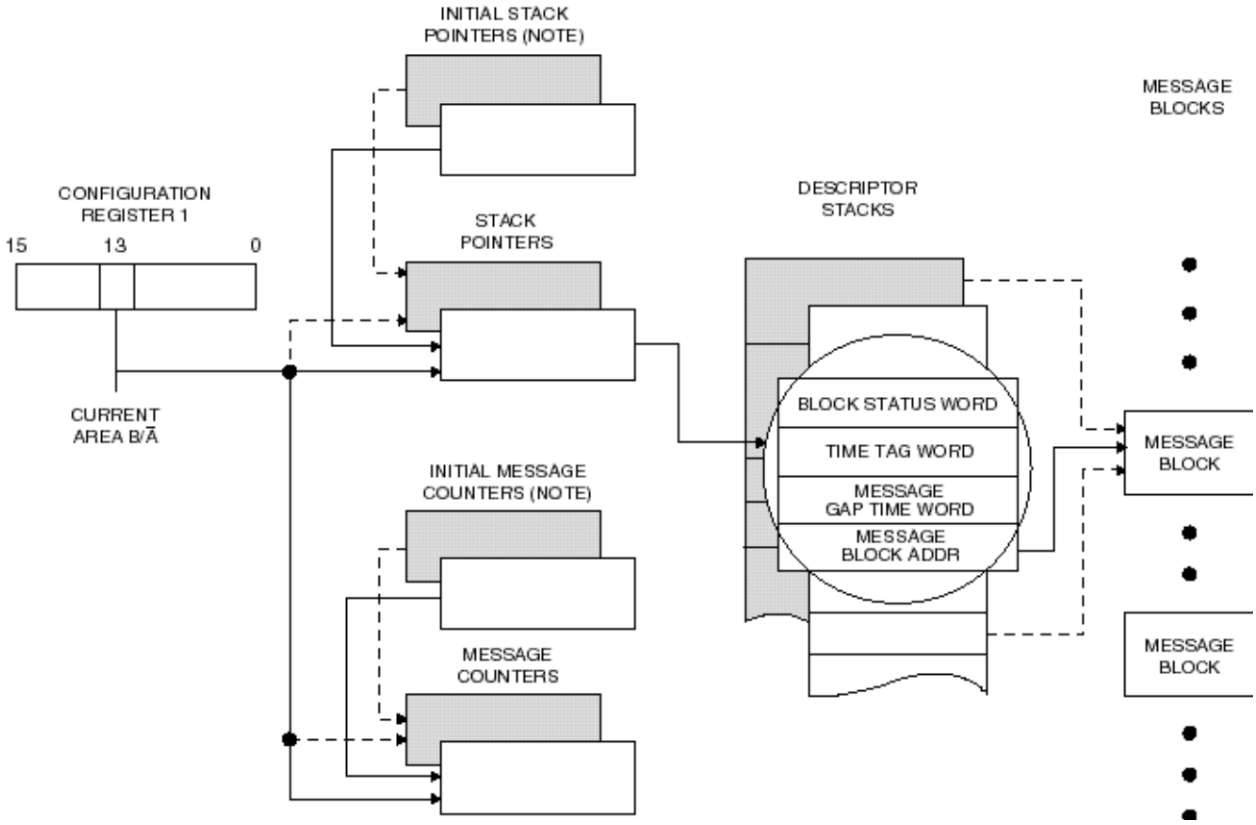


Figure 4. Legacy BC Memory Management

A variation on the global buffering scheme is the use of "multiple buffering." That is, instead of using the Enhanced Mini-ACE 's ACTIVE AREA B/A* feature, it is possible to program **several** message frame scenarios. This is done by positioning a number of descriptor stacks at different areas within the Enhanced Mini-ACE shared RAM address space. In turn, the pointer words for the individual message block descriptors in the stacks can reference message blocks anywhere within the address space. When one message frame has been completed, the host processor need only re-assign the values of the Stack Pointer and Message Counter to initiate processing of the next BC message frame.

To process a single message frame, the "active area" stack pointer and message count locations must be initialized by the host processor before processing each individual message frame. For the frame auto-repeat mode, the values for the initial stack pointer and initial message counter locations must be initialized. The initial pointer and counter need be initialized only **once**, prior to the processing of the first message frame.

At any point in time, the stack pointer points to the first word of the block descriptor for the current message. As illustrated in Figure 5, there are four words in the descriptor stack for each BC message. The first two locations are reserved for the Block Status Word and Time Tag Word. These two words are written by the Enhanced Mini-ACE 's BC protocol logic at the beginning and end of each message processed. The BC Block Status Word contains bits relating to message status and completion, validity, and bus channel. The time tag word reflects the contents of the Enhanced Mini-ACE's Time Tag Register at the beginning (and end) of a message. The time tag register has a programmable resolution of 2 to 64 µs/LSB, in powers of two. The Time Tag counter may also be clocked from an external oscillator.

The host processor must load the second two locations within the BC block descriptor. The Message Gap Time Word is accessed if the Enhanced Mini-ACE is in ENHANCED MODE and INTER-MESSAGE GAP TIME ENABLED (bit 05 of Configuration Register #1) is programmed to logic "1." The Inter-message Gap Time Word specifies the time from the **beginning** of the current message to the **beginning** of the subsequent message. Reference Figure 5.

The resolution of the Inter-message Gap is 1 µs/LSB. The Message Block Address provides a pointer to the first word of the message block (the BC Control Word) for the respective message. The value of the active area Stack Pointer is incremented by four following each message processed by the Enhanced Mini-ACE BC.

The message count (or initial message count) location must be initialized by the host to correspond to the **ones complement** of the number of messages to be processed in a message frame. For example, if a message frame contains one (1) message, the (Initial) Message Counter location should be loaded with a value of FFFE. The value of the (Initial) Message Counter is incremented by one at the end of each message processed.

As illustrated in Figure 5, the BC Control Word is the first word (word number "0") within the individual BC message block. The BC Control Word is **not** transmitted on the 1553 bus.

Figure 3 illustrates the message block structures for all of the possible BC message formats. The words to be transmitted and received are in the order they appear in the BC message blocks. The BC Control Word is the principal control entity for individual BC messages. The bits in the BC Control Word contain information relating to the message format, bus channel, interrupt enabling, 1553A vs. 1553B error handling, off-line self-test, retries, and Status Word bit masking.

If the Enhanced Mini-ACE is programmed for ENHANCED MODE **and** EXPANDED BC CONTROL WORD ENABLED, bit 12 of Configuration Register #4, is programmed to logic "1," then all 15 bits of the BC Control Word are used (bit 15 is "NOT USED"). If ENHANCED BC MODE is logic "0," then only bits 7,6,5,2,1, and 0 are used. This includes the 7 STATUS MASK bits.

The individual STATUS MASK bits designate various RT Status Word bits as either "care" (if logic "0") or "don't care" (if logic "1"). If one or more of the designated "care" bits are set to logic "1" in a responding RT's Status Word, then item 1, and possibly items 2, 3, and 4 below will occur:

1. The STATUS SET bit (bit 11) of the BC Block Status Word will be logic "1."

2. If STATUS SET, bit 1 of Interrupt Mask Register #1 is logic "1," an interrupt request will be issued.

3. If STATUS SET, bit 1 of Interrupt Mask Register #1 is logic "1" **or** ENHANCED INTERRUPTS, bit 15 of Configuration Register #2 is logic "1," then STATUS SET bit 1 of INTERRUPT STATUS REGISTER #1, will be logic "1."

4. If RETRY ENABLED (bit 4 of Configuration Register #1) **and** RETRY IF STATUS SET (bit 9 of Configuration Register #4) **and** RETRY ENABLED (bit 8 of the BC Control Word) are all logic "1," the message will be retried.

The host processor must write the (first) Command Word in the next location after the BC Control Word. After this word, a possible second Command Word (for RT-to-RT transfers), and Data Words to be transmitted by the BC must be loaded by the host. In the subsequent addresses, locations must be reserved for the Loopback Word and received Status and Data Words.

5.6.2 Message Block Formats

In both the legacy and enhanced BC mode, the Enhanced Mini-ACE supports all MIL-STD-1553B message formats. In the legacy mode, for each 1553B message format, the Enhanced Mini-ACE requires a specific sequence of words within the BC Message Block. This includes locations for the Control, Command, and (transmitted) Data Words that are loaded by the host processor to be read from RAM by the BC protocol logic. In addition, subsequent contiguous locations must be allocated for storage of received Loopback, RT Status, and Data Words. illustrates the bit mapping of the command word and Table illustrates the bit mappings for the status word (for more information on 1553 command and status words, refer to DDC's MIL-STD-1553 Designer's Guide).

Figure 3 illustrates the organization of the BC message blocks for the various MIL-STD-1553B message formats. Note that for all of the message formats for the legacy BC mode, the BC Control Word is located in the first location of the message block.

Table 85. MIL-STD-1553B Command Word

Bit	Description
15(MSB)	REMOTE TERMINAL ADDRESS BIT 4
□ □	□ □
11	REMOTE TERMINAL ADDRESS BIT 0
10	TRANSMIT RECEIVE
9	Subaddress/MODE CODE BIT 4
□ □ □	□ □ □
5	Subaddress/MODE CODE BIT 0
4	DATA WORD COUNT/MODE COUNT BIT 4
□ □ □	□ □ □
0(LSB)	DATA WORD COUNT/MODE CODE BIT 0

Table 86. MIL-STD-1553B Status Word	
Bit	**Description**
15(MSB)	REMOTE TREMINAL ADDRESS BIT 4
14	REMOTE TERMINAL ADDRESS BIT 3
13	REMOTE TERMINAL ADDRESS BIT 2
12	REMOTE TERMINAL ADDRESS BIT 1
11	REMOTE TERMINAL ADDRESS BIT 0
10	MESSAGE ERROR
9	INSTRUMENATION
8	SERVICE REQUEST
7	RESERVED
6	RESERVED
5	RESERVED
4	BROADCAST COMMAND RECEIVED
3	BUSY
2	SUBSYSTEM FLAG
1	DYNAMIC BUS CONTROL ACCEPTANCE
0(LSB)	TERMINAL FLAG

Figure 5. BC Message Block Formats

RT-TO-BC TRANSFER		RT-TO-BC TRANSFER
CONTROL WORD		CONTROL WORD
RECEIVE COMMAND WORD		TRANSMIT COMMAND WORD
DATA WORD #1		TRANSMIT COMMAND WORD LOOPED BACK
DATA WORD #2		RECEIVED STATUS WORD
• • •		RECEIVED DATA WORD #1
LAST DATA WORD		RECEIVED DATA WORD #2
LAST DATA WORD LOOPED BACK		• • •
RECEIVED STATUS WORD		LAST RECEIVED DATA WORD

Figure 5. BC Message Block Formats (1 of 3) (Cont.)

RT-TO-RT TRANSFER		**MODE CODE; NO DATA**		**TX MODE CODE WITH DATA**
CONTROL WORD		CONTROL WORD		CONTROL WORD
RECEIVE COMMAND		MODE COMMAND		TX MODE COMMAND
TRANSMIT COMMAND		MODE COMMAND LOOPED BACK		MODE COMMAND LOOPED BACK

TRANSMIT COMMAND LOOPED BACK		STATUS RECEIVED		STATUS RECEIVED
Tx RT STATUS WORD				DATA WORD
DATA #1				
DATA #2				
• • •				
LAST DATA				
Rx RT STATUS WORD				

Figure 5. BC Message Block Formats (2 of 3) (Cont.)

Rx MODE CODE WITH DATA		BROADCAST		RT-TO-RTs (BROADCAST) TRANSFER
CONTROL WORD		CONTROL WORD		CONTROL WORD
Rx MODE COMMAND		BROADCAST COMMAND		Rx BROADCAST COMMAND
DATA WORD		DATA #1		Tx COMMAND
DATA WORD LOOPED BACK		DATA #2		Tx COMMAND LOOPBACK
RECEIVED STATUS		• • •		Tx RT STATUS
				DATA #1
		LAST DATA		DATA #2
		LAST DATA LOOPED BACK		• • •
				LAST DATA

Figure 5. BC Message Block Formats (3 of 3) (Cont.)

BROADCAST MODE CODE NO DATA		BROADCAST MODE CODE WITH DATA
CONTROL WORD		CONTROL WORD
BROADCAST MODE COMMAND		BROADCAST MODE COMMAND
BROADCAST MODE COMMAND LOOPED BACK		DATA WORD
		DATA WORD LOOPED BACK

5.6.3 BC Control Word

For each of the BC Message Block formats in the legacy BC mode, the first word in the block is the BC Control Word. For the enhanced BC mode, the BC Control Word is the first word of the message's control/status block. The BC Control Word is **not** transmitted on the 1553 bus. Instead, it contains bits that select the active bus and message format, enable off-line self-test, and specify the "expected value" of the BROADCAST COMMAND RECEIVED RT Status bit. The bit mapping and definitions of the BC Control Word are as shown in Table 87*.*

Table 87. BC Control Word Register

BIT	DESCRIPTION
15(MSB)	TRANSMIT TIME TAG FOR SYNCHRONIZE MODE COMMAND
14	MESSAGE ERROR MASK (S10)
13	SERVICE REQUEST BIT MASK (S08)
12	SUBSYS BUSY BIT MASK (S03)
11	SUBSYS FLAG BIT MASK (S02)
10	TERMINAL FLAG BIT MASK (S00)
9	RESERVED BITS MASK
8	RETRY ENABLED
7	BUS CHANNEL A/B*
6	OFF LINE SELF TEST
5	MASK BROADCAST BIT
4	EOM INTERRUPT ENABLE
3	1553A/B SELECT
2	MODE CODE FORMAT
1	BROADCAST FORMAT
0(LSB)	RT-TO-RT FORMAT

***Note**: Bits 14-8, 4, and 3 are applicable only if ENHANCED MODE ENABLED and EXPANDED BC CONTROL WORD ENABLE, bit 12 of Configuration Register #4, are logic "1." If these two conditions are not met, the Enhanced Mini-ACE BC utilizes its non-expanded BC Control Word. The non-expanded BC Control Word consists of bits 7, 6, 5, 2, 1, and 0 only.*

With the non-expanded BC Control Word, a "Status Set" condition indicates either a non-matching RT Address field **or** if **any** of the 8 non-Reserved RT Status bits are set. An exception is that for the Broadcast Command Received bit, a "Status Set" condition will occur if the value of the Broadcast Command Received bit in the RT Status Word is **different** than the value of the MASK BROADCAST bit.

If the expanded BC Control Word option is used, a "Status Set" condition indicates a non-matching RT Address field **or** that one or more of the RT Status Word bits, **in which the respective MASK bit(s) in the BC Control Word has been programmed to logic "0,"** is set (logic "1") in the received RT Status Word. When the Expanded BC Control Word option is used, the value of received RT Status Word bits for which the respective MASK bit is programmed for logic "1" becomes "don't care," in terms of affecting a "Status Set" condition.

Table 88 summarizes the operation of the MASKED STATUS SET bit, for all status word bits except for Broadcast Command Received.

Table 88. Operation of BC Control Word Status Mask Bits

RESPECTIVE "MASK" BIT (BITS 14-9) IN BC CONTROL WORD	RT STATUS WORD BIT	Will this status word bit contribute to a MASKED STATUS SET condition?
0	0	NO
0	1	YES
1	X	NO

TRANSMIT TIMETAG FOR SYNCHRONIZE MODE COMMAND (bit 15): This bit is only applicable for a Synchronize (with data) mode code message. If LOAD/TRANSMIT TIMETAG FOR SYNCHRONIZE (bit 5 of Configuration Register #2) **and** TRANSMIT TIMETAG FOR SYNCHRONIZE MODE COMMAND are both logic "1," the Enhanced Mini-ACE BC will transmit the value of its Time Tag Register as the data word for a Synchronize (with data) mode code. In this case, if ENHANCED TIMETAG SYNCHRONIZE, bit 2 of Configuration Register #7, is programmed to logic "1," the transmitted data word (Time Tag) will always contain an LSB with a value of "0."

MESSAGE ERROR MASK (bit 14): Applicable only if ENHANCED MODE ENABLED **and** EXPANDED BC CONTROL WORD ENABLE. If MESSAGE ERROR MASK is logic "0," a Status Set condition will occur, if the Message Error bit is logic "1" in the received RT Status Word. If MESSAGE ERROR MASK is logic "1," the value of the Message Error bit in the received RT Status Word becomes "don't care," in terms of affecting the occurrence of a "Status Set" condition.

SERVICE REQUEST MASK (bit 13): Applicable only if ENHANCED MODE ENABLED **and** EXPANDED BC CONTROL WORD ENABLE. If SERVICE REQUEST MASK is logic "0," a Status Set condition will occur if the Service Request bit is logic "1" in the received RT Status Word. If SERVICE REQUEST MASK is logic "1," the value of the Service Request bit in the received RT Status Word becomes "don't care," in terms of affecting the occurrence of a "Status Set" condition.

BUSY MASK (bit 12): Applicable only if ENHANCED MODE ENABLED **and** EXPANDED BC CONTROL WORD ENABLE. If BUSY MASK is logic "0," a Status Set condition will occur if the Busy bit is logic "1" in the received RT Status Word. If BUSY MASK is logic "1," the value of the Busy bit in the received RT Status Word becomes "don't care," in terms of affecting the occurrence of a "Status Set" condition.

SUBSYSTEM FLAG MASK (bit 11): Applicable only if ENHANCED MODE ENABLED **and** EXPANDED BC CONTROL WORD ENABLE. If SUBSYSTEM FLAG MASK is logic "0," a Status Set condition will occur if the Subsystem Flag bit is logic "1" in the received RT Status Word. If SUBSYSTEM FLAG MASK is logic "1," the value of the Subsystem Flag bit in the received RT Status Word becomes "don't care," in terms of affecting the occurrence of a "Status Set" condition.

TERMINAL FLAG MASK (bit 10): Applicable only if ENHANCED MODE ENABLED **and** EXPANDED BC CONTROL WORD ENABLE. If TERMINAL FLAG MASK is logic "0," a Status Set condition will occur if the Terminal Flag bit is logic "1" in the received RT Status Word. If TERMINAL FLAG MASK is logic "1," the value of the Terminal Flag bit in the received RT Status Word becomes "don't care," in terms of affecting the occurrence of a "Status Set" condition.

RESERVED BITS MASK (bit 9): Applicable only if ENHANCED MODE ENABLED **and** EXPANDED BC CONTROL WORD ENABLE. If RESERVED MASK is logic "0," a Status Set condition will occur if one or more of the 3 Reserved bits are logic "1" in the received RT Status Word. If RESERVED BITS MASK is logic "1," the value of the 3 Reserved bits in the received RT Status Word becomes "don't care," in terms of affecting the occurrence of a "Status Set" condition.

RETRY ENABLED (bit 8): Applicable only if ENHANCED MODE ENABLED **and** EXPANDED BC CONTROL WORD ENABLE. If RETRY ENABLED is logic "0," the message will **not** be retried. If RETRY ENABLED, bit 4 of Configuration Register #1, is logic "1" **and** RETRY ENABLED is logic "1," a message will be retried as the result of a response timeout or format error condition.

If RETRY ENABLED (bit 4 of Configuration Register #1 is logic "1") **and** if "RETRY IF 1553A AND MESSAGE ERROR" (bit 10 of Configuration Register #4 is logic "1")_ **and** "1553 A/B* SELECT" (bit 3 of the BC Control Word, is logic "1") , the Enhanced Mini-ACE BC will also attempt a message retry as the result of the Message Error bit being set in the RT Status Word.

If RETRY ENABLED (bit 4 of Configuration Register #1 is logic "1") **and** RETRY IF STATUS SET (bit 9 of Configuration Register #4 is logic "1") **and** RETRY ENABLED is logic "1," the Enhanced Mini-ACE BC will attempt a message retry as the result of a "Status Set" condition in the received RT Status Word. A "Status Set" condition indicates either a non-matching RT Address field **or** that one or more of the

RT Status Word bits, **in which the respective MASK bit(s) in the BC Control Word has been programmed to logic "0,"** is set in the received RT Status Word. When the expanded BC Control Word option is used, the value of received RT Status Word bits, for which the respective MASK bit is programmed for logic "1," becomes "don't care" in terms of affecting a "Status Set" condition.

The conditions where message retries will occur are summarized in Table 89.

Table 89. BC Message Retry Conditions

ENHANCED MODE (bit 15 of Configuration Register #1)	EXPANDED BC CONTROL WORD ENABLE (bit 12 of Configuration Register #4)	RETRY ENABLED (bit 4 of Configuration Register #1)	RETRY ENABLED (bit 8 of BC Control Word)	Response Timeout or Message Error Condition	RETRY IF 1553A AND MESSAGE ERROR (bit 10 of Configuration Register #4)	1553 A/B* SELECT(bit 3 of the BC Control Word)	Message Error Status Word	RETRY IF STATUS SET (bit 9 of Configuration Register #4)	"Status Set" Condition (see tables X and X)	Retry Message ?
0	X	X	X	X	X	X	X	X	X	No
X	0	X	X	X	X	X	X	X	X	No
X	X	0	X	X	X	X	X	X	X	No
X	X	X	0	X	X	X	X	X	X	No
X	X	X	X	0	One or more of these is "0"			0	X	No
X	X	X	X	0	One or more of these is "0"			X	No	No
1	1	1	1	1	X	X	X	X	X	Yes
1	1	1	1	X	1	1	1	X	X	Yes
1	1	1	1	X	X	X	X	1	Yes	Yes

The number of retry attempts is specified by DOUBLE/SINGLE* RETRY, bit 3 of Configuration Register #1: one retry if DOUBLE/SINGLE* RETRY is logic "0," two retries if DOUBLE/SINGLE* RETRY is logic "1." The channel selection (same or alternate) for the first and second retry attempts is specified by bits 8 and 7 of Configuration Register #4.

BUS CHANNEL A/B* (bit 7): Selects whether the message will be processed on Channel A or Channel B. If the bit is logic "1," the message will be processed on Channel A; if the bit is logic "0," the message will be processed on Channel B.

OFF-LINE SELF-TEST (bit 6): If this bit is set, it enables the off-line self-test for the respective message. In an off-line self-test message, the 1553 transmitter is inhibited; there is no activity on the external 1553 bus. The off-line self-test exercises the digital protocol portion of the Enhanced Mini-ACE by routing the output of the Manchester II serial encoder directly to the decoder input of the selected bus channel. After the message has been processed, the user can determine the success or failure of the off-line self-test by reading the Loopback Word and the LOOP TEST FAIL bit of the Block Status Word.

MASK BROADCAST (bit 5): If BROADCAST MASK ENABLED/XOR*, bit 11 of Configuration Register #4 is logic "0" **and** MASK BROADCAST is logic "1," the "expected value" of the Broadcast Command Received bit becomes 1, rather than 0. That is, a value of logic "**0**" (rather than logic "1") for the Broadcast Command Received bit in the received RT Status Word will result in a "Status Set" condition.

If ENHANCED MODE ENABLED **and** EXPANDED BC CONTROL WORD ENABLE **and** BROADCAST MASK ENA/XOR* (bit 11 of Configuration Register #4) is programmed to logic "1," MASK BROADCAST is used as a mask bit, rather than performing an "XOR" operation with the Broadcast Received Status Word bit. In this instance, a Status Set condition arising from the Broadcast Command Received RT Status bit occurs when MASK BROADCAST is logic "0" and the Broadcast Command Received RT Status Word bit is logic "1." If BROADCAST MASK ENABLED/XOR* is logic "1" **and** MASK BROADCAST is logic "1," the value of the Broadcast Command Received bit in the received RT Status Word becomes "don't care" in affecting a "Status Set" condition.

Table 90 summarizes the operation of the MASK BROADCAST bit.

Table 90. Effect of Broadcast command received status word bit on STATUS SET condition

ENHANCED MODE ENABLE (bit 15 of Configuration Register #3)	BROADCAST MASK ENABLED /XOR* (bit 11 of Configuration Register #4)	MASK BROADCAST (bit 5 in BC Control Word)	Broadcast Command Received bit in RT Status Word	Will this result in a STATUS SET condition?
0	X	0	0	No
	or	0	1	Yes
X	0	1	0	Yes
		1	1	No
1	1	0	0	No
		0	1	Yes
		1	X	No

NOTE: "X" = don't care

EOM INTERRUPT ENABLE (bit 4): Applicable only if ENHANCED MODE ENABLED **and** EXPANDED BC CONTROL WORD ENABLE. If RT/BC MESSAGE INTERRUPT, bit 4 of Interrupt Mask Register #1 is set, setting EOM INTERRUPT

ENABLE to logic "1" will result in an Interrupt Request at the end of the current message.

1553 A/B* SELECT (bit 3): Applicable only if ENHANCED MODE ENABLED **and** EXPANDED BC CONTROL WORD ENABLE. If 1553 A/B* SELECT is programmed to logic "0," the Enhanced Mini-ACE BC verifies the validity of the RT response in accordance with MIL-STD-1553B. That is, it anticipates that an RT will respond to mode code commands with a T/R* bit of logic "1" and an MSB of the Mode Code field (bit 4) of logic "1" with a Status Word followed by a single Data Word. In addition, for an anticipated "1553B" response, assuming that RETRY IF STATUS SET bit 9 of Configuration Register #4 is logic "0," the Enhanced Mini-ACE BC will **not** attempt a message retry as the result of the Message Error bit being set in the RT Status Word.

If 1553 A/B* SELECT is programmed to logic "1," the Enhanced Mini-ACE BC verifies the validity of the RT response in accordance with MIL-STD-1553A. That is, it anticipates that an RT will respond to mode code commands with a T/R* bit of logic "1" and an MSB of the Mode Code field (bit 4) of logic "1" with a Status Word only and no Data Word. In addition, if RETRY ENABLED bit 4 of Configuration Register #1 is logic "1," **and** RETRY IF 1553A AND MESSAGE ERROR bit 10 of Configuration Register #4 is logic "1," **and** RETRY ENABLED bit 8 of the BC Control Word is logic "1" **and** 1553 A/B* SELECT is logic "1," the Enhanced Mini-ACE BC **will** attempt a message retry as the result of the Message Error bit being set in the RT Status Word. In addition, if 1553 A/B* SELECT is programmed to logic "1," then mode commands with the T/R equaling 0 will have no data words associated with them.

The operation of the 1553A/B* SELECT bit is summarized in Table 91.

Table 91. Effects of BC Control Word 1553A/B* BIT

1553 A/B* SELECT (bit 3 of BC Control Word)	Mode Code Message with T/R* bit = "1," and the MSB of the Mode Code field = "1"	Mode Code Message with T/R* bit = "0"	Retry if Message error status bit set?
0 (1553B)	BC only considers RT response of status word plus one data word to be valid.	If the MSB of the command word mode code field = "1," then the BC transmits Command word plus one data word. A mode code command with T/R* bit = 0 and MSB of mode code field = 0 is not defined by MIL-STD-1553B.	Only if RETRY ENABLED (bit 4 of Configuration Register #1) = RETRY IF 1553A AND MESSAGE ERROR (bit 10 of Configuration Register #4) = RETRY ENABLED (bit 8 of BC Control Word) = logic "1."
1 (1553A)	BC only considers RT response of status word plus no data words to be valid.	The BC transmits command word plus no data words.	Only if MESSAGE ERROR MASK (bit 14 of BC Control Word) = logic "0," and RETRY ENABLED (bit 4 of Configuration Register #1) = RETRY IF STATUS SET (bit 9 of Configuration Register #4) = RETRY ENABLED (bit 8 of the BC Control Word) = logic "1"

MODE CODE, BROADCAST, RT-TO-RT (bits 2, 1, 0): Selects MIL-STD-1553B message format as follows:

Table 92. BC Message Formats			
BIT 2 MODE CODE	**BIT 1 BROADCAST**	**BIT 0 RT-TO-RT**	**MESSAGE FORMAT**
0	0	0	BC-TO-RT (if T/R* BIT = 0) OR RT-to-BC (if T/R* BIT = 1)
0	0	1	RT-TO-RT
0	1	0	BROADCAST
0	1	1	RT-TO-RTs (BROADCAST)
1	0	0	MODE CODE
1	0	1	NOT USED
1	1	0	BROADCAST MODE CODE
1	1	1	NOT USED

In the legacy BC mode, the next word in RAM after the BC Control Word is the MIL-STD-1553B Command Word (for an RT-to-RT or RT-to-Broadcast transfer, it will be the first of two Command Words). This word is read by the 1553 protocol logic and transmitted on the 1553 bus. The (first) Command Word is possibly followed by a second Command Word or Data Words to be read from RAM and transmitted. The location in RAM after the **last** transmitted word is reserved for the Loopback Word (used for test purposes). Subsequent locations in the shared RAM are reserved for Status and possibly Data Words anticipated to be received from the responding RT(s). Assuming that the RT responds before a BC response timeout occurs, these word(s) are stored in the allocated locations in the shared RAM. If the Loopback test passes, and the RT responds before the BC Response Timer times out with a "Correct" RT Status Word (correct RT address and the "expected value" for the lower 11 bits), followed by the correct number of valid Data Words, the Block Status Word will be written to indicate "End of Message, No Errors" during the BC End-of-Message (EOM) sequence. Note that for an RT-to-RT transfer, the Enhanced Mini-ACE BC checks the Status Words from **both** the transmitting and receiving RTs.

5.6.4 Descriptor Stack

In the legacy BC mode, the host processor may determine the status of individual messages by reading the first two locations of the respective descriptor block. The first location within the descriptor block contains the Block Status Word. The BC mode Block Status Word contains information relating to whether the message is in progress or has been completed, which bus channel it was transmitted on and whether there were any errors in the message. The bit map and bit descriptions for the BC Block Status Word are indicated below.

Table 93. BC Mode Block Status Word	
BIT	**DESCRIPTION**
15(MSB)	EOM
14	SOM
13	CHANNEL B/A*
12	ERROR FLAG
11	STATUS SET
10	FORMAT ERROR
9	NO RESPONSE TIMEOUT
8	LOOP TEST FAIL
7	MASKED STATUS SET
6	RETRY COUNT 1
5	RETRY COUNT 0
4	GOOD DATA BLOCK TRANSFER
3	WRONG STATUS ADDRESS/NO GAP
2	WORD COUNT ERROR
1	INCORRECT SYNC TYPE
0(LSB)	INVALID WORD

Note: *If a message is retried, the bits of the Block Status Word reflect the result of the latest message retry.*

END-OF-MESSAGE (EOM) (bit 15): Set at the completion of a BC message, regardless of whether or not there were any errors in the message.

START-OF-MESSAGE (SOM) (bit 14): Set at the start of a BC message and cleared at the end of the message.

CHANNEL B/A* (bit 13): This bit will be logic “0” if the message was processed on Channel A, or logic “1” if the message was processed on Channel B.

ERROR FLAG (bit 12): If this bit is logic “1” and one or more of bits 10, 9, and/or 8 are high, this indicates one or more of the following errors occurred in the message: Format Error, Response Timeout and/or Loop Test Fail.

If this bit is logic "1,” the Enhanced Mini-ACE is configured for its transparent mode of processor interface, **and** bits 10, 9, and 8 are all logic "0,” this indicates that a **Handshake Failure** has occurred. There are two conditions that can cause a Handshake Failure. For both conditions, the maximum allotted time is 10.5 µs for a 20 MHz clock input, 10.0 µs for a 16 MHz clock input, 9.0 µs for a 12 MHz clock input, and 8.5 µs for a 10 MHz clock input. The two conditions are:

1) When the Data Transfer Grant (DTGRT*) input is not asserted within the allotted time after the Enhanced Mini-ACE's Data Transfer Request (DTREQ*) output has been asserted.

2) When the STRBD* input signal is held low too long at the end of a processor transfer cycle; i.e., following the falling edge of the handshake signal READYD*. Note that STRBD* asserted low for too long will **not** result in a HANDSHAKE-FAILURE condition in the Enhanced Mini-ACE's buffered mode configuration. If a Handshake Failure occurs, the message should be considered invalid. The Enhanced Mini-ACE will immediately terminate processing of a BC frame following occurrence of a Handshake Failure.

STATUS SET (bit 11): If this bit is logic "1," this indicates that one of the lower 11 bits the RT Status Word received from a responding RT contained an unexpected bit value. The expected value for these 11 bits is normally zero (0), with one exception: if {ENHANCED MODE ENABLE or BROADCAST MASK ENABLED/XOR* (bit 11 of Configuration Register #4) is logic "0"} and the MASK BROADCAST bit of the message's BC Control Word is logic "1," the expected value of the Broadcast Command Received bit becomes 1, rather than 0. The value of STATUS SET is not affected by the values of the other mask bits (bits 14 through 9) of the message's BC Control Word.

Table 94. summarizes the operation of the Broadcast command received status word bit on resulting in a STATUS SET condition.

Table 94. Effect of Broadcast Command Received Status Word Bit on STATUS SET Condition

Enhanced Mode Enable (bit 15 of Configuration Register #3)	Broadcast Mask Enabled /XOR* (bit 11 of Configuration Register #4)	Mask Broadcast (bit 5 in BC Control Word)	Broadcast Command Received bit in RT Status Word	Will this result in a Status Set condition?
0 Or X	X Or 0	0	0	No
		0	1	Yes
		1	0	Yes
		1	1	No
1	1	0	0	No
		0	1	Yes
		1	X	No

NOTE: "X" = don't care.

FORMAT ERROR (bit 10): If this bit is set, this indicates that the received portion of a message contained one or more violations of the 1553 message validation criteria (sync, encoding, parity, bit count, word count, etc.), or the RT's status word received from a responding RT contained an incorrect RT address field (Bits 0-2 provide additional information).

RESPONSE TIMEOUT (bit 9): If set, indicates that an RT has either not responded or has responded later than the BC No Response Timeout time. The Enhanced Mini-ACE 's No Response Timeout Time is defined per MIL-STD-1553B as the time from the mid-bit crossing of the parity bit to the mid-sync crossing of the RT Status Word. In the ENHANCED MODE DISABLE, the value of the BC Response Timeout is 17.5 to 19.5 µs. If ENHANCED MODE ENABLED is Logic "1," the value of the No

Response Timeout value is programmable from among the nominal values 18.5, 22.5, 50.5, and 130 µs (±1 µs) by means of bits 10 and 9 of Configuration Register #5.

LOOP TEST FAIL (bit 8): A loopback test is performed on the transmitted portion of every message in BC mode. A validity check is performed on the received version of every word transmitted by the Enhanced Mini-ACE BC. In addition, a bit-by-bit comparison is performed on the last word transmitted by the BC for each message. If either the received version of any transmitted word is invalid (sync, encoding, bit count, and/or parity error) **and/or** the received version of the last word transmitted by the Enhanced Mini-ACE BC does not match the transmitted version of this word, the LOOP TEST FAIL bit will be set.

IMPORTANT NOTE: If ENHANCED MODE DISABLED, bits 7 through 0 will always return logic "1."

MASKED STATUS SET (bit 7): Applicable only if ENHANCED MODE ENABLED **and** EXPANDED BC CONTROL WORD ENABLE. It will be set if one or both of the following conditions occur: (1) If one (or more) of the Status Mask bits (14 through 9) in the BC Control Word is logic "0" **and** the corresponding bit(s) is (are) logic "1" in the received RT Status Word. In the case of the RESERVED BITS MASK (bit 9) set to logic "0," any or all of the 3 Reserved Status bits being set will result in a MASKED STATUS SET condition; **and/or** (2) If BROADCAST MASK ENABLED/XOR* (bit 11 of Configuration Register #4) is logic "1" **and** the MASK BROADCAST bit of the message's BC Control Word is logic "0" **and** the BROADCAST COMMAND RECEIVED bit in the received RT Status Word is logic "1." Reference Table 91 and Table 93.

RETRY COUNT 1 AND RETRY COUNT 0 (bits 6, 5): Applicable only if ENHANCED MODE ENABLED **and** EXPANDED BC CONTROL WORD **and** the RETRY ENABLED bit (bit 4 of Configuration Register #1) is set to logic "1," **and** the RETRY ENABLED bit (bit 8) of the respective BC Control Word is set to logic "1." Also affected by the RETRY are the following bits, IF 1553A and MESSAGE ERROR bit (bit 10) and RETRY IF STATUS SET bit (bit 9) of Configuration Register #4 and the 1553 A/B* SELECT bit (bit 3) of the BC Control Word. The number of times that a message is retried is delineated by these two bits as shown in Table 95.

Table 95. Number of Message Retries

Retry Count 1 (bit 6)	Retry Count 0 (bit 5)	Number of Retries
0	0	0
0	1	1
1	0	2
1	1	2

GOOD DATA BLOCK TRANSFER (bit 4): Applicable only if ENHANCED MODE ENABLED. Set to logic "1" following completion of a valid (error-free) RT-to-BC transfer, RT-to-RT transfer, or transmit mode code with data message. This bit is set to logic "0" following an invalid message. GOOD DATA BLOCK TRANSFER is **always** logic "0" following a BC-to-RT transfer, or a mode code message. The Loop Test has **no effect** on GOOD DATA BLOCK TRANSFER. The GOOD DATA BLOCK TRANSFER may be used to determine if the transmitting portion of an RT-to-RT transfer was error free. An RT-to-RT transfer with both the ERROR FLAG and GOOD BLOCK TRANSFER bits set in Block Status Word indicates that the transmitting RT responded correctly, but there was an error detected in the receiving portion of the message.

WRONG STATUS ADDRESS/NO GAP (bit 3): Applicable only if ENHANCED MODE ENABLED. This bit is set if either or both of the following occur: (1) The RT address field of a responding RT does not match the RT address in the Command Word; and/or (2) If the GAP CHECK ENABLE, bit 8 of Configuration Register #5 is set to logic "1" **and** a responding RT responds with a response time of less than 4 µs, per MIL-STD-1553B (mid-parity bit to mid-sync).

WORD COUNT ERROR (bit 2): Applicable only if ENHANCED MODE ENABLED and for an RT-to-BC transfer, RT-to-RT transfer, or transmit mode code with data message. If set, indicates that a responding RT did not transmit the correct number of Data Words. Will always be logic "0" following a BC-to-RT transfer, receive mode code message, or transmit mode code without data message.

INCORRECT SYNC TYPE (bit 1): Applicable only if ENHANCED MODE ENABLED. If set, indicates that a responding RT responded with a Data sync in a Status Word and/or a Command/Status sync in a Data Word.

INVALID WORD (bit 0): Applicable only if ENHANCED MODE ENABLED. Indicates an RT responded with one or more words containing one or more of the following error types: sync field error, Manchester encoding error, parity error, and/or bit count error.

The second location of the legacy BC Message Block Description contains the Time Tag Word. The current value of the internal Time Tag Register is written to the Time Tag Word during both the BC Start-of-Message (SOM) and End-of-Message (EOM) transfer sequences.

INVALID WORD (bit 0): Applicable only if ENHANCED MODE ENABLED. Indicates an RT responded with one or more words containing one or more of the following error types: sync field error, Manchester encoding error, parity error, and/or bit count error.

The second location of the legacy BC Message Block Description contains the Time Tag Word. The current value of the internal Time Tag Register is written to the Time Tag Word during both the BC Start-of-Message (SOM) and End-of-Message (EOM) transfer sequences.

The third location of the legacy BC Message Block Descriptor is RESERVED in non-ENHANCED BC mode. This location contains the value of the programmed time-to-next message if ENHANCED MODE **and** MESSAGE GAP TIME ENABLED (bit #5 of Configuration Register #1) is programmed to logic "1." This location, which must be written by the host processor, is used to program the time from the start of the current message to the start of the subsequent message. It is programmable with a resolution of 1 µs/LSB and a maximum range of 65.535 ms.

The fourth location of the legacy BC mode descriptor is used to store the MESSAGE BLOCK ADDRESS Word. The host processor must write the MESSAGE BLOCK ADDRESS **before** the message is processed. It is then used as a pointer by the Enhanced Mini-ACE BC memory management logic for accessing the start of the respective Message Block.

For the legacy BC mode with ENHANCED MODE two other fixed locations in the shared RAM address space that must be initialized by the host processor are the Stack Pointer and Message Counter locations. The Stack Pointers are located in address locations 0100 (for Area A) and 0104 (for Area B). The Stack Pointer should be initialized to point to the first word of the Message Block Descriptor (Block Status Word) for the first message to be processed.

The Message Counters are located in addresses 0101 (for Area A) and 0105 (for Area B). The Active Area Message Counter must be preloaded by the host processor with the **ones complement** of the number of messages to be processed (i.e., FFFE represents a message count of 1). The Message Counter is incremented by one following each BC message processed.

Where ENHANCED MODE and the Enhanced Mini-ACE legacy BC is programmed for FRAME AUTO-REPEAT operation, the **initial** Stack Pointer (location 106,7) and initial Message Counter locations 102,3, rather than the Stack Pointer and Message Counter locations must be initialized.

5.6.5 BC Time-to-Next Message Time

The Enhanced Mini-ACE contains a programmable BC time-to-next message timer. This timer provides a 1 µs/LSB resolution, and a maximum value of 65.535 ms. The BC time-to-next message is defined as the time from the start of the current message to the start of the next message (reference Figure 6). The message gap timer is enabled if ENHANCED MODE **and** MESSAGE GAP TIMER ENABLE (bit 5 in Configuration Register #1) is programmed to logic "1."

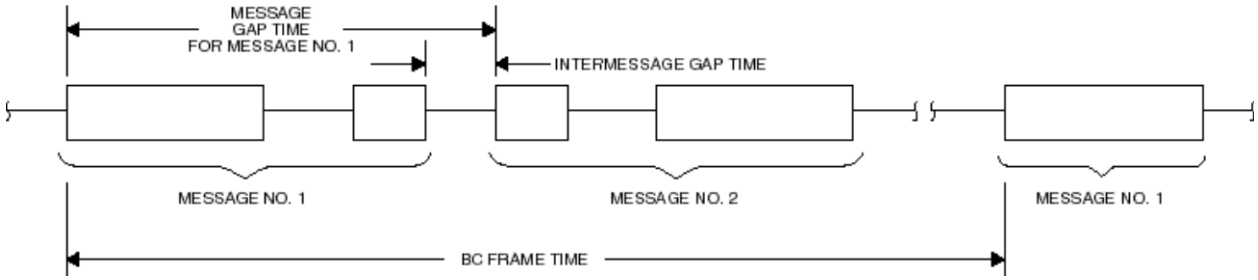


Figure 6. BC Time-to-Next Message Time

The value of the programmed time-to-next message time is stored in the third word location of the legacy BC stack descriptor for the respective message. If the message gap timer is disabled, this location in the descriptor stack is not used. Specifying a message gap time value that is less than the time of the current message will cause the next message to start **immediately** following the end of the current message. In this case, the message gap time defaults to the message time plus the minimum inter-message gap time, approximately 8 to 11 µs (measured from the last mid-parity zero crossing for the previous message to the first mid-sync crossing for the subsequent message). This feature allows the BC to implement minor frame cycle times with no host processor intervention.

5.6.6 BC Frame Auto-Repeat

The Enhanced Mini-ACE's legacy BC mode has the capability to define a BC frame which can run continuously based on an internal frame timer, an external hardware trigger, or under host processor control. The BC auto-repeat feature is only available if ENHANCED MODE ENABLE.

Enabling the legacy BC Frame Auto-Repeat mode requires that the BC Stack Pointer and BC Message Count values must be stored in the **INITIAL** BC STACK POINTER and **INITIAL** BC MESSAGE COUNTER fixed locations in RAM (word locations 0102 and 0103 for Area A or word locations 0106 and 0107 for Area B). Data should not be stored in the BC STACK POINTER and BC MESSAGE COUNT fixed locations in RAM (word locations 100 and 101 for area A or word locations 0104 and 0105 for Area B).

Upon receiving the BC trigger condition (software, internal, or external) the Enhanced Mini-ACE will read the values in the INITIAL BC STACK POINTER and INITIAL BC MESSAGE COUNTER locations and copy them into the current (as specified by CURRENT AREA B/A*) BC STACK POINTER and BC MESSAGE COUNT locations. Processing is then started in the BC frame. Two separate locations for these values are needed because the Enhanced Mini-ACE will modify the STACK POINTER and MESSAGE COUNT as the current BC frame is processed.

In the Frame Auto-Repeat mode, the frame time is programmable in increments of 100 µs/LSB by means of the BC Frame Time/RT Last Command/MT Trigger Register (register address 01101). This provides a range of programmable BC frame times up to a maximum value of 6.5535 seconds.

5.6.7 Minor and Major Frames

In many systems, the BC is required to process messages to the various RTs/subaddresses at a variety of periodicities. For example, some messages may be required to be transmitted at a 5 Hz rate, others at a 10 Hz rate, 20 Hz rate, . . . 100Hz, etc. A common mechanism for supporting varying data rates in a 1553 system is the use of minor and major frames, as illustrated in Figure 7.

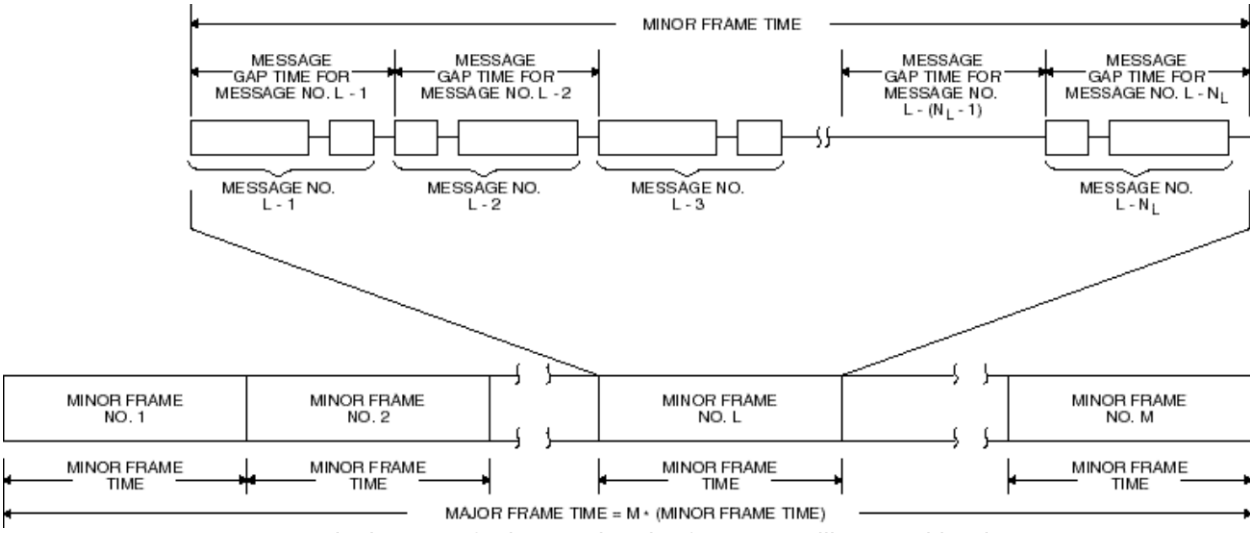


Figure 7. BC Major And Minor Frames

In the figure, the message scenario is organized into minor frames. A major frame comprises multiple minor frames. If the minor frame time is assumed to be 10 ms, message rates of up to 100 Hz may be supported. That is, a 100 Hz message will appear in **every** minor frame, a 50 Hz message in every other minor frame, ... while a 1 Hz message will appear once every 100 minor frames.

Using the Enhanced Mini-ACE legacy BC architecture, minor frame structures may be composed by means of the time-to-next message feature. The Enhanced Mini-ACE time-to-next message field specifies the time from the start of the current message to the start of the subsequent message. By judicious use of the time-to-next message, it is possible to formulate minor frames. The minor frame time is the sum of all time-to-next message times within a minor frame. All minor frame times are identical (e.g., 10 ms).

If the time required to process a message is longer than the programmed value of the message's time-to-next message, the message (including any retries) **will be processed to completion**. The resultant inter-message gap time prior to the next message will be approximately 8 to 11 µs. If automatic retries are used, it is recommended that the time-to-next-message times are set long enough to allow for a single or double retry, if possible. This will allow messages to be retried without overrunning the minor frame time, thus maintaining minor frame timing.

The BC major frame is comprised of a group of minor frames. To implement a major frame, the frame auto-repeat mode should be used. In this way, the Enhanced Mini-ACE frame time becomes the system major frame time. As an alternative, it may be desirable to synchronize the start of the major frame from a timing mechanism that is external to the Enhanced Mini-ACE . In this instance, INTERNAL TRIGGER ENABLE should be programmed to logic "0" and EXTERNAL TRIGGER ENABLE should be programmed to logic "1."

In this configuration, the start of the major frame will be triggered by a rising edge on the EXT_TRIG input.

5.6.8 BC Start Sequence and Options

The Enhanced Mini-ACE legacy BC offers several options for BC frame control. The Enhanced Mini-ACE legacy BC can be programmed to process either a single BC frame or repetitive frames. In addition, the start of the first BC frame may be initiated by either a software BC Start command or by a low-to-high ("0" to "1") transition on the EXT_TRIG input.

The BC start sequence configuration is defined by means of bits 8, 7, and 6 of Configuration Register #1. If FRAME AUTO-REPEAT (bit 8 of Configuration Register #1) is logic "0" **or** if INTERNAL TRIGGER ENABLED (bit 6 of Configuration Register #1) is logic "0," the Enhanced Mini-ACE BC will process **only a single message frame.** A message frame consists of from 1 to 512 messages, in accordance with the programmed value of the Message Count or Initial Message Count location. For more information refer to Table 96*.*

If FRAME AUTO-REPEAT is logic "1" **and** INTERNAL TRIGGER ENABLED is logic "1," then the BC is programmed for automatic repetitive frame operation. The timing diagram of Figure 7 illustrates the definition of the legacy BC frame time for the frame auto-repeat mode. Note that the BC frame is defined as the time from the beginning of the first message ("message #1") for one frame to the corresponding time in the subsequent frame.

The source of the values for Stack Pointer and Message Count is programmed by means of FRAME AUTO-REPEAT. If FRAME AUTO-REPEAT is logic "0," the Enhanced Mini-ACE BC protocol logic reads the active area Stack Pointer and Message Counter locations. If FRAME AUTO-REPEAT is logic "1," the BC protocol logic reads the addresses for the **Initial** Stack Pointer and **Initial** Message Counter. In the FRAME AUTO-REPEAT mode, the Stack Pointer and Message Counter locations are loaded at the beginning of every frame (from the values stored in the respective "Initial" locations) and incremented following every message processed.

For single-frame operation, or for starting the first frame for auto-repeat operation, the first message may always be initiated by means of a software BC START operation; that is, by writing 0002 (hex) to the Start/Reset Register. In addition, if EXTERNAL TRIGGER ENABLED (bit 7 of Configuration Register #1) is logic "1," the first BC frame may be initiated by means of an external signal; that is, by presenting a low-to-high transition on the Enhanced Mini-ACE's EXT_TRIG input. Table 96 summarizes the various BC START sequences.

Table 96. BC Start Sequences

FRAME AUTO-REPEAT (BIT 8 OF C.R. #1)	EXTERNAL TRIGGER ENABLED (BIT 7 OF C.R. #1)	INTERNAL TRIGGER ENABLED (BIT 6 OF C.R. #1)	BC START (REPEAT) SEQUENCE
0	0	X	Single frame; start by software BC Start command; Stack Pointer and Message Count must be loaded into locations 100, 101 (or 104, 105) prior to each frame.
0	1	X	Single frame; start by either software BC Start command or via EXT_TRIG input; Stack Pointer and Message Count must be loaded into locations 100, 101 (or 104, 105) prior to each frame.
1	0	0	Single frame; start by software BC Start command; Stack Pointer and Message Count must be loaded into locations 102, 103 (or 106, 107) one time.
1	0	1	Repeat frame; start first frame by software BC Start command; frame repeats in accordance with internal frame timer; Stack Pointer and Message Count must be loaded into locations 102, 103 (or 106, 107) one time.
1	1	0	Single frame; start by either software BC start or via EXT_TRIG input; Stack Pointer and Message Count must be loaded into locations 102, 103 (or 106, 107) one time.
1	1	1	Repeat frame; first frame is initiated by either software BC Start command or via EXT_TRIG input; frames repeat in accordance with the internal frame timer.

5.6.9 BC Interrupts

The Enhanced Mini-ACE legacy BC offers an array of conditions that can result in interrupt requests to the host CPU. These can be selected by means of Interrupt Mask Register #1. It should be noted that if ENHANCED INTERRUPTS are used, the host may determine that various events have occurred by polling the Interrupt Status Register. Using ENHANCED INTERRUPTS, the various bits in Interrupt Status Register #1 may become set to indicate the occurrence of conditions, regardless of the programming of the Interrupt Mask Register. The use of the eight possible BC interrupt conditions is summarized below. The bit number designations in parentheses refer to Interrupt Mask Register #1 and Interrupt Status Register #1.

BC END OF FRAME (bit 3): For most BC applications, it is desirable to issue an interrupt request following the completion of a multi-message frame of messages. This may be enabled by setting the BC_END_OF_FRAME bit in Interrupt Mask Register #1. In both single frame and frame auto-repeat modes, this interrupt will occur following the completion of each frame of messages.

END OF MESSAGE (bit 0): This interrupt will occur at the end of every message. For a retried message, the interrupt will occur after the **last** retry.

BC MESSAGE INTERRUPT (bit 4): Interrupts may be generated at the end of **selected** messages in ENHANCED BC Mode. This is enabled by configuring the Enhanced Mini-ACE for ENHANCED BC Mode by programming ENHANCED MODE (bit 15 in Configuration Register #3) to logic "1," **and** EXPANDED BC CONTROL WORD ENABLED (bit 12 of Configuration Register #4) for logic "1," **and** by setting the BC MESSAGE INTERRUPT bit (bit 4 in Interrupt Mask Register #1) to logic "1." In this mode, an EOM interrupt will be generated if the EOM INTERRUPT ENABLE bit, bit 4 in the BC Control Word, is programmed to logic "1."

FORMAT ERROR (bit 2): This interrupt request will be issued following any message containing an invalid word or wrong number of words.

RETRY (bit 8): This interrupt will occur after the **last** retry attempt (whether successful or unsuccessful) for any message that is retried.

STATUS SET (bit 1): This interrupt will be issued following a message with either an incorrect RT address in a Status Word and/or one or more bits set to logic "1" in the RT Status Word. If ENHANCED MODE ENABLE , Status Word bits that have been masked by the respective bits in the BC Control Word **will not** result in a STATUS SET interrupt.

COMMAND STACK ROLLOVER (bit 12): This interrupt request occurs when the BC Command Stack rolls over at a predefined boundary in the Enhanced Mini-ACE address space. This boundary (modulo address) is programmable from among 256, 512, 1024, or 2048 words.

TIME TAG ROLLOVER (bit 6): This interrupt occurs when the value of the Enhanced Mini-ACE 's Time Tag Register counter rolls over from FFFF to 0000.

5.7 Other BC Functions

5.7.1 Automatic Retries

The Enhanced Mini-ACE BC will perform automatic retries based on no response timeout, a message error, the Message Error Status Word bit set by a MIL-STD-1553A RT, or a Status Set condition. Retries can only be enabled in the ENHANCED mode. This requires the ENHANCED MODE. Retries are then enabled for individual messages by setting the RETRY ENABLE bit (bit 8) in the respective BC Control Word(s).

Retry Conditions: A no response timeout or a message format error will always cause a retry, if retry is enabled for the current message. A retry on a "status set" condition will only occur if the RETRY IF STATUS SET bit (bit 9 in Configuration Register #4) is set to logic "1." The status set condition is based on the status mask bits in the BC Control Word. A message format error condition occurs when:

a) the RT address in the status response does not match the RT address in the command word

or

b) an invalid word (parity, manchester error, etc.)

or

c) an incorrect sync type (for both status and data words)

or

d) a low or high word count.

A retry will also occur if the Message Error bit in the status word response is set to logic "1" **and** the 1553 A/B* SELECT bit (bit 3 in the BC Control Word) is set to logic "1" (1553A mode) **and** the RETRY IF -1553A AND MESSAGE ERROR bit (bit 10 in Configuration Register #5) is set to logic "1." The reason this retry is enabled for 1553A mode only is that in MIL-STD-1553B mode, the Message Error bit (S10) is used only to indicate illegal commands. MIL-STD-1553A, on the other hand, uses the Message Error bit as a means for the RT to indicate to the BC that it received a valid command, but one of the associated Data Words had a parity, Manchester encoding, or bit count error (a 1553B RT would not respond at all to this message).

Number of Retries: The Enhanced Mini-ACE will attempt a maximum of two retries before it indicates a no response timeout or other retry condition. The maximum number of retries that will be attempted for any particular message is programmable by means of DOUBLE/SINGLE* RETRY, bit 3 of Configuration Register #1. If DOUBLE/SINGLE* RETRY is logic "0," only one retry will be attempted; if DOUBLE/SINGLE* RETRY is logic "1," a maximum of two retries will be attempted.

Retry Channel Selection: The bus that the first retry is performed on (alternate or same, with respect to the original bus channel) is selected by the programming of the 1ST RETRY ALT/SAME* bit (bit 8 in Configuration Register #4). This bit should be programmed to logic "0" to cause the first retry to occur on the same bus, or to logic "1" to cause the first retry to occur on the alternate bus). If there is a second retry, the bus that the second retry is performed on is selected by the programming of 2ND RETRY ALT/SAME* bit (bit 7 in Configuration Register #4) to logic "0" for the same bus, or to logic "1," for the alternate bus. This allows for six possible retry scenarios: same, alternate, same/same, same/alternate, alternate/same, alternate/alternate.

Retry Block Status Word Bits: The End-of-Message for a retried message occurs **after** the completion of message retries, not after the initial failed message, or after an unsuccessful first of two retries. The Enhanced Mini-ACE writes the Block Status Word to shared RAM during the End-of-Message transfer sequence. RETRY COUNT 1 (bit 5 in the BC Block Status Word,) indicates that one retry occurred when it is set to logic "1." A logic "1" in the RETRY COUNT 2 bit (bit 6 in the Block Status Word) indicates that two retries were attempted. Logic "0" in both RETRY COUNT 1 and RETRY COUNT 2 indicates that no retries occurred. If the second retry fails, the message is aborted and the cause of the failure is stored in the Block Status Word (no response timeout, format error, Status Set, etc).

Retry Interrupts: If enabled by the Interrupt Mask Register, the EOM and/or BC RETRY interrupt requests will be issued **after** the completion of the message retries, for either an unsuccessful retry **or** a successful retry.

If a retry is enabled for a particular message, the retry **will** be attempted even if one or more of the following bits of Configuration Register #1 (bits 12 through 9) are set to logic "1": MESSAGE STOP-ON-ERROR, FRAME STOP-ON-ERROR, STATUS SET STOP-ON-MESSAGE, and STATUS SET STOP-ON-FRAME. Assuming that MESSAGE or FRAME STOP-ON-ERROR is set and that the retry(ies) is(are) not successful, the processing of BC messages will stop at the end of the current message or message frame. However, the processing of subsequent BC messages within a frame and/or the processing of subsequent BC frames **will continue** if a failed message is successfully retried.

5.7.2 BC Response Timeout

MIL-STD-1553B defines RT response time as the delay from the mid-parity zero crossing of the parity bit of the last word received from the BC (or another RT) to the mid-sync zero crossing of the RT's Status Word. In accordance with this definition, the -1553B standard specifies that an RT must respond within 12 µs and that a BC must wait a **minimum** of 14 µs before determining that an RT "no response" has occurred.

The response timeout value for the Enhanced Mini-ACE bus controller is software programmable. If ENHANCED MODE DISABLED, the value of the BC response timeout timer defaults to a nominal value of 18.5 µs. If ENHANCED MODE ENABLE the Enhanced Mini-ACE supports the use of long buses and/or repeaters by allowing the nominal value of the BC timeout to be selected from among 18.5, 22.5, 50.5, and 130 µs by means of bits 10 and 9 (RESPONSE TIMEOUT 1, 0) of Configuration Register #5. Refer to Table 97.

Table 97. BC Response Timeout Select

Bit 10 Response Timeout Select 1	Bit 9 Response Timeout Select 0	Response Timeout Time Value (µs)
0	0	18.5
0	1	22.5
1	0	50.5
1	1	130

Note: Default value for non-ENHANCED mode is 18.5 µs.

5.7.3 BC Status Word Masking

The Enhanced Mini-ACE BC has the capability of masking selected Status Word bits for individual messages in a BC frame, assuming that ENHANCED MODE ENABLE **and** EXPANDED BC CONTROL WORD ENABLE. Status word masking is applicable to both legacy and enhanced BC modes.

If ENHANCED MODE DISABLE **or** if EXPANDED BC CONTROL WORD DISABLE, only bits 7, 6, 5, 2, 1, and 0 of the BC Control Word are operative. In this case, the only operative "Status Mask" bit in the BC Control Word is MASK BROADCAST (bit 5). However, if ENHANCED MODE ENABLE **and** EXPANDED BC CONTROL WORD ENABLE , **all 15** bits of the BC Control Word (bits 14 through 0), including **all** of the "Status Mask" bits (bits 14 through 9, and bit 6) are operative.

The Status Word Mask bits, in the BC Control Word, control which bits in the responding RT Status Word(s) will cause a "Status Set" condition to occur. A "Status Set" condition will:

a) cause a bit to be set in the Block Status Word

b) can cause an interrupt

c) can halt the BC after the current message or at the end of the current BC frame and/or initiate an automatic retry.

A logic "1" in the proper bit position in the BC Control Word will cause the Enhanced Mini-ACE to **ignore ("don't care")** about the logic sense of the respective RT Status Word Bit. Any designated subset of the following bits may be enabled in determining a Status Set condition: Message Error, Service Request, Busy, Subsystem flag, Terminal flag, and/or the Reserved bits. The Broadcast bit (S04) can either be masked (ignored) or verified to be logic "0" or logic "1." If the corresponding mask bit is programmed to logic "0," the bit **is included** in determining if a "Status Mask" condition occurs.

With the exception of the Broadcast Command Received Status Word bit, the effect of the ENHANCED MODE, EXPANDED BC CONTROL WORD ENABLE, the various "Status Mask" BC Control Word bits, and the value of the respective received RT Status Word on the "Masked Status Set" condition is summarized in Table 98*.*

Table 98. Operation of Status Masking (Other Than Broadcast Command Received)

Enhanced Mode (bit 15 of Configuration Register #3)	Expanded BC Control Word Enabled (bit 12 of Configuration Register #4)	"MASK" bit for the particular Status Word bit (in BC Control Word)	Value of the respective bit in Received RT Status Word	Masked Status Set Condition
0	X	X	X	No
Or				
X	0			
1	1	0	0	No
		0	1	Yes
		1	0	No
		1	1	No

The function of the Broadcast Mask Bit is determined by the value of the BRDCST MASK ENA/XOR* bit (bit 11 in Configuration Register #4). If the BRDCST MASK ENA/XOR* bit is programmed to logic "1," a value of logic "1" in the BC Control Word MASK BROADCAST bit (bit 5) will result in the Broadcast Command Received bit in the responding RT Status Word(s) to be ignored ("don't care"), while a logic "0" in the

MASK BROADCAST bit will result in a STATUS SET condition, if the Broadcast Command Received bit in the RT Status Word is logic "1."

Programming BRDCST MASK ENA/XOR* to logic “0” will cause the Enhanced Mini-ACE to compare the Broadcast Bit in the received RT Status Word to the value in the MASK BROADCAST BIT (bit 5 in the BC Control Word). In the case that they **do not match,** a "Status Set" condition will be generated. The operation of the BRDCST MASK ENA/XOR* and MASK BROADCAST bits is summarized in Table 99*.*

Table 99. Operation of Status Masking (Including Broadcast Command Received)

Enhanced Mode (bit 15 of Configuration Register #3)	Broadcast Mask Enabled/XOR* (bit 11 Configuration Register #4)	Expanded BC Control Word Enabled (bit 12 of Configuration Register #4)	Mask Broadcast (bit 5 of BC Control Words	Value of "Broadcast Command Received" bit in Received RT StatusWord	Masked Status Set Condition
0	X	X	0	0	No
OR			0	1	Yes
			1	0	Yes
1	0	X	1	1	No
1	1	X	0	0	No
			0	1	Yes
			1	0	No
			1	1	No

The Block Status Word contains two bits describing the status set condition. The first is the STATUS SET bit (bit 11). This bit will be set to logic "1" if **any** of the bits in the status response are logic "1" regardless of the status mask. MASKED STATUS SET 2 (bit 7) will only be set to logic "1" if a bit in the Status Word response is set **and** that bit is not masked by the status mask in the BC Control Word (with the exception of the Broadcast Command Received bit "expected value" option, as described above).

An interrupt will be generated for a Status Set condition (based on the status mask criteria) in the ENHANCED BC Mode, if the BC STATUS SET bit (bit 1 in the Interrupt Status Mask) is set to logic "1.” The interrupt will occur at the end of the current message (EOM), not immediately following the receipt of the Status Word (in the case of a transmit command).

A Status Set condition, assuming that ENHANCED MODE, can cause the bus controller to halt in one of two ways. First, if the MESSAGE STOP-ON-ERROR bit (bit 12 in Configuration Register #1) is set to logic "1,” the BC will halt the current frame upon completion of the current message. In the FRAME AUTO-REPEAT mode, if STATUS SET STOP-ON-FRAME (bit 9 in Configuration Register #1) is set to logic "1,” the BC will halt the current frame upon completion of the last message in the frame, if a Status Set condition occurs.

5.7.4 Legacy BC Software Initialization Sequence

The following software sequence is typical of the steps the host processor should perform following power turn-on to configure the Enhanced Mini-ACE for legacy BC operation. For most applications, many of the steps indicated may be skipped.

1. Perform a software reset, by writing a value of 0001 (hex) to the Start/Reset Register.

2. If any of the ENHANCED mode functions (e.g., use of programmable retries, message gaps, expanded BC Control Word, etc.) are to be used, invoke the Enhanced Mini-ACE 's ENHANCED MODE by writing a value of 8000 (hex) to Configuration Register #3.

3. Initialize Interrupt Mask Register #1. For most BC applications, the BC END-OF- FRAME interrupt should be enabled. The END-OF-MESSAGE (EOM) bit causes an interrupt request to be issued following the end of **every** completed message. BC CONTROL WORD interrupt allows interrupt requests to be issued following completion of **selected** (by means of the BC Control Word) messages. BC RETRY will result in an interrupt **after** a message is retried (either successfully or, unsuccessfully).

FORMAT ERROR will cause an interrupt request to be issued following any RT response containing either a word error (sync or Manchester encoding, bit count, or parity error) or a high or low word count error. A STATUS SET interrupt results from one of three conditions: (1) A non-matching RT address in the Status Word from a responding RT; (2) If EXPANDED BC CONTROL WORD is not enabled, one or more of the 8 non-reserved Status Word bits is logic "1"; or (3) If EXPANDED BC CONTROL WORD is enabled, and for one or more of the RT Status Word bits the respective Status Mask bit in the BC Control Word is programmed for "care" (logic "0") **and** the value of the received RT Status Word bit is logic "1."

Initialize Configuration Register #1. Bits 15 and 14 must both be initialized to logic "0" to configure the Enhanced Mini-ACE for BC mode. CURRENT AREA B/A* should be designated. MESSAGE STOP-ON-ERROR, FRAME-STOP-ON-ERROR, MESSAGE-STOP-ON-STATUS SET, and FRAME-STOP-ON-STATUS SET should be selected, if desired. The STOP-ON-ERROR bits enable a "graceful halt" (at the **end** of the current message or frame) in the case of a response timeout, format error or loop test failure. The STOP-ON-STATUS SET bits enable a "graceful halt" condition for a "Status Set" condition, as defined above. It should be noted that if a message retry is enabled for a particular message, the retry would be attempted **before** the "stop" takes place. That is, if the retry is successful, the message frame will **continue** (will not stop). If the retry (one or two retries) is unsuccessful, then the processing of messages will be aborted at the end of the current message or frame.

If it is desired to initiate a BC frame using the EXT_TRIG input, EXTERNAL TRIGGER ENABLED must be programmed to logic "1." Regardless of the programming of EXTERNAL TRIGGER ENABLED and INTERNAL TRIGGER ENABLED, a BC frame may be initiated by means of a software BC START command. If it is desired to have the programmed BC frame repeat automatically (with no host processor intervention), it is necessary to program FRAME AUTO-REPEAT **and** INTERNAL TRIGGER to logic "1." If it desirable to start the first BC frame via the EXT_TRIG input and have the frame automatically repeat subsequently, FRAME AUTO-REPEAT, INTERNAL TRIGGER ENABLED and EXTERNAL TRIGGER ENABLED must be programmed to logic "1."

In order to control the BC message gap times using the third word of the BC Block Descriptor, MESSAGE GAP TIME ENABLED must be programmed to logic "1." If MESSAGE GAP TIME ENABLED is logic "0," the start-of-current message to start-of-subsequent message time will default such that the BC's inter-message gap time (as defined by MIL-STD-1553B) defaults to its minimum value of approximately 9 μs.

If message retries are to be enabled by means of bit 8 of the BC Control Words (RETRY ENABLED), it is necessary to program RETRY ENABLED to logic "1." If retries are enabled, the maximum number of retries for each message (either 1 or 2) is specified by means of DOUBLE/SINGLE* RETRY.

4. Initialize Configuration Register #2. For BC mode, it is strongly recommended that 256-WORD BOUNDARIES DISABLED be set to logic "1" in order to make best use of the Enhanced Mini-ACE's address space for BC message blocks. LEVEL/PULSE* INTERRUPT should be initialized to logic "1" if the host CPU requires a level, rather than a pulse, type of interrupt request input signal. TIME-TAG RESOLUTION 2-0 should be programmed to initialize the resolution of the Time-Tag Register. The default resolution ("000") is 64 μs/LSB.

5. Initialize Configuration Register #3. If any of the lower 15 bits of this register or any of the other ENHANCED mode features are to be used, ENHANCED MODE ENABLED (bit 15) must be maintained at logic "1" while writing to this register. The size of the Stack may be programmed by means of bits 14 and 13. The choices for the stack size are 256 words (default, for 64 BC messages), 512, 1024, and 2048 words (512 messages).

6. Initialize Configuration Register #4. In order to allow the use of bits 15-8, 4, and 3 of the BC Control Word, EXPANDED BC CONTROL WORD must be set to logic "1." This includes use of the Status Word Masking function, retries, 1553A/B selection, and interrupts on a message basis. BROADCAST MASK ENABLED/XOR* should be programmed to logic "1" if it is desired to use the "MASK BROADCAST BIT" (bit 5) of the BC Control Word as an actual mask, rather than to specify the anticipated value of the Broadcast Command Received bit in the RT Status Word.

RETRY IF -1553A AND MESSAGE ERROR should be set if it is desired to retry messages in which the 1553A/B* SELECT bit (bit 3) of the BC Control Word is logic "1" and the Message Error bit is logic "1" in the RT Status Word. RETRY IF STATUS SET should be set to logic "1" if it is desired to retry messages in which one or more of the "unmasked" Status Word bits is logic "1" in the RT Status Word. A Status Word bit is considered "unmasked" if the corresponding "MASK" bit in the BC Control Word has been programmed to logic "0."

If VALID BUSY/NO DATA and/or VALID MESSAGE ERROR/NO DATA is set logic "1," an RT response will be considered valid if the BUSY (MESSAGE ERROR) bit(s) is set in the RT Status Word and there are no following Data Words. Otherwise, such an RT response will be considered invalid. Message validity affects the setting of the FORMAT ERROR bit in the Block Status Word, the issuing of interrupts, and message retries.

Initialize Configuration Register #5. The default clock frequency for the Enhanced Mini-ACE is 16 MHz. To select 12 MHz operation, 12 MHZ SELECT may be programmed to logic "1."

7. RESPONSE TIMEOUT SELECT 1-0 selects the time value for the BC response timeout from among 18.5 µs (default), 22.5, 50.5, or 130 µs. If GAP CHECK ENABLED is set to logic "1," the BC will verify for a minimum bus dead time of 2 µs prior to RT responses. If this gap time is violated, the BC will set the FORMAT ERROR bit in the Block Status Word. As a result, an ERROR interrupt may be issued and/or the message may be retried.

8. If desired, initialize the Time Tag Register. It should be noted that the value of the Time-Tag Register may be reset to zero concurrent with the BC Start by writing logic "1" to the TIME-TAG RESET bit of the Start/Reset Register as part of step (15).

9. Initialize CR#6 with logic “1” in bit 14 to enable Enhanced CPU Access and bits 0 & 1 if desired to change base clock frequency.

10. If using the Frame Auto-Repeat mode (FRAME AUTO-REPEAT and INTERNAL TRIGGER ENABLED bits of Configuration Register #1 programmed to logic "1"), initialize the BC Frame Time Register. This register is programmable with a resolution of 100 µs/LSB.

11. Load the starting location of the Stack into the active area Stack Pointer RAM location. If the Frame Auto-Repeat mode is to be used, the Initial Stack Pointer RAM location for the active area should also be loaded.

12. Initialize the Active Area Stack. For the message descriptor for each message to be processed, the Message Block Address, providing the pointer to the first word of the respective BC message block (the BC Control Word) must be written by the host processor.

If the Message Gap-Time feature is used, the Message Gap-Time word must also be written for each message. The resolution of the Message Gap-Time Word is 1 µs/LSB. The programmed value of the Message Gap-Time field represents the time from the **start** of the current message to the **start** of the subsequent message. If this time is less than the time required for the current message, the gap prior to the start of the subsequent message defaults to the minimum value of approximately 9 µs.

If it is desired to poll the stack during the processing of the BC frame, it is recommended that the values of the Block Status Words be initialized to zero by the host CPU.

13. Load the BC Control, Command, and Data Words to be transmitted into the respective BC message blocks. Optionally, the locations of the anticipated Loopback Words should be loaded with a **different** bit pattern than the last word to be transmitted by the BC. The host processor must ensure that sufficient address locations are allocated after the last word to be transmitted to accommodate the Loopback Word and anticipated received Status and Data Words.

14. The Active Area Message Count location should be loaded with the **ones complement** of the number of messages to be processed in the frame. If the Frame Auto-Repeat mode is to be used, the Initial Message Count RAM location for the active area should be loaded.

15. If EXTERNAL TRIGGER ENABLED is programmed to logic "0," a BC frame must be initiated by performing a BC START operation. This is invoked by writing a value of 0002 (hex) to the Start/Reset Register. If EXTERNAL TRIGGER ENABLED is programmed to logic "1," a BC frame may be initiated either by a BC START operation or by applying a rising edge on the EXT_TRIG input.

5.7.5 Legacy BC Pseudo Code Example

The following example illustrates the programming steps necessary to initialize the Enhanced Mini-ACE legacy BC and initiate a frame of messages.

As illustrated in Figure 8, the example consists of three messages: a BC-to-RT transfer, an RT-to-RT transfer, and a Synchronize with data mode code message.

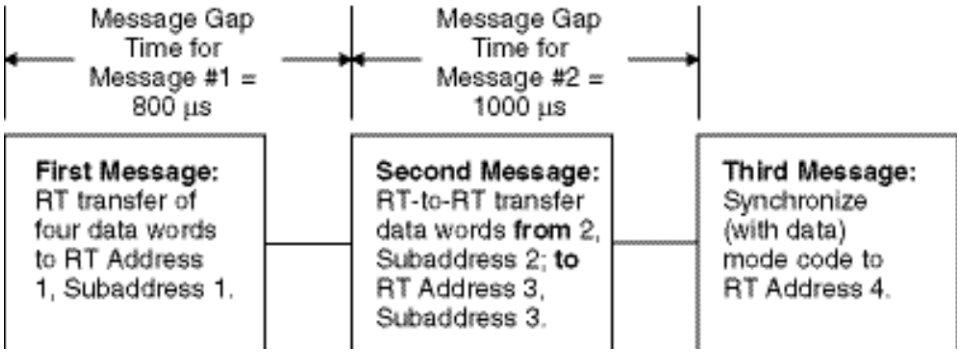


Figure 8. Message Sequence For Legacy BC Pseudo Code Example

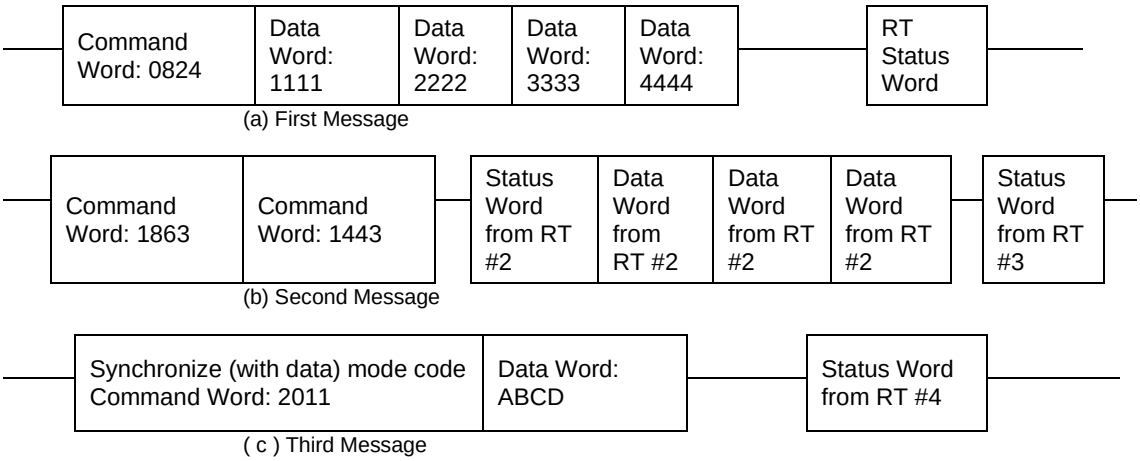


Figure 9. Messages For BC Pseudo Code Example: (a) First Message, (b) Second Message, (c) Third Message

Table 100 Illustrates the memory map to program the example sequences of messages.

Table 100. Memory Map For BC Example Pseudo Code

Address	Data	Description	Portion of Memory, Comment
0	0	Message #1 Block Status Word.	Message #1 Block Descriptor (in Stack Area). Note that the Block Status Word and Time Tag locations are initialized to 0000. The Enhanced Mini-ACE will overwrite these locations when the Message is processed.
1	0	Message #1 Time-Tag Word.	
2	320	800 µs Message Gap-Time Word for Message #1.	
3	108	Message Block Pointer for Message #1.	
4	0	Message #2 Block Status Word.	Message #2 Block Descriptor (in Stack Area). Note that the Block Status Word and Time Tag locations are initialized to 0000. The Enhanced Mini-ACE will overwrite these locations when the Message is processed.
5	0	Message #2 Time-Tag Word.	
6	3E8	1000 µs Message Gap-Time Word for Message #2.	
7	110	Message Block Pointer for Message #2.	
8	0	Message #3 Block Status Word.	Message #3 Block Descriptor (in Stack Area). Note that the Block Status Word and Time Tag locations are initialized to 0000. The Enhanced Mini-ACE will overwrite these locations when the Message is processed.
9	0	Message #3 Time-Tag Word.	
00A	0	0 µs Message Gap- Time Word for Message #3 (doesn't matter).	
00B	119	Message Block Pointer for Message #3.	
100	0	Active Area (Area A) Stack Pointer.	Fixed locations
101	FFFC	Active Area (Area A) Message Count Register. Note that 00FC is the ones complement of the number of messages to be processed (3).	
108	90	BC Control Word for Message #1. Note that for this message, a "BC Control Word" interrupt is enabled. Also, the message will be transmitted on Channel A.	Message Block for Message #1.
109	824	Command Word for Message #1.	
10A	1111	First Data Word to be transmitted for Message #1.	
10B	2222	Second Data Word to be transmitted for Message #1.	
10C	3333	Third Data Word to be transmitted for Message #1.	
10D	4444	Fourth Data Word to be transmitted for Message #1.	
10E	0	Location for anticipated loopback of data word #4.	
10F	0	Location for anticipated received Status Word for Message #1 programmed to 0000.	
110	101	BC Control Word for Message #2. Note that for this message, retries are enabled, the message will be processed on Channel B, and the message format is an RT-to-RT transfer.	Message Block for Message #2
111	1863	Receive Command Word (to RT Address #3).	
112	1443	Transmit Command Word (to RT Address #2).	
113	0	Location for anticipated loopback of transmit command.	
114	0	Anticipated location for received Status Word from the transmitting RT (RT Address #2).	
115	0	Anticipated location for the first received Data Word from RT #2.	
116	0	Location for the second anticipated received Data Word from RT #2.	
117	0	Location for the third anticipated received Data Word from RT #2.	
118	0	Location for the anticipated received Status Word from the receiving RT (RT Address #3).	
119	84	BC Control Word for Message #3. The message will be processed on Channel A, and is a mode-code message.	Message Block for message #3.
11A	2011	Synchronize with data mode-code Command Word to RT Address 4.	
11B	ABCD	Data Word associated for the Synchronize mode command.	
11C	0	Location for anticipated loopback of data word.	
11D	0	Location for anticipated received Status Word from the receiving RT (RT Address #4).	

5.7.6 Pseudo Code

The following pseudo code is the series of register and memory write transfers required to initiate the example message frame sequence. The notation "Rxy ←" represents a write access to Enhanced Mini-ACE register address xy. The notation "Mwxyz ←" represents a write access to Enhanced Mini-ACE shared RAM address wxyz.

R03 ← 0001-Software reset via the Start/Reset Register
R07 ← 8000-Set ENHANCED MODE bit in Configuration Register #3 to enable enhanced
BC features (retries, Message gap times, etc.)
R00 ← 0018-Interrupt Mask Register: Enable interrupts for BC Control Word (individual
message(s)) and BC_END_OF_FRAME
R01 ← 0030-Configuration Register #1: Configures for BC mode, enables variable Message gap times and message retries
R02 ← 0408-Configuration Register #2: Enables 256-WORD BOUNDARIES DISABLED,
Level interrupt
R08 ← 1060-Configuration Register #4: Enables EXPANDED BC CONTROL WORD, VALID BUSY/NO DATA, VALID MESSAGE ERROR/NO DATA
R09 ← 0A00-Configuration Register #5: Enables EXPANDED ZERO CROSSING, programs BC Response Timeout to 22.5 µs
R05 ← 0000-Initialize Time-Tag Counter Register to 0000
R18 ← 4000-Set Enhanced CPU Access
M0100 ← 0000-Initialize Area A Stack Pointer to 0000
M0101 ← FFFC-Initialize Area A Message Counter for three messages
M0000 ← 0000-Initialize Message #1 Block Status Word
M0001 ← 0000-Initialize Message #1 Time-Tag Word
M0002 ← 0320-Message #1 Message Gap-Time Word
M0003 ← 0108-Message #1 Message Block Pointer
M0004 ← 0000-Initialize Message #2 Block Status Word
M0005 ← 0000-Initialize Message #2 Time-Tag Word
M0006 ← 03E8-Message #2 Message Gap-Time Word
M0007 ← 0110-Message #2 Message Block Pointer
M0008 ← 0000-Initialize Message #3 Block Status Word
M0009 ← 0000-Initialize Message #3 Time-Tag Word
M000A ← 0000-Message #3 Message Gap-Time Word
M000B ← 0119-Message #3 Message Block Pointer
M0108 ← 0090-BC Control Word for Message #1
M0109 ← 0824-Command Word for Message #1
M010A ← 1111-First Data Word for Message #1
M010B ← 2222-Second Data Word for Message #1
M010C ← 3333-Third Data Word for Message #1
M010D ← 4444-Fourth Data Word for Message #1
M010E ← 0000-Initialize Loopback word location
M010F ← 0000-Initialize Message #1 anticipated Status Word location

M0110 ← 0101-BC Control Word for Message #2
M0111 ← 1863-First Command Word (receive command) for Message #2
M0112 ← 1443-Second Command Word (transmit command) for Message #2
M0113 ← 0000-Initialize Loopback word location
M0114 ← 0000-Initialize location for anticipated transmitting RT Status Word
M0115 ← 0000-Initialize location for first anticipated received Data Word
M0116 ← 0000-Initialize location for second anticipated received Data Word
M0117 ← 0000-Initialize location for third anticipated received Data Word
M0118 ← 0000-Initialize location for anticipated receiving RT Status Word for Message #2
M0119 ← 0084-BC Control Word for Message #3
M011A ← 2011-Command Word for Message #3
M011B ← ABCD-Data Word for Message #3
M011C ← 0000-Initialize Loopback word location
M011D ← 0000-Initialize location for anticipated received Status Word for Message #3
R03 ← 0002-Start/Reset Register: BC START command, to initiate (single) message frame

5.7.7 Servicing In-Progress or Completed BC Frames

In the Enhanced Mini-ACE's legacy BC mode, the end of BC messages and frames may be determined by means of either polling or interrupt techniques.

There are several polling techniques that may be used. These involve bits in either Configuration Register #1 or the Interrupt Status Register. In addition, the active area Stack Pointer and Message Count Register may be polled. The Stack Pointer increments by four at the end of each BC message. At the end of a BC frame, it will point to **4 locations beyond (modulo the stack size)** the first word of the message block descriptor (the location of the BlockStatus Word), for the last message of the BC frame. The Message Counter increments by one at the end of each BC message. When the frame has been completed, the Message Count location will have a value of FFFF (hex).

If ENHANCED MODE ENABLED, the lower three bits of Configuration Register #1 may be polled as a means of determining BC status. BC ENABLED (bit 2) will return logic "1" after a BC frame has been initiated (by either a BC START command or from an external trigger) and up to the time that a single frame has completed or repeat frames have been halted. BC ENABLED will then transition to logic "0."

BC FRAME IN PROGRESS is similar to BC ENABLED, with the following exception: In the frame auto-repeat mode, BC FRAME IN PROGRESS will return logic "0" during the time following the End-of-Message (EOM) sequence for the last message of the frame, up to the beginning of the Start-of-Message (SOM) sequence for the first message of the subsequent frame. BC MESSAGE IN PROGRESS will return logic "1" between the time of the SOM sequence and the EOM sequence for each message processed.

If ENHANCED INTERRUPTS are enabled (bit 15 of Configuration Register #2 programmed to logic "1"), and the Interrupt Mask Register is programmed to logic "0" (disabling interrupt requests from the Enhanced Mini-ACE), the Interrupt Status Register may still be polled for a number of conditions in BC mode. These include BC COMMAND STACK ROLLOVER (bit 11), BC RETRY (bit 8), TIME TAG ROLLOVER (bit 6), BC MESSAGE INTERRUPT (bit 4), BC END OF FRAME (bit 3), FORMAT ERROR (bit 2), STATUS SET (bit 1), and END OF MESSAGE (bit 0).

Note: *Any of the conditions listed in the previous paragraph may also be used to trigger an interrupt request to the host CPU. In most systems, an interrupt request will be enabled to signify a BC END OF FRAME condition. This indicates that a BC frame has been completed. In other systems the BC RETRY interrupt request (for **selected** messages, as programmed in the BC Control Words) or the END-OF-MESSAGE interrupt request (for **all** messages) may be used.*

The FORMAT ERROR and BC RETRY interrupt conditions may be used to inform the host of any bus error conditions. STATUS SET may be used to indicate to the CPU that one of the unmasked Status Word bits has been set in a responding RT's Status Word. A particular Status Word bit may be enabled to cause a Status Set condition by programming the respective Status Mask bit BC Control Word to logic "0."

The Status Mask bits may be used in conjunction with the STATUS SET STOP-ON-MESSAGE (bit 10) of Configuration Register #1. In this way (or via the ERROR-STOP-ON-MESSAGE bit), the host is able to interject asynchronous messages. An example of such an asynchronous message is for the BC to process a single-message frame consisting of a Transmit Vector Word mode command following reception of an RT Status Word with the Service Request bit set. After the host has processed this message and captured the RT's Vector Word, it may then resume processing of the in-line BC frame.

5.7.8 Terminating of BC Frames

Under most circumstances, a programmed legacy BC frame will process all of the programmed messages in the frame. That is, the Enhanced Mini-ACE BC will continue to process messages until the Message Count location has incremented to FFFF. In the frame auto-repeat mode with INTERNAL TRIGGER ENABLED, the subsequent BC frame will automatically restart after one frame has been completed.

The Enhanced Mini-ACE provides a number of mechanisms for aborting BC frames. Bits 12 through 9 of Configuration Register #1 provide mechanisms for automatically halting the Enhanced Mini-ACE BC. If set to logic "1," ERROR STOP-ON-MESSAGE and STATUS SET STOP-ON-MESSAGE will cause the Enhanced Mini-ACE BC to stop processing messages at the end of the **current message,** if a Format Error or Status Set condition occurs. If the Enhanced Mini-ACE BC is programmed for the frame auto-repeat mode, ERROR STOP-ON-FRAME and STATUS SET STOP-ON-FRAME will cause the Enhanced Mini-ACE BC to stop processing messages at the end of the **current frame,** if a Format Error or Status Set condition occurs.

Some of the bits in the Start/Reset Register provide a mechanism for the host CPU to terminate the processing of messages by the host BC. RESET will result in an **immediate** (that is, aborting the current message) termination of message processing. BC STOP- ON-MESSAGE and BC STOP-ON-FRAME will cause the Enhanced Mini-ACE to terminate message processing at the **end** of the current message or frame.

5.7.9 Bus Controller Start-of-Message, End-of-Message, and Retry Transfer Sequences

At the start and end of each message, and prior to the processing of a message retry, the Enhanced Mini-ACE performs the following sequences of transfers from/to the shared RAM:

5.7.10 BC Start-of-Message (SOM) Sequence

1. The Stack Pointer is read from the active area Stack Pointer location. This address is used for accessing the BC descriptor block in the active area Command Stack.

2. The Message Gap-Time word is read from the third location in the block descriptor.

3. The Message Block Pointer word is read from the fourth location in the block descriptor. This pointer provides the starting address of the BC message block (address of the BC Control Word).

4. The BC Control Word is read from the first location in the BC message block.

5. The (first) Command Word is read from the second location in the BC message block.

6. The Time-Tag word is written to the second location in the block descriptor.

7. The Block Status Word is written to the first location in the block descriptor.

5.7.11 BC End-of-Message (EOM) Sequence

1. The Message Count word is read from the active area Message Counter location. If the value of this word is less than FFFF (hex), the Enhanced Mini-ACE (internally) increments the value by one. If the value of this word is equal to FFFF (hex), this denotes that the current message is the last message of the frame. The current frame is terminated following the end of the current EOM sequence.

2. The Time-Tag word is written to the second location in the block descriptor.

1. The Block Status Word is written to the first location in the block descriptor.

2. The Message Count Word is written to the active area Message Counter location.

5. The value of the Stack Pointer is incremented by four. The updated value is written to the active area Stack Pointer location.

5.7.12 BC Message Retry Sequence

1. The Message Count word is read from the active area Message Counter location.

2. The BC Control Word is read from the first location in the BC message block.

3. The (first) Command Word is read from the second location in the BC message block.

5.7.13 BC Exception Conditions

In response to various message errors and other exception conditions, the Enhanced Mini-ACE bus controller takes actions and provides a number of indications. Table 101 indicates the respective Block Status Word bits that will be set, automatic retry activity, and interrupt requests that are issued and Status Register bits that become set as a result of these conditions.

Table 101. BC Exception Conditions				
	BLOCK STATUS WORD BITS	**AUTOMATIC RETRIES**	**INTERRUPTS, INTERRUPT STATUS WORD BITS**	**OTHER EFFECTS**
NO RESPONSE	ERROR FLAG, NO RESPONSE TIMEOUT, RETRY COUNT(1,0) (if enabled)	YES	FORMAT ERROR, BC RETRY (if enabled)	
RECEIVED WORD COUNT ERROR	ERROR FLAG, WORD COUNT ERROR, FORMAT ERROR, RETRY COUNT(1,0)(if enabled)	YES	FORMAT ERROR, BC RETRY (if enabled)	
INCORRECT RECEIVED SYNC TYPE	ERROR FLAG, INCORRECT SYNC TYPE, FORMAT ERROR, RETRY COUNT (0,1)(if enabled)	YES	FORMAT ERROR, BC RETRY (if enabled)	
INVALID RECEIVED WORD (MANCHESTER ENCODING, BIT COUNT, OR PARITY)	ERROR FLAG, FORMAT ERROR, INVALID WORD, RETRY COUNT(1,0)(if enabled)	YES	FORMAT ERROR, BC RETRY (if enabled)	**Note:** If the Enhanced Mini-ACE BC receives an invalid Data Word, it will continue to receive (but not store) all subsequent, contiguous Data Words. It will wait until it senses an idle bus before performing an EOM or retry transfer sequence, performing a message retry, or transmitting the next message.
WRONG RT ADDRESS IN RECEIVED STATUS WORD	ERROR FLAG, WRONG STATUS ADDRESS/NO GAP, FORMAT ERROR, RETRY COUNT(1,0)(if enabled)	YES	STATUS SET, BC RETRY (if retry enabled for Status Set)	

Table 101. BC Exception Conditions				
	BLOCK STATUS WORD BITS	**AUTOMATIC RETRIES**	**INTERRUPTS, INTERRUPT STATUS WORD BITS**	**OTHER EFFECTS**
HANDSHAKE FAIL. **Note** : In BC mode, a Handshake Failure will not occur during a Start-of-Message (SOM), End-of-Message (EOM), or Retry transfer sequence. A Handshake Failure can occur during the transfer of a second Command Word (for an RT-to-RT transfer), Data Word, or RT Status Word. A HANDSHAKE FAILURE CAN OCCUR IN THE TRANSPARENT MODE ONLY, NOT IN THE BUFFERED.	BLOCK STATUS WORD FROM START-OF-MESSAGE	NO	HANDSHAKE FAIL	BC FRAME IS TERMINATED
LESS THAN 2μs GAP BEFORE STATUS WORD RESPONSE AND ENHANCED MODE AND GAP CHECK ENABLED, BIT 7 OF CONFIGURATION REGISTER #5 IS LOGIC "1"	ERROR FLAG, FORMAT ERROR, WRONG STATUS ADDRESS/NO GAP, RETRY COUNT(1,0)(if enabled)	YES	FORMAT ERROR, BC RETRY (if enabled)	
LOOP TEST FAIL	ERROR FLAG, LOOP TEST FAIL	NO	FORMAT ERROR	
TRANSMITTER TIMEOUT:TRANS-MITTER ATTEMPTS TO TRANSMIT FOR LONGER THAN 668μs	BLOCK STATUS WORD STORED DURING START-OF-MESSAGE SEQUENCE	NO	BC/RT TRANSMITTER TIMEOUT	BC FRAME IS TERMINATED
NON-ENHANCED MODE OR EXPANDED BC CONTROL WORD NOT ENABLED AND ONE OR MORE BITS SET IN RT STATUS WORD	ERROR FLAG, STATUS SET, RETRY COUNT(1,0)(if RETRY IF STATUS SET, bit 9 of Configuration Register #4, is programmed to logic "1")	YES, if RETRY IF STATUS SET, bit 9 of Configuration Register #4, is programmed to logic "1"	BC STATUS SET, BC RETRY(if retry enabled for Status Set)	

Table 101. BC Exception Conditions				
	BLOCK STATUS WORD BITS	**AUTOMATIC RETRIES**	**INTERRUPTS, INTERRUPT STATUS WORD BITS**	**OTHER EFFECTS**
ENHANCED MODE AND EXPANDED BC CONTROL WORD ENABLED, AND ONE OR MORE BITS SET IN RT STATUS WORD WITH THE CORRESPONDING STATUS SET BIT(s) IN THE BC CONTROL WORD PROGRAMMED TO LOGIC "0"	ERROR FLAG, STATUS SET, MASKED STATUS SET, RETRY COUNT(1,0)(if retry enabled for Status Set)	YES, IF RETRY IF STATUS SET, bit 9 of Configuration Register #4, is programmed to logic "1"	BC STATUS SET, BC RETRY(if retry enabled for Status Set)	
ENHANCED MODE AND EXPANDED BC CONTROL WORD ENABLED, AND ONE OR MORE BITS SET IN RT STATUS WORD WITH THE CORRESPONDING STATUS SET BIT(s) IN THE BC CONTROL WORD PROGRAMMED TO LOGIC "1" AND NO BITS SET IN THE RT STATUS WORD WITH THE CORRESPONDING STATUS SET BIT(s) IN THE BC CONTROL WORD PROGRAMMED TO LOGIC "0"	ERROR FLAG, STATUS SET	NO	NONE	
WITH VALID M.E./NO DATA = "0"; IN RESPONSE TO A TRANSMIT COMMAND, MESSAGE ERROR BIT SET IN STATUS WORD, FOLLOWED BY NO DATA WORDS	ERROR FLAG, STATUS SET, MASKED STATUS SET (unless using Expanded BC Control Word and the M.E. MASK bit is logic "1"), FORMAT ERROR, WORD COUNT ERROR, RETRY COUNT(1,0) (if enabled)	YES	FORMAT ERROR, BC STATUS SET (if Expanded BC Control Word is not enabled or if the M.E. MASK bit in the BC Control Word is logic "0"), BC RETRY (if enabled)	

Table 101. BC Exception Conditions				
	BLOCK STATUS WORD BITS	**AUTOMATIC RETRIES**	**INTERRUPTS, INTERRUPT STATUS WORD BITS**	**OTHER EFFECTS**
WITH VALID M.E./NO DATA = "0"; IN RESPOSE TO A TRANSMIT COMMAND, MESSAGE ERROR BIT SET IN STATUS WORD, FOLLOWED BY THE CORRECT NUMBER OF DATA WORDS	ERROR FLAG, STATUS SET, MASKED STATUS SET (unless using Expanded BC Control Word and the M.E. MASK bit is logic "1"), RETRY COUNT(1,0) (if retry enabled for Status Set, unless using Expanded BC Control Word and the M.E. MASK bit is logic "1")	YES, (if retry enabled for Status Set, unless using Expanded BC Control Word and the M.E. MASK bit is logic "1")	BC STATUS SET (if Expanded BC Control Word is not enabled or if the M.E. MASK bit is logic "0"), BC RETRY (if retry enabled for Status Set, unless using Expanded BC Control Word and the M.E. MASK bit is logic "1")	

5.7.14 BC Off-Line and On-Line Self-Tests

In addition to the Enhanced Mini-ACE's autonomous built-in protocol and RAM self-tests, the BC mode of the Enhanced Mini-ACE terminals provides a number of self-test features. The internal registers and shared RAM are accessible to the host processor at all times. In addition, the Enhanced Mini-ACE BC includes wraparound test provisions for both an off-line self-test and an on-line self-test.

The internal registers and shared RAM can be tested by means of host processor software routines to implement checkerboard, walking zero, walking one and counting patterns and reading back and verifying the contents of the internal RAM.

The BC off-line self-test provides a means of exercising and verifying the parallel address and data paths, encoder, serial data path, decoder, and portions of the BC message format and word count logic, protocol state machine and memory management logic. In the off-line self-test, the Enhanced Mini-ACE does **not** transmit on the external 1553 bus. Instead, the Manchester II encoder output is routed directly to the decoder input. The off-line self-test can be run following power turn-on as part of system self-test or when the Enhanced Mini-ACE hybrid has been functioning in RT mode, as part of a software controlled response to a Reset RT mode code command. A common element of the off-line and on-line BC self-tests is the method by which loopback words are checked. In each case, the received version of all transmitted words is checked for validity (sync, encoding, parity, bit count) and the received version of the last word transmitted by the BC is compared to the transmitted version of the word. The loopback test is considered to have failed if the validity and/or comparison tests do not verify.

IMPORTANT NOTE:

It is important to note that the TX_INH_A and TX_INH_B inputs must be connected to logic "0" in order to pass the off-line self-test. The BC off-line self-test will fail if the respective transmitter inhibit input (TX_INH_A[B]) is connected to logic "1." Note that applying logic "1"

to these inputs provides a mechanism for self-testing the transmit inhibit function.

In order to run the off-line self-test for a particular message, bit 6 in the BC Control Word (OFF-LINE SELF-TEST) must be programmed to logic "1." As the result of a non-broadcast self-test message, the RESPONSE TIMEOUT bit of the message's Block Status Word **should be set**. Following a broadcast self-test message, the RESPONSE TIMEOUT bit should **not** be set. If the self-test passes, the LOOP TEST FAIL bit of the Block Status Word will not be set. The other portion of determining the success of the BC self-test is to verify that the Loopback Word contents match those of the last transmitted word.

In order to make the off-line self-test as comprehensive as possible, a number of self-test messages should be processed on each bus. To exercise the various portions of the BC protocol and memory management logic, the message block starting address, message format, data word count and contents of the last word to be transmitted should be varied for the individual test messages.

The off-line self-test may also exercise the ERROR, EOM, BC/RT MESSAGE, and BC_EOM interrupt request features. This may be done by setting the respective bit(s) in the Interrupt Mask register. If the Enhanced Mini-ACE is configured for a multi-message frame of off-line self-test messages, an interrupt will occur after every message if the EOM interrupt is enabled. Similarly, an ERROR interrupt request will occur following every non-broadcast off-line self-test message, due to the RESPONSE TIMEOUT condition. If the BC_EOM interrupt is enabled but the EOM interrupt is not, an interrupt request will only be issued after the **last** message of the frame is processed.

The BC STOP-ON-ERROR feature may be exercised by setting the respective bit in the Configuration Register, configuring the Enhanced Mini-ACE for a multi-message BC frame of off-line self-test messages and verifying that the BC stops processing messages after the first non-broadcast message of the frame has been processed.

The message gap-time and Time-Tag features may be self-tested by programming the Message gap time(s) for a multi-message frame and verifying the elapsed time of the frame by means of the Time-Tag Register. Automatic retries can be tested since a retry will occur, if programmed, as a result of the RESPONSE TIMEOUT condition resulting from a non-broadcast off-line self-test message.

For the BC on-line self-test, the last word transmitted on the 1553 bus is monitored by the receiver and fed back to the decoder to formulate the Loopback Word. Similar to the off-line test, the LOOP TEST FAIL bit in the Block Status Word is either set (for fail) or cleared as a result of the Loopback test and the Loopback Word is stored in the Shared RAM. In addition to the digital circuitry exercised by the off-line self-test, the on-line test verifies the operation of the transmitter, receiver, and to a large extent, the external transformers, stub and bus cabling, coupling boxes and termination resistors. Open circuits or other faults in these external components will result in signal reflections; these reflections can result in failures of the loopback test.

5.8 Enhanced BC Mode Architecture

5.8.1 Introduction

For new bus controller applications of the Enhanced Mini-ACE, it is strongly recommended that the Enhanced BC mode, rather than the legacy BC mode be used as it provides much more powerful control. The Enhanced BC includes a user programmable message sequence control engine. In order to configure the Enhanced Mini-ACE for the Enhanced BC mode, bit 15 (RT/BC-MT*) and 14 (MT/BC-RT*) should be programmed to logic "0," while bit 15 of Configuration Register #3 (ENHANCED MODE ENABLE), along with bit 15 of Configuration Register #6 (ENHANCED BUS CONTROLLER) must be programmed to logic "1."

The Enhanced BC's message sequence control engine provides a high degree of flexibility for implementing major and minor frame scheduling; capabilities for inserting asynchronous messages in the middle of a frame. It separates 1553 message data from control/status data for the purpose of implementing double buffering and performing bulk data transfers; and implements message retry schemes. It includes the capability for automatic bus channel switchover for failed messages; and for reporting various conditions to the host processor by means of 4 user-defined interrupts and a general-purpose queue.

Like the legacy BC mode, the Enhanced Mini-ACE's Enhanced BC mode implements all MIL-STD-1553B message formats. Message format is programmable on a message-by-message basis by means the BC Control Word and the T/R* bit of the Command Word for the respective message. The BC Control Word allows 1553 message format, 1553A/B type RT, bus channel, self-test, and Status Word masking to be specified on an individual message basis. In addition, automatic retries and/or interrupt requests may be enabled or disabled for individual messages. The BC performs all error checking required by MIL-STD-1553B. This includes validation of response time, sync type and sync encoding, Manchester II encoding, parity, bit count, word count, Status Word RT Address field, and various RT-to-RT transfer errors. The Enhanced Mini-ACE BC response timeout value is programmable with choices of 18.5, 22.5, 50, and 130 μs. The longer response timeout values allow for operation over long buses and/or use of the repeaters.

In the legacy mode, the Enhanced Mini-ACE may be programmed to process BC frames of up to 512 messages with no processor intervention. In the Enhanced BC mode, there is no explicit limit to the number of messages that may be processed in a frame. In both modes, it is possible to program for either single frame or frame auto-repeat operation. In the auto-repeat mode, the frame repetition rate may be controlled either internally, using a programmable BC frame timer, or from an external trigger input.

5.8.2 Enhanced BC Mode: Message Sequence Control

One of the salient architectural features of the Enhanced Mini-ACE series is its advanced capability for BC message sequence control. The Enhanced Mini-ACE supports highly autonomous BC operation, which greatly offloads the operation of the host processor.

The operation of the Enhanced Mini-ACE 's message sequence control engine is illustrated in Figure 10. The BC message sequence control involves an instruction list pointer register; an instruction list which contains multiple 2-word entries; a message control/status stack, which contains multiple 8-word or 10-word descriptors; and data blocks for individual messages.

The initial value of the instruction list pointer register is initialized by the host processor (via Register 0D), and is incremented by the BC message sequence processor (host readable via Register 03). During operation, the message sequence control processor fetches the operation referenced by the instruction list pointer register from the instruction list.

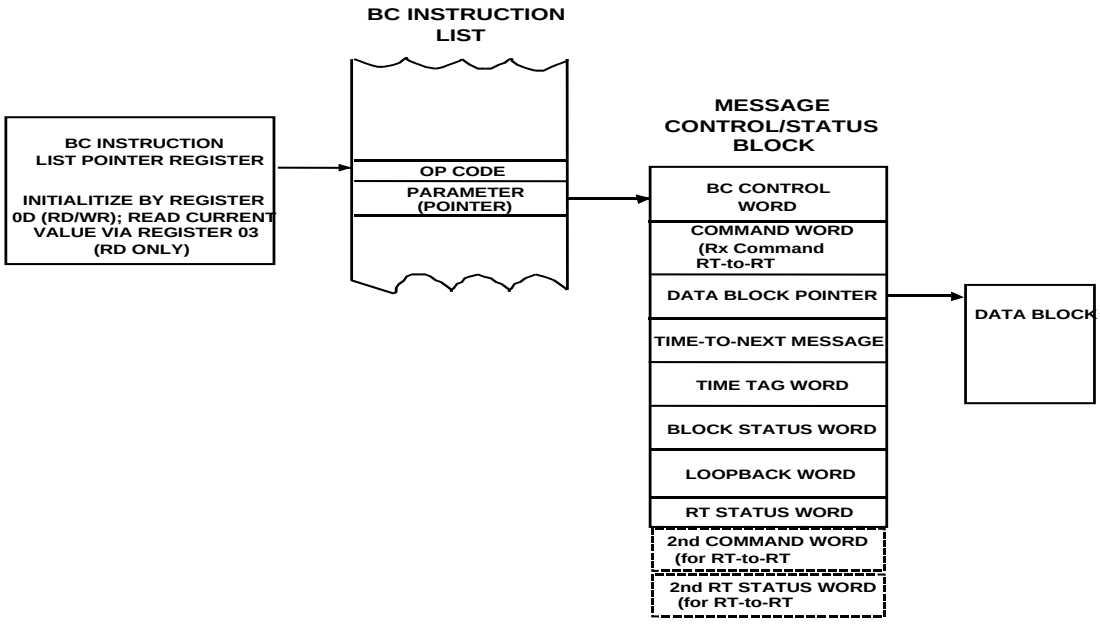


Figure 10. BC Message Sequence Control

Note that the pointer parameter referencing the first word of a message's control/status block (the BC Control Word) must contain an address value that is **modulo 8**. Also, note that if the message is an RT-to-RT transfer, the pointer parameter) must contain an address value that is **modulo 16**.

5.8.3 BC Instruction Set

The instruction list pointer register references a pair of words in the BC instruction list: an op code word, followed by a parameter word. The format of the op code word, which is illustrated in Figure 11, includes a 5-bit op code field and a 5-bit condition code field. The op code identifies the instruction to be executed by the BC message sequence controller.

Most of the operations are conditional, with execution dependent on the contents of the condition code field. Bits 3-0 of the condition code field identify the particular condition. Bit 4 of the condition code field identifies the logic sense ("1" or "0") of the selected condition code on which the conditional execution is dependent. Table 102 lists all the op codes, along with their respective mnemonic, code value, parameter, and description. Table 103 defines all the condition codes.

Eight of the condition codes (8 through F) are set or cleared as the result of the most recent message. The other eight are defined as "General Purpose" condition codes GP0 through GP7. There are three mechanisms for programming the values of the General Purpose Condition Code bits: (1) They may be set, cleared, or toggled by the host processor, by means of the BC GENERAL PURPOSE FLAG REGISTER; (2) they may be set, cleared, or toggled by the BC message sequence control processor, by means of the GP Flag Bits (FLG) instruction; and (3) GP0 and GP1 **only** (but none of the others) may be set or cleared by means of the BC message sequence control processor's Compare Frame Timer (CFT) or Compare Message Timer (CMT) instructions.

The host processor also has read-only access to the BC condition codes by means of the BC CONDITION CODE REGISTER.

Note that four (4) instructions are **unconditional**. These are Compare to Frame Timer (CFT), Compare to Message Timer (CMT), GP Flag Bits (FLG), and Execute and Flip (XQF). For these instructions, the Condition Code Field is "don't care." That is, these instructions are **always** executed, regardless of the result of the condition code test.

All other instructions are conditional. That is, they will only be executed if the condition code specified by the condition code field in the op code word tests true. If the condition code field tests false, the instruction list pointer will skip down to the next instruction.

As shown in Table 102, many of the operations include a single-word parameter. For an XEQ (execute message) operation, the parameter is a pointer to the start of the message's control/status block. For other operations, the parameter may be an address, a time value, an interrupt pattern, a mechanism to set or clear general purpose flag bits, or an immediate value. For several op codes, the parameter is "don't care" (not used).

As described above, some of the instructions will cause the message sequence control processor to execute messages. In this case, the parameter references the first word of a message control/status block. With the exception of RT-to-RT transfer messages, all message status/control blocks are eight words long: a block control word, time-to-next-message parameter, data block pointer, command word, status word, loopback word, block status word, and time tag word.

In the case of an RT-to-RT transfer message, the size of the message control/status block increases to 16 words. However, in this case, the last six words are not used; the ninth and tenth words are for the second command word and second status word.

The third word in the message control/status block is a pointer that references the first word of the message's data word block. Note that the data word block stores **only data words**, which are to be either transmitted or received by the BC. By segregating data words from command words, status words, and other control and "housekeeping" functions, this architecture enables the use of convenient, usable data structures, such as circular buffers and double buffers.

Other operations support program flow control; i.e., jump and call capability. The call capability includes maintenance of a call stack, which supports a maximum of four **(4)** entries; there is also a return instruction. In the case of a call stack overrun or underrun, the BC will issue a CALL STACK POINTER REGISTER ERROR interrupt, if enabled.

Other op codes may be used to delay for a specified time; start a new BC frame; wait for an external trigger to start a new frame; do comparisons based on frame time and time-to-next message; load the time tag or frame time registers; halt; and issue host interrupts. In the case of host interrupts, the message control processor passes a 4-bit user-defined interrupt vector to the host, by means of the Enhanced Mini-ACE 's Interrupt Status Register.

The purpose of the FLG instruction is to enable the message sequence controller to set, clear, or toggle the value(s) of any or all of the eight general-purpose condition flags.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Odd Parity	Op Code Field					0	1	0	1	0	Condition Code Field				

Figure 11. BC Op Code Format

The op code parity bit encompasses all sixteen bits of the op code word. This bit must be programmed for odd parity. If the message sequence control processor fetches;

a) an undefined op code word

b) an op code word with even parity

or

c) bits 9-5 of an op code word do not have a binary pattern of 01010

then the message sequence control processor will immediately halt the BC's operation.

In addition, if enabled, a BC TRAP OP CODE interrupt will be issued. Also, if enabled, a parity error will result in an OP CODE PARITY ERROR interrupt. Table 103 describes the condition codes.

The **Execute Message (XEQ)** instruction is the primary BC op code. By means of its pointer parameter, this instruction references the Message Control/Status Block (and in turn, the Data Word Block) for an individual message. In its simplest form, a BC instruction list could contain nothing but in-line XEQ instructions, referencing frames of messages to be processed.

The **Jump (JMP)** instruction provides a conditional (or unconditional) "GOTO" operation. **Subroutine Call (CAL)** and **Subroutine Return (RTN)** provide the capability to embed subroutines into the BC code. Note that the BC supports subroutine nesting up to **four** deep. The subroutine call stack is maintained in on-chip registers. If there is an attempt to overflow or underflow this stack, an error will occur and the BC will halt operation.

The Enhanced Mini-ACE BC provides three mechanisms for reporting information back to the BC host processor: (1) general purpose flag bits; (2) user-definable interrupts; and (3) a general-purpose queue.

The **GP Flag Bits (FLG)** instruction allows for setting, clearing, or toggling of one or more of any of the 8 general-purpose flag bits. These bits may also be set, cleared, or toggled by the BC's host processor. The **Interrupt Request (IRQ)** instruction allows the BC to issue a user-defined interrupt request to the BC's host processor. The parameter for the IRQ instruction is a 4-bit interrupt bit pattern. The general-purpose queue is a 64-word data structure that the BC can write words to. The **Push**

Time Tag Register (PTT), Push Block Status Word (PBS), Push Immediate Value (PSI), and **Push Indirect (PSM)** instructions allow the BC to push various types of words on the General Purpose Queue. The Block Status Word conveys information about the most recently completed message. The Push Indirect allows, for example, for the BC to autonomously post arbitrary sequences of received data words to the General Purpose Queue.

There are several instructions providing various capabilities for timing control. The **Delay (DLY)** instruction allows a programmed delay time between instructions, with a resolution of 1 µs/LSB. The **Compare to Frame Timer (CFT)** and **Compare to Message Timer (CMT)** instructions enable the current values of these timers to be compared to a specified value. The Less Than (LT/GP0) and Equal (EQ/GP1) flags will be updated as the result of these comparisons. The **Load Frame Timer (LFT)** and **Start Frame Timer (SFT)** instructions provide the means for loading and starting the frame timer. The frame timer, which has a resolution of 100 µs/LSB, may be used for minor or major frame control, in conjunction with the CFT instruction; and/or as a watchdog timer for the BC message sequence processor.

The BC can assign the value of the Time Tag Register by means of the **Load Time Tag Counter (LTT)**. The **Wait for External Trigger (WTG)** will cause the BC to wait, and then go to the next instruction following a rising edge of the EXT_TRIG input signal. The **Halt (HLT)** instruction will cause the BC to cease operation. When the BC halts, the value of the frame timer freezes; i.e. it stops incrementing, but does NOT reset to 0000h. If a Hardware or Software reset is subsequently applied the value of the frame timer WILL reset to 0000h. Conversely, if you don't apply a hardware or software reset after halting the BC, when you re-start the BC the frame timer will assume the same value as when you halted the BC.

5.8.4 Execute and Flip Operation

The **Execute and Flip (XQF)** instruction is unconditional. It references a particular message. If the condition code tests true *after* the message has been processed, then the value of bit 4 of the message's control/status block pointer will be toggled. In this case, the next time that the particular XQF code line is executed, the pointer will reference a *different* Control/Status block and therefore a different message will be processed. The operation of the XQF instruction is illustrated in Figure 12.

See Appendix "D" for important user information **IF** terminal is in BC mode with Enhanced BC Mode enabled **AND** in buffered processor interface configuration **AND** with ENHANCED CPU ACCESS enabled.

The Enhanced Mini-ACE BC's XQF, or "Execute and Flip" operation, provides some unique capabilities. Following execution of this unconditional instruction, if the condition code tests TRUE, the BC will modify the value of the current XQF instruction's pointer parameter by toggling bit 4 in the pointer. That is, if the selected condition flag tests true, the value of the parameter will be **updated** to the value = **old address XOR 0010h**. As a result, the next time that this line in the instruction list is executed, the Message Control/Status Block at the updated address (old address XOR 0010h), will be processed, rather than the one at the old address,. The operation of the XQF instruction is illustrated in Figure 12.

There are multiple ways of utilizing the “execute and flip” functionality. One is to facilitate the implementation of a double buffering data scheme for individual messages. This allows the message sequence control processor to “ping-pong” between a pair of data buffers for a particular message.

By so doing, the host processor can access one of the two Data Word blocks, while the BC reads or writes the alternate Data Word block.

A second application of the “execute and flip” capability is in association with

message retries. This allows the BC to not only switch buses when retrying a failed message, but to automatically switch buses **permanently** for all future times that the same message is to be processed. This not only provides a high degree of autonomy from the host CPU, but also saves BC bandwidth, by eliminating future attempts to process messages on an RT’s failed channel.

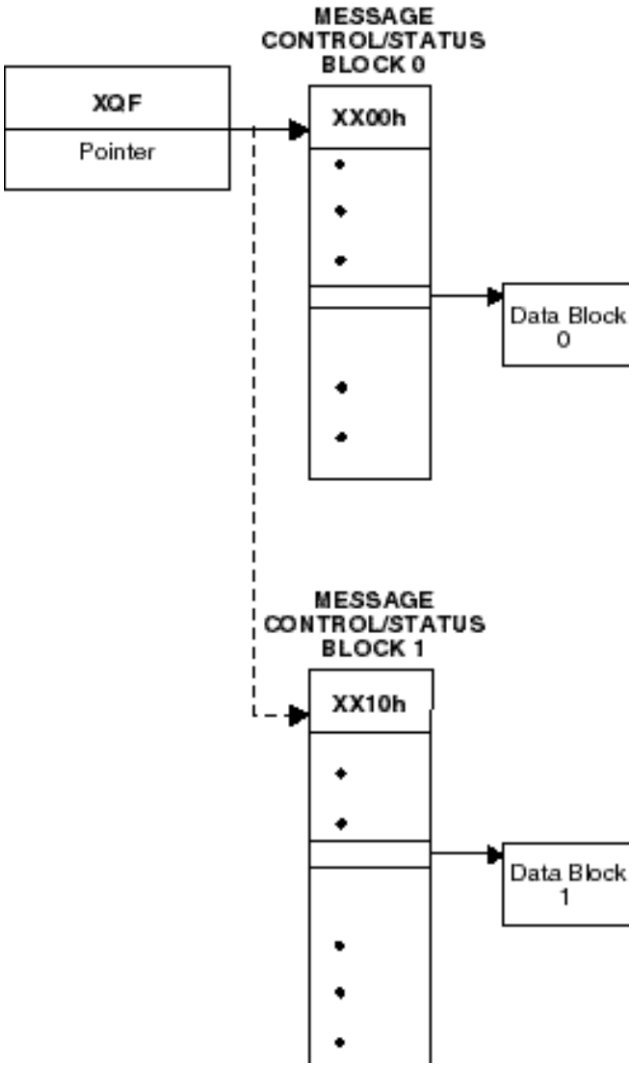


Figure 12. Use of Execute and Flip (XQF) Operation

Table 102. BC Operations for Message Sequence Control					
INSTRUCTION	**MNEMONIC**	**OP CODE (HEX)**	**PARAMETER**	**CONDITIONAL OR UNCONDITIONAL**	**DESCRIPTION**
EXECUTE MESSAGE	XEQ	0001	MESSAGE CONTROL/ STATUS BLOCK ADDRESS	CONDITIONAL (See NOTE)	Executes the message at the specified Message Control/Status Block Address if the condition flag tests TRUE, otherwise continue execution at the next OpCode in the instruction list.
JUMP	JMP	0002	INSTRUCTION LIST ADDRESS	CONDITIONAL	Jump to the OpCode specified in the Instruction List if the condition flag tests TRUE, otherwise continue execution at the next OpCode in the instruction list.
SUBROUTINE CALL	CAL	0003	INSTRUCTION LIST ADDRESS	CONDITIONAL (See NOTE)	Jump to the OpCode specified by the Instruction List Address and push the Address of the Next OpCode on the Call Stack if the condition flag test TRUE, otherwise continue execution at the next OpCode in the instruction list. Note that the maximum depth of the subroutine call stack is four.
SUBROUTINE RETURN	RTN	0004	NOT USED (Don't Care)	CONDITIONAL	Return to the OpCode popped off the Call Stack if the condition flag tests TRUE, otherwise continue execution at the next OpCode in the instruction list.
INTERRUPT REQUEST	IRQ	0006	INTERRUPT BIT PATTERN IN 4 LS BITS	CONDITIONAL	Generate an interrupt if the condition flag tests TRUE, otherwise continue execution at the next OpCode in the instruction list. The passed parameter (IRQ Bit Pattern) specifies which of the ENHANCED BC IRQ bit(s) (bits 5-2) will be set in Interrupt Status Register #2. Only the four LSBs of the passed parameter are used. A parameter where the four LSBs are logic "0" will not generate an interrupt.

Table 102. BC Operations for Message Sequence Control					
INSTRUCTION	**MNEMONIC**	**OP CODE (HEX)**	**PARAMETER**	**CONDITIONAL OR UNCONDITIONAL**	**DESCRIPTION**
HALT	HLT	0007	NOT USED (Don't Care)	CONDITIONAL	Stop execution of the Message Sequence Control Program until a new BC Start is issued by the host if the condition flag tests TRUE, otherwise continue execution at the next OpCode in the instruction list.
DELAY	DLY	0008	DELAY TIME VALUE (resolution = 1 μs/LSB)	CONDITIONAL	Delay the time specified by the Time parameter before executing the next OpCode if the condition flag tests TRUE, otherwise continue execution at the next OpCode without delay. The delay generated will use the Time to Next Message Timer.
WAIT UNTIL FRAME TIMER = 0	WFT	0009	NOT USED (Don't care)	CONDITIONAL	Wait until Frame Time counter is equal to Zero before continuing execution of Message Sequence Control Program if the condition flag tests TRUE, otherwise continue execution at the next OpCode without delay.
COMPARE TO FRAME TIMER	CFT	000A	DELAY TIME VALUE (resolution = 100 μs/LSB)	UNCONDITIONAL	Compare Time Value to Frame Time Counter and set or clear the LT and EQ flag based on the results of the compare. If the value of the CFT's parameter is less than the value of the frame time counter, then the LT/GP0 and NE/GP1* flags will be set, while the GT-EQ/GP0* and EQ/GP1* flags will be cleared. If the value of the CFT's parameter is greater than the current value of the frame time counter, then the GT-EQ/GP0* and NE/GP1* flags will be set, while the LT/GP0 and EQ/GP1 flags will be cleared.

Table 102. BC Operations for Message Sequence Control					
INSTRUCTION	**MNEMONIC**	**OP CODE (HEX)**	**PARAMETER**	**CONDITIONAL OR UNCONDITIONAL**	**DESCRIPTION**
COMPARE TO MESSAGE TIMER	CMT	000B	DELAY TIME VALUE (resolution = 1 μs/LSB)	UNCONDITIONAL	Compare Time Value to Message Time Counter. When XEQ or XQF is followed by a CMT instruction the value of the message time used for the compare is always '0000'. The message timer (initiated by the XEQ or XQF instruction) counts down to '0000' prior to fetching the CMT instruction. Result of a CMT
COMPARE TO MESSAGE TIMER (CONT)	CMT	000B	DELAY TIME VALUE (resolution = 1 μs/LSB)	UNCONDITIONAL	instruction in cases of a non-zero value CMT parameter is GT-EQ/GP0* and NE/GP1 flags are always set, LT/GP0 and EQ/GP1 flags are always cleared. If the value of the CMT parameter is '0000', GT-EQ/GP0* and EQ/GP1 flags are set, LT/GP0 and NE/GP1* flags are cleared. As a result of a CMT instruction, there is never a situation where LT/GP0 and NE/GP1* flags are set and GT-EQ/GP0* and EQ/GP1 flags are cleared.
GP FLAG BITS	FLG	000C	USED TO SET CLEAR, OR TOGGLE GP (General Purpose) FLAG BITS (See Description)	UNCONDITIONAL	Used to set, toggle, or clear any or all of the eight general purpose flags. The table below illustrates the use of the GP Flag Bits instruction for the case of GP0 (General Purpose Flag 0). Bits 1 and 9 of the parameter byte affect flag GP1, bits 2 and 10 affect GP2, etc., according to the following rules: Bit 8 Bit 0 Effect on GP0 0 0 No Change 0 1 Set Flag 1 0 Clear Flag 1 1 Toggle Flag

Table 102. BC Operations for Message Sequence Control					
INSTRUCTION	**MNEMONIC**	**OP CODE (HEX)**	**PARAMETER**	**CONDITIONAL OR UNCONDITIONAL**	**DESCRIPTION**
LOAD TIME TAG COUNTER	LTT	000D	TIME VALUE. RESOLUTION (μs/LSB) IS DEFINED BY BITS 9, 8, AND 7 OF CONFIGURATION REGISTER #2.	CONDITIONAL	Load Time Tag Counter with Time Value if the condition flag tests TRUE, otherwise continue execution at the next OpCode in the instruction list.
LOAD FRAME TIMER	LFT	000E	TIME VALUE (resolution = 100 μs/LSB)	CONDITIONAL	Load Frame Timer Register with the Time Value parameter if the condition flag tests TRUE, otherwise continue execution at the next OpCode in the instruction list.
START FRAME TIMER	SFT	000F	NOT USED (Don't Care)	CONDITIONAL	Start Frame Time Counter with Time Value Frame register if the condition flag tests TRUE , otherwise continue execution at the next OpCode in the instruction list.
PUSH TIME TAG REGISTER	PTT	0010	NOT USED (Don't Care)	CONDITIONAL	Push the value of the Time Tag Register on the General Purpose Queue if the condition flag tests TRUE, otherwise continue execution at the next OpCode in the instruction list.
PUSH BLOCK STATUS WORD	PBS	0011	NOT USED (Don't Care)	CONDITIONAL	Push the Block Status Word for the most recent message on the General Purpose Queue if the condition flag tests TRUE, otherwise continue execution at the next OpCode in the instruction list. Bits 15 (EOM) and 14 (SOM) are always written to the General Purpose Queue as '0'.
PUSH IMMEDIATE VALUE	PSI	0012	IMMEDIATE VALUE	CONDITIONAL	Push Immediate data on the General Purpose Queue if the condition flag tests TRUE, otherwise continue execution at the next OpCode in the instruction list.
PUSH INDIRECT	PSM	0013	MEMORY ADDRESS	CONDITIONAL	Push the data stored at the specified memory location on the General Purpose Queue if the condition flg tests TRUE, otherwise continue execution at the next OpCode in the inst list

Table 102. BC Operations for Message Sequence Control					
INSTRUCTION	**MNEMONIC**	**OP CODE (HEX)**	**PARAMETER**	**CONDITIONAL OR UNCONDITIONAL**	**DESCRIPTION**
WAIT FOR EXTERNAL TRIGGER	WTG	0014	NOT USED (Don't Care)	CONDITIONAL	Wait until a logic "0"-to-logic "1" transition on the EXT_TRIG input signal before proceeding to the next OpCode in the instruction list if the condition flag tests TRUE, otherwise continue execution at the next OpCode without delay.
EXECUTE AND FLIP	XQF **NOTE:** SEE APPENDIX "G" FOR IMPORTANT USER INFORMATION	0015	MESSAGE CONTROL STATUS BLOCK ADDRESS	UNCONDITIONAL	Execute (unconditionally) the message for the Message Control/Status Block Address. Following the processing of this message, if the condition flag tests TRUE, then flip bit 4 in the Message Control/Status Block Address, and store the new Message Block Address as the updated value of the parameter following the XQF instruction code. As a result, the next time that this line in the instruction list is executed, the Message Control/Status Block at the updated address (old address XOR 0010h), rather than the old address, will be processed. If the condition flag tests FALSE, the value of the Message Control/Status Block Address parameter will not change.

NOTE: While the XEQ (Execute Message) instruction is conditional, not all condition codes may be used to enable its use. The ALWAYS and NEVER condition codes may be used. The eight general purpose flag bits, GP0 through GP7, may also be used. However, if GP0 through GP7 are used, it is imperative that the host processor not modify the value of the specific general purpose flag bit that enabled a particular message while that message is being processed. Similarly, the LT, GT-EQ, EQ, and NE flags, which the BC only updates by means of the CFT and CMT instructions, may also be used. However, these two flags are dual use. Therefore, if these are used, it is imperative that the host processor not modify the value of the specific flag (GP0 or GP1) that enabled a particular message while that message is being processed. The NORESP, FMT ERR, GD BLK XFER, MASKED STATUS SET, BAD MESSAGE, RETRY0, and RETRY1 condition codes are not available for use with the XEQ instruction and should not be used to enable its execution.

Table 103. BC Condition Codes			
BIT CODE	**NAME (Bit 4 = 0)**	**INVERSE (Bit 4 = 1)**	**FUNCTIONAL DESCRIPTION**
0	LT/GP0	GT-EQ/ $\overline{GP0}$	Less Than or GP0 flag. This bit is set or cleared based on the results of the compare. If the value of the CMT's parameter is less than the value of the message time counter, then the LT/GP0 and NE/ $\overline{GP1}$ flags will be set, the GT-EQ/GP0 and EQ/ $\overline{GP1}$ flags will be cleared. If the value of the CMT's parameter is equal to the value of the message time counter, then the GT-EQ/ $\overline{GP0}$ and EQ/GP1 flags will be set, while the LT/GP0 and NE/GP1* flags will be cleared. If the value of the CMT's parameter is greater than the current value of the message time counter, than the GT-EQ/ $\overline{GP0}$ and NE/ $\overline{GP1}$ flags will be set, while the LT/GP0 and EQ/GP1 flags will be cleared. Also, General Purpose Flag 1 may also be set or cleared by the FLG operation.
1	EQ/GP1	NE/ $\overline{GP1}$	Equal Flag. This bit is set or cleared after CFT or CMT operation. If the value of the CMT's parameter is equal to the value for the message time counter, then the EQ/GP1 flag will be set and the NE/ $\overline{GP1}$ bit will be cleared. If the value of the CMT's parameter is not equal to the message time counter, then the NE/ $\overline{GP1}$ flag will be set and the EQ/GP1 bit will be cleared. Also, General Purpose Flag 1 may be also be set or cleared by a FLG operation.
2	GP2	$\overline{GP2}$	General Purpose Flags set or cleared by FLG operation or by host processor. The host processor can set, clear, or toggle these flags in the same way as the FLG instruction by means of the BC GENERAL PURPOSE FLAG REGISTER.
3	GP3	$\overline{GP3}$	
4	GP4	$\overline{GP4}$	
5	GP5	$\overline{GP5}$	
6	GP6	$\overline{GP6}$	
7	GP7	$\overline{GP7}$	
8	NORESP	RESP*	NORESP indicates that an RT has either not responded or has responded later than the BC No Response Timeout time. The Enhanced Mini-ACE 's No Response Timeout Time is defined per MIL-STD-1553B as the time from the mid-bit crossing of the parity bit to the mid-sync crossing of the RT Status Word. The value of the No Response Timeout value is programmable from among the nominal values 18.5, 22.5, 50.5, and 130 μs (±1 μs) by means of bits 10 and 9 of Configuration Register #5.
9	FMT ERR	$\overline{FMT\,ERR}$	FMT ERR indicates that the received portion of the most recent message contained one or more violations of the 1553 message validation criteria (sync, encoding, parity, bit count, word count, etc.), or the RT's status word received from a responding RT contained an incorrect RT address field.
A	GD BLK XFER	$\overline{GD\,BLK}$ $\overline{XFER}$	For the most recent message, GD BLK XFER will be set to logic "1" following completion of a valid (error-free) RT-to-BC transfer, RT-to-RT transfer, or transmit mode code with data message. This bit is set to logic "0" following an invalid message. GOOD DATA BLOCK TRANSFER is always logic "0" following a BC-to-RT transfer, a mode code with data, or a mode code without data. The Loop Test has no effect on GOOD DATA BLOCK TRANSFER. GOOD DATA BLOCK TRANSFER may be used to determine if the transmitting portion of an

Table 103. BC Condition Codes			
BIT CODE	**NAME (Bit 4 = 0)**	**INVERSE (Bit 4 = 1)**	**FUNCTIONAL DESCRIPTION**
			RT-to-RT transfer was error free.
B	MASKED STATUS SET	$\overline{\text{MASKED}}$ $\overline{\text{STATUS}}$ $\overline{\text{SET}}$	Indicates that one or both of the following conditions have occurred for the most recent message: (1) If one (or more) of the Status Mask bits (14 through 9) in the BC Control Word is logic "0" and the corresponding bit(s) is (are) set (logic "1") in the received RT Status Word. In the case of the RESERVED BITS MASK (bit 9) set to logic "0," any or all of the 3 Reserved Status bits being set will result in a MASKED STATUS SET condition; and/or (2) If BROADCAST MASK ENABLED/ $\overline{\text{XOR}}$ (bit 11 of Configuration Register #4) is logic "1" and the MASK BROADCAST bit of the message's BC Control Word is logic "0" and the BROADCAST COMMAND RECEIVED bit in the received RT Status Word is logic "1.".
C	BAD MESSAGE	GOOD MESSAGE	BAD MESSAGE indicates either a format error, loop test fail, or no response error for the most recent message. Note that a “Status Set” condition has no effect on the “BAD MESSAGE/GOOD MESSAGE” condition code.
D	RETRY1	$\overline{\text{RETRY1}}$	If bits 0-3 of the Condition Code contain a 0 x D and bit 4 is a zero then this means one retry. If bit 4 is a one then this means zero retries.
E	RETRY2	$\overline{\text{NA}}$	If bits 0-3 of the Condition Code contain a 0 x E and bit 4 is a zero then this means two retries. Bit 4 = 1 is not a defined condition.
F	ALWAYS	NEVER	The ALWAYS bit should be set (bit 4 = 0) to designate an instruction as unconditional. The inverse NEVER bit (bit 4 = 1) can be used to implement a NOP or “skip” instruction.

5.8.5 BC Message Sequence Control

The BC Enhanced Mini-ACE BC message sequence control capability enables a high degree of offloading of the host processor. This includes using the various timing functions to enable autonomous structuring of major and minor frames. In addition, by implementing conditional jumps and subroutine calls, the message sequence control processor greatly simplifies the insertion of asynchronous, or “out-of-band” messages.

5.8.6 General Purpose Queue

The Enhanced Mini-ACE BC allows for the creation of a general purpose queue. This data structure provides a means for the message sequence processor to convey information to the BC host. The BC op code repertoire provides mechanisms to push various items on this queue. These include the contents of the Time Tag Register, the Block Status Word for the most recent message, an immediate data value, or the contents of a specified memory address.

Figure 13 illustrates the operation of the BC General Purpose Queue. Note that the BC General Purpose Queue Pointer Register will always point to the **next** address location (modulo 64); that is, the location **following** the last location written by the BC message sequence control engine. If enabled, a BC GENERAL PURPOSE QUEUE ROLLOVER interrupt will be issued when the value of the queue pointer address rolls over at a 64-word boundary.

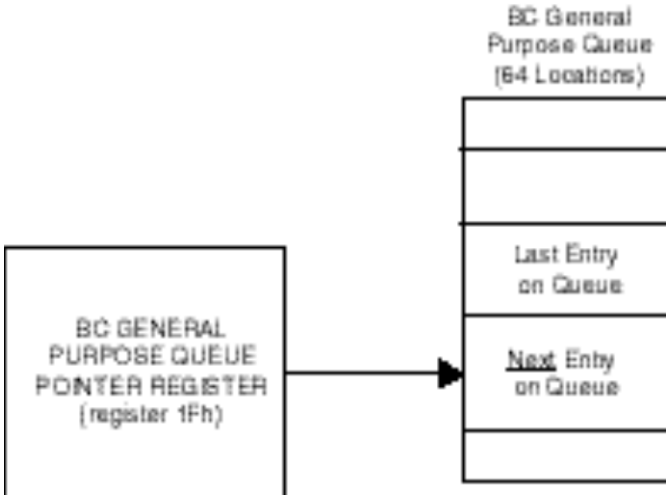


Figure 13. BC General Purpose Queue

5.9 Application Examples of the Enhanced BC Mode

5.9.1 Minor and Major Frames

Many avionics applications involve the use of periodic polling. The Enhanced Mini-ACE bus controller provides a number of mechanisms for message timing control. This involves the implementation of minor and major frames and control of inter-message gaps.

Figure 14 and Figure 15 illustrate the concepts of minor and major BC frames. A minor frame has a fixed time duration (e.g., 10 ms or 20 ms), while a major frame is comprised of multiple minor frames. Depending on the periodicity of individual messages, they will either be processed in a single minor frame within the major frame, or in multiple minor frames within the major frame.

Minor and major frames may be used as a mechanism for regulating periodic, highly deterministic message traffic. For example, if the BC's minor frame time is 10 ms with a major frame time of 1 second, it is a relatively simple matter to program specific messages with varying periodicities. For example, a 1 Hz message would appear in 1 minor frame within a major frame, a 2 Hz message would appear in every 5th minor frame, a 10 Hz message would appear in every tenth minor frame, etc.

MIL-STD-1553B defines inter-message gap time as the time from the mid-parity bit crossing of the last word of one message to the time of the mid-sync crossing of the command word of the subsequent message. As shown in Figure 14, inter-message gap time may be controlled by means of the Enhanced Mini-ACE BC's Time-to-Next Message parameter in the BC Control/Status block.

The time-to-next message parameter defines the time from the start of the current message to the start of the subsequent message. The Enhanced Mini-ACE BC's minimum inter-message gap time is approximately 10 µs. Therefore, if the programmed time-to-next message is less than the time needed to process the message plus 10 µs, the resulting inter-message gap time will be about 10 µs.

Another mechanism that may be used for message timing control is the Delay (DLY) instruction. The Delay instruction allows for a programmed delay up to 65.535 ms, in increments of 1 µs/LSB. One purpose of the Delay instruction (or the Time-to-Next Message parameter) is to increase the inter-message gap for the case of a BC "conversing" with slower RTs/systems.

A third mechanism that may be used for timing control is the frame timer. There are several ways of using the frame timer:

1) As illustrated in Figure 14 and Figure 15, the frame timer may be used for minor frame control. In general, minor frames consist of one or more messages (although "blank" minor frames containing no messages are also possible). A major BC frame consists of one or more minor frames. After the last minor frame is processed, the major frame completes and the first minor frame within the major frame is repeated.

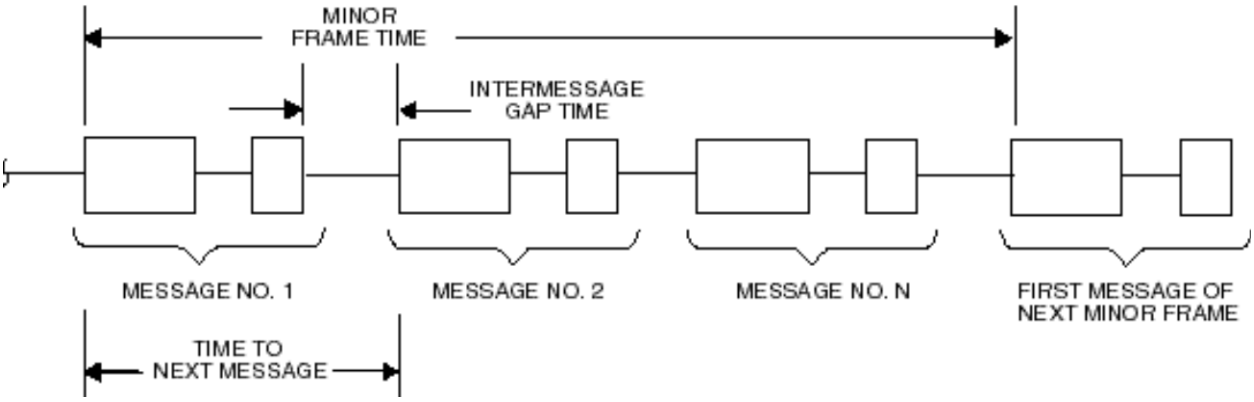


Figure 14. Intermessage Gap Time, Minor Frame Time

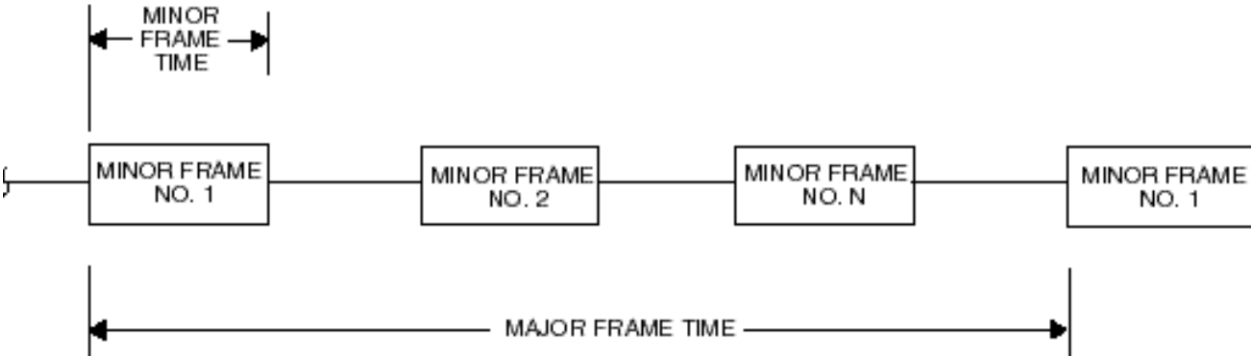


Figure 15. Minor and Major Frames

The example of instruction list code in illustrates the use of the frame timer for implementing minor frames. Since waiting for a minor frame timer to expire, and then loading and starting the frame timer for the next minor frame is an operation that gets performed repeatedly, it is possible to reduce the BC instruction list code size by means of a subroutine. In this and other code examples, PTR_X refers to the pointer to the Control/Status block for message number "X."

Table 104. Code Example for Minor Frame Control				
ADDRESS LABEL	**INSTRUCTION MNEMONIC**	**CONDITION CODE (blank = unconditional)**	**PARAMETER**	**COMMENT**
	LFT		MINOR FRAME TIME	Frame timer ← minor frame time. Note that the resolution for the frame timer is 100 µs/LSB.
	SFT			Start minor frame timer.
	XEQ		PTR_{1-1}	First message of first minor frame.
	XEQ		PTR_{1-2}	Second message of first minor frame.
		• • •		
	XEQ		PTR_{1-N}	Last message of first minor frame.
	CAL		NXTFRM	Call subroutine that will wait for minor frame timer to expire and start subsequent minor frame.
	XEQ		PTR_{2-1}	First message of second minor frame.
		• • •		
	XEQ		PTR_{2-N}	Last message of second minor frame.
	CAL		NXTFRM	Call subroutine to start third minor frame.
	XEQ		PTR_{3-1}	First message of third minor frame.
		• • •		
NXTFRM	WTF			Start of subroutine to finish one minor frame and start subsequent minor frame. Wait for frame timer to count down to 0.
	LFT		MINOR FRAME TIME	Frame timer ← minor frame time
	SFT			Start new minor frame timer.
	RTN			Subroutine return

Similarly, the frame timer may also be used as a mechanism for major frame control, by using either the Time-to-Next Message parameter or the DLY instruction for controlling minor frames.

A third use of the frame timer is as a watchdog timer for the BC message sequence control processor. This function is enabled by setting bit 1 of Configuration Register #7, ENHANCED BC WATCHDOG TIMER ENABLED, and bit 3 of Interrupt Mask Register #1, BC EOF, to values of logic "1."

If ENHANCED BC WATCHDOG TIMER ENABLED is programmed to logic "1," the frame timer will function as a watchdog, or "failsafe" timer for the BC processor. That is, if the frame timer counts down to zero, the BC processor will issue an interrupt (assuming ENHANCED BC WATCHDOG is enabled as above) to the host processor. This protects against a scenario in which the BC processor gets "lost" due to a corrupted instruction code or parameter.

The code example of Table 105 below is a modified version of the NXTFRM subroutine illustrated above. In this routine, the WFT instruction is replaced by a CFT (Compare Frame Timer) instruction. Note that the parameter for the CFT instruction is 0001, which specifies a time value of 100 µs. This allows time to execute the next three instructions without the frame timer timing out. To compensate for this difference, the value loaded into the frame timer by the LFT instruction should be about 100 µs (1 LSB) more than the actual desired minor frame time.

If the operation of the BC processor gets corrupted such that this subroutine is not executed, the frame timer will count down to zero, and the BC can be set to issue a BC EOF interrupt.

Table 105. Code Example for Use of Minor Frame Timer as BC Processor Watchdog Timer

ADDRESS LABEL	INSTRUCTION MNEMONIC	CONDITION CODE (blank = unconditional)	PARAMETER	COMMENT
NXTFRM	CFT		0001	Compare the value of the frame timer to 100 µs.
	JMP	GT FLAG	NXTFRM	Go back/repeat CFT instruction if the value of frame timer > 100 µs.
	LFT		MINOR FRAME TIME	Frame timer ← minor frame time (resolution = 100 µs/LSB)
	SFT			Start minor frame timer
	RTN			Subroutine return

5.9.2 Asynchronous Message Frame Insertion

One of the salient advantages of the Enhanced Mini-ACE enhanced BC architecture is its capability to process asynchronous messages or asynchronous message frames. This capability allows for the host processor to queue up an asynchronous message while the BC is processing a scheduled message frame. At the conclusion of the current message, but before the next message in the scheduled frame is processed, the queued message will receive immediate attention. Once the asynchronous message(s) has been processed, the (previously) scheduled frame will continue where it left off.

The code example of Table 106 illustrates an implementation of an asynchronous message frame. In this example, the host will program the asynchronous messages and then set General Purpose Flag 3 (GP3) to direct the BC to process the asynchronous messages.

Note that the host processor should fully load all of the message control/status blocks, as well as any data words to be transmitted to data blocks for the asynchronous message frame prior to setting the GP3 flag. In the conditional CAL (subroutine call) operation, the BC processor checks to determine if the host processor has set the GP3 flag. If so, this will trigger the execution of the asynchronous message frame.

Table 106. Code Example of Asynchronous Message Insertion

Address Label	Instruction Mnemonic	Condition Code (blank = unconditional)	Parameter	Comment
	XEQ		PTR_1	First scheduled message.
	CAL	GP3	ASYNCH	If general purpose flag GP3 has been set by the host, then call the asynchronous messages subroutine.
	XEQ		PTR_2	Second scheduled message.
		• • •		
ASYNCH	XEQ		PTR_{A-1}	First message of asynchronous frame
		• • •		
	XEQ		PTR_{A-N}	Last message of asynchronous frame
	FLG		0800	Clear GP3
	RTN			Subroutine return

5.9.3 Data Block Double Buffering

Typical BC applications involve the need to receive or send the same parameter or parameter set periodically. For the case of received data, the process of filling individual data blocks is under the control of the bus controller. For the case transmitted data, the process of filling data blocks is under control of the host software.

For an RT/sub address sub address being polled many times per second, the process of the application software requiring access to a particular parameter may be asynchronous to the process of the BC polling the RT/sub address. For an autonomous BC such as the Enhanced Mini-ACE, the same message will typically be processed in multiple minor frames within a major frame. However, the application software's need to access the various parameters will not necessarily be synchronous with the BC.

For example, for the case of data received during an RT-to-BC (or RT-to-RT) transfer, the host software often needs to reliably access the latest version of a particular parameter received from a particular RT/sub address. In so doing, it is generally a requirement to be able to ensure data validity and data sample consistency. What is meant by data sample consistency is that there needs to be a guarantee that the host does not read a mixture of new data and previously received data within a data block.

A commonly used method to ensure data sample consistency for asynchronously accessed data is the use of double buffering. For a BC receiving data blocks, the BC may be configured to automatically "ping-pong" between two data blocks each time that a message is processed. As illustrated in Figure 16, the Enhanced Mini-ACE BC's Execute and Flip (XQF) instruction provides an autonomous mechanism for doing this. With the XQF instruction, the BC can be configured to alternate between two blocks of received data for the same message. That is, after the message defined by the Control/Status block at XX00 is processed, the pointer parameter associated with the XQF op code may be defined to toggle its bit 4. This will result in the pointer referencing the Control/Status block at location XX10 the next time that the message is processed.

As a means of reducing overall BC instruction list and control/status block code size, it is best to create a subroutine to process a particular message. This subroutine may then be executed in multiple minor frames within a major BC frame. The subroutine code in Table 107 is an example of double buffering using the XQF instruction.

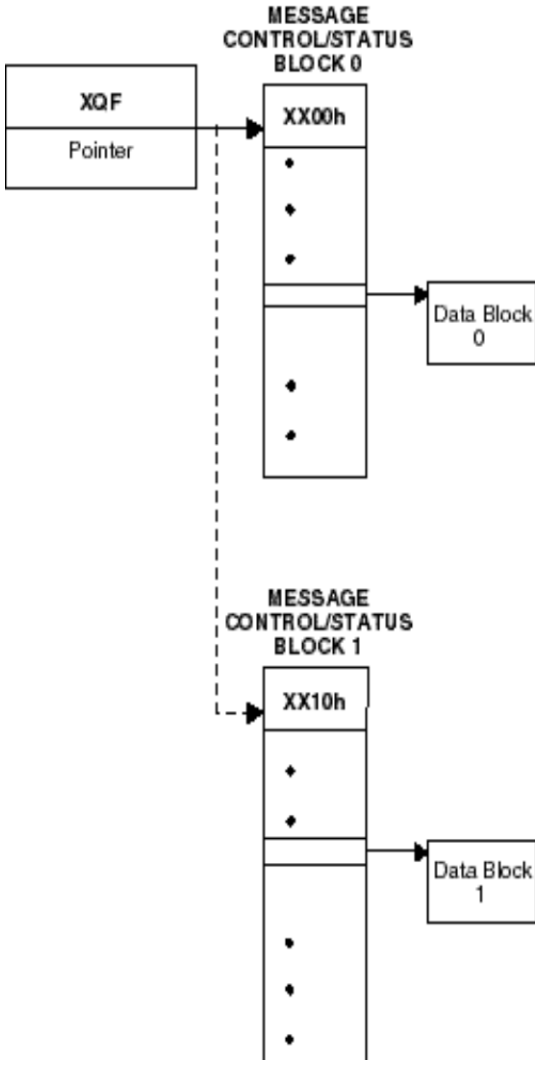


Figure 16. Use of Execute and Flip (XQF) Instruction For Sub address Double Buffering

Table 107. Example of Double Buffering Using XQF Instruction				
Address Label	**Instruction Mnemonic**	**Condition code (blank = unconditional)**	**Parameter**	**Comment**
START	XQF NOTE: See Appendix "G" for important user information	**Error! Objects cannot be created from editing field codes.**	PTR1	Start of subroutine. Process the message using the Execute and Flip (XQF) operation. The condition code for this instruction should be the $\overline{GP3}$ flag bit. That is, the first time this line of code is executed, the control/status block will be PTR1. Assuming that $\overline{GP3}$ is TRUE, (i.e., auto-toggling is enabled), then PTR1 ← PTR1 XOR 0010.
	JMP	BAD MESSAGE	FAULT	If the BAD MESSAGE flag is TRUE, then jump to the "FAULT" portion of the subroutine.
	RTN	$\overline{GP3}$		If $\overline{GP3}$ is true, this indicates that auto-toggling is currently enabled. In this case, return from the subroutine.
	FLG		0010	Since $\overline{GP3}$ was false (indicating that block auto-toggling is currently disabled), set the GP4 general purpose flag, which tells the host processor that a message was received while the host was reading the received message data block.
	RTN			Subroutine return.
FAULT	PSM		START	To indicate to the BC's host which message failed, push the value of the message's instruction list address on the general purpose queue.
	PBS			To identify the precise message fault(s), push the message's block status word on the general purpose queue.
	IRQ		bit pattern	Issue an interrupt to the host processor to indicate that the message had failed.
	RTN			Subroutine return.

To ensure data consistency in reading the most recently received data block, the host software should perform the following steps:

Set the general-purpose flag GP3 (i.e., clear $\overline{GP3}$) by means of the BC General Purpose Flag Register. This will ensure data sample consistency by temporarily **disabling** the BC from toggling control/status blocks and received data blocks while the host is accessing the received data. Read the current value of the control/status block pointer, which is stored at address = START + 1.

Compute the pointer of the control/status block for the most recently received message to the particular RT/sub address, by the equation:

PTR ← [START + 1] XOR 0016

To ensure that the most recently processed message was valid, read and verify the value of the message's Block Status Word, located at address = PTR + 5.

Assuming that the message was valid, the host should read the received data block, starting at the data block pointer address, which may be read from address PTR + 2.

After the host has read the entire data block, it should read the BC Condition Code Register. If Bit 4 (GP4) is set, this indicates that a message was received while the host was reading the previous data block. In this case, the host should toggle the control/status block pointer by the equation:

$PTR_1 \leftarrow PTR_1$ XOR 0010, and then clear GP4 by means of the BC General Purpose Flag Register.

To re-enable auto-toggling of the message's control/status blocks and data blocks, the host should clear GP3 (set GP3*) by means of the BC General Purpose Flag Register.

For the case of data to be transmitted by the BC (by BC-to-RT(s) messages), the message data blocks are written by the host processor rather than by the BC. As a result, the necessary operations to implement double buffering for transmit data are simpler than for received data.

In this case, the double buffering is fully controlled by the host software. That is, all the host needs to do is to:

Write a new data block to be transmitted.

After the data block has been completely written, the host should then write the value of the new control/status block to be processed as the parameter for an XEQ instruction. Since the block auto-toggling is performed by the host, the XEQ instruction rather than XQF instruction may be used to execute the message for the BC-to-RT transfer.

Bulk Data Transfers. Another common type of application is the transfer of large data structures. Examples include program downloads, sensor data, map data, and audio.

The older ACE and Mini-ACE (Plus) BC architecture combined the BC control word and the 1553 command, data, and status words (plus the internal loopback word) into a single message block. The BC architecture of the Enhanced Mini-ACE represents a major departure from this by storing the 1553 data words in a separate data block from the control and status information.

The major benefit of this is that structures of 1553 data words to be transmitted or received may be consolidated into contiguous data structures. This serves to greatly simplify the host software. The use of contiguous data structures facilitates bulk transfers to or from regions of the Enhanced Mini-ACE's shared RAM by processor block moves, DMA transfers from back plane buses, or to/from Enhanced Mini-ACE RT circular buffers.

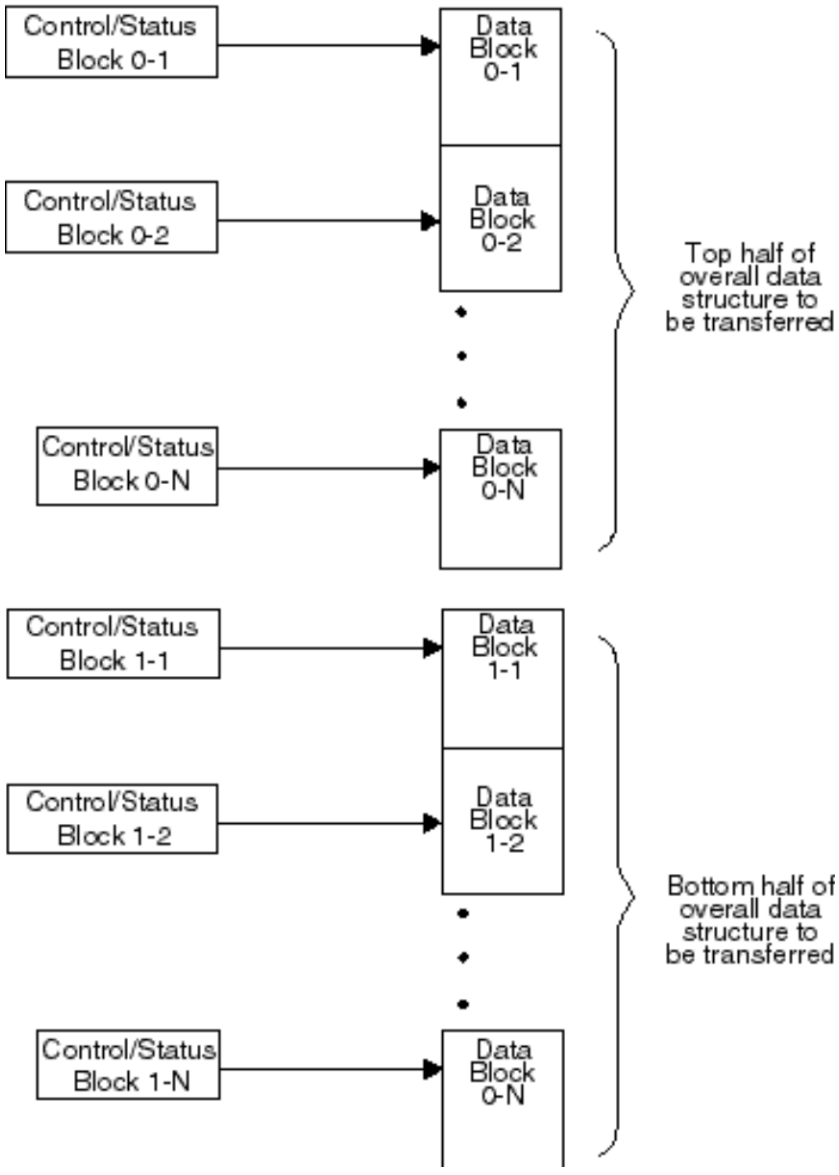


Figure 17. Bulk Data Transfers

Figure 17 provides an illustration of bulk data transfers. This diagram illustrates a method of implementing double buffering on a large scale, by dividing a bulk data structure into two sub-structures. For purpose of illustration, these are designated as the “top half” and “bottom half” of the overall data structure to be transferred. That is, by “ping-ponging” between two separate large contiguous blocks, the Enhanced Mini-ACE BC can transfer one block over the 1553 bus, while the host processor accesses the alternate data block. The Enhanced Mini-ACE BC can signal to the host that one of the two large blocks has been transferred by means of the BC’s user-definable interrupts.

In systems containing either two bus controllers with a common host, or a bus controller and one or more RT(s) with a common host, there is sometimes a need to move data between two terminals. In this case, two (or more) Enhanced Mini-ACEs may be connected to the host/RAM bus in a DMA configuration, as illustrated in Figure 18.

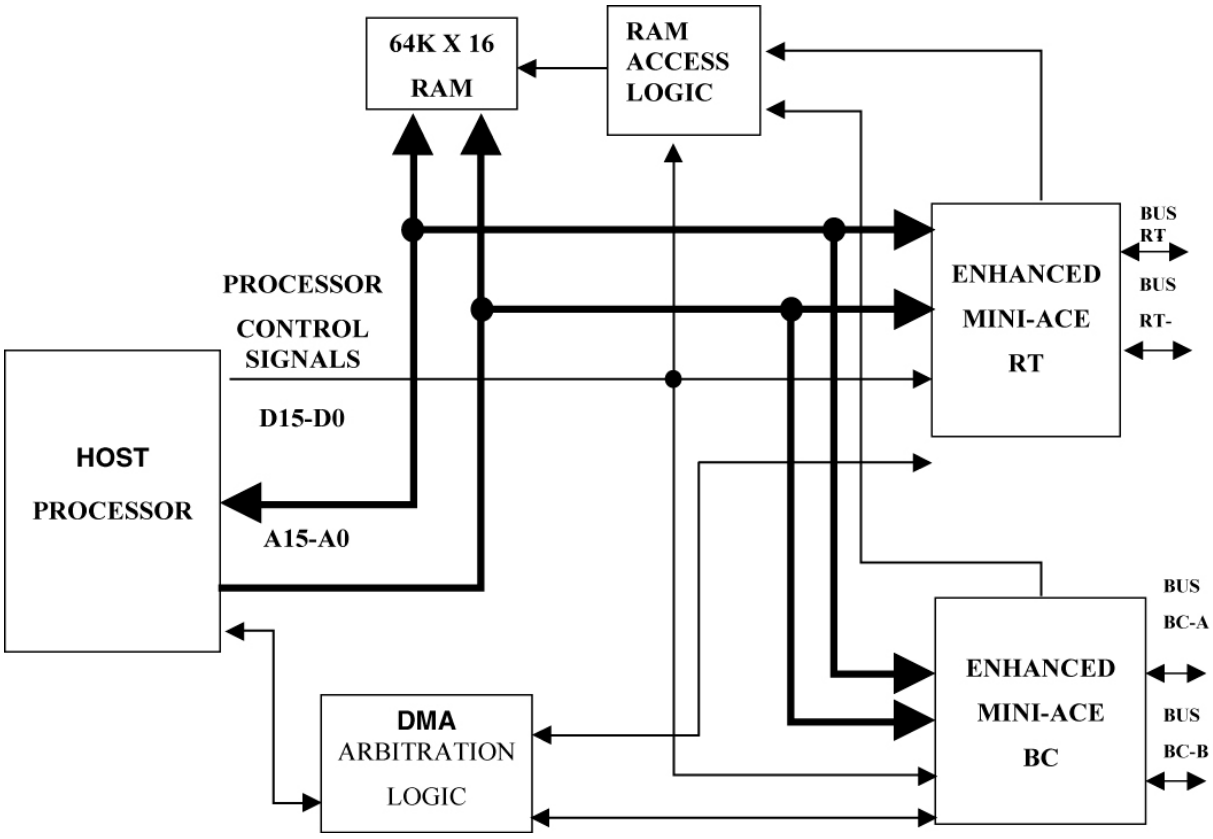


Figure 18. Enhanced Mini-ACE RT and BC in DMA Configuration with Shared DMA Address Space

In the DMA configuration, the two (or more) terminals will have access to a common host address space. It is possible to do this by designating **different** 1K X 16 areas of host RAM as the individual terminals' "fixed areas" of RAM, by means of the upper 6 bits of Configuration Register #7. In this way, the "fixed areas" of RAM (stack pointers, lookup tables, etc.) for the individual BCs or RTs are in **non-conflicting** areas of host address space.

Under this configuration, it is possible to transfer data between BC and/or RT terminals connected to two or more 1553 buses with **minimal intervention** by the host processor. That is, this arrangement eliminates the need for the host to copy individual data words.

For example, for transferring data received by a remote terminal to be transmitted by a bus controller, the Enhanced Mini-ACE's RT circular buffer feature could be used; i.e., the top half and bottom half of the data in Figure 18 could coincide with the first and second half of an Enhanced Mini-ACE RT circular buffer. If the RT circular buffer size is programmed to its maximum size of 8K words and the circular buffer 50% and 100% rollover interrupts are enabled, the circular buffer could directly coincide with the overall data structure to be transferred in Figure 18.

After the RT receives the first 4K words, the RT will issue a 50% circular buffer rollover. At that time, the host can issue a BC start to initiate the BC's transmission of these 4K words. While this is occurring, the next 4K words will be received by the RT and stored to the "bottom half" of the circular buffer. After this area is filled, assuming that the frame of the "upper half" data has been processed, the RT will issue another interrupt to the host. At this time, the host will then start a BC frame to transmit the "lower half" data.

For the case of the RT receiving bulk data that's to be re-transmitted by the BC, the host software sequence should be as follows:

1. The RT is initialized, with the receive sub address being used for the bulk data transfer configured for a sub address circular buffer.

2. When the RT issues a 50% sub address circular buffer rollover interrupt, the host sets a general purpose flag bit which enables the BC to execute a message frame to transmit the "top half" data.

3. If the RT issues a 100% sub address circular buffer rollover interrupt before the BC completes the message frame enabled in step 2 (or possibly in step 6), the host should set a general purpose flag bit which will enable a message frame to transmit the "bottom half" data. In addition, it should set the RT's "Busy" bit for the active receive sub address.

4. When the BC finishes the frame started in step 2 (or possibly in step 6), the BC should clear the general purpose flag bit the host set in that step and issue a host interrupt. In addition, if the host had set the "Busy" bit for the active sub address in step 3, it should clear the "Busy" bit at this time. If the host had not set the RT's "Busy" bit in step 3, it should wait for the RT to issue a 100% sub address rollover interrupt. When this occurs, the host should set a general purpose flag bit

which will enable the BC to process a message frame to transmit the "bottom half" data.

5. When the RT issues a 100% sub address circular buffer rollover interrupt, the host sets a general purpose flag bit which enables the BC to execute a message frame to transmit the "bottom half" data.

6. If the RT issues a 50% sub address circular buffer rollover interrupt before the BC completes the message frame enabled in step 5, the host should set a general purpose flag bit which will initiate a message frame to transmit the "top half" data. In addition, the host should set the RT's "Busy" bit for the active receive sub address.

When the BC finishes the frame started in step 5 (or possibly in step 3), the BC should clear the general purpose flag bit the host set in that step and issue a host interrupt. If the host had set the "Busy" bit for the active subaddress in step 6, it should clear the "Busy" bit at this time. If the host had not set the "Busy" bit in step 6, it should wait for the RT to issue a 50% sub address rollover interrupt. When this occurs, the host should set a general purpose flag bit which will enable the BC to process a message frame to transmit the "top half" data.

Steps 2 through 7 should be repeated until all data is transferred.

For the case of the BC receiving bulk data that's to be re-transmitted by the RT, the host software sequence should be as follows:

1. The BC executes the frame to receive the "top half" data.

2. The BC executes the frame to receive the "bottom half" data.

3. When the frame in step 2 is completed, the RT transmit sub address being used for the bulk data transfer is put on-line, with the data received from the BC frames in steps 1 and 2 defined to occupy a sub address circular buffer.

4. When the host receives a 50% circular rollover interrupt from the RT, it initiates a BC frame to receive more "top half" data.

5. When the host receives a 100% circular rollover interrupt from the RT, it initiates a BC frame to receive more "bottom half" data.

Steps 4 and 5 should be repeated until all data is transferred.

Retry and Bus Switching Strategies. The architecture of the Enhanced Mini-ACE BC may be used for combining message retry and bus switching strategies. In this way, when the Enhanced Mini-ACE BC determines that a particular RT has failed, it can automatically switch the message **permanently** from the original bus to the alternate bus. This saves BC bandwidth by eliminating the need to retry messages on failed RT channels. Table 108 illustrates the use of the XQF instruction to implement autonomous bus switching.

Table 108. Code Example of Channel Switching Using XQF Instruction				
ADDRESS LABEL	**INSTRUCTION MNEMONIC**	**CONDITION CODE (blank = unconditional)**	**PARAMETER**	**COMMENT**
	FLG		1000	Initialize, by clearing GP4.
MESSAGE	XQF	BAD MESSAGE	PTR1	Process message, allowing one retry for a failed message on the original bus. The XQF "flip" condition will be "BAD MESSAGE." If a "flip" occurs, the new control/status block pointer will be: PTRNEW = PTR1 XOR 0010
	JMP	GOOD MESSAGE	NEXT	If the message was successful, proceed to the next message.
	JMP	GP4	FAULT	Conditional jump to fault subroutine if the GP4 general purpose flag bit was set. For this instruction, if GP4 is set, this indicates that the message had failed retries on both buses.
	FLG		0010	Set GP4 (unconditionally).
	JMP		MESSAGE	Retry the message, this time using the control/status block at address PTRNEW, which will try the new message on the alternate bus.
FAULT	PSI		MESSAGE	Push the value of the message's instruction list address on the general purpose queue, indicating that the message failed on both buses.
	PBS			Push the failed message's block status word on the general purpose queue, indicating the reason(s) for the failure.
	IRQ		BIT PATTERN	Issue a host interrupt to notify of the message's fault on both buses.
NEXT	••••••••••			Next message.

5.9.4 Data Logging using the General Purpose Queue

In addition to logging failed messages, another application of the General Purpose Queue is for logging data. This allows the host to periodically read trend data for a specific parameter or parameters from the general-purpose queue.

Consider the case of a BC logging and time stamping of a particular 16-bit parameter. This method, shown in Table 109**,** may be extended to a larger number of parameters.

Table 109. Code Example of Data Logging Using the General Purpose Queue

Address Label	Instruction Mnemonic	Condition Code (blank = unconditional)	Parameter	Comment
	XEQ		PTR	Execute a transmit command message, in which the data parameter designated by the hex number “1223” is transmitted by the RT to the BC.
	PSI		1223	Push the identifying label “1223” on the general-purpose queue (immediate push).
	PSM		data word address	Push the data word received and stored at a specific address (the PSM instruction’s parameter) on the general purpose queue.
	PTT			To timestamp the posted value of parameter “1223,” push the value of the BC’s time tag register on the general-purpose queue.

5.9.5 Use of External Trigger

The Enhanced Mini-ACE BC provides the capability to synchronize the time tags RTs on a 1553 bus to the BC’s time tag register using the Synchronize (with data word) mode command. This capability is enabled by setting ENHANCED TIME TAG SYNCHRONIZE, bit 2 of Configuration Register #7, to logic “1.” As a means for extending this capability to multiple bus controllers, the Enhanced Mini-ACE includes an EXT_TRIG input signal. For the purpose of time synchronization, the EXT_TRIG input from any number of Enhanced Mini-ACE BCs may be connected to the output of a common time synchronization source. Table 110 provides an example of the use of the external trigger.

Table 110. Code Example of External Trigger

Address Label	Instruction Mnemonic	Condition Code (blank = unconditional)	Parameter	Comment
	WTG			Wait for a rising edge on the Enhanced Mini-ACE’s EXT_TRIG input before proceeding to the next instruction.
	LTT		0000	Clear the value of the Time Tag Register to 0000 (note that a different time value may also be loaded).
	XEQ		PTR	Execute the message, the transmission of a Synchronize (with data word) mode code command. This message may be sent as a broadcast command.

6 RT OPERATION

6.1 Introduction

The Enhanced Mini-ACE's Remote Terminal (RT) architecture builds upon that of the Enhanced Mini-ACE and Mini-ACE (Plus). The Enhanced Mini-ACE provides multi-protocol support, with full compliance to all of the commonly used data bus standards, including MIL-STD-1553A, MIL-STD-1553B Notice 2, STANAG 3838, General Dynamics 16PP303, and McAirA3818, A5232, and A5690. For the Enhanced Mini-ACE RT mode, there is programmable flexibility enabling the RT to be configured to fulfill any set of system requirements. This includes the capability to meet the MIL-STD-1553A response time requirement of 2 to 5 μs, and multiple options for mode code subaddresses, mode codes, RT status word, and RT BIT word.

The Enhanced Mini-ACE RT protocol design implements all of the MIL-STD-1553B message formats and dual redundant mode codes. The design has passed validation testing for MIL-STD-1553B compliance. The Enhanced Mini-ACE RT performs comprehensive error checking, word and format validation, and checks for various RT-to-RT transfer errors. One of the main features of the Enhanced Mini-ACE RT is its choice of memory management options. These include single buffering by subaddress, double buffering for individual receive subaddresses, circular buffering by individual subaddresses and a global circular buffering option for multiple (or all) subaddresses.

Other features of the Enhanced Mini-ACE RT include a set of interrupt conditions, internal command illegalization, programmable busy by subaddress and multiple options for time tagging.

The Enhanced Mini-ACE RT provides full software compatibility for legacy applications written for the older generation ACE and Mini-ACE (Plus). In addition, it provides a number of new architectural features, including a global circular buffer option, 50% rollover interrupts for circular buffers, an interrupt status queue with filtering based on valid and/or invalid messages and an "auto-boot" feature which allows the RT to initialize as an online RT with the busy bit set following power turn-on.

The Enhanced Mini-ACE provides a number of programmable options for RT memory management. The choice of memory management scheme is fully programmable on a transmit/receive/broadcast basis. The RT memory management options include a single message mode, a circular buffer mode to support bulk data transfers and a double buffering mode for individual receive subaddresses to ensure data consistency. Circular buffers may be allocated on an individual transmit and/or receive subaddress basis. In addition, there is a global circular buffer option, by which data words received to any subset of subaddresses (or all subaddresses) may be stored to a single circular buffer.

By making use of the double buffering feature, the host processor will easily be able to access the most recent, complete received block of valid data words for any given subaddress. In compliance with MIL-STD-1553B Notice 2, received data from broadcast messages may be optionally separated from non-broadcast received data.

With the circular buffer option, a variable-sized (128 to 8192 words) buffer may be allocated for data storage. Individual circular buffers may be allocated to specific subaddresses. Alternatively, received data to any subset of the 30 receive subaddresses may be stored to a common global circular buffer. In addition to helping ensure data consistency, the circular buffer feature provides a means of greatly reducing host processor overhead for bulk data transfer applications.

End-of-message interrupts may be enabled either globally, following error messages, on a Tx/Rx/Bcst subaddress or mode code basis, or when any particular Tx/Rx/Bcst subaddress circular buffer reaches its 50% boundary or lower boundary. Interrupt status registers allow the host processor to determine the cause of all interrupts by means of one or two read operations.

The Enhanced Mini-ACE implements internal RT command illegalization. The internal illegalization eliminates the need for an external PROM, PLD or RAM device. The illegalization scheme allows for any subset of the 4096 possible combinations of broadcast/own RT address, T/R* bit, subaddress and word count/mode code to be illegalized.

The Enhanced Mini-ACE RT provides options for requesting interrupts following messages for individual mode codes as well as for storing data words for the various mode codes in separate RAM locations.

The Enhanced Mini-ACE offers multiple options for designating the Remote Terminal address. Six input pins, RTAD4 through RTAD0 plus RTADP, need to be correctly strapped for RT address and odd address parity to enable RT operation. Another option allows the RT address to be latched by providing a rising edge to the input signal RT_AD_LAT. Alternatively, the Enhanced Mini-ACE's RT address may also be configured to be software programmable.

The circular buffer and double buffer features of the Enhanced Mini-ACE are enabled by setting the ENHANCED RT MEMORY MANAGEMENT bit (bit 1 of Configuration Register #2) to logic "1." If the ENHANCED RT MEMORY MANAGEMENT option is not chosen, each T/R-subaddress is mapped to a single data block by means of its respective lookup table entry. In this mode, the data block for each T/R-subaddress is then repeatedly overwritten or overread. For any given T/R*-subaddress, there are four options of memory management selectable by means of the respective subaddress control word. The four options are: (1) single buffer; (2) double buffer; (3) subaddress-specific circular buffer; (4) global circular buffer.

As a programmable option, the Enhanced Mini-ACE circular buffer pointers may be programmed to not update following the reception of invalid data blocks. This feature is enabled by setting the OVERWRITE INVALID DATA bit (bit 11) of Configuration Register #2. By so doing, retried data transmitted by the bus controller (or another RT) will automatically overwrite any invalid data blocks. This serves to facilitate bulk data transfers. The host processor needs only to initialize the Lookup Table Pointer, wait for a circular buffer rollover interrupt, and service the interrupt by accessing the multi-message block of valid data words. In this mode, the RT's host processor does not need to be concerned about servicing individual messages, retries, or errors.

Other RT options controlled by Configuration Register #2 include automatic clearing of the Service Request Status Word bit following a Transmit Vector Word mode command, and capabilities to clear and/or load the Time Tag Register following receipt of Synchronize mode commands.

See Appendix "F" for important information as Time Tag Register may not clear **IF** terminal is operating in RT Mode **AND** Interrupt Status Queue is enabled (i.e., bit 6 of Configuration Register #6 is Logic "1") **AND** bits 6, 7 or 14 (Time Tag Rollover, RT Address Parity Error, or RAM Parity Error respectively) of Interrupt Mask Register #1 are enabled (Logic "1").

It should be noted that these three features, and the use of circular buffers may be used in the NON-ENHANCED mode (bit 15 of Configuration Register #3 programmed to logic "0"), as well as in the ENHANCED mode.

Many of the salient features of the Enhanced Mini-ACE RT operate only in the ENHANCED mode (bit 15 in Configuration Register #3 programmed to logic "1"). In the ENHANCED mode, interrupts may be generated for individual mode commands, and separate fixed memory locations may be allocated for individual mode code data words (transmit and receive). The busy bit in the status word may set based on broadcast/valid RT address, transmit/receive bit, and subaddress. MIL-STD-1553B Notice 2 states that if the Busy bit is set, it should be set for a particular subaddress only.

In the ENHANCED mode, the Enhanced Mini-ACE provides RT subaddress double buffering. The RT subaddress double buffering mode allocates two 32-word data buffers to a selected subaddress. Received data is stored alternatively into each of these buffers. In many RT applications, the host processor needs to access only the data from the latest received message for a given subaddress. In this scenario, the use of the RT subaddress double buffer option serves to ensure data sample consistency by allowing the host processor to easily locate and read the most recent, consistent, valid data block received for the particular subaddress.

The Enhanced Mini-ACE also provides a combined RT/Selective Monitor Mode. In this mode, all of the Advanced RT features are available, as well as a full selective message-based monitor. The selective message monitor mode allows the user to selectively monitor data based on RT address, T/R bit, and subaddress. The message monitor has separate command and data stacks.

6.2 RT Memory Organization

Table 111 illustrates a typical memory map for an Enhanced Mini-ACE RT with 4K RAM. The two Stack Pointers reside in fixed locations in the shared RAM address space: address 0100 (hex) for the Area A Stack Pointer and address 0104 for the Area B Stack Pointer. In addition to the Stack Pointer, there are several other areas of the shared RAM address space that are designated as fixed locations (all shown in bold). These are for the Area A and Area B lookup tables, the illegalization lookup table, the busy lookup table, and the mode code data tables.

The RT lookup tables (reference Table 112) provide a mechanism for allocating data blocks for individual transmit, receive, or broadcast subaddresses. The RT lookup tables include subaddress control words as well as the individual data block pointers. If command illegalization is used, address range 0300-03FF is used for command illegalizing. The descriptor stack RAM area, as well as the individual data blocks, may be located in any of the non-fixed areas in the shared RAM address space. Note that in Table 111 there is no area allocated for "Stack B." This is shown for purpose of illustration. Also, note that in Table 111 the allocated area for the RT command stack is 256 words. However, larger stack sizes are possible. That is, the RT command stack size may be programmed for 256 words (64 messages), 512, 1024, or 2048 words (512 messages) by means of bits 14 and 13 of Configuration Register 3.

Table 111. Typical RT Memory Map (Shown For 4K RAM)	
Address (hex)	**Description**
0000-00FF	Stack A
0100	**Stack Pointer A**
0101	**Global Circular Buffer A Pointer**
0102-0103	RESERVED
0104	**Stack Pointer B**
0105	**Global Circular Buffer B Pointer**
0106-0107	RESERVED
0108-010F	**Mode Code Selective Interrupt Table**
0110-013F	**Mode Code Data**
0140-01BF	**Lookup Table A**
01C0-023F	**Lookup Table B**
0240-0247	**Busy Bit Lookup Table**
0248-025F	(not used)
0260-027F	Data Block 0
0280-02FF	Data Block 1-4
0300-03FF	**Command Illegalizing Table**
0400-041F	Data Block 5
0420-043F	Data Block 6
• • •	• • •
0FE0-0FFF	Data Block 100

6.3 RT Memory Management

The Enhanced Mini-ACE provides a variety of RT memory management capabilities. As with the ACE and Mini-ACE (Plus), the choice of memory management scheme is fully programmable on a Tx/Rx/Bc subaddress basis.

In compliance with MIL-STD-1553B Notice 2, received data from broadcast messages may be optionally separated from non-broadcast received data. For each Tx/Rx/Bcst subaddress, either a single-message data block, a double buffered configuration (two alternating Data Word blocks), or a variable-sized (128 to 8192 words) subaddress circular buffer may be allocated for data storage. The memory management scheme for individual subaddresses is designated by means of the subaddress control word (reference Table 12).

For received data, there is also a global circular buffer mode. In this configuration, the data words received from multiple (or all) subaddresses are stored in a common circular buffer structure. Like the sub address circular buffer, the size of the global circular buffer is programmable, with a range of 128 to 8192 data words.

The double buffering feature provides a means for the host processor to easily access the most recent, complete received block of valid data words for any given subaddress. In addition to helping ensure data sample consistency, the circular buffer options provide a means of greatly reducing host processor overhead for multi-message bulk data transfer applications.

End-of-message interrupts may be enabled either globally (following all messages), following error messages, on a Tx/Rx/Bcst subaddress or mode code basis, or when a circular buffer reaches its midpoint (50% boundary) or lower (100%) boundary. A pair of interrupt status registers allow the host processor to determine the cause of all interrupts by means of a single read operation.

Table 112. Lookup Tables			
Area A	**Area B**	**Description**	**Comment**
0140 • • • 015F	01C0 • • • 01DF	Rx(/Bcst) SA0 • • • Rx(/Bcst) SA31	Receive (/Broadcast) Lookup Pointer Table
0160 • • • 017F	01E0 • • • 01FF	Tx SA0 • • • Tx SA31	Transmit Lookup Pointer Table
0180 • • • 019F	0200 • • • 021F	Bcst SA0 • • • Bcst SA31	Broadcast Lookup Pointer Table (Optional)
01A0 • • • 01BF	0220 • • • 023F	SACW SA0 • • • SACW SA31	Subaddress Control Word Lookup Table (Optional)

6.4 Subaddress Control Word

In the Enhanced RT Memory Management mode, each of the 32 Subaddress control words specify the memory management and interrupt schemes for the respective subaddress. For each subaddress control word, five bits control the memory management scheme and interrupts for each of Tx, Rx, and Bcst message. In addition, bit 15 (MSB) may be used to enable subaddress double buffering and use of the global circular buffer for Rx (and/or Bcst/Rx) subaddresses. Table 113 illustrates the register bits programming needed to enable the different data buffering options, and provides a summary of the subaddress control word bit functions.

For each Tx (or Rx or Bcst) subaddress, three bits are used to specify the memory management scheme. For each Rx(/Bcst) subaddress, the memory management scheme may be selected from among the single message mode (as in the non-enhanced mode), the subaddress-specific circular buffer mode, the global circular buffer mode, or the double buffered mode. For each Tx subaddress, the memory management scheme may be selected from among the single message mode or the

subaddress-specific circular buffer mode. Note that the double buffered and global circular buffered modes are not applicable for Tx subaddresses.

It should be noted that for mode code messages, the Subaddress Control Word is only applicable if ENHANCED MODE CODE HANDLING is disabled. ENHANCED MODE CODE HANDLING is disabled in the non-ENHANCED mode or if bit 0 of Configuration Register #3 is logic "0." ENHANCED MODE CODE HANDLING is enabled in the ENHANCED MODE by setting bit 0 of Configuration Register #3 to logic "1."

In the single buffer mode, a single data block is repeatedly read (for transmit data) or overwritten (for Rx or Bcst data). Alternatively, in the circular buffer mode, data words for successive messages to/from any particular Tx, Rx or Bcst subaddresses are read from or written to the next contiguous block of locations in the respective circular buffer.

The size of the circular buffer for each Tx, Rx, or Bcst subaddress, or the global circular buffer for receive data, may be programmed for 128, 256, 512, 1024, 2048, 4096, or 8192 words. For each Tx, Rx or Bcst subaddress, two bits of the subaddress control word are used to enable interrupts. One of these bits will result in an interrupt following every message directed to the specific Tx, Rx or Bcst subaddress. The other bit will result in an interrupt at the end of a message if a) the message resulted in the Lookup table pointer for the respective transmit, receive or broadcast-subaddress crossing the 50% boundary (if enabled) b) and/or the 100% boundary (if enabled) of the respective circular buffer.

In the subaddress double-buffered mode, a pair of 32-word data blocks are allocated for a particular receive (and/or Bcst Rx) subaddress. In this mode, successive messages received to the subaddress are stored in alternating data blocks.

Table 113. Register Bits Used To Enable RT Memory Management Features						
Feature	**Subaddress Double Buffer Enable (bit 12 of Configuration Register # 2)**	**Global Circular Buffer Enables (bit 12 of Configuration Register #6)**	**Overwrite Invalid Data (Configuration Register # 2, bit 11)**	**Enhanced RTMemory Management (Configuration Register #2, bit 1)**	**Separate Broadcast (Configuration Register #2, bit 0)**	**Enhanced Mode Enabled (Configuration Register #3, bit 15)**
Default (power turn-on) Mode: Single Message for ALL Transmit, Receive or Broadcast Subaddresses	0	0	0	0	0	0
Single Message mode for all transmit subaddresses; Double Buffering for ALL receive (and broadcast) subaddresses	1 (See Note)	0	0	0	X	1 (See Note)
Broadcast Separation	X	X	X	X	1	X
Enable circular buffers for individual subaddresses; NOT overwriting invalid data	X	X	0	1	X	X
Enable circular buffers for individual subaddresses; WITH overwriting invalid data	X	X	1	1	X	X
Enable global circular buffer for receive and/or broadcast receive data; NOT overwriting invalid data.	X	1	0	1	X	1
Enable global circular buffer for receive and/or broadcast receive data; WITH overwriting invalid data.	X	1	1	1	X	1
Enable subaddress double buffering for individual receive (and broadcast) subaddresses	1 (See Note)	X	X	1	X	1 (See Note)

Note: In order to enable the subaddress double buffering mode, ENHANCED MODE (bit 15 of Configuration Register #3) must be programmed to logic "1" before Subaddress DOUBLE BUFFERING ENABLED (bit 12 of Configuration Register #2) is written as logic "1.

Table 114. Control Word Bit Map (Read/Write 04h)	
Bit	**Description**
15 (MSB)	RX: DOUBLE BUFFER ENABLE or Global Circular Buffer Enable
14	TX: EOM INT
13	TX: CIRC BUF INT
12	TX: MEMORY MANAGEMENT 2 (MM2)
11	TX: MEMORY MANAGEMENT 1 (MM1)
10	TX: MEMORY MANAGEMENT 0 (MM0)
9	RX: EOM INT
8	RX: CIRC BUF INT
7	RX: MEMORY MANAGEMENT 2 (MM2)
6	RX: MEMORY MANAGEMENT 1 (MM1)
5	RX: MEMORY MANAGEMENT 0 (MM0)
4	BCST: EOM INT
3	BCST: CIRC BUF INT
2	BCST: MEMORY MANAGEMENT 2 (MM2)
1	BCST: MEMORY MANAGEMENT 1 (MM1)
0(LSB)	BCST: MEMORY MANAGEMENT 0 (MM0)

Table 115. RT Subaddress Control Word Memory Management Options					
Double-Buffered or Global Circular Buffer (bit 15)	**Subaddress Control Word Bits**			**Memory Management Subaddress Buffer Scheme Description**	
	MM2	**MM1**	**MM0**		
0	0	0	0	Single Message	
1	0	0	0	For Receive or Broadcast: Double Buffered: For Transmit: Single Message	
0	0	0	1	128-Word	Subaddress-specific circular buffer of specified size
0	0	1	0	256-Word	
0	0	1	1	512-Word	
0	1	0	0	1024-Word	
0	1	0	1	2048-Word	
0	1	1	0	4096-Word	
0	1	1	1	8192-Word	
1	1	1	1	For receive and/or broadcast subaddresses only: Global Circular Buffer: The size of the global circular buffer may be programmed for 128, 256, 512, 1024, 2048, 4096, or 8192 words, by means of bits 11, 10, and 9 of Configuration Register #6. The pointer to the global circular buffer is stored at address 0101 (for Area A) or address 0105 (for Area B).	

Notes:

In order to utilize subaddress double buffering, the Enhanced Mini-ACE must be programmed to ENHANCED MODE (bit 15 of Configuration Register #3 must be logic "1").

It is recommended that a value of 0 be used for X to ensure compatibility with future versions.

In order to select subaddress double buffering by means of the Subaddress Control Word, the RX Subaddress DOUBLE BUFFERING ENABLE bit (bit 13) and the ENHANCED RT MEMORY MANAGEMENT bit (bit 1) of Configuration Register #2 must be programmed to logic "1." In order to use the global circular buffer option, ENHANCED MODE, ENHANCED RT MEMORY MANAGEMENT, and GLOBAL CIRCULAR BUFFER ENABLED, bit 12 of Configuration Register #6, must all be programmed to logic "1."

If the Enhanced Mini-ACE is in ENHANCED MODE and RX Subaddress DOUBLE BUFFERING ENABLE is logic "1" and ENHANCED RT MEMORY MANAGEMENT is logic "0," the subaddress double buffering mode will be used for ALL receive (and broadcast) subaddresses.

6.5 Single Message Mode

If bit 1 of Configuration Register #2 is logic "0," the Enhanced Mini-ACE memory management scheme assumes its default or non-enhanced mode. In the non-enhanced RT operation, the single message memory management mode is used for all receive, transmit, or broadcast subaddresses. It should be noted, that under the enhanced RT memory management scheme, the single message mode may still be used for individual Rx, Tx and/or Bcst subaddresses. This is the case if the Subaddress RX DOUBLE BUFFERING bit (bit 15) and the three applicable "memory management" bits in the respective Subaddress Control Word are logic "0."

The operation of the single message RT mode is illustrated in Figure 19. In the single message mode, the respective Lookup Table entry must be loaded by the host processor. At the start of each message, the lookup table entry is stored in the third address location of the respective message block descriptor in the stack area of RAM. Received data words are written to or transmitted data words are read from the Data Word Block referenced by the lookup table pointer. In the single message mode, the respective lookup table pointer is not written to by the Enhanced Mini-ACE memory management logic at the end of a message. Therefore, if a subsequent message is received for the same subaddress, the same Data Word block will be overwritten or read.

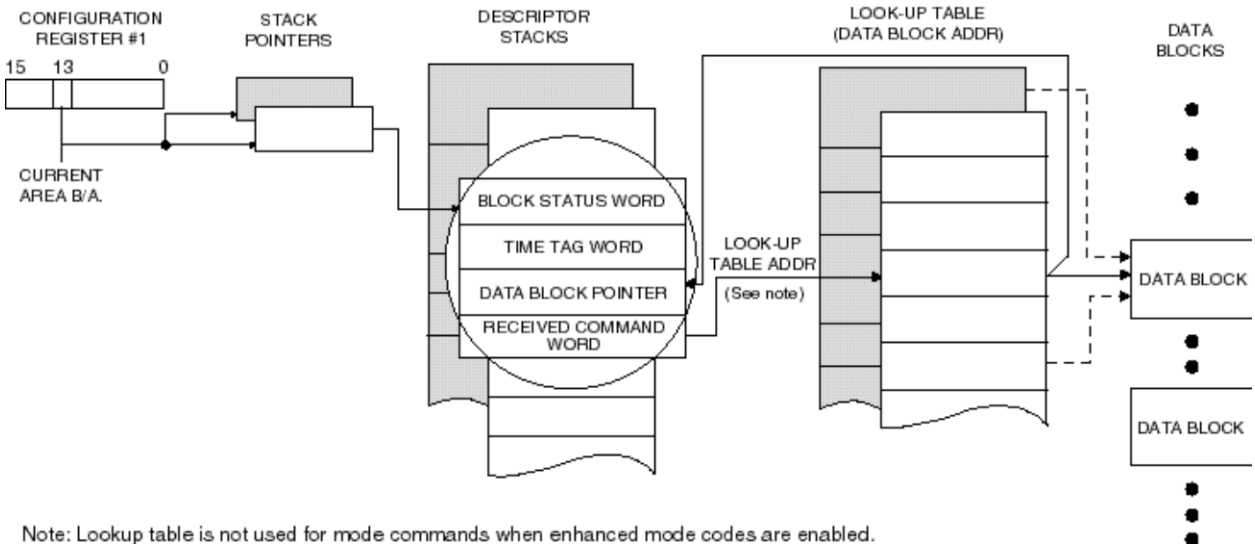


Figure 19. RT Memory Management – Single Message Mode

6.6 256-Word Boundaries

The programming of bit 10 of Configuration Register # 2, 256-WORD BOUNDARY DISABLE, must be considered for both the default memory management mode (bit 1 of Configuration Register #2 = 0) or for any Tx/Rx/Bcst subaddresses in the enhanced mode (bit 1 of Configuration Register #2 = logic “1”), using the single message mode. If 256-WORD BOUNDARY DISABLE is logic 0, the operation of the address counter for accessing RT Data Word Blocks for the single buffer mode will observe 256-word boundaries in the Enhanced Mini-ACE shared RAM address space. That is, if 256-WORD BOUNDARY DISABLE is logic 0, the internal Data Word address pointer will roll over from XXFF to XX00 (hex), rather than increment to (XX + 1) 00.

If the 256-WORD BOUNDARY DISABLE bit is set to logic "1" however, the Enhanced Mini-ACE address counter will not roll over at 256-word boundaries. In this instance, the data word addresses are generated from the output of a 16-bit counter, rather than an 8-bit counter. That is, the address counter will increment from XXFF to (XX + 1) 00, rather than roll back to XX00.

6.7 RT Subaddress Double Buffering Mode

The Enhanced Mini-ACE provides a double buffering mechanism for **received** data, optionally selectable on a subaddress basis for all Rx (and/or Bcst) subaddresses. It should be noted that the Subaddress Double Buffering mode is applicable for receive data only, **not for transmit data.**

Note: *Double buffering feature is not supported on PCI-Enhanced Mini-ACE, PCI Mini-ACE Mark3, or PCI-Micro-ACE-TE.*

Double buffering of transmit messages may be easily implemented by software techniques as shown below.

For transmitting of synchronous single-message data blocks, a software double buffering technique may be employed. That is, the host may alternate ("ping-pong") between two buffers of Data Words to be transmitted. The critical step is for the CPU to re-assign the lookup table pointer after it has written a new block of Data Words to be transmitted. This ensures data consistency by eliminating the possibility of transmitting a mixture of old and new Data Words. It should be noted that the Enhanced Mini-ACE's protocol logic samples (reads) the Lookup Table pointer only at the start of a message sequence. That is, after the Command Word is received. As a result, it will not switch blocks during the processing of a message.”

The purpose of the double buffering mode is to provide the host processor with the highest possible degree of data sample consistency. This is accomplished by allocating two 32-word data word blocks for each individual Rx (and/or Bcst/Rx) subaddress. One of the blocks will be designated as the active 1553 block while the other will be considered inactive. The data accompanying the next receive command to that subaddress will be stored in the active block. Upon completion of the message, provided that the message was valid and Receive Double Buffering is enabled, the Enhanced Mini-ACE will automatically switch the active and inactive

blocks for that subaddress. This means that the latest, valid, complete data block is always readily available to the host processor.

Operation in the double buffering RT memory management mode is illustrated in Figure 20 . The subaddress double buffer mode is available only in the ENHANCED MODE (bit 15 in Configuration #3 set). If the ENHANCED RT MEMORY MANAGEMENT ENABLE bit (bit 1 in Configuration Register #2) is programmed to logic "0," then the selective double buffer mode is enabled by simply setting the DOUBLE BUFFER ENABLE bit (bit 12 in Configuration Register #2) to logic "1." In this case (global double buffering), double buffering is enabled for all Rx subaddresses (and all Bcst/Rx subaddresses if Bcst separation is enabled).

If ENHANCED RT MEMORY MANAGEMENT ENABLE bit is programmed to logic "1," then the double buffer mode is enabled for selected subaddresses by setting the DOUBLE BUFFER ENABLE bit (bit 12 in Configuration Register #2) to logic "1" and by the programming of the desired Subaddress Control Words. The Subaddress Control word must be programmed for receive single message mode (RX:MM2-0 (bits 7-5) set to logic "0") and the DOUBLE BUFFER ENABLE bit (bit 15) must be programmed to logic "1." If SEPARATE BROADCAST is enabled (bit 0 in Configuration Register #2 is set to logic "1"), then the broadcast memory management scheme should also be set to single message mode (RX:MM2-0 (bits 2-0) programmed to logic "0") if double buffering of broadcast receive commands is desired. Reference Table 113.

The algorithm for reading the latest data block is to first disable double buffering for the desired subaddress. If ENHANCED RT MEMORY MANAGEMENT is not enabled (bit 1 of Configuration Register #2 programmed to logic "0"), double buffering must be disabled for all subaddresses by setting RECEIVE SUBADDRESS DOUBLE BUFFERING ENABLE (bit 12 in Configuration Register #2) to logic "0."

If ENHANCED RT MEMORY MANAGEMENT is enabled (the strongly recommended implementation), then double buffering can be disabled on a subaddress basis by programming the DOUBLE BUFFER ENABLE bit (bit 15) of the appropriate Subaddress Control Word to logic "0." The host processor should then read the current value of the data block pointer in the lookup table. This pointer references the active data word block. The last consistent received data block can then be accessed in the inactive block by inverting bit 5 of the current data block pointer. The current lookup table entry should not be modified.

After reading the data block, the host processor should re-enable double buffering by setting the RX DOUBLE BUFFER ENABLE bit (if ENHANCED MEMORY MANAGEMENT is not enabled) or by setting the RX DOUBLE BUFFER ENABLE bit (bit 15) in the appropriate Subaddress Control Word to logic "1" (if ENHANCED MEMORY MANAGEMENT is enabled).

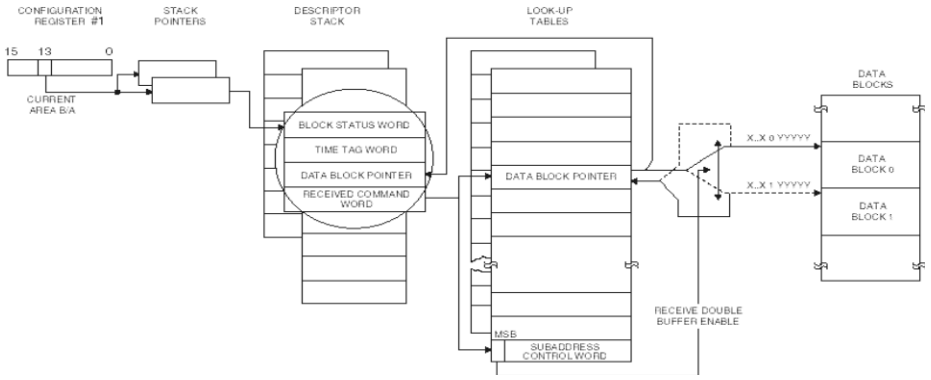


Figure 20. RT Memory Management – Subaddress Double Buffering Mode

Warning: Where user cannot guarantee to service a message before a second message to the same Subaddress is completed, it may be necessary to manually 'flip' the pointer before re-enabling Double Buffering after checking the Descriptor Stack for activity.

Note: Double Buffering is best suited to data types where messages are received at a high rate but only read occasionally, with un-read messages discarded (eg. Millisecond time update read only once per second). Otherwise Circular Buffering is more desirable.

6.8 Circular Buffer Mode

Circular buffers may be allocated on an individual transmit, receive/(/broadcast), or broadcast subaddress basis. Alternatively, there is a global circular buffer which may be utilized by any subset (or all) receive (/broadcast) or broadcast subaddresses. The operation of the circular buffer RT memory management mode is illustrated in Figure 21. As in the single message mode, the individual Lookup Table entries are initially loaded by the host processor. At the start of each message, the Lookup Table entry is stored in the third position of the respective message block descriptor in the stack area of RAM. Rx or Tx data words are transferred to/from the circular buffer, starting at the location referenced by the Lookup Table pointer. If the OVERWRITE INVALID DATA bit (bit 11) of Configuration Register #2 is logic "0," the location **after** the last word accessed for the message is stored into the respective Lookup Table location, **regardless of whether or not there were any errors in the just completed message.** By so doing, data for the **next** message for the respective Tx, Rx or Bcst subaddress will be accessed to/from the next lower contiguous block of locations in the circular buffer.

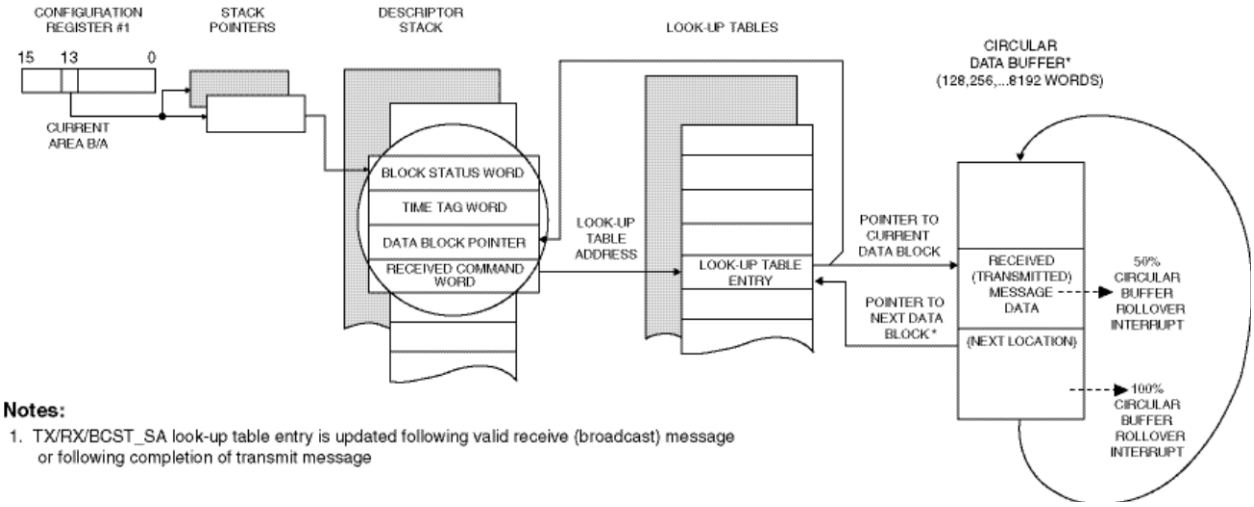


Figure 21. RT Memory Management – Subaddress-Specific Circular Buffer Mode

If the OVERWRITE INVALID DATA bit (bit 11) of Configuration Register #2 is programmed to logic "1," the location after the last word accessed for the message is stored in the respective lookup table location only following a valid received (or transmitted) message. Assuming that the value of the Lookup Table pointer is updated, data for the next message for the respective Tx, Rx or Bcst subaddress will be accessed to/from the next contiguous block of locations in the circular buffer. If the OVERWRITE INVALID DATA bit is logic "1" however, the Lookup Table pointer will not be updated at the end of the message if there was an error in the message. This allows failed messages in a bulk data transfer to be retried without disturbing the circular buffer data structure, and without intervention by the RT's host processor.

Note : *It is strongly recommended that OVERWRITE INVALID DATA be programmed to logic "1" when using the circular buffer mode.*

When the pointer reaches the lower boundary of the circular buffer (located at 128, 256, . . ., 8192-word “modulo address” boundaries in the shared RAM address space), the pointer rolls back to the top boundary of the circular buffer, as shown in Figure 21. It should be noted that the pointer to the start of the RT data word block is stored in the third location of the message block descriptor (in the stack) for the single buffer mode as well as for the circular buffer mode.

Note : *Regarding “modulo address” boundaries in the shared RAM address space. If the circular buffer size is set to 1024 words it “Rolls-Over” at modulo 1024 increments. Whatever size selected for the circular buffer (128, 256, 512, 1024, 2048, 4096, 8192) will cause a “Roll-Over” at that respective modulo.*

To make best use of the circular buffer feature for a receive subaddress, the OVERWRITE INVALID DATA bit (bit 11 of Configuration Register #2) **and** RX: CIRCULAR BUFFER ROLLOVER bit (bit 8) in the Subaddress Control Word should be programmed to logic "1.” The host processor needs to initialize the circular buffer lookup table pointer, and then wait for the circular buffer rollover interrupt. After this interrupt occurs, the PROCESSOR may then read the contiguous, multi-message block of valid, received data words from the shared RAM. Use of the RT circular buffer feature eliminates the need for the host PROCESSOR to service individual messages, or be concerned with message errors or retries.

In order to enable use of the circular buffer for a particular Bcst subaddress, you must NOT use the "separate bcst" feature (i.e., you must set SEPARATE BCST DATA, bit 0 of Configuration Register #1, to logic "0"), AND you must set bits 7, 6, and 5 (RX:MEMORY MANAGEMENT 2:0) to logic "1" AND bits 2, 1, and 0 (BCST:MEMORY MANAGEMENT 2:0) to logic "1.” This will result in data words going to the circular buffer for either BC-to-RT (broadcast) OR RT-to-RT (broadcast) messages.

If you set SEPARATE BCST DATA, bit 0 of Configuration Register #1, to logic "1" (i.e., enable broadcast separation), then the data words for broadcast messages will NOT be stored in the global circular buffer. The words will be stored in the location referenced by the receive subaddress-specific lookup table pointer.

6.9 Global Circular Buffer

Beyond the programmable choice of single buffer mode, double buffer mode, or circular buffer mode, programmable on an individual subaddress basis, the Enhanced Mini-ACE RT architecture provides an additional option, a variable sized **global** circular buffer. The Enhanced Mini-ACE RT allows for a mix of single buffered, double buffered, and individually circular buffered subaddresses, **along with** the use of the global double buffer for any arbitrary group of receive (/broadcast) or broadcast subaddresses.

In the global circular buffer mode, the data for **multiple** receive subaddresses is stored in the same circular buffer data structure. The size of the global circular buffer may be programmed for 128, 256, 512, 1024, 2048, 4096, or 8192 words, by means of bits 11, 10, and 9 of Configuration Register #6. As shown in Table 4 individual subaddresses may be mapped to the global circular buffer by means of their respective subaddress control words.

The pointer to the Global Circular Buffer will be stored in location 0101 (for Area A), or location 0105 (for Area B).

The global circular buffer option provides a highly efficient method for storing received message data. It allows for frequently used subaddresses to be mapped to individual data blocks (or subaddress-specific circular buffers), while also providing a method for assigning asynchronously received messages to infrequently used subaddresses to be logged to a common area. Alternatively, the global circular buffer provides an efficient means for storing the received data words for **all** subaddresses. Under this method, all received data words are stored chronologically, regardless of subaddress illustrates the concept of Global Circular Buffering.

Figure 22 Illustrates the concept of Global Circular Buffering.

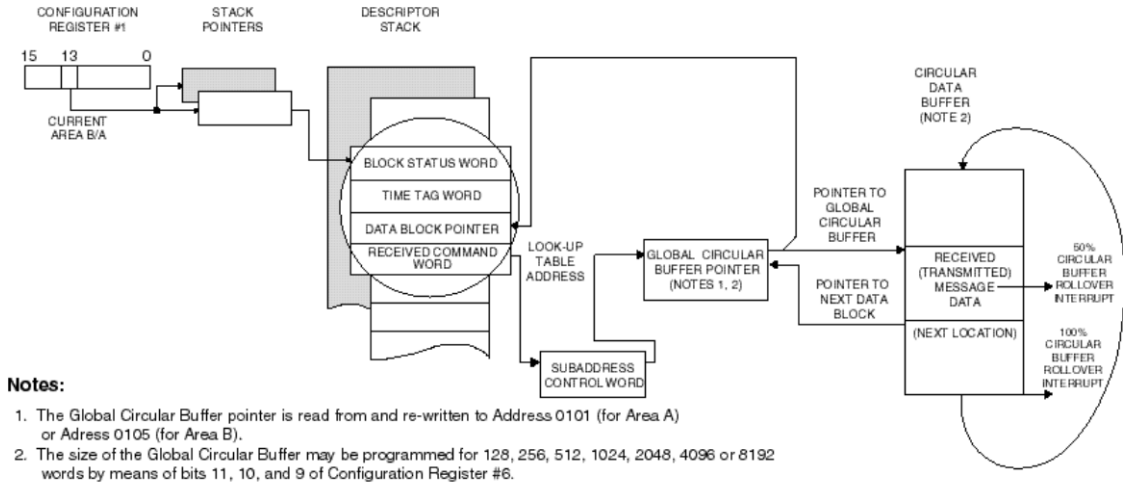


Figure 22. RT Memory Management - Global Circular Buffer

6.10 RT Descriptor Stack

The descriptor stack provides a chronology of all messages processed by the Enhanced Mini-ACE RT. Reference Figure 19, Figure 20, Figure 21 and Figure 22. Similar to BC mode, there is a 4-word block descriptor in the stack for each message processed. The four entries to each block descriptor are the Block Status Word, Time Tag Word, the pointer to the start of the message's data block, and the 16-bit received Command Word.

The RT Block Status Word includes indications of whether a particular message is ongoing or has been completed, what bus channel it was received on, indications of illegal commands, and flag bits denoting various message error conditions. For the double buffering, subaddress circular buffering, and global circular buffering modes, the data block pointer may be used for locating the data blocks for specific messages. Note that for mode code commands, there is an option to store the transmitted or received data word as the third word of the descriptor, in place of the data block pointer.

The Time Tag Word provides a 16-bit indication of relative time for individual messages. The resolution of the Enhanced Mini-ACE's time tag is programmable from among 2, 4, 8, 16, 32, or 64 µs/LSB. There is also a provision for using an external clock input for the time tag (consult factory). If enabled, there is a time tag rollover interrupt, which is issued when the value of the time tag rolls over from FFFF to 0. Other time tag options include the capabilities to clear the time tag register following receipt of a Synchronize (without data) mode command and/or to set the time tag following receipt of a Synchronize (with data) mode command. For that latter, there is an added option to filter the "set" capability based on the LSB of the received data word being equal to logic "0."

6.11 RT Interrupts

The Enhanced Mini-ACE offers a great deal of flexibility in terms of RT interrupt processing. By means of the Enhanced Mini-ACE's two Interrupt Mask Registers, the RT may be programmed to issue interrupt requests for the following events/conditions: End-of-(every)Message, Message Error, Selected (transmit or receive) Subaddress, 100% Circular Buffer Rollover, 50% Circular Buffer Rollover, 100% Descriptor Stack Rollover, 50% Descriptor Stack Rollover, Selected Mode Code, Transmitter Timeout, Illegal Command, and Interrupt Status Queue Rollover.

Interrupts for 50% Rollovers of Stacks, Circular Buffers. The Enhanced Mini-ACE RT and Monitor are capable of issuing host interrupts when a subaddress circular buffer pointer or stack pointer crosses its mid-point boundary**.** For RT circular buffers, this is applicable for both transmit and receive subaddresses. Reference Figure 23. There are four interrupt mask and interrupt status register bits associated with the 50% rollover function:

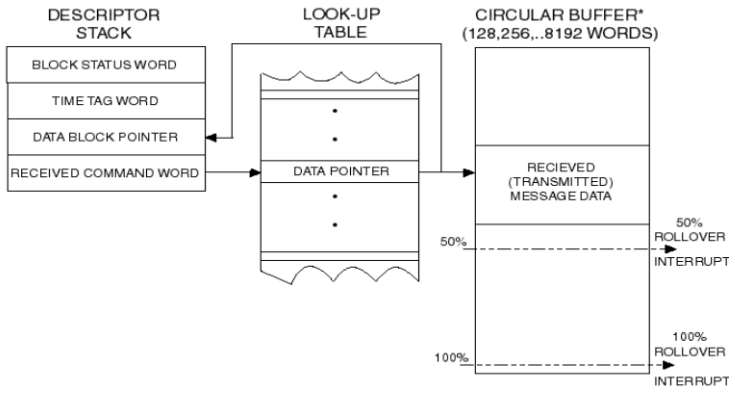
1. RT circular buffer;

2. RT command (descriptor) stack;

3. MT command (descriptor) stack; and

4. MT data stack.

The 50% rollover interrupt is beneficial for performing bulk data transfers. For example, when using circular buffering for a particular receive subaddress, the 50% rollover interrupt will inform the host processor when the circular buffer is half full. At that time, the host may proceed to read the received data words in the upper half of the buffer, while the Enhanced Mini-ACE RT writes received data words to the lower half of the circular buffer. Later, when the RT issues a 100% circular buffer rollover interrupt, the host can proceed to read the received data from the lower half of the buffer, while the Enhanced Mini-ACE RT continues to write received data words to the upper half of the buffer.



Note: This figure is for an RT Subaddress Circular Buffer. The 50% and 100% Rollover Interrupts are also applicable to the RT Global Circular Buffer, RT Command Stack, Monitor Stack and Monitor Data Stack.

Figure 23. 50% and 100% Rollover Interrupts

6.12 RT Block Status Word

The bit map and bit definitions for the RT Block Status Word are indicated in Table 116.

Table 116. RT Mode Block Status Word

Bit	Description
15(MSB)	EOM
14	SOM
13	CHANNEL B/A*
12	ERROR FLAG
11	RT-RT FORMAT
10	FORMAT ERROR
9	NO RESPONSE TIMEOUT
8	LOOP TEST FAIL
7	DATA STACK ROLLOVER
6	ILLEGAL COMMAND WORD
5	WORD COUNT ERROR
4	INCORRECT DATA SYNC
3	INVALID WORD
2	RT-RT GAP/SYNCH/ADDRESS ERROR
1	RT-RT 2ND COMMAND ERROR
0(LSB)	COMMAND WORD CONTENTS ERROR

END-OF-MESSAGE (EOM) (bit 15): Set at the completion of an RT message, regardless of whether or not there were any errors in the message.

START-OF-MESSAGE (SOM) (bit 14): Set approximately 3 to 4 µs following the receipt (mid-parity bit) of the Command Word and cleared at the end of the message.

CHANNEL B/A* (bit 13): This bit will be logic “0” if the message was processed on Channel A or logic “1” if the message was processed on Channel B.

ERROR FLAG (bit 12): If this bit is logic "1," and one or more of bits 10, 9, and/or 8 are logic "1," this indicates one or more of the following errors have occurred in the message: Format Error Response Timeout and/or Loop Test Fail.

If this bit is logic "1," the Enhanced Mini-ACE is configured for its transparent mode of processor interface, and bits 11 through 8 are all logic "0," this indicates that a

handshake failure has occurred. A handshake failure occurs when the input signal DTGRT* is either not asserted low or is asserted low too late after the time that the output signal DTREQ* is asserted low. A handshake failure also occurs if the PROCESSOR transfer control input STRB* is asserted for too long after the Enhanced Mini-ACE's READYD* output has been asserted (low). If a handshake failure occurs, a message should be considered invalid. The allotted time for the PROCESSOR providing the DTGRT* signal or clearing the STRBD* input is 10 µs.

RT-to-RT FORMAT (bit 11): Applicable for ENHANCED MODE only (ENHANCED MODE ENABLED, bit 15 of Configuration Register #3, set to logic "1"). This bit will be set if the Enhanced Mini-ACE is the **receiving** RT in an RT-to-RT transfer. Note that this bit will **not** be set if the Enhanced Mini-ACE is the **transmitting** RT for an RT-to-RT transfer.

FORMAT ERROR (bit 10): If set, indicates that the received portion of a message contained one or more violations of the 1553 message validation criteria (sync, encoding, parity, bit count, word count, etc.). This bit is a summation of bits 5, 4, 3, 2, 1, and 0.

RESPONSE TIMEOUT (bit 9): If set, indicates that the Enhanced Mini-ACE was the receiving RT for an RT-to-RT transfer **and** that the transmitting RT has either not responded or has responded later than the programmed value for the No Response Timeout time. The Enhanced Mini-ACE's RT-to-RT No Response Timeout Time is defined as the time from the mid-bit crossing of the parity bit of the Transmit Command Word to the mid-sync crossing of the RT Status Word. In the non-enhanced mode (ENHANCED MODE ENABLED, bit 15 of Configuration Register #3, is logic "0"), the value of the BC Response Timeout is 17.5 to 19.5 µs. If ENHANCED MODE ENABLED is Logic “1,” the value of the No Response Timeout value is programmable from among the nominal values 18.5, 22.5, 50.5, and 128 µs (±1 µs) by means of bits 10 and 9 of Configuration Register #5.

LOOP TEST FAIL (bit 8): A loopback test is performed on the transmitted portion of every non-broadcast message in RT mode. A validity check is performed on the received version of every word transmitted by the Enhanced Mini-ACE RT. In addition, a bit-by-bit comparison is performed on the last word transmitted by the RT for each message. If either the received version of any transmitted word is determined to be invalid (sync, encoding, bit count, and/or parity error) and/or the received version of the last transmitted word does not match the transmitted version, the LOOP TEST FAIL bit will be set.

Note: *The following 2 definitions will be used frequently throughout the text.*

ENHANCED MODE requires bit 15 of Configuration Register #3 programmed to logic "1.”

ENHANCED MODE DISABLE requires bit 15 of Configuration Register #3 programmed to logic "0.”

6.13 Bits that can be set with Enhanced Mode Only

This means that the ENHANCED MODE ENABLED bit 15 of Configuration Register #3 has been set to logic "1."

CIRCULAR BUFFER ROLLOVER (bit 7): If ENHANCED RT MEMORY MANAGEMENT is enabled (bit 1 of Configuration Register # 2 is set to logic "1") **and** the circular buffer option is enabled for the Bcst/Tx/Rx-subaddress for the current message, by means of the Subaddress Control Word. This bit will be set if the lookup table address pointer crossed the upper boundary of its circular buffer, resulting in a rollover. If OVERWRITE INVALID DATA is enabled (bit 11 of Configuration Register #2 set to logic "1"), this bit will only be set following completion of a transmit message or a **valid** receive message that resulted in a rollover. If OVERWRITE INVALID DATA is disabled (bit 11 of Configuration Register #2 set to logic "0"), this bit will be set when a rollover occurs, independent of message validity.

It should be noted that in the ENHANCED mode disabled, bits 7 through 0 will always be logic "0."

ILLEGAL COMMAND WORD (bit 6): If this bit is set, it indicates that the message has been illegalized. A message is illegalized if (ENHANCE MODE ENABLE, bit 15 of Configuration Register #3 is logic "0" **or** ILLEGALIZATION DISABLE, bit 7 of Configuration Register #3 is logic "0") **and** the appropriate bit for the respective Bcst/Tx/Rx-Subaddress-Word Count/Mode Code combination is set in the illegalization table, address locations 0300-03FF in the shared RAM.

WORD COUNT ERROR (bit 5): If set, indicates that the BC did not transmit the correct number of data words.

INCORRECT DATA SYNC (bit 4): If set, indicates that the BC transmitted a Command sync in a Data Word.

INVALID WORD (bit 3): Indicates the BC (or transmitting RT in an RT-to-RT transfer) transmitted one or more words containing one or more of the following error types: sync field error, Manchester encoding error, parity error, and/or bit count error.

RT-to-RT GAP/SYNC/ADDRESS ERROR (bit 2): This bit is set if the Enhanced Mini-ACE RT is the receiving RT for an RT-to-RT transfer and one or more of the following occur: (1) If the GAP CHECK ENABLED bit (bit 8) of Configuration Register #5 is set to logic "1" and the transmitting RT responds with a response time of less than 4 µs, per MIL-STD-1553B (mid-parity bit to mid-sync); i.e., less than 2 µs dead time; and/or (2) There is an incorrect sync type or format error (encoding, bit count, and/or parity error) in the transmitting RT Status Word; and/or (3) The RT address field of the transmitting RT Status Word does not match the RT address in the transmit Command Word.

RT-to-RT SECOND COMMAND ERROR (bit 1): If the Enhanced Mini-ACE is the receiving RT for an RT-to-RT transfer, this bit set indicates one or more of the following error conditions in the transmit Command Word: (1) T/R* bit = logic "0"; (2) subaddress = 00000 or 11111; and/or (3) same RT address field as the receive Command Word.

COMMAND WORD CONTENTS ERROR (bit 0): Indicates a received command word is not defined in accordance with MIL-STD-1553B. This includes the following undefined Command Words: (1) BROADCAST DISABLED, bit 7 of Configuration Register #5 is logic "0" and the Command Word is a non-mode code, Bcst, Tx command; (2) The OVERRIDE MODE T/R* ERROR bit, bit 6 of Configuration Register #3, is logic "0" and a message with a T/R* bit of "0," a subaddress/mode field of 00000 or 11111 and a mode code field between 00000 and 01111; (3) BCST DISABLED, bit 7 of Configuration Register #5 is logic "0" and a mode code command that is not permitted to be broadcast (e.g. Transmit status) is sent to the Bcst address (11111).

6.14 Time Tag Word

The Time Tag Word, the second location of the message block descriptor in the RT Command Stack, is updated (written) during both the Start-of-Message (SOM) and End-of-Message (EOM) sequences. The SOM sequence occurs immediately after reception of a valid Command Word to the RT's address or the Bcst address. The EOM sequence occurs approximately 3 to 4 µs after the last word transmitted or received in a message.

During these sequences, the current value of the Enhanced Mini-ACE's internal read/writable Time Tag Register (register address 05) is written to the respective RAM location. The resolution of the Time Tag counter is programmable from among 2, 4, 8, 16, 32, and 64 µs/LSB, or an externally provided clock (consult factory), by means of bits 9, 8, and 7 of Configuration Register #2.

The value of the Time Tag Register will roll over from FFFF (hex) to 0000 after every 65,536 counts (LSB times). When the rollover occurs, a TIME TAG ROLLOVER interrupt request will occur, if enabled by means of the Interrupt Status Register. In addition, the TIME TAG ROLLOVER bit in the Interrupt Status Register will become set following the rollover if (1) the interrupt is enabled, or (2) ENHANCED INTERRUPTS are enabled (ENHANCED MODE and bit 15 of Configuration Register #2 is programmed to logic "1").

If CLEAR TIME TAG ON SYNCHRONIZE, bit 6 of Configuration Register #2, is programmed to logic "1," the value of the Enhanced Mini-ACE RT Time Tag Register will be cleared to 0000 following receipt of a Synchronize (without data) mode command.

∗ **See Appendix "F"** for important information regardingTime Tag Rollover (i.e., bit 6 of Interrupt Register #1 is Logic "1") used in conjunction with Interrupt Status Queue (i.e., bit 6 of Configuration Register #6 is Logic "1").

If LOAD TIME TAG ON SYNCHRONIZE, bit 5 of Configuration Register #2, is programmed to logic "1," the value of the received Data Word will be loaded into the Enhanced Mini-ACE RT Time Tag Register following receipt of a valid Synchronize with data mode command and the accompanying Data Word.

6.15 Data Block Pointer or Mode Code Data Word

The third word location within the RT message descriptor is used for two different purposes. For non-mode code messages, or for mode code messages with ENHANCED MODE CODE HANDLING disabled (bit 15 or bit 0 of Configuration Register #3 programmed to logic "0"), the value read from the RT lookup table is stored in this location. This value indicates the starting location of the Data Word block for the respective message.

For mode code messages with data and ENHANCED MODE CODE HANDLING enabled, the Data Word that is transmitted or received for a mode code message with data is written to this location during the RT End-of-Message (EOM) sequence.

For mode code messages without data, no word is written to the third location of the message block descriptor.

6.16 Command Word Received

For all messages, the received Command Word is stored in the fourth location in the message block descriptor during the RT Start-of-Message (SOM) sequence.

6.17 Superceding Commands

A superceded message sequence occurs when a valid message begins on one bus, followed by a time gap, followed by a new command on the alternate bus. If both the old and the new command are to the same RT address, the RT must stop processing the first command, and begin processing the new command. If the commands are to different RT addresses, the terminal responding to the first command must complete processing the message and ignore the activity on the alternate bus.

For a superceding command to its RT address, the Enhanced Mini-ACE RT will abort processing the first message and begin processing the new message. The only exception to this is when the Enhanced Mini-ACE is operating in the combined RT/Selective Message mode and the first command is to the Enhanced Mini-ACE's RT address and the second command is to a different, non-broadcast, RT address. As an RT, the Enhanced Mini-ACE will continue processing the first command (in compliance with MIL-STD-1553), and ignore the new command to a different RT on the alternate bus.

The Enhanced Mini-ACE selective message monitor will supercede a message on the same bus except when the superceding command may be interpreted as a status word. Consequently, a RT status response with the wrong RT address in the status word will NOT appear to the Enhanced Mini-ACE selective message monitor as a new command, but rather will appear to be a bad status word.

When a message is superceded, a normal Start Of Message (SOM) sequence is performed on the new (superceding) message. Note that an End Of Message (EOM) sequence is **not** executed on the original (superceded) message. This will result in a command stack entry with the Start Of Message (SOM) bit in the block status word set to logic "1" and the End Of Message (EOM) bit set to logic "0." The host processor can distinguish between a message in progress and a superceded message by the value of the monitor command stack pointer. If the monitor command stack pointer has incremented beyond the command stack entry in question and the block status word indicates an SOM state, then the message must have been superceded.

The procedure used to increment the Command Stack Pointer is determined by means of Configuration Register # 6 , bit 13 (**Command Stack Pointer Increment on EOM**). If this bit is programmed to logic "0" (default, ACE/Mini-ACE (Plus) compatible), the value of the Command Stack Pointer RAM location will be incremented by four (4) during the message's **SOM** (start-of-message) sequence. If this bit is programmed to logic "1," the value of the Command Stack Pointer will be incremented by four (4) during the message's **EOM** (end-of-message) sequence.

In **either** case (i.e., for Command Stack Pointer Increment on EOM = 0 **or** = 1), There **will** be a descriptor created in the RT Command Stack. For the Block Status Word of this descriptor the EOM bit will be "0," and the SOM bit will be "1."

Note: *For new Enhanced Mini-ACE RT or Message Monitor applications, it is recommended that COMMAND STACK POINTER INCREMENT ON EOM both be programmed to values of logic "1."*

6.18 RT Interrupts

The Enhanced Mini-ACE offers a great deal of flexibility in terms of RT interrupt processing. In some systems, the transmission or reception of a message with a particular subaddress denotes the end of a complete set of consistent data. In this instance, the user should use the RT Subaddress CONTROL WORD INTERRUPT in order to issue an interrupt request only for a particular T/R-subaddress, rather than following every message. One technique would then be for the host processor to switch the active area of shared RAM, by toggling bit 13 of Configuration Register #1 at this time.

An interrupt request for a circular buffer rollover condition (if enabled) will occur only following the end of a transmit message during which the last location in the circular buffer has been read **or** following the end of a valid receive or broadcast message in which the last location in the circular buffer has been written.

If ENHANCED MODE CODES are enabled (bit 0 of Configuration Register #3 is logic "1"), interrupts may be enabled following receipt of specific mode code messages. These interrupts may be enabled by means of the Mode Code Selective Interrupt Table, address locations 0108-010F in shared RAM.

6.19 Interrupt Status Queue

See Appendix "F" for important information **IF** THE Interrupt Status Queue is enabled **AND** terminal is operating in RT Mode **AND** bits 6, 7 or 14 (Time Tag Rollover, RT Address Parity Error, or Ram Parity Error respectively) of Interrupt Mask Register #1 are enabled (logic "1").

The Enhanced Mini-ACE RT, Monitor, and combined RT/Monitor modes include the capability for generating an interrupt status queue. As illustrated in Figure 24, this provides a chronological history of interrupt generating events and conditions. In addition to the Interrupt Mask Register, the Interrupt Status Queue provides additional filtering capability, such that only valid messages and/or only invalid messages may result in the creation of an entry to the Interrupt Status Queue. Queue entries for invalid and/or valid messages may be individually **disabled** by means of bits 8 and 7 respectively of Configuration Register #6.

The pointer to the Interrupt Status Queue is stored in the INTERRUPT VECTOR QUEUE POINTER REGISTER (register address 1F). This register must be initialized by the host, and is subsequently incremented by the RT message processor. The interrupt status queue is 64 words deep, providing the capability to store entries for up to 32 messages.

The queue rolls over at addresses of modulo 64. The events that result in queue entries include both message-related and non-message related events. Note that the Interrupt Vector Queue Pointer Register will always point to the next location (modulo 64) **following** the last vector/pointer pair written by the Enhanced Mini-ACE RT, Monitor, or RT/Monitor.

Each event that causes an interrupt results in a two-word entry to be written to the queue. The first word of the entry is the interrupt vector. The vector indicates which interrupt event(s)/condition(s) caused the interrupt.

The interrupt events are classified into two categories: message interrupt events and non-message interrupt events. Message-based interrupt events include End-of-Message, Selected mode code, Format error, Subaddress control word interrupt, RT Circular buffer Rollover, Handshake failure, RT Command stack rollover, transmitter timeout, MT data stack rollover, MT command stack rollover, RT Command stack 50% rollover, MT data stack 50% rollover, MT command stack 50% rollover, and RT Circular buffer 50% rollover. Non-message interrupt events/conditions include time tag rollover, RT address parity error, RAM parity error, and BIT completed.

Bit 0 of the interrupt vector (interrupt status) word indicates whether the entry is for a message interrupt event (if bit 0 is logic "1") or a non-message interrupt event (if bit 0 is logic "0"). It is **not** possible for one entry on the queue to indicate both a message interrupt and a non-message interrupt.

For a message interrupt event, the parameter word is a pointer. The pointer will reference the first word of the RT or MT command stack descriptor (i.e., the Block Status Word).

For a RAM Parity Error non-message interrupt, the parameter will be the RAM address where the parity check failed. For the RT address Parity Error, Protocol Self-test Complete, and Time Tag Rollover non-message interrupts, the parameter is not used; it will have a value of 0000.

If enabled, an INTERRUPT STATUS QUEUE ROLLOVER interrupt will be issued when the value of the queue pointer address rolls over at a 64-word address boundary.

Table 117 defines the RT/Monitor Interrupt status word for message and non-message interrupt events. Detailed bit descriptions are listed following the table.

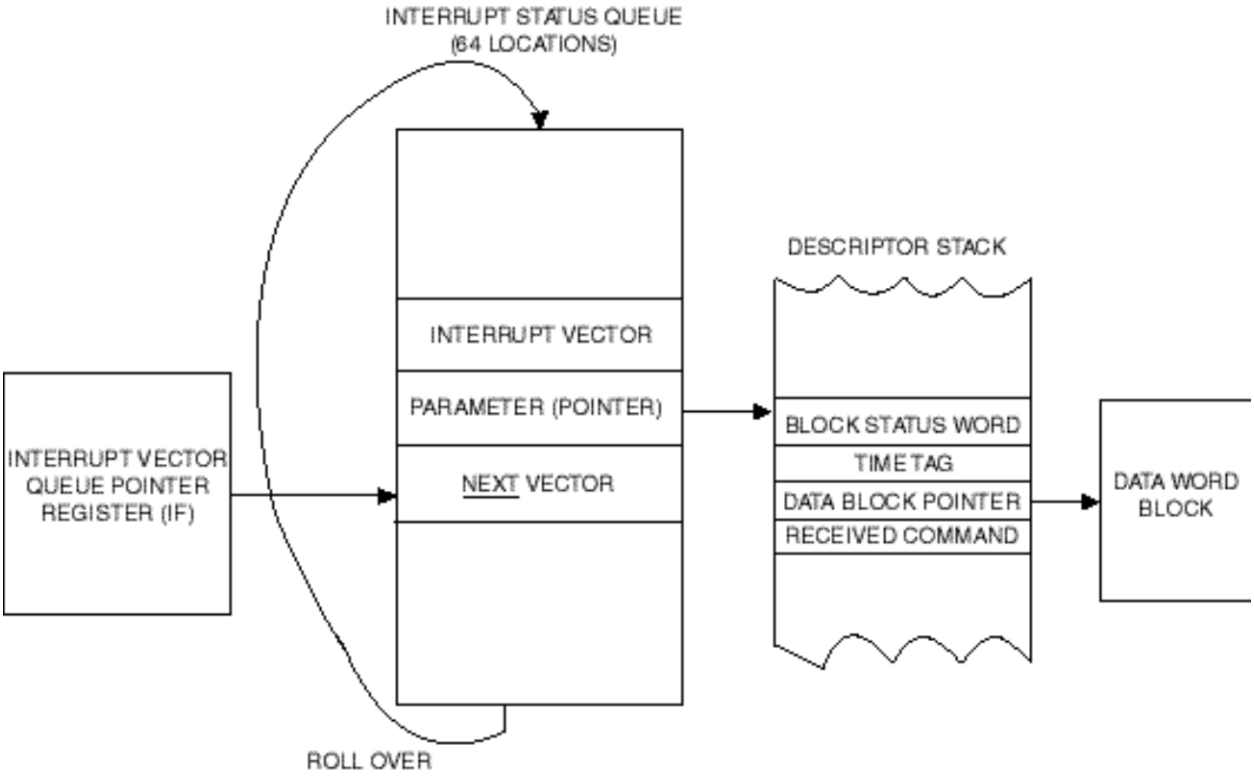


Figure 24. RT (and Monitor) Interrupt Status Queue (shown for message interrupt event)

RT Monitor Interrupt Vector Word: The format of the RT/Monitor Interrupt Vector Word is illustrated in Table 117. For each entry in the queue, bit 0 denotes whether it was caused by a message related or non-message related event or condition. Bits 15-1 then specify the actual event or condition that caused the interrupt.

Table 117. RT/Monitor Interrupt Vector Word (for Interrupt Status Queue)		
Bit	**Definition for Message Interrupt Event**	**Definition for Non-Message Interrupt Event**
15	TRANSMITTER TIMEOUT	NOT USED
14	ILLEGAL COMMAND	NOT USED
13	MONITOR DATA STACK 50% ROLLOVER	NOT USED
12	MONITOR DATA STACK ROLLOVER	NOT USED
11	RT CIRCULAR BUFFER 50% ROLLOVER	NOT USED
10	RT CIRCULAR BUFFER ROLLOVER	NOT USED
9	MONITOR COMMAND (DESCRIPTOR) STACK 50% ROLLOVER	NOT USED
8	MONITOR COMMAND (DESCRIPTOR) STACK ROLLOVER	NOT USED
7	RT COMMAND (DESCRIPTOR) STACK 50% ROLLOVER	NOT USED
6	RT COMMAND (DESCRIPTOR) STACK ROLLOVER	NOT USED
5	HANDSHAKE FAIL	NOT USED
4	FORMAT ERROR	TIME TAG ROLLOVER
3	MODE CODE INTERRUPT	RT ADDRESS PARITY ERROR
2	SUBADDRESS CONTROL WORD EOM	PROTOCOL SELF-TEST COMPLETE
1	END-OF-MESSAGE (EOM)	RAM PARITY ERROR
0	"1" FOR MESSAGE INTERRUPT EVENT; "0" FOR NON-MESSAGE INTERRUPT EVENT NOT USED	

MESSAGE INTERRUPT EVENT BITS

RT TRANSMITTER TIMEOUT (bit 15): This bit indicates that the Enhanced Mini-ACE's transmitter watchdog timer has timed out. This occurs if the Enhanced Mini-ACE's encoder attempts to transmit for longer than 660.5 µs.

MONITOR DATA STACK 50% ROLLOVER (bit 13): For Selective Monitor mode, this bit indicates that the Monitor data stack pointer has crossed an address boundary which is an exact multiple of half of the programmed value of the Monitor Data Stack size. If the data stack pointer was initialized at an address, which is an exact multiple of its programmed size, then this interrupt will indicate that the data stack is half full. Note that this interrupt will occur at the end of the message in which the 50% rollover occurred.

MT DATA STACK ROLLOVER (bit 12): This bit indicates a rollover of the Word Monitor or Message Monitor Data Stack. The size of the Data Stack is programmable from among 512, 1024, 2048, 4096, 8192, 16,384, 32,768, or 65,536 words by means of bits 10, 9, and 8 of Configuration Register #3.

RT CIRCULAR BUFFER 50% ROLLOVER (bit 11): For RT mode, this bit indicates that an RT circular buffer (either for an individual transmit, receive(/broadcast), or broadcast subaddress, or the global circular buffer) has crossed an address boundary which is an exact multiple of half of the programmed value of the circular buffer size.

If the circular buffer lookup table pointer was initialized at an address, which is an exact multiple of its programmed size, then this interrupt indicates that the stack is half full. Note that this interrupt occurs at the end of the message in which the 50% rollover occurred.

RT CIRCULAR BUFFER ROLLOVER (bit 10): This bit will be set at the end of a message in RT mode, provided that the Enhanced Mini-ACE is in the ENHANCED RT Memory Management mode (bit 2 of Configuration Register #2 = logic “1”) **and** the "Interrupt at Rollover" bit is set in the Subaddress Control Word for the Tx/Rx/Bcst subaddress of the just completed message **and** the current message caused the data block Lookup Table address pointer to cross the lower boundary of the respective circular buffer, resulting in a rollover. This interrupt is applicable for rollovers of either a subaddress-specific circular buffer, or the global circular buffer.

Note that if OVERWRITE INVALID DATA (bit 11 of Configuration Register #2) is logic "0, "this interrupt request will occur immediately when the address location at the upper boundary of a circular buffer is accessed. If OVERWRITE INVALID DATA is logic "1," the interrupt request will occur at the end of a valid message in which the last location in the circular buffer was accessed. If OVERWRITE INVALID DATA is logic "1," an RT CIRCULAR BUFFER ROLLOVER will not occur following an invalid received message.

MONITOR COMMAND STACK 50% ROLLOVER (bit 9): For Selective Monitor mode, this bit indicates that the Monitor descriptor stack (command stack) pointer has crossed an address boundary which is an exact multiple of half of the programmed value of the Monitor Command Stack size. If the command stack pointer was initialized at an address that is an exact multiple of its programmed size, then this interrupt indicates that the command stack is half full.

The timing for this interrupt request depends on the programming of COMMAND STACK POINTER INCREMENT ON EOM, bit 13 of Configuration Register #6. If COMMAND STACK POINTER INCREMENT ON EOM is logic "0" (default), then the command stack 50% rollover interrupt occurs during the SOM (start-of-message) sequence for the message in which the 50% rollover occurred. This happens following receipt of the command word. However, if COMMAND STACK POINTER INCREMENT ON EOM has been programmed to logic "1,” then the command stack 50% rollover interrupt will occur at the end of the EOM (END-of-message) sequence, for the message in which the value of the stack pointer incremented past the 50% point of the command stack. The “50% rollover” address will be an exact multiple of half of the programmed stack size.

MT COMMAND STACK ROLLOVER (bit 8): This bit indicates an interrupt following a rollover of the Message Monitor Command Stack. This is applicable for both the Message Monitor as well as the combined RT/Message Monitor modes. The size of the MT Command Stack is programmable from among 256 (64 messages), 1024, 4096, and 16,384 words (4096 messages) by means of bits 12 and 11 of Configuration Register #3.

RT COMMAND STACK 50% ROLLOVER (bit 7): For RT mode, this bit indicates that the RT descriptor stack (command stack) pointer has crossed an address boundary which is an exact multiple of half of the programmed value of the Command Stack size. If the stack pointer was initialized at an address that is an exact multiple of its programmed size, then this interrupt indicates that the stack is half full.

The timing for this interrupt depends on the programming of COMMAND STACK POINTER INCREMENT ON EOM, bit 13 of Configuration Register #6. If COMMAND STACK POINTER INCREMENT ON EOM is logic "0" (default), then the command stack 50% rollover interrupt will occur during the SOM (start-of-message) sequence for the message in which the 50% rollover occurred, which occurs following receipt of the command word. However, if COMMAND STACK POINTER INCREMENT ON EOM has been programmed to logic "1," then the command stack 50% rollover interrupt occurs at the end of the EOM (END-of-message) sequence, for the message in which the value of the stack pointer incremented past the 50% point of the command stack. The “50% rollover” address will be an exact multiple of half of the programmed stack size.

RT COMMAND STACK ROLLOVER (bit 6): This bit indicates a rollover of the BC/RT Command Stack. The size of the BC/RT Command Stack 1 is programmable from among 256 words (64 messages), 512, 1024, and 2048 words (512 messages) by means of bits 14 and 13 of Configuration Register #3. The rollover will occur after a stack address of modulo the stack size has been accessed.

HANDSHAKE FAILURE (bit 5): This bit indicates an interrupt has occurred following a handshake timeout during a transfer between the 1553 protocol section and the RAM. A Handshake Failure can **only** occur in the **transparent** configuration of the Enhanced Mini-ACE host interface. There are two conditions that can cause a Handshake Failure. For both conditions, the maximum allotted time is 10.5 μs for a 20 MHz clock input, 10.0 μs for a 16 MHz clock input, 9.0 μs for a 12 MHz clock input, and 8.5 μs for a 10 MHz clock input:

Condition 1 occurs when the Data Transfer Grant (DTGRT*) input is not asserted within the allotted time after the Enhanced Mini-ACE's Data Transfer Request (DTREQ*) output has been asserted.

Condition 2 occurs when the STRBD* input signal is held low too long at the end of a processor transfer cycle (as indicated by the falling edge of READYD*). Note that STRBD* asserted low for too long will **not** result in a HANDSHAKE-FAILURE condition in the buffered mode configuration.

FORMAT ERROR (bit 4): This bit indicates an interrupt request for any of the following conditions:

Loop Test Failure: A loopback test is performed on all messages transmitted by the RT (except broadcast messages in RT mode). The received version of all transmitted words is checked for validity and correct sync type. In addition, a 16-bit comparison is performed on the last word transmitted by the RT. If any of these checks or comparisons do not verify, the loopback test is considered to have failed. Loop Test Failure is not applicable in Monitor mode.

Message Error: A received message contained a violation of the 1553 message validation criteria (encoding, parity, bit count, word count, etc.).

Response Timeout: In RT mode, if the Enhanced Mini-ACE is the receiving RT in an RT-to-RT transfer and the transmitting RT has not responded with its Status Word within the programmed value of the RT-to-RT Response Timeout time after the Transmit Command Word.

RT Mode Code Interrupt (bit 3): This interrupt can only occur if Enhanced Mode Code Handling is enabled (bit 0 of Configuration Register #3 is set to logic “1”). If this bit is set, mode code interrupts for individual broadcast- T/R bit mode codes may be enabled by setting the appropriate bit(s) in address location 0108-010F in the shared RAM. Reception of an enabled mode code message will then cause a MODE CODE interrupt to occur at the end of the message.

RT Subaddress CONTROL WORD EOM (bit 2): For RT mode, this bit indicates that the Enhanced Mini-ACE is in the Enhanced Memory Management RT mode **and** the "Interrupt at EOM" bit is set in the Subaddress Control Word for the respective Tx/Rx/Bcst subaddress, with the interrupt occurring at the end of the message.

END OF MESSAGE (EOM) (bit 1): This bit indicates the completion of the message (regardless of validity).

NON-MESSAGE INTERRUPT EVENT BITS

TIME TAG ROLLOVER (bit 4): This bit indicates that the Time Tag Register

has rolled over from FFFF to 0000.

RT ADDRESS PARITY ERROR (bit 3): This bit indicates that the parity sum of the internal RTAD4-RTAD0 and RTADP signals is even, rather than odd, as required for the Enhanced Mini-ACE to respond to messages directed to its own RT address in RT mode.

BIT TEST COMPLETE (bit 2): This bit indicates that the protocol built-in self-test or the RAM built-in self-test has been completed. The result of the test may be determined by reading the BIT Test Status Register.

RAM PARITY ERROR (bit 1): This bit indicates a RAM parity error. This bit is only applicable for the 64K X 17 RAM versions of Enhanced Mini-ACE. It is **not** applicable for the 4K X 16 RAM versions. By programming RAM PARITY ENABLE, bit #14 of Configuration Register #2 to logic ”1,” the 64K X 17 RAM versions of the Enhanced Mini-ACE can be programmed to generate a parity bit on all write accesses to 17-bit RAM. A parity check is then performed on all read accesses to the 17-bit RAM. A RAM PARITY ERROR interrupt indicates a failure of this parity check.

For a RAM PARITY ERROR interrupt, the value of the parameter word on the interrupt status queue will indicate the shared RAM address where the parity error was detected.

6.20 Implementing Bulk Data Transfers

In systems involving bulk data transfers over the 1553 bus to/from the same subaddress, the host processor should set the OVERWRITE INVALID DATA bit (bit 11 of Configuration Register #2) and enable the RT 50% CIRCULAR BUFFER ROLLOVER and RT 100% CIRCULAR BUFFER ROLLOVER interrupt requests. By so doing, the routine transfer of multiple messages to the selected subaddress, including errors and retries, is transparent to the host processor. For a particular subaddress, the Enhanced Mini-ACE will issue an interrupt request only after the circular buffer pointer has crossed an address boundary of modulo the programmed circular buffer size for a 100% rollover interrupt, or modulo half of the programmed circular buffer size for a 50% circular buffer rollover interrupt.

6.21 RT Command Illegalization

The Enhanced Mini-ACE provides an internal mechanism for RT Command Word illegalization. The scheme utilizes a 256-word area in the Enhanced Mini-ACE shared RAM space. A benefit of this feature is reduced P.C. board space requirements, by eliminating the need for an external PROM, PLD, or RAM device to perform the illegalization function. The Enhanced Mini-ACE illegalization scheme provides the maximum in flexibility, allowing any subset of the 4096 possible combinations of broadcast/own address, T/R* bit, subaddress, and word count/mode code to be illegalized. Another advantage of the RAM-based illegalization technique is that it provides self-testability.

The power turn-on default condition is for RT command illegalization to be enabled. Command illegalization may be disabled by first setting bit 15 of Configuration Register #3, ENHANCED MODE, to logic "1" and then setting bit 7 of Configuration Register #3, ILLEGALIZATION DISABLED to logic “1” while rewriting bit 15, ENHANCED MODE ENABLED, to logic "1.”

If command illegalization is used, address locations 0300 through 03FF are dedicated for the message illegalizing function and must not be used for stack or data block storage. If RT command illegalization is disabled, the Enhanced Mini-ACE assumes that all valid, defined, received command words are legal. If the illegalization option is disabled, address locations 0300 through 03FF may be used for the storage of the descriptor stack or data blocks.

The Enhanced Mini-ACE shared RAM allocates 256 words, address locations 0300 to 03FF (hex), for RT command illegalization. Broadcast commands are illegalized separately from non-broadcast commands.

Commands may be illegalized down to the word count level. For example, a one-word receive command to subaddress 1 may be legal, while a two-word receive command to subaddress 1 may be illegalized.

6.22 Effects of Illegalization

If the Enhanced Mini-ACE RT protocol logic determines that a non-broadcast message has been illegalized, the Enhanced Mini-ACE will respond with the Message Error bit set in the RT Status Word. If a transmit command has been illegalized, the Enhanced Mini-ACE will respond with its Status Word with the Message Error bit set; no data words will be transmitted.

If a receive command has been illegalized and the Enhanced Mini-ACE is in non-ENHANCED mode or bit 4 of Configuration Register #3, ILLEGAL RECEIVE TRANSFER DISABLE is programmed to logic "0," data words received in a BC-to-RT (or RT-to-RT) transfer will be stored to the shared RAM. However, if the Enhanced Mini-ACE is in ENHANCED MODE and ILLEGAL RECEIVE TRANSFER DISABLE is programmed TO logic "1," received data words will not be stored to RAM.

In the case of an illegalized broadcast command, the Enhanced Mini-ACE will not respond, but will set the Message Error and Broadcast Command Received bits in its internal RT Status Register. If the next message is a Transmit status or Transmit last command mode code, the Enhanced Mini-ACE RT will then respond with the Message Error bit set to logic "1." For a broadcast receive command, the storage or non-storage of data words is controlled by the ILLEGAL RECEIVE TRANSFER DISABLE bit, as described above.

If the Enhanced Mini-ACE RT is programmed for the ENHANCED MODE, ILLEGAL COMMAND WORD bit 6 of the RT Block Status Word, will be set to logic "1" when the Block Status Word is written to the message block descriptor in the Command Stack during both the Start-of-Message (SOM) and End-of-Message (EOM) transfer sequences.

6.23 Illegalization RAM Memory Map

Table 118. Illegalization RAM Address Definition	
Bit	**Description**
15(MSB)	LOGIC “0”
14	LOGIC “0”
13	LOGIC “0”
12	LOGIC “0”
11	LOGIC “0”
10	LOGIC “0”
9	LOGIC “1”
8	LOGIC “1”
7	BROADCAST*/OWN RTADDRESS
6	T/R*
5	SA4
4	SA3
3	SA2
2	SA1
1	SA0
0(LSB)	WC4/MC4

Notes:

1. Address bit 7, BRDCST*/OWN RT ADDR, is logic "0" for broadcast commands, logic "1" for non-broadcast commands.
2. Address bit 6, T/R*, is high for transmit commands, low for receive commands.
3. Bits 5 through 1, SA4 through SA0, define the command subaddress. SA4-SA0 are 00000 or 11111 for mode code commands. SA4-SA0 assume a value between 00001 and 11110 for non-mode code messages.
4. Address bit 0, WC4/MC4, specifies the MSB of the command's Word Count/Mode Code field: Word Count for 00001. SA4-SA0. 11110, Mode Code for SA4-SA0 = 00000 or SA4-SA0 = 11111. If WC4/MC4 is logic "0," the referenced word in the illegalization RAM is used to program command illegalization for Word Counts/Mode Codes 15 through 0. If WC4/MC4 is Logic “1,” the referenced word in the command illegalization RAM is used to program illegalization for Word Counts/Mode Codes 31 through 16.

WC=00000 for a 32 word message as in the WC field of a command word.

The organization of the illegalization table is illustrated in Table 118. As shown, the base address of the illegalization table is 0300 (hex). The index into the illegalizing RAM is formulated by means of BROADCAST/OWN RT ADDRESS*, T/R* bit, Subaddress (4-0), and the MSB of the Word Count/Mode Code field (WC4/MC4), as defined by Table 120.

Commands may be illegalized down to the word count level. For example, a 1-word receive command to subaddress 1 can be legal, while a 2-word receive command may be illegalized.

The first 64 words of the ILLEGALIZATION table are used to illegalize Broadcast Receive Commands (two words per subaddress). The next 64 words refer to Broadcast Transmit Commands. Since non-mode code broadcast transmit commands are not defined by MIL-STD-1553B, the section of the illegalization table between (and including) address locations 0342(H) and 037D(H) do not need to be programmed by the user. The next 64 words correspond to non-broadcast receive commands. The final 64 words refer to non-broadcast transmit commands.

For each index into the illegalization RAM table (broadcast/own RT address-T/R*-subaddress), a pair of words (32 bits) are allocated for the purpose of illegalizing any combination of the 32 possible word counts or mode codes.

The programming of the individual words in the illegalization table is defined by Table 120.

Table 119. Illegalization RAM Map

Address (hex)	Description
300	Bcst/Rx, SA 0, MC15-0
301	Bcst/Rx, SA 0, MC31-16
302	Bcst/Rx, SA 1, WC15-0
303	Bcst/Rx, SA 1, WC31-16
• • •	• • •
033F	Bcst/Rx, SA 31, MC31-16
340	Bcst/Tx, SA 0, MC15-0
341	Bcst/Tx, SA 0, MC31-16
342	Bcst/Tx, SA 1, WC 15-0
• •	• •
{ **Note**: Non-Mode Code Broadcast/Transmit Commands (SA1-30) are not defined by MIL-STD-1553B. Therefore, addresses 0342-037D do not need to be programmed.}	
• •	• •
037D	Bcst/Tx, SA 30, WC 31-16
37	Bcst/Tx, SA 31, MC 15-0
037F	Bcst/Tx, SA 31, MC 31-16
380	Own RT Addr/Rx, SA 0, MC 15-0
381	Own RT Addr/Rx, SA 0, MC 31-16
382	Own RT Addr/Rx, SA 1, WC 15-0

Table 119. Illegalization RAM Map	
Address (hex)	**Description**
383	Own RT Addr/Rx, SA 1, WC 31-15
• • •	• • •
03BE	Own RT Addr/RX, SA 31, MC 15-0
03BF	Own RT Addr/Rx, SA 31, MC 31-16
03C0	Own RT Addr/Tx, SA 0, MC 15-0
03C1	Own RT Addr/Tx, SA 0, MC 31-16
03C2	Own RT Addr/Tx, SA 1, WC 15-0
03C3	Own RT Addr/Tx, SA 1, WC 31-16
• •	• •
03FC	Own RT Addr/Tx, SA 30, WC 15-0
03FD	Own RT Addr/Tx, SA 30, WC 31-16
03FE	Own RT Addr/Tx, SA 31, MC 15-0
03FF	Own RT Addr/TX, SA 31. MC 31-16

6.23.1 Subaddress Illegalization

Table 120. Illegalization RAM Word By Bit Definition		
Bit	Description	
	Even-numbered addresses (WC/MC4=0)	Odd-numbered addresses (WC/MC4=1)
15(MSB)	WC/MC = 15 Illegal	WC/MC = 31 Illegal
14	WC/MC = 14 Illegal	WC/MC = 30 Illegal
13	WC/MC = 13 Illegal	WC/MC = 28 Illegal
12	WC/MC = 12 Illegal	WC/MC = 28 Illegal
11	WC/MC = 11 Illegal	WC/MC = 27 Illegal
10	WC/MC = 10 Illegal	WC/MC = 26 Illegal
9	WC/MC = 9 Illegal	WC/MC = 25 Illegal
8	WC/MC = 8 Illegal	WC/MC = 24 Illegal
7	WC/MC = 7 Illegal	WC/MC = 23 Illegal
6	WC/MC = 6 Illegal	WC/MC = 22 Illegal
5	WC/MC = 5 Illegal	WC/MC = 21 Illegal
4	WC/MC = 4 Illegal	WC/MC = 20 Illegal
3	WC/MC = 3 Illegal	WC/MC = 19 Illegal
2	WC/MC = 2 Illegal	WC/MC = 18 Illegal
1	WC/MC = 1 Illegal	WC/MC = 17 Illegal
0(LSB)	WC= 32 Illegal,MC = 0 Illegal	WC/MC = 16 Illegal

Notes:

1. To **illegalize** a particular word count for a given broadcast/own RT address-T/R*-subaddress, the appropriate bit position in the respective illegalization word should be programmed to logic **"1."** A bit value of logic "0" designates the respective Command Word as a legal command.

2. For subaddresses 00001 through 11110, the "WC/MC" field specifies the Word Count field of the respective Command Word. For subaddresses 00000 and 11111, the "WC/MC" field specifies the Mode Code field of the respective Command Word.

3. Since non-mode code broadcast transmit messages are not defined by MIL-STD-1553B, the sixty (60) words in the illegalization RAM, addresses 0342(H) through 037D (H), corresponding to these commands do **not** need to be initialized. The Enhanced Mini-ACE will not respond to a non-mode code broadcast transmit command, but will automatically set the Message Error bit in its internal Status Word Register, regardless of whether or not corresponding bit in the illegalization RAM has been set. If the next message is a Transmit Status or Transmit Last Command mode code, the Enhanced Mini-ACE will respond with its Message Error bit set.

6.24 Accessing the Illegalization Table

In order to use the illegalizing feature, the host processor should write to the 256-word illegalizing RAM table as part of the Enhanced Mini-ACE's initialization procedure following power turn-on. After the illegalization RAM has been initialized, the host processor may then read it back in order to verify. When the illegalization RAM initialization has been completed, the host processor should put the Enhanced Mini-ACE on-line in RT mode by writing to Configuration Register #1.

The Enhanced Mini-ACE's 1553 protocol logic will perform a single read access of the illegalization table during the RT Start-of-Message (SOM) sequence. As a result of this read access, the Enhanced Mini-ACE will determine if the particular Command Word has been illegalized by the host PROCESSOR. Since the illegalization RAM should not be used for stack or message data (assuming illegalization is enabled), the Enhanced Mini-ACE's 1553 logic will never write to this section of memory.

6.25 Enhanced Mode Code Handling

For all non-mode code messages, and for mode code messages with ENHANCED MODE CODE HANDLING disabled, the third word of the message descriptor in the Enhanced Mini-ACE includes a mechanism for storing data words associated with specific mode code commands in individual locations in the shared RAM. In addition, the Enhanced Mini-ACE has the ability to generate selective interrupts for specific mode commands based on a lookup table. These features are enabled in the Enhanced Mini-ACE RT Enhanced mode, by setting ENHANCED MODE followed by setting ENHANCED MODE CODE HANDLING bit (bit 0 in Configuration Register #3) to logic "1."

ENHANCED MODE CODE HANDLING enables three aspects of handling mode code messages:

1. For all non-mode code messages, and for mode code messages with ENHANCED MODE CODE HANDLING disabled, the third word of the message descriptor in the stack is reserved for the DATA BLOCK POINTER. Reference FIGURES 17, 18, 19 and 20. The DATA BLOCK POINTER references the starting location of the Data Word block for received or transmitted data. In the case of mode code messages, the Data Word block consists of a single Data Word.

2. For mode code commands with data, if ENHANCED MODE CODE HANDLING is enabled, the third word of the message descriptor in the RT stack will contain the actual Data Word transmitted or received, rather than a pointer to the (single word) data block. For the PCI enhanced mini-ACE, for mode commands with data and ENHANCED MODE CODE HANDLING enabled, the third word of the message descriptor in the RT stack will contain 0000h. For mode commands without data, the third word of the descriptor is not written.

3. ENHANCED MODE CODE HANDLING affects the address mapping of Data Words transmitted or received for mode code messages. With ENHANCED MODE CODE HANDLING enabled, for mode commands with data words associated with them (transmit and receive commands 10 to 1F hex), the

Enhanced Mini-ACE will read the data from or store the data to individual (for each mode code) fixed locations in the RAM. The address locations associated with receive mode commands are 110-11F hex. These locations are accessed based on Mode Code bits 3-0. Transmit mode code data will be read from locations 120-12F based on Mode Code bits 3-0. If the SEPARATE BROADCAST option is selected (bit 0 of Configuration Register #2 is set to logic "1"), broadcast mode code receive data words will be stored in locations 130-13F hex. If the SEPARATE BROADCAST option is not selected (bit 0 of Configuration Register #2 is set to logic "0"), broadcast mode receive data will be stored along with the non-broadcast receive data words in locations 110-11F hex. Table 121 illustrates the RAM locations for each of the mode commands with data.

Mode code selective interrupts are enabled in the Enhanced Mini-ACE RT Mode by setting the ENHANCED MODE CODE HANDLING bit (bit 0 of Configuration Register #3) to logic "1" **and** by setting the RT SELECTED MODE CODE INTERRUPT bit (bit 1 in the Interrupt Mask Register) to logic "1" and initializing the MODE COMMAND SELECTIVE INTERRUPT Table (locations 108-10F hex in the RAM). Entries in the MODE COMMAND SELECTIVE INTERRUPT Table are addressed by appending the 3-bit value formed by broadcast, T/R* bit, and MODE CODE bit 4 to the base address of 108 hex. The bit location within this 16-bit word that determines if the given mode command will generate an interrupt is specified by the 4-bit value formed by MODE CODE bits 3-0. If the appropriate bit has been programmed to logic "1," the Enhanced Mini-ACE will generate an interrupt at the end of the current message. Note that some of the possible Command Word combinations are invalid. As long as the Command Word meets the 1553 criteria for word validation, the interrupt will be generated at the end of the message, even if the particular command is illegal or invalid. Refer to Table 124 and Table 125.

Table 121. Enhanced Mode Code Data Locations	
RAM Location (h)	**Mode Code**
110	UNDEFINED
111	SYNCHRONIZE WITH DATA
112	UNDEFINED
113	UNDEFINED
114	SELECTED TRANSMITTER SHUTDOWN
115	OVERRIDE SELECTED TRANSMITTER SHUTDOWN
0116-011F	RESERVED (RECEIVE MODE CODES)
120	TRANSMIT VECTOR WORD
121	UNDEFINED
122	TRANSMIT LAST COMMAND
123	TRANSMIT BIT WORD
124	UNDEFINED
125	UNDEFINED
0126-012F	RESERVED (TRANSMIT MODE CODES)
130	UNDEFINED BROADCAST
131	BROADCAST SYNCHRONIZE WITH DATA
132	UNDEFINED BROADCAST
133	UNDEFINED BROADCAST
134	BROADCAST SELECTED TRANSMITTER SHUTDOWN
135	BROADCAST OVERRIDE SELECTED TRANSMITTER SHUTDOWN
0136-013F	RESERVED BROADCAST

Table 122. Mode Code Interrupt Lookup Table RAM Map	
Address (h)	**Description**
108	Receive Mode Commands 0-15 (Undefined)
109	Receive Mode Commands 16-31 (With Data)
010A	Transmit Mode Commands 0-15 (Without Data)
010B	Transmit Mode Commands 16-31 (With Data)
010C	Broadcast Receive Mode Commands 0-15 (Undefined)
010D	Broadcast Receive Mode Commands 16-31 (With Data)
10	Broadcast Transmit Mode Commands 0-15 (Without Data)
010F	Broadcast Transmit Mode Commands 16-31 (Undefined/Reserved)

Table 123. Sample Mode Command Interrupt Lookup	
BIT	**DESCRIPTION**
15(MSB)	RESERVED MODE CODE
14	RESERVED MODE CODE
13	RESERVED MODE CODE
12	RESERVED MODE CODE
11	RESERVED MODE CODE
10	RESERVED MODE CODE
9	RESERVED MODE CODE
8	RESET REMOTE TERMINAL
7	OVERRIDE INHIBIT TERMINAL FLAG
6	INHIBIT TERMINAL FLAG
5	OVERRIDE Tx SHUTDOWN
4	TRANSMITTER SHUTDOWN
3	INITIATE SELF TEST
2	TRANSMIT STATUS
1	SYNCHRONIZE
0(LSB)	DYNAMIC BUS CONTROL

6.26 Broadcast Option

In RT mode, the Enhanced Mini-ACE allows the use of broadcast messages as a software-programmable option. In the non-ENHANCED RT Mode, if the BROADCAST DISABLED bit (bit 7 in Configuration Register #5) is programmed to logic "0," the Enhanced Mini-ACE will recognize RT address 31 as the broadcast address. If BROADCAST DISABLED is programmed to logic "1," then RT address 31 will not be recognized as the broadcast address and may be used as a discrete terminal. Note that MIL-STD-1553B stipulates that RT address 31 shall **not** be assigned as a discrete terminal address.

If broadcast is enabled and the Enhanced Mini-ACE RT receives a broadcast Command Word (RT address 31), followed **contiguously** by a Transmit Command Word to the Enhanced Mini-ACE RT's own RT address, indicating an RT-to-RTs (broadcast) message, the broadcast Command Word will be superceded and the Enhanced Mini-ACE RT will respond to the transmit command.

6.27 Busy Bit (See Table 124 for Tabular Mapping of Conditions Listed Below)

If the host processor asserts the BUSY* bit low in Configuration Register #1, the Enhanced Mini-ACE will respond to **any** command with the BUSY bit set in its RT Status Word. Similarly, if ALTERNATE RT STATUS WORD ENABLED (bit 5 of Configuration Register #3) is programmed to logic "1," then the BUSY Status Word Bit is directly controlled by means of bit 4 (S03) of Configuration Register #1. If the Enhanced Mini-ACE is programmed for the ENHANCED mode disabled **or** if BUSY RECEIVE TRANSFER DISABLE, bit 3 of Configuration Register #3 is logic "0," for a receive command, data words **will be** written to the data block in the shared RAM referenced by the respective Lookup Table location. If the Enhanced Mini-ACE is programmed for the ENHANCED mode **and** if BUSY RECEIVE TRANSFER DISABLE, bit 3 of Configuration Register #3 is logic "1," for a non-mode code receive command, received data words will **not** be written to the data block in the shared RAM referenced by the respective Lookup pointer.

For a non-mode code transmit command, the Enhanced Mini-ACE will respond with Status/BUSY, but **no** data words will be transmitted.

If the Alternate RT Status Word option is **not** selected, the Enhanced Mini-ACE may optionally set the busy bit based on the combination of broadcast/own RT address, T/R* bit, and subaddress values. ALTERNATE STATUS WORD ENABLE is non-selected if the Enhanced Mini-ACE is in ENHANCED mode disabled **or** if bit 5 of Configuration Register #3, ALTERNATE STATUS WORD ENABLE, is logic "0."

Assuming that ALTERNATE STATUS WORD is **not** enabled, the Enhanced Mini-ACE's "Busy by Broadcast-T/R*-Subaddress" option is available in the Enhanced Mode only. The Busy Bit Lookup Table is enabled by setting bit 13 of Configuration Register #2, BUSY LOOKUP TABLE ENABLE, to logic "1."

The Busy Bit Lookup Table occupies eight RAM locations, 0240 through 0247 (hex). As illustrated in Table 126, the offset into the lookup table is formulated for a specific command based on BROADCAST/OWN RT ADDRESS*, TRANSMIT/RECEIVE*, and the MSB of the Subaddress field (SA4).

For any given BROADCAST/OWN RT ADDRESS*, and TRANSMIT/RECEIVE* combination, a pair of words (32 bits) are allocated in the Busy Bit Lookup Table for the purpose of setting the busy bit in response to a command to any of the 32 possible subaddresses. The MSB (SA4) of the subaddress is used to select which word is to be used, and Subaddress bits 3 through 0 (SA3-SA0) are used to determine which of the 16 bits in the selected word is to be used to program a particular subaddress as busy. A logic "0" in the respective bit location indicates that the busy bit will not be set for that command, while a logic "1" indicates that the busy bit will be set in the next response to the next message to the selected subaddress.

If the Enhanced Mini-ACE is busy for a Transmit vector word mode command, a data word (vector word) will not be transmitted in the non-ENHANCED mode **or** if MODE COMMAND OVERRIDE BUSY, bit #13 of Configuration Register #3, is logic"0." Similarly, if the Enhanced Mini-ACE is busy for a Synchronize with data mode

command, the data word **will** be stored to shared RAM in the non-ENHANCED mode **or** if BUSY RX TRANSFER DISABLE, bit 3 of Configuration Register #3 is logic “0.”

If the Enhanced Mini-ACE is programmed for ENHANCED MODE **and** MODE COMMAND OVERRIDE BUSY is programmed to logic "1," then a Data Word **will** be transmitted for a Transmit Vector Word mode code. In addition, a data word **will** be stored for a Synchronize with data mode code, even if the Enhanced Mini-ACE is Busy **and** BUSY RECEIVE TRANSFER DISABLE is programmed to logic "1.”

If the Enhanced Mini-ACE is Busy and receives a Transmit BIT word mode command, the data word (BIT word) **will be transmitted** if the Enhanced Mini-ACE is programmed for its non-ENHANCED MODE **or** if INHIBIT BIT WORD IF BUSY, bit 14 of Configuration Register #4, is logic "0.” The Data Word (BIT Word) **will NOT be transmitted** if the Enhanced Mini-ACE is programmed for its ENHANCED MODE **and** if INHIBIT BIT WORD IF BUSY, bit 14 of Configuration Register #4, is logic "1.” The operation of the RT Busy bit is summarized in Table 124.

Table 124. Operation of RT Busy Bit											
Configuration Register (and RAM) Bits									Result		
ENHANCED MODE ENABLE (bit 15 CR #3)	ALTERNATE RT STATUS WORD ENABLE (bit 5 CR#3)	BUSY* (bit 10 of C.R. #1)	S03 (bit 4 of C.R. #1)	BUSY LOOKUP TABLE ENABLE (bit 13 of CR #2)	Respective bit in BUSY lookup table (shared RAM locations 0240-0247)	BUSY RECEIVE TRANSFER DISABLE (bit 3 of CR #3)	MODE COMMAND OVERRIDE BUSY (bit 13 of CR #3)	INHIBIT BIT WORD IF BUSY (bit 14 of CR #4)	RT status word Busy bit	Store data word(s) to RAM (for receive command)	Transmit data word(s) (for transmit command)
0	X	1	X	X	X	X	X	X	0	YES	No, except **will** transmit data word for Transmit BIT word mode command.
0	X	0	X	X	X	X	X	X	1	YES	No, except **will** transmit data word for Transmit BIT word mode command.
1	0	1	X	0	X	0	0	0	0	YES	No, except **will** transmit data word for Transmit BIT word mode command.
1	0	0	X	0	X	0	0	0	1	YES	No, except **will** transmit data word for Transmit BIT word mode command.
1	1	X	0	X	X	0	0	0	0	YES	No, except **will** transmit data word for Transmit BIT word mode command.
1	1	X	1	X	X	0	0	0	1	YES	No, except **will** transmit data word for Transmit BIT word mode command.

Table 124. Operation of RT Busy Bit											
Configuration Register (and RAM) Bits									Result		
ENHANCED MODE ENABLE (bit 15 CR #3)	ALTERNATE RT STATUS WORD ENABLE (bit 5 CR#3)	BUSY* (bit 10 of C.R. #1)	S03 (bit 4 of C.R. #1)	BUSY LOOKUP TABLE ENABLE (bit 13 of CR #2)	Respective bit in BUSY lookup table (shared RAM locations 0240-0247)	BUSY RECEIVE TRANSFER DISABLE (bit 3 of CR #3)	MODE COMMAND OVERRIDE BUSY (bit 13 of CR #3)	INHIBIT BIT WORD IF BUSY (bit 14 of CR #4)	RT status word Busy bit	Store data word(s) to RAM (for receive command)	Transmit data word(s) (for transmit command)
1	0	1	X	1	0	0	0	0	0	YES	No, except **will** transmit data word for Transmit BIT word mode command.
1	0	1	X	1	1	0	0	0	1	YES	No, except **will** transmit data word for Transmit BIT word mode command.

Table 125. Configuration Register (and RAM) Bits											
Configuration Register (and RAM) Bits									Result		
ENHANCED MODE ENABLE (bit 15 CR #3)	ALTERNATE RT STATUS WORD ENABLE (bit 5 CR#3)	BUSY* (bit 10 of C.R. #1)	S03 (bit 4 of C.R. #1)	BUSY LOOKUP TABLE ENABLE (bit 13 of CR #2)	Respective bit in BUSY lookup table (shared RAM locations 0240-0247)	BUSY RECEIVE TRANSFER DISABLE (bit 3 of CR #3)	MODE COMMAND OVERRIDE BUSY (bit 13 of CR #3)	INHIBIT BIT WORD IF BUSY (bit 14 of CR #4)	RT status word Busy bit	Store data word(s) to RAM (for receive command)	Transmit data word(s) (for transmit command)
1	BUSY (NOTE 3)					1	0	0	1	NO	No, except **will** transmit data word for Transmit BIT word mode command.
1	BUSY (NOTE 3)					0	1	0	1	YES	No, except **will** transmit data word for Transmit BIT word and Transmit vector word mode commands.
1	BUSY (NOTE 3)					1	1	0	1	NO, except **will** store data for Synchronize with data mode code.	No, except **will** transmit data word for Transmit BIT word and Transmit vector word mode commands.
1	BUSY (NOTE 3)					0	0	1	1	YES	NO
1	BUSY (NOTE 3)					1	0	1	1	**NO**	NO
1	BUSY (NOTE 3)					0	1	1	1	YES	No, except **will** transmit data word for Transmit vector word mode command.

Table 125. Configuration Register (and RAM) Bits											
Configuration Register (and RAM) Bits									Result		
ENHANCED MODE ENABLE (bit 15 CR #3)	ALTERNATE RT STATUS WORD ENABLE (bit 5 CR#3)	BUSY* (bit 10 of C.R. #1)	S03 (bit 4 of C.R. #1)	BUSY LOOKUP TABLE ENABLE (bit 13 of CR #2)	Respective bit in BUSY lookup table (shared RAM locations 0240-0247)	BUSY RECEIVE TRANSFER DISABLE (bit 3 of CR #3)	MODE COMMAND OVERRIDE BUSY (bit 13 of CR #3)	INHIBIT BIT WORD IF BUSY (bit 14 of CR #4)	RT status word Busy bit	Store data word(s) to RAM (for receive command)	Transmit data word(s) (for transmit command)
1	BUSY (NOTE 3)					1	1	1	1	NO, except **will** store data for Synchronize with data mode code.	No, except **will** transmit data word for Transmit vector word mode commands.

NOTES:

1. "CR" = Configuration Register.
2. "X" = don't care.
3. For these table entries, "BUSY" = {ENHANCED MODE ENABLE = "1"} AND {(ALTERNATE STATUS ENABLE = "0") AND BUSY* = "0")] OR [(ALTERNATE STATUS ENABLE = "1") AND (S03* = "1")] OR [(ALTERNATE STATUS ENABLE = "0") AND (BUSY LOOKUP TABLE ENABLE = 1) AND (RESPECTIVE BIT IN BUSY TABLE = "1")]}

Table 126. Busy Bit Lookup Table Address Definition	
BIT	**DESCRIPTION**
15(MSB)	LOGIC “0”
14	LOGIC “0”
13	LOGIC “0”
12	LOGIC “0”
11	LOGIC “0”
10	LOGIC “0”
9	LOGIC “1”
8	LOGIC “0”
7	LOGIC “0”
6	LOGIC “1”
5	LOGIC “0”
4	LOGIC “0”
3	LOGIC “0”
2	BCST/OWN RT ADDRESS*
1	T/R*
0(LSB)	SA4

Notes:

1. Address bit 2, BCST/OWN RT ADDR*, is logic "1" for broadcast commands, logic "0" for non broadcast commands.

2. Address bit 1, T/R*, is high for transmit commands, low for receive commands.

3. Address bit 0, SA4 specifies the MSB of the command's subaddress field.

6.28 Subaddress Busy Word

Table 127. Busy Bit Lookup Table for Definition		
Bit	**Description**	
	(For SA4 = 0)	**(For SA4 = 1)**
15(MSB)	Subaddress 15 BUSY	Subaddress 31 BUSY
14	Subaddress 14 BUSY	Subaddress 30 BUSY
13	Subaddress 13 BUSY	Subaddress 29 BUSY
12	Subaddress 12 BUSY	Subaddress 28 BUSY
11	Subaddress 11 BUSY	Subaddress 27 BUSY
10	Subaddress 10 BUSY	Subaddress 26 BUSY
9	Subaddress 9 BUSY	Subaddress 25 BUSY
8	Subaddress 8 BUSY	Subaddress 24 BUSY
7	Subaddress 7 BUSY	Subaddress 23 BUSY
6	Subaddress 6 BUSY	Subaddress 22 BUSY
5	Subaddress 5 BUSY	Subaddress 21 BUSY
4	Subaddress 4 BUSY	Subaddress 20 BUSY
3	Subaddress 3 BUSY	Subaddress 19 BUSY
2	Subaddress 2 BUSY	Subaddress 18 BUSY
1	Subaddress 1 BUSY	Subaddress 17 BUSY
0(LSB)	Subaddress 0 BUSY	Subaddress 16 BUSY

6.29 RT Address Inputs

The Enhanced Mini-ACE offers several different options for designating the Remote Terminal address. These include the following: (1) hardwired, by means of the 5 RT ADDRESS inputs and the RT ADDRESS PARITY input; (2) by means of the RT ADDRESS (and PARITY) inputs, but latched via hardware, on the rising edge of the RT_AD_LAT input signal; (3) input by means of the RT ADDRESS (and PARITY) inputs, but latched via host software; and (4) fully software programmable, by means of an internal register. In all four configurations, the RT address is readable by the host processor.

In order for the Enhanced Mini-ACE to respond as an RT to a discrete (non-broadcast) RT address, the address of a received Command Word must match the value programmed for pins RTAD4-RTAD0, and RTADP must be programmed to create an odd parity sum with RTAD4-0. Unless broadcast is disabled (i.e., by programming BROADCAST DISABLED, bit 7 of Configuration Register #5, to logic "1"), the Enhanced Mini-ACE's capability to receive messages to the broadcast address, RT address 31 (11111), is **not** affected by the programming of RTAD4-0 and RTADP. In the Enhanced Mini-ACE's RT mode, the programmed value of the RT address is sampled approximately 2 µs after the mid-parity zero crossing of a received command word.

Odd parity requires that there be an **odd** number of logic "1"s in RTAD4 through RTAD0 and RTADP. Therefore, the RT address parity bit (RTADP) must be programmed to logic "0" for RT addresses 1, 2, 4, 7, 8, 11, 13, 14, 16, 19, 21, 22, 25, 26, 28, and 31 (if broadcast is disabled). RTADP must be programmed to logic "1" for RT addresses 0, 3, 5, 6, 9, 10, 12, 15, 17, 18, 20, 23, 24, 27, 29, and 30. There are internal active current source pull-ups between the RT address inputs, RTAD4-RTAD0 and RTADP, and V_{CC}. The value of the pull-up current for these inputs is in the range of 50 to 350 uA. If there is a minimal P.C. board trace length (e.g., 1 or 2 inches) from the input pins for these signals to on-board jumper points, the internal pull-up resistors may be used to establish a logic "1" signal level, without external pull-ups.

Note: if the connection involves a longer signal trace, particularly to an external connector, it is strongly recommended that a direct connection to +5 volts be made to provide a logic "1" input signal.

If this is not possible, it is recommended that low level value pull-up resistors (less than 10K ohms) be used to increase the noise immunity for providing a logic "1" input.

Note: However, to configure the RT address inputs (or any other logic inputs) for logic “0,” the signals should be connected **directly** to logic ground. Pull-down resistors should **not** be used for the RT address inputs (or any other logic inputs).

There are four methods for designating the Enhanced Mini-ACE's RT address:

1. If the input signal RT_AD_LAT is connected to logic "0," the RT address is specified **directly** by the values presented on RTAD4-RTAD0 and RTADP.

2. The RT address may be latched on the rising edge of RT_AD_LAT. RTAD4-RTAD0 and RTADP must meet a minimum 10 ns setup time and 0 ns hold time relative to the rising edge of RT_AD_LAT. By this method, which may be used in MIL-STD-1760 applications, the Enhanced Mini-ACE's (internal) RT address will **not** change (for example due to a broken wire) after it has been latched by the rising edge of RT_AD_LAT.

3. The RT address may be latched from RTAD4-RTAD0 and RTADP under software control. This operation is performed as follows:

   a. Connect RT_AD_LAT to logic "1."

   b. Program ENHANCED MODE (bit 15 of Configuration Register #3) to logic "1."

   c. Program RT ADDRESS SOURCE (bit 5 of Configuration Register #6) to logic **"0."**

   d. Program LATCH RT ADDRESS WITH CONFIGURATION REGISTER # 5 (bit 3 of Configuration Register #4) to logic **"1."**

   e. Perform a write operation to Configuration Register #5. This will cause the Enhanced Mini-ACE's RT address to be latched from the values presented on RTAD4-RTAD0 and RTADP. Note that for this operation, the logic values written by the host (on D5-D0) **do not** effect the value of the Enhanced Mini-ACE's internal RT address.

   f. To prevent the RT address from being inadvertently overwritten by a subsequent write to Configuration Register #5, it is recommended to then program LATCH RT ADDRESS WITH CONFIGURATION REGISTER # 5 (bit 3 of Configuration Register #4) to logic **"0."**

4. The fourth method allows for a fully software programmable RT address. This operation is performed as follows:

   a. Connect RT_AD_LAT to logic "1."

   b. Program ENHANCED MODE (bit 15 of Configuration Register #3) to logic "1."

   c. Program RT ADDRESS SOURCE (bit 5 of Configuration Register #6) to logic "1."

d. Program LATCH RT ADDRESS WITH CONFIGURATION REGISTER # 5 (bit 3 of Configuration Register #4) to logic “1.”

e. Perform a write operation to Configuration Register #5. The value of the Enhanced Mini-ACE’s internal RT address bits 4-0 will be latched from processor data bus bits 5-1 (D5-D1), and internal RTADP to be latched from processor data bus bit 0 (D0).

f. To prevent the RT address from being inadvertently overwritten by a subsequent write to Configuration Register #5, it is suggested to then program LATCH RT ADDRESS WITH CONFIGURATION REGISTER # 5 (bit 3 of Configuration Register #4) to logic “0.”

Regardless of which method specifying RT address is used, the host may determine the value of the RT_AD_LAT input by means of the read-only bit RT ADDR LATCH/TRANSPARENT*, bit 6 of Configuration Register #5. In addition, the host may determine the value of the **internal** RTAD4-RTAD0 by means of bits 5-1 and RTADP by means of bit 0, of Configuration Register #5.

6.30 RT Status Word

The Enhanced Mini-ACE provides two options for the host processor to program the bits of the RT Status Word:

1. The standard or "non-alternate" Status Word: For MIL-STD-1553B applications, this option is normally used. In this configuration, the Enhanced Mini-ACE automatically updates the values of the Message Error, Broadcast Command Received, and Dynamic Bus Control bits in accordance with MIL-STD-1553B. The values of the Busy, Service Request, and Subsystem Flag bits are programmable by the host PROCESSOR. In addition, the values for the Instrumentation and Reserved bits are automatically set to logic "0" in the RT's Status Word response. There is also an option for the Terminal Flag bit to be automatically set for the response to the subsequent non-broadcast message following a failure of the Enhanced Mini-ACE RT's on-line self-test.

2. The "Alternate" status word mode: With this option, **all 11** RT Status Word bits are programmable by the host processor, by means of bits 11 through 1 of Configuration Register #1. This mode may be used to support MIL-STD-1553A, McAir, G.D. F16, or other "non-1553B" applications.

The default (power turn-on value) is for the standard (1553B) "non-Alternate" Status Word. The Enhanced Mini-ACE configures to this mode in the non-enhanced mode (bit 15 of Configuration Register #3 programmed to logic "0" **or** ALTERNATE STATUS WORD ENABLED, bit 5 of Configuration Register #3 programmed to logic "0").

To configure the Enhanced Mini-ACE RT for the Alternate RT Status Word mode, the Enhanced Mini-ACE must be programmed for by programming bits 15, ENHANCED MODE ENABLED, **and** bit 5, ALTERNATE STATUS WORD ENABLED, of Configuration Register #3, to logic "1."

Both options support command illegalization.

In either of the two modes, the values programmed in Configuration Register #1 are sampled approximately 4 to 5 µs after the mid-parity bit crossing of the received Command Word.

In either of the two modes, the value of the RT Status Word that was transmitted in response to the **last** non-broadcast message processed by the Enhanced Mini-ACE RT may be read from the read-only RT Status Word Register (register address 01110).

The programming of the Enhanced Mini-ACE RT Status Word bits is summarized in Table 128.

Table 128. RT Status Word Programming Options			
Bit Number (per MIL-STD-1553B)	**Bit Function (per MIL-STD-1553B)**	**Operation in Standard ("non-Alternate") Status Mode**	**Operation in Alternate Status Mode (See Notes 7 and 8)**
1-3	Sync Field	Sync Field	Sync Field
4-8	RT address	RT address	RT address
9	Message Error	Set to logic "1" following an error in the Data Word portion of a received message, or for an illegalized Command Word, in accordance with MIL-STD-1553B. See Note 1.	Controlled by S10, bit 11 of Configuration Register #1. Also, set to logic "1" for illegalized Command Word, in accordance with MIL-STD-1553B. See Notes 9 and 10.
10	Instrumentation	Logic "0"	Controlled by S9, bit 10 of Configuration Register #1.
11	Service Request	Controlled by means of SERVICE REQUEST*, bit 9 of Configuration Register #1. As an option, may be automatically cleared by a Transmit Vector mode command. See Note 1.	Controlled by S8, bit 9 of Configuration Register #1.
12	Reserved	Logic "0"	Controlled by S7, bit 8 of Configuration Register #1.
13	Reserved	Logic "0"	Controlled by S6, bit 7 of Configuration Register #1.
14	Reserved	Logic "0"	Controlled by S5, bit 6 of Configuration Register #1.
15	Broadcast Command Received	Operates in compliance with MIL-STD-1553B. See Note 2.	Controlled by S4, bit 5 of Configuration Register #1.
16	Busy	Controlled by means of BUSY*, bit 10 of Configuration Register #1 and Busy Lookup Table. See Note 4.	Controlled by S3, bit 4 of Configuration Register #1. Can have an effect on received data words. See Notes 11, 12, and 13.
17	Subsystem Flag	Controlled by means of SUBSYSTEM FLAG*, bit 8 of Configuration Register #1, and SSFLAG* input signal. See note 4.	Controlled by S2, bit 3 of Configuration Register #1.
18	Dynamic Bus Control Accepted	Controlled in accordance with MIL-STD-1553B by means of DYNAMIC BUS CONTROL ACCEPTANCE*, bit 11 of Configuration Register #1. See Note 5.	Controlled by S1, bit 2 of Configuration Register #1.
19	Terminal Flag	In ENHANCED MODE (bit 15 of Configuration Register #3 set to logic "1"), controlled by RTFLAG*, bit 7 of Configuration Register #1. Optionally, may be automatically set as the result of a self-test failure. See Note 6.	Controlled by S0, bit 1 of Configuration Register #1. See Note 14.
20	Parity	Odd parity, per MIL-STD-1553B.	Odd parity, per MIL-STD-1553B.

Notes:

1. For an error in the Data Word portion of a received message (sync or Manchester encoding, bit count, word count, or parity error), the Enhanced Mini-ACE RT will not respond to the current message. However, the internal Message Error bit will be set to logic "1." This value will be reflected in the read-only RT Status Word Register. If the Enhanced Mini-ACE receives a Command Word that has been illegalized by means of the illegalization table (see section on RT COMMAND ILLEGALIZATION), the Enhanced Mini-ACE will respond with the Message Error bit set in its Status Word. An illegalized command will result in ILLEGAL COMMAND WORD, bit 6 of the RT Block Status Word, to be set to logic "1." For an illegalized transmit command, the Enhanced Mini-ACE will transmit the Status Word only with the Message Error bit set; it will not transmit any data words. For a valid illegalized receive command, the Enhanced Mini-ACE will store the received data words unless: the Enhanced Mini-ACE is in ENHANCED MODE and ILLEGAL RECEIVE TRANSFER DISABLE, bit 4 of Configuration Register #3, is programmed to logic "1." In the latter case, received data words will not be stored to the Enhanced Mini-ACE shared RAM.
In either case, if the next message is a Transmit Status or Transmit Last Command mode code, the Enhanced Mini-ACE RT will respond to the next command with the Message Error bit set to logic "1." To all other subsequent commands, the Enhanced Mini-ACE RT will respond with the Message Error bit set to logic "0." Note that programming SERVICE REQUEST* to logic "0" in Configuration Register #1 results in a value of logic "1" for the Service Request bit transmitted in the RT Status Word. Also, note that this bit is effected by the value programmed for CLEAR SERVICE REQUEST, bit 2 of Configuration Register #2. If CLEAR SERVICE REQUEST is logic "1," the value of SERVICE REQUEST* will automatically clear (to logic "1") after the Enhanced Mini-ACE RT has responded to a Transmit Vector Word mode code command. That is, if CLEAR SERVICE REQUEST is logic "1" and SERVICE REQUEST is logic "0," the Enhanced Mini-ACE RT will respond with the Service request bit set to logic "1" until the Enhanced Mini-ACE responds to a Transmit Vector Word command. For this message, the Enhanced Mini-ACE will respond with the Service Request bit still set to logic "1" in its Status Word. Following this message, the value of SERVICE REQUEST* clears to logic "1" and stays cleared until re-asserted to logic "0" by the host processor.
2. In accordance with MIL-STD-1553B, the value of the internal Broadcast Command Received bit will be set to logic "1" following reception of a valid Broadcast Command Word. This value will be reflected in the read-only RT Status Word Register. If the next message is a Transmit status or Transmit last command mode code, the Enhanced Mini-ACE RT will respond with the Broadcast command received bit set to logic "1." To all other commands, the Enhanced Mini-ACE will respond with the Broadcast command received bit set to logic "0."
3. Note that programming BUSY* to logic "0" in Configuration Register #1 results in a value of logic "1" for the Busy bit transmitted in the RT Status Word.

If BUSY* is programmed to logic "0" or the Enhanced Mini-ACE receives a Command Word (broadcast, T/R* bit, subaddress) that has been programmed for a BUSY response by means of the Busy lookup table (see BUSY BIT section), the Enhanced Mini-ACE will respond with the Busy bit set in its Status Word.

For the response to a transmit command when Busy, the Enhanced Mini-ACE will transmit the Status Word only with the Busy bit set; it will not transmit any data words. For a "Busy" receive command, the Enhanced Mini-ACE will store the received data words unless: the Enhanced Mini-ACE is in ENHANCED MODE and BUSY RECEIVE TRANSFER DISABLE, bit 3 of Configuration Register #3, is logic "1." In the latter case, received data words will not be stored in the Enhanced Mini-ACE shared RAM.

In either case, if the next message is a Transmit Status or Transmit last Command mode code, the Enhanced Mini-ACE RT will respond with the Busy bit set to logic "1." To all other commands, the Enhanced Mini-ACE will respond with the value of the Busy bit determined by the value of BUSY* in Configuration Register #1 and the programming of the Busy lookup table for that command (not the previous command).
4. Programming SUBSYSTEM FLAG* to logic "0" in Configuration Register #1 results in a value of logic "1" for the Subsystem Flag bit transmitted in the RT Status Word.

The Subsystem Flag Status Word bit will also be set to logic "1" if the value of logic "0" is sampled on the SSFLAG* input signal during the RT Start-of-Message (SOM) sequence, approximately 4 us after the mid-parity bit of the received Command Word. A possible use of the SSFLAG* input is to indicate failure of the host PROCESSOR, by connecting SSFLAG* to the output of a processor watchdog timer. Note that the value presented on SSFLAG* has no effect on the value of the SUBSYSTEM FLAG* bit written or read in Configuration Register #1. Also, note that the value presented on the SSFLAG* input has no effect in the Alternate RT Status mode.

5. In accordance with MIL-STD-1553B, the Dynamic Bus Control Acceptance Status Word bit will only be set to logic "1" if DYNAMIC BUS CONTROL ACCEPTANCE* (bit 11 of Configuration Register #1) is programmed for a value of logic "0" and the Enhanced Mini-ACE RT is responding to a Dynamic Bus Control mode command. For all other commands, the Dynamic Bus Control Acceptance Status Word bit will be logic "0." It should be noted that the Enhanced Mini-ACE will not automatically switch from RT to BC mode following reception (and acceptance) of a Dynamic Bus Control mode command.

6. In ENHANCED MODE, the value of the transmitted RT flag Status Word bit can be set to logic "1" by programming RTFLAG*, bit 7 of Configuration Register #1, to logic "0."

Alternatively, in ENHANCED MODE, the Enhanced Mini-ACE RT may be programmed to automatically transmit logic "1" for the RT Flag Status Word bit following a failure of the Enhanced Mini-ACE RT's on-line self-test. In this case, if the on-line self-test for a particular message fails, the Terminal Flag Status Word bit will be set to logic "1" in the response to the subsequent non-broadcast message. This is done by programming RTFAIL-RTFLAG AUTOWRAP ENABLE, bit 2 of Configuration Register #2, to logic "1." In RT mode, the self-test is performed for every non-broadcast message processed by the Enhanced Mini-ACE. The self-test is considered to have failed under either of two circumstances:

(a) **Loop Test Failure:** A loopback test is performed on the transmitted portion of every non-broadcast message. A validity check is performed on the received version of every word transmitted by the Enhanced Mini-ACE. In addition, a bit-by-bit comparison is performed on the **last** word transmitted by the RT for each message. If either the received version of any transmitted word is determined to be invalid (sync, encoding, bit count, or parity error) and/or the received version of the last word does not match the transmitted version, the loop test is considered to have failed.

(b) **Transmitter Timeout:** A transmitter timeout condition occurs when the Enhanced Mini-ACE's 660.5 us Transmitter Watchdog Timer times out and aborts transmission on the 1553 bus. This indicates a fault in the Manchester II encoder, RT state machine, or word count logic.

(c) **Built-In Protocol Self-Test Failure:** If RTFAIL-TO-TERMINAL FLAG WRAP ENABLE, bit 2 of Configuration Register #3, has been programmed to logic "1" and the protocol logic built-in self-test fails, the RT Terminal flag status bit will be set to logic "1."

As a result, the last loop test performed prior to protocol self-test becomes "lost." That is, if the loop test fails for the last message before the protocol self-test has been performed (e.g., for the response to an Initiate Self-test mode command) and the self-test passes, the Terminal flag bit will then be logic "0" for the first message following the self-test. Note that if the protocol self-test fails, then RT FAIL (and Terminal Flag) will remain set regardless of the subsequent loop test results, until the protocol test is re-run and passes, or the host writes logic "1" to CLEAR SELF-TEST REGISTER, bit 10 of the Start/Reset Register. If the protocol self-test passes however, a subsequent failure of the loop test will still result in the setting of the Terminal flag bit.

7. In the Alternate Status mode, Status Word bit positions 9 through 19 (per MIL-STD-1553B) are controlled directly by means of S10 through S0, bits 11 through 1 of Configuration Register #1. That is, the respective RT Status Word bits are set to logic "1" by programming the respective Configuration Register #1 bits to logic "1" (not logic "0").
8. The following functions are not applicable in the Alternate Status Word mode:
- Service Request Auto-Clear.
- Operation of the MIL-STD-1553B Broadcast Command Received bit.
- SSFLAG* input signal.
- Operation of the MIL-STD-1553B Dynamic Bus Control Acceptance bit.
- Effect of the RT on-line self-test on bit 19 ("Terminal Flag," per MIL-STD-1553B).

9. In the Alternate RT Status Word mode, for an error in the data word portion of a received message following a valid Command Word (sync or Manchester encoding, bit count, word count, or parity error), the Enhanced Mini-ACE RT will not respond to the current message. However, the internal Message Error bit will be set to logic "1." This value will be reflected in the read-only RT Status Word Register. It should be noted that the value of this bit has no effect on the Message Error bit in the Status Word response to the next message.

10. In the Alternate RT Status Word mode, if the Enhanced Mini-ACE receives a Command Word that has been illegalized by means of the illegalization table (see RT COMMAND ILLEGALIZATION section), the Enhanced Mini-ACE will respond with the Message Error bit set in its Status Word. An illegalized command will result in ILLEGAL COMMAND WORD, bit 6 of the RT Block Status Word, to be set to logic "1." For an illegalized transmit command, the Enhanced Mini-ACE will transmit the Status Word only with the Message Error bit set; it will not transmit any data words. For a valid illegalized receive command, the Enhanced Mini-ACE will store the received data words unless: the Enhanced Mini-ACE is in ENHANCED MODE and ILLEGAL RECEIVE TRANSFER DISABLE, bit 4 of Configuration Register #3, is logic "1." In the latter case, received data words will not be stored in the Enhanced Mini-ACE shared RAM.
11. In the Alternate RT Status Word mode, if S3, bit 4 of Configuration Register #1, is set to logic "1," the Enhanced Mini-ACE will respond to a transmit command with a Status Word (with bit 16, per MIL-STD-1553B, set to logic "1"), followed by the requested number of data words.
12. In the Alternate RT Status Word mode, if S3 is logic "1," and BUSY RECEIVE TRANSFER DISABLE, bit 3 of Configuration Register #3 is programmed to logic "0" and received data words will be stored to the Enhanced Mini-ACE shared RAM. If both S3 and BUSY RECEIVE TRANSFER DISABLE are programmed to logic "1," received data words will not be stored in the Enhanced Mini-ACE shared RAM.
13. In the Alternate Status Word mode, the Busy lookup table will affect the value of bit 16 ("Busy," per MIL-STD-1553B) for transmitted RT Status Words. However, the Busy lookup table has no effect on the transmission or storage of data words.
14. In the Alternate Status Word mode, an RTFAIL condition (wraparound test failure) will not affect the value of the RT Flag Status Word bit, regardless of the value of the RTFAIL-RTFLAG AUTOWRAP ENABLE bit, bit 2 of Configuration Register #2.

6.31 RT-to-RT Response Timeout

The Enhanced Mini-ACE's response timeout time is applicable to RT mode. When the Enhanced Mini-ACE RT is the receiving RT in an RT-to-RT transfer message, the timer is used to determine that the transmitting RT has not responded in time. The value of the RT-to-RT timeout timer corresponds to the time between the mid-parity bit zero crossing of the Transmit Command Word and the mid-sync zero crossing of the transmitting RT's Status Word. In the non-ENHANCED mode, the value of this timer defaults to a nominal value of 18 µs. In order to accommodate long buses, the value of this timeout is programmable by the host processor. In the ENHANCED MODE (bit 15 of Configuration Register #3 programmed to logic "1"), the value of the RT-to-RT timeout is programmable by means of Configuration Register #5, as illustrated in Table 129.

Table 129. RT-to-RT Response Timeout Select

Bit 10 of C.R. #5 Response Timeout Select 1	Bit 9 of C.R. #5 Response Timeout Select 0	Response Timeout Time Value (us)
0	0	18.5
0	1	22.5
1	0	50.5
1	1	130

6.32 RT Built-In-Test (Bit) Word

The Enhanced Mini-ACE RT offers two options for implementing the RT Built-In-Test (BIT) Word: an Internal BIT Word and an External BIT Word.

Using the Internal BIT Word option, the Enhanced Mini-ACE RT responds to a Transmit BIT Word mode command with the Status Word, followed by the contents of the Enhanced Mini-ACE RT's internal BIT Word Register. The format and bit descriptions for this word are defined in Table 130. With the External BIT Word option, the Enhanced Mini-ACE RT responds with a BIT Word that is stored in a location in the Enhanced Mini-ACE shared RAM. The value of this word is fully software programmable by the host PROCESSOR.

In the ENHANCED MODE, it should be noted that the host processor may read the value of the internal BIT Word by means of the read-only BIT Word Register, register address 0F (hex). This register may be read, regardless of whether the Enhanced Mini-ACE RT is programmed to respond with the Internal or External BIT Word.

In the NON-ENHANCED mode, **or** if EXTERNAL BIT WORD ENABLE, bit 15 of Configuration Register #4, is programmed to logic "0," the BIT Word transmitted is accessed from the Enhanced Mini-ACE's internal BIT Word register.

If the Enhanced Mini-ACE is programmed for ENHANCED MODE **and** if EXTERNAL BIT WORD ENABLE is programmed to logic "1," the BIT Word transmitted will be read from a memory location. In this case, if ENHANCED MODE CODE HANDLING is disabled (ENHANCED MODE disabled **or** ENHANCED MODE CODE HANDLING disabled (bit 0 of Configuration Register #3 is programmed to logic "0")), the location accessed for the external BIT Word will be the address referenced by the RT lookup table pointer for subaddress 00000 or subaddress 11111. In this case, it should be noted that for a given subaddress (00000 or 11111), the **same** data word will be transmitted in response to either a Transmit BIT word **or** a Transmit vector word mode command.

However, if ENHANCED MODE CODES are enabled (ENHANCED MODE **and** ENHANCED MODE HANDLING enabled (bit 0 of Configuration Register #3 is programmed to logic "1")), the external BIT Word will be accessed from address location 0123.

If the Enhanced Mini-ACE is Busy (either globally, or for transmit subaddress 00000 or 11111), for a Transmit BIT Word mode command, the data word (BIT Word) **will be transmitted** if the Enhanced Mini-ACE is programmed for its non-ENHANCED MODE **or** if INHIBIT BIT WORD IF BUSY, bit 14 of Configuration Register #4 is logic “0.” If the Enhanced Mini-ACE is Busy for a Transmit BIT Word mode command, the Data Word (Bit Word) **will NOT be transmitted** if the Enhanced Mini-ACE is programmed for its ENHANCED MODE **and** if INHIBIT BIT WORD IF BUSY, bit 14 of Configuration Register #4, is logic "1.”

The bit map and bit descriptions for the internal RT Built-in-Test (BIT) Word are indicated in Table 130.

Table 130. RT Bit Word (Read 0Fh)

Bit	Description
15(MSB)	TRANSMITTER TIMEOUT
14	LOOP TEST FAILURE B
13	LOOP TEST FAILURE A
12	HANDSHAKE FAILURE
11	TRANSMITTER SHUTDOWN B
10	TRANSMITTER SHUTDOWN A
9	TERMINAL FLAG INHIBITED
8	BIT TEST FAIL
7	HIGH WORD COUNT
6	LOW WORD COUNT
5	INCORRECT SYNC RECEIVED
4	PARITY/MANCHESTER ERROR RECEIVED
3	RT-RT GAP/SYNC/ADDRESS ERROR
2	RT-RT NO RESPONSE ERROR
1	RT-RT 2ND COMMAND WORD ERROR
0(LSB)	COMMAND WORD CONTENTS ERROR

NOTE: Bits 15 through 9 are cleared only following a MSTCLR* input, a software reset via the Start/Reset Register, or reception of a Reset Remote Terminal mode command. Bit 8 is updated as a result of the most recent protocol built-in self-test. Bits 7 through 0 are updated as a result of every message processed.

Transmitter Timeout (bit 15): Set if the Enhanced Mini-ACE's failsafe timer detected a fault condition. The transmitter timeout circuit will automatically shut down the CH. A or CH. B transmitter if it transmits for longer than 668 µs. In RT mode, the Enhanced Mini-ACE will terminate the processing of the current message as the result of a transmitter timeout, however, it **will respond** to the next message received.

Ch. B Loop Test Failure (bit 14), Ch. A Loop Test Failure (bit 13): A loopback test is performed on the transmitted portion of every non-broadcast message. A validity check is performed on the received version of every word transmitted by the Enhanced Mini-ACE. In addition, a bit-by-bit comparison is performed on the last word transmitted by the RT for each message. If either the received version of any transmitted word is determined to be invalid (sync, encoding, bit count, or parity error) and/or the received version of the last transmitted word does not match the transmitted version, or a failsafe timeout occurs on the respective channel, the LOOP TEST FAILURE bit for the respective bus channel will be set.

Handshake Failure (bit 12): A handshake can only occur in the Enhanced Mini-ACE's transparent configuration for the processor interface. A handshake failure **cannot occur** in the buffered mode. If this bit is set, it indicates that the subsystem has failed to respond with the DMA handshake input DTGRT* asserted within the allotted time, in response to the Enhanced Mini-ACE asserting DTREQ*. Alternatively, a handshake failure will occur if the host PROCESSOR fails to clear STRBD* (high) within the allotted time, after the Enhanced Mini-ACE has asserted its READYD* output (low). The allotted time is 4 µs for a 16 MHz clock, or 3.5 µs for a 12 MHz clock.

Ch. B Transmitter Shutdown, Ch. A Transmitter Shutdown (bits 11, 10): Indicates that the transmitter on the respective bus channel has been shut down by a Transmitter shutdown mode code command received on the alternate channel. If an Override transmitter shutdown mode code command is received on the alternate channel, this bit will revert back to logic "0."

Terminal Flag Inhibited (bit 9): Set to logic "1" if the Enhanced Mini-ACE's Terminal Flag RT Status bit has been disabled by an Inhibit terminal flag mode code command. Will revert to logic "0" if an Override inhibit terminal flag mode code command is received.

BIT Test Fail (bit 8): Represents the result of the Enhanced Mini-ACE RT's most recent built-in protocol self-test. A value of logic "0" for bit 8 indicates that the test passed. The bit will return a value of logic "1" if the Enhanced Mini-ACE has failed its most recent protocol self-test. If a subsequent performing of the protocol self-test passes, bit 8 will clear to "0." Also, note that the RAM self-test has no effect on bit 8.

High Word Count (bit 7): Set to logic "1" if the most recent message had a high word count error.

Low Word Count (bit 6): Set to logic "1" if the most recent message had a low word count error.

Incorrect Sync Type Received (bit 5): If set, indicates that the Enhanced Mini-ACE detected a Command sync in a received Data Word.

Invalid Word (bit 4): Indicates that the Enhanced Mini-ACE RT received a Data Word containing one or more of the following error types: sync field error, Manchester encoding error, parity error, and/or bit count error.

RT-to-RT Gap/Sync/Address Error (bit 3): This bit is set if the Enhanced Mini-ACE RT is the receiving RT for an RT-to-RT transfer and one or more of the following occur: (1) If the GAP CHECK ENABLED bit (bit 8) of Configuration Register #5 is set to logic "1" and the transmitting RT responds with a response time of less than 4 µs, per MIL-STD-1553B (mid-parity bit to mid-sync); i.e., less than 2 µs dead time; and/or (2) There is an incorrect sync type or format error (encoding, bit count, and/or parity error) in the transmitting RT Status Word; and/or (3) The RT address field of the transmitting RT Status Word does not match the RT address in the transmit Command Word.

RT-to-RT Response Timeout (bit 2): If set, indicates that, for the previous message, the Enhanced Mini-ACE was the receiving RT for an RT-to-RT transfer **and** that the transmitting RT either did not respond or responded later than the Enhanced Mini-ACE's RT-to-RT Timeout time. The Enhanced Mini-ACE's RT-to-RT Response Timeout Time is defined as the time from the mid-bit crossing of the parity bit of the transmit Command Word to the mid-sync crossing of the transmitting RT Status Word. The value of the RT-to-RT Response Timeout is nominally 18.5 µs in the non-Enhanced mode, or programmable from among nominal values of 18.5, 22.5, 50.5, or 130 µs in the enhanced mode.

RT-to-RT Second Command Error (bit 1): If the Enhanced Mini-ACE is the receiving RT for an RT-to-RT transfer, this bit set indicates one or more of the following error conditions in the transmit Command Word: (1) T/R bit = logic "0"; (2) subaddress = 00000 or 11111; (3) same RT address field as the receive Command Word.

Command Word Contents Error (bit 0): Indicates a received command word is not defined in accordance with MIL-STD-1553B. This includes the following undefined Command Words: (1) BROADCAST DISABLED, bit 7 of Configuration Register #5 is logic "0" **and** the Command Word is a non-mode code, broadcast, transmit command; (2) The OVERRIDE MODE T/R* ERROR bit, bit 6 of Configuration Register #3, is logic "0" **and** a message with a T/R* bit of "0," a subaddress/mode field of 00000 or 11111 and a mode code field between 00000 and 01111; (3) BROADCAST DISABLED, bit 7 of Configuration Register #5 is logic "0" **and** a mode code command that is not permitted to be broadcast (e.g., Transmit status) is sent to the broadcast address (11111).

6.33 RT Start-of-Message and End-of-Message Transfer Sequences

Approximately 1.25 µs following the mid-parity bit crossing of a received Command Word, the Enhanced Mini-ACE performs the RT Start-of-Message (SOM) sequence. Approximately 6 µs after the end of the last word transmitted by the RT (or received, for a broadcast message), the Enhanced Mini-ACE performs the RT End-of-Message (EOM) Sequence. The SOM and EOM sequences consist of sequences of words read from and written to the Enhanced Mini-ACE's shared RAM. The SOM and EOM sequences are summarized below:

6.34 RT Start-of-Message (SOM) Sequence

Steps 1 and 2 will only occur if there is a non-message interrupt condition just prior to beginning of the RT Start-of-Message sequence:

1. If a non-message interrupt condition occurs, the interrupt vector word will be written to the Interrupt Status Queue. Non-message interrupt conditions include time tag rollover, RT address parity error, RAM parity error, and BIT completed

2. If a non-message interrupt condition had occurred, the interrupt parameter word will be written to the general purpose queue. For a RAM Parity Error non-message interrupt, the parameter will be the RAM address where the parity check failed. For an RT address Parity Error, Protocol Self-test Complete, and Time Tag Rollover non-message interrupts, the parameter is not used; for these conditions, a value of 0000 will be written.

3. If command illegalization is used, the appropriate illegalization word is read from the Illegalization lookup table.

4. If the selective Busy option is used, the appropriate "Busy" word is read from the Busy lookup table.

Steps 5, 7 and 8 only occur for the case of a superceded message:

5. The Command Stack Pointer is written.

6. The Command Stack Pointer is read.

7. If a message-related interrupt occurred for the superceded message, the interrupt vector word is written to the Interrupt Status Queue.

8. If a message-related interrupt occurred for the superceded message, the interrupt parameter word is written to the Interrupt Status Queue.

9. If ENHANCED RT MEMORY MANAGEMENT is enabled (bit 1 of Configuration Register #2 programmed to logic "1"), allowing the use of

circular buffers and/or double buffering, the Subaddress Control Word is read from the Subaddress Control Word portion of the RT lookup table.

10. With the exception of a mode command with no Data Word or if the message is a mode code and ENHANCED MODE CODE HANDLING is enabled, the Data Block Address is read from the appropriate RT lookup table location.

11. The Command Word is written to the fourth location in the block descriptor.

12. With the exception of a mode command with no Data Word or if the message is a mode code and ENHANCED MODE CODE HANDLING is enabled, the Data Block Address is written to the third location in the block descriptor.

13. The Time Tag word is written to the second location in the block descriptor.

14. The Block Status Word is written to the first location in the block descriptor. The value of the block status word will be 4000 (i.e., SOM bit set, all other bits are cleared).

15. The value of the Stack Pointer read in step 6 is incremented by four and written to the active area Stack Pointer location.

Steps 16 and 17 are only performed if a command stack rollover occurs:

16. An interrupt vector word indicating a command stack rollover interrupt is written to the Interrupt Status Queue.

17. The interrupt parameter word, a pointer to the start of the descriptor (the Block Status Word) for the just completed message, is written to the Interrupt Status Queue.

6.35 RT End-of-Message (EOM) Sequence

1. If the current message is using circular buffering or double buffering, the Subaddress Control Word is read from the Subaddress Control Word section of the RT lookup table.

2. If the current message is using receive subaddress double buffering, the Data Block Address is read from the RT lookup table; or, if the message was a mode command with data and ENHANCED MODE CODE HANDLING is enabled, the Data Word transmitted or received for a mode code message with data is written to the third location in the block descriptor. If ENHANCED MODE CODE HANDLING is enabled, no word is stored to the third location in the RT descriptor for a mode code message without data.

3. If the current message is using circular buffering or double buffering and the pointer address needs to be updated, the updated value of the pointer is written to the RT lookup table.

4. The Time Tag word is written to the second location in the block descriptor.

5. The Block Status Word is written to the first location of the block descriptor.

6.36 Summary of RT Exception Conditions

In response to various message errors and other exception conditions, the Enhanced Mini-ACE remote terminal takes actions and provides a number of indications. Table 131 indicates the respective RT response and effect on the RT Status Word, Block Status Word bits that will be set, RT Built-in-Test (BIT) Word bits, and interrupt requests that are issued and Interrupt Status Register bits that become set as a result of these conditions.

It should be noted that the responses to error conditions for Mode code messages are delineated separately in Table 131.

Table 131. RT Exception. Conditions				
	RT Response, Effect on RT Status Word Register Bits	**RT Block Status Word Bits (assuming Enhanced Mode)**	**RT Built-in-Test (BIT) Word Bits**	**Interrupt Conditions, Interrupt Status Register Bits (if enabled)**
Invalid Command Word	No response (message ignored)	None (No SOM or EOM sequence)	No effect	None
RT address Parity Error	RT will not receive words or respond to messages sent to its own RT address. RT will receive words to the broadcast address (31), unless BROADCAST DISABLED, bit 7 of Configuration Register #5, is logic "1." For a broadcast message, the Broadcast Command Received bit is set to logic "1" in the internal Status Word Register.	No Block Status Word for a message to the RT's own address. Normal Block Status Word, including EOM bit, for a broadcast message (if enabled).	None	RT ADDRESS PARITY ERROR
Command Type Sync in Data Word Following Reception of Valid Command Word	No response. MESSAGE ERROR bit set in internal Status Word Register. If the message was broadcast, the Broadcast Command Received bit is also set to logic "1" in the internal Status Word Register.	EOM, ERROR FLAG, FORMAT ERROR, INCORRECT DATA SYNC, INVALID WORD	INCORRECT SYNC RECEIVED	END OF MESSAGE; FORMAT ERROR; RT SUBADDRESS CONTROL WORD or RT MODE CODE
Valid Command Word Followed by Reception of Invalid Data Word(s) (Manchester encoding, bit count, parity)	No response. MESSAGE ERROR bit set in internal Status Word Register. If the message was broadcast, the Broadcast Command Received bit is set to logic "1" in the internal Status Word Register.	EOM, ERROR FLAG, FORMAT ERROR, INVALID WORD	PARITY/ MANCHESTER ERROR RECEIVED	END OF MESSAGE; FORMAT ERROR; RT SUBADDRESS CONTROL WORD or RT MODE CODE (if selected)
Valid Command Word Followed by Incorrect Number of data words	No response. MESSAGE ERROR bit set in the internal Status Word Register. If the message was broadcast, the Broadcast Command Received bit is also set to logic "1" in the internal Status Word Register.	EOM, ERROR FLAG, FORMAT ERROR, WORD COUNT ERROR	HIGH WORD COUNT or LOW WORD COUNT	END OF MESSAGE; FORMAT ERROR; RT SUBADDRESS CONTROL WORD or RT MODE CODE (if selected)
Enhanced Mini-ACE is receiving RT in a correct RT-to-RT transfer sequence	Normal Status Word response. If the message was received to the broadcast address, the Broadcast Command Received bit is set to logic "1" in the internal Status Word Register.	EOM, RT-to-RT FORMAT	None	END OF MESSAGE; RT SUBADDRESS CONTROL WORD or RT MODE CODE (if selected) (CHECK IF SELECTED)
RT-to-RT Timeout: Enhanced Mini-ACE is Receiving RT in an RT-to-RT Transfer and the transmitting RT Does Not Respond in Time	No response. MESSAGE ERROR bit set in internal Status Word Register. If the message was broadcast, the Broadcast Command Received bit is also set to logic "1" in the internal Status Word Register.	EOM, ERROR FLAG, RT-to-RT FORMAT, NO RESPONSE TIMEOUT	RT-to-RT, NO RESPONSE ERROR	FORMAT ERROR; END OF MESSAGE; RT SUBADDRESS CONTROL WORD or RT MODE CODE (if selected) (AT SET)

Table 131. RT Exception. Conditions				
	RT Response, Effect on RT Status Word Register Bits	**RT Block Status Word Bits (assuming Enhanced Mode)**	**RT Built-in-Test (BIT) Word Bits**	**Interrupt Conditions, Interrupt Status Register Bits (if enabled)**
ENHANCED MODE CODE disabled or ENHANCED MODE CODE HANDLING disabled; Receive valid, defined mode code message (including RESERVED mode codes).	If the message is a Transmit Status or Transmit Last Command mode code, the RT Status Word resulting from the previous message is transmitted and the internal Status Word is not updated. Otherwise, may affect the following RT Status Word bits, as applicable: MESSAGE ERROR (if illegal), BUSY (per Configuration Register #1 and Busy lookup table), DYNAMIC BUS CONTROL ACCEPTANCE, TERMINAL FLAG. If the message was broadcast, the Broadcast Command Received bit is also set to logic "1" in the internal Status Word Register. The lookup table pointer value for subaddress 0 or 31 is stored in the third location of the message block descriptor. For a Transmit Last Command or Transmit BIT Word mode command (unless EXTERNAL BIT WORD is enabled), the Data Word transmitted is read from an internal register. For other mode commands with data, the Data Word is accessed from/to the location referenced by the lookup table pointer for subaddress 0 or 31.	EOM; if illegal command: ILLEGAL COMMAND	Any of the following may be set or cleared, as applicable: TERMINAL FLAG INHIBITED, TRANSMITTER SHUTDOWN A, TRANSMITTER SHUTDOWN B.	RT SUBADDRESS CONTROL WORD; EOM (if Selected)
ENHANCED MODE enabled and ENHANCED MODE CODE HANDLING enabled; Receive valid, defined mode code message (including RESERVED mode codes).	If the message is a Transmit Status or Transmit Last Command mode code, the RT Status Word resulting from the previous message is transmitted and the internal Status Word is not updated. Otherwise, affects the following RT Status Word bits, as applicable: MESSAGE ERROR (if illegal), BUSY (per Busy lookup table), DYNAMIC BUS CONTROL ACCEPTANCE, TERMINAL FLAG. If the message was broadcast, the Broadcast Command Received bit is also set to logic "1" in the internal Status Word Register. For a Transmit Last Command or Transmit BIT Word (unless EXTERNAL BIT WORD is enabled) mode command, the Data Word transmitted is read from an internal register. For other mode codes with data, the Data Word is accessed	EOM; if illegal command: ILLEGAL COMMAND	Any of the following may be set or cleared, as applicable: TERMINAL FLAG INHIBITED, TRANSMITTER SHUTDOWN A, TRANSMITTER SHUTDOWN B.	RT MODE CODE (if selected for the particular mode command by means of the Mode Code Selective Interrupt Table, locations 0108-010F); EOM

Table 131. RT Exception. Conditions				
	RT Response, Effect on RT Status Word Register Bits	**RT Block Status Word Bits (assuming Enhanced Mode)**	**RT Built-in-Test (BIT) Word Bits**	**Interrupt Conditions, Interrupt Status Register Bits (if enabled)**
	from/to the mode code Data Word table, address locations 0110-013F, which is mapped by broadcast, T/R*, and MC3-MC0. In addition, the Data Word received or transmitted will be stored in the third location in the message block descriptor.			
Loop Test Failure: **The received version of a transmitted word was determined to be invalid (encoding, bit count, parity) and/or the received version of the last word transmitted did not match the transmitted version.**	If ENHANCED MODE is enabled and RTFAIL-RTFLAG WRAP ENABLE, bit 2 of Configuration Register #3 is logic "1," the Terminal Flag Status Word bit will be set to logic "1" in response to the next non-broadcast message.	EOM, ERROR FLAG, LOOP TEST FAIL	LOOP TEST FAILURE A or LOOP TEST FAILURE B	FORMAT ERROR; EOM; RT SUBADDRESS CONTROL WORD or RT MODE CODE (if selected)
Transmitter Timeout: **The transmitter failsafe timer timed out after the Enhanced Mini-ACE RT attempted to transmit for longer than 668 µs.**	Response is terminated as a result of the timeout. If ENHANCED MODE is enabled and RTFAIL-RTFLAG WRAP ENABLE, bit 2 of Configuration Register #3, is logic "1," the Terminal flag Status Word bit will be set to logic "1" in response to the next non-broadcast message. A Transmitter Timeout has no effect on the RT responding to subsequent messages.	EOM	TRANSMITTER TIMEOUT	EOM, RT SUBADDRESS CONTROL WORD or RT MODE CODE (if selected)
Handshake Failure: **For a Start-of-Message (SOM) or Data Word (read or write) transfer sequence. Note that a handshake failure will not occur during an RT End-of-Message (EOM) sequence.** **In DMA mode, the host processor did not assert DTGRT* in time (10.5 µs for 20MHzclock,10.0 µs for a 16 MHz clock, 9.0 µs for a 12 MHz clock, 8.5 µs for 10 MHz clock), after the Enhanced Mini-ACE asserted its DTREQ* output or** **In transparent mode, the PROCESSOR kept STRBD* asserted too long after the Enhanced Mini-ACE asserted its READYD* handshake output.**	If the Handshake Failure occurs during the RT Start-of-Message (SOM) transfer sequence, the Enhanced Mini-ACE terminates processing of the message: the message will be ignored, and therefore will not result in a descriptor being written to the stack. Storage of received Command Word and/or data words, or response of transmit data words is terminated as a result of the handshake timeout.	If the Handshake Failure occurred during the Start-of-Message (SOM) transfer sequence: NO bits will be set: that is, the message will be completely ignored. If the Handshake Failure occurs during a Data Word transfer sequence: EOM, ERROR FLAG	HANDSHAKE FAILURE	HANDSHAKE FAILURE

Table 131. RT Exception. Conditions				
	RT Response, Effect on RT Status Word Register Bits	**RT Block Status Word Bits (assuming Enhanced Mode)**	**RT Built-in-Test (BIT) Word Bits**	**Interrupt Conditions, Interrupt Status Register Bits (if enabled)**
ENHANCED MODE and Valid receive Command Word received that has been illegalized by means of the illegalization table	The RT responds with the Message Error bit set. The Message Error bit is set to logic "1" in the internal Status Word Register. If the message was broadcast, the Broadcast Command Received bit is also set to logic "1" in the internal Status Word Register. If ILLEGAL RECEIVE TRANSFER DISABLE, bit 4 of Configuration Register #3, is set to logic "0," received data words are stored to the shared RAM. If ILLEGAL RECEIVE TRANSFER DISABLE is programmed to logic "1," received Data words are not stored to the shared RAM.	EOM, ILLEGAL COMMAND WORD, FORMAT ERROR	None	RT SUBADDRESS CONTROL WORD or RT MODE CODE (if selected); FORMAT ERROR; END OF MESSAGE
ENHANCED MODE and Valid transmit Command Word received that has been illegalized by means of the illegalization table	The RT responds with the Message Error bit set. No data words are transmitted. The Message Error bit is set to logic "1" in the internal Status Word Register. If the message was broadcast, the Broadcast Command Received bit is also set to logic "1" in the internal Status Word Register.	EOM, ILLEGAL COMMAND WORD	None	RT SUBADDRESS CONTROL WORD or RT MODE CODE (if selected); END OF MESSAGE
ENHANCED MODE and RT is Busy for a valid receive Command (either globally, or in response to a particular valid receive command)	The RT responds with the Busy bit set. The Busy bit is set to logic "1" in the internal Status Word Register. If the message was broadcast, the Broadcast Command Received bit is also set to logic "1" in the internal Status Word Register. If BUSY RECEIVE TRANSFER DISABLE, bit 3 of Configuration Register #3, is set to logic "0," received Data words are stored to the shared RAM. If BUSY RECEIVE TRANSFER DISABLE is programmed to logic "1," received Data words are not stored to the shared RAM.	EOM, ERROR FLAG, FORMAT ERROR	None	RT SUBADDRESS CONTROL WORD or RT MODE CODE (if selected); FORMAT ERROR; END OF MESSAGE
ENHANCED MODE and RT is Busy for a valid Transmit Command (either globally, or in Response to a Particular Valid Transmit Command)	The RT responds with the Busy bit set. No data words are transmitted. The Busy bit is set to logic "1" in the internal Status Word Register. If the message was broadcast, the Broadcast Command Received bit is also set to logic "1" in the internal Status Word Register.	EOM, ILLEGAL COMMAND WORD	None	RT SUBADDRESS CONTROL WORD or RT MODE CODE (if selected); END OF MESSAGE

Table 131. RT Exception. Conditions				
	RT Response, Effect on RT Status Word Register Bits	**RT Block Status Word Bits (assuming Enhanced Mode)**	**RT Built-in-Test (BIT) Word Bits**	**Interrupt Conditions, Interrupt Status Register Bits (if enabled)**
ENHANCED MODE and the Enhanced Mini-ACE RT is the receiving RT in an RT-to-RT transfer and: GAP CHECK ENABLED, bit 8 of Configuration Register #5, is programmed to logic "1" and the transmitting RT's response time gap is less than 2 µs, or Incorrect Sync Type or Format Error (encoding, bit count and/or parity) in the transmitting RT's Status Word, or The RT address in the Transmitting RT's Status Word does not match the RT address in the transmit Command Word.	No RT response. The Message Error bit is set to logic "1" in the internal RT Status Word. If the message was received at the broadcast address, the Broadcast Command Received bit is also set to logic "1" in the internal Status Word Register.	EOM, ERROR FLAG, RT-to-RT FORMAT, FORMAT ERROR, RT-RT GAP/SYNC/ ADDRESS ERROR	RT-RT GAP/SYNC/ ADDRESS ERROR	FORMAT ERROR; RT SUBADDRESS CONTROL WORD or RT MODE CODE (if selected); END OF MESSAGE
ENHANCED MODE and the Enhanced Mini-ACE RT is receiving RT in RT-to-RT Transfer and: Error in Command Word to Transmitting RT: T/R* bit = 0, or SUBADDRESS = 00000, or 11111, or same RT address as receive Command Word.	No RT response. The Message Error bit is set to logic "1" in the internal RT Status Word. If the message was received at the broadcast address, the Broadcast Command Received bit is also set to logic "1" in the internal Status Word Register.	EOM, ERROR FLAG, RT-to-RT FORMAT, FORMAT ERROR, RT-RT SECOND COMMAND ERROR	RT-RT SECOND COMMAND WORD ERROR	FORMAT ERROR; RT SUBADDRESS CONTROL WORD or RT MODE CODE (if selected); END OF MESSAGE
ENHANCED MODE and Enhanced Mini-ACE is Receiving RT for RT-to-RT Transfer and there is an error in the Transmitting RT's Response: sync or Manchester encoding, bit count, parity, word count. This includes a response by the transmitting RT with the Message Error and/or Busy bits set to logic "1," followed by no data words.	No RT response. The Message Error bit is set to logic "1" in the internal RT Status Word. If the message was received at the broadcast address, the Broadcast Command Received bit is also set to logic "1" in the internal Status Word Register.	EOM, ERROR FLAG, RT-to-RT FORMAT, FORMAT ERROR, and one of the following: WORD COUNT ERROR or INCORRECT DATA SYNC or INVALID WORD	One of the following (as appropriate): HIGH WORD COUNT or LOW WORD COUNT or INCORRECT SYNC RECEIVED or PARITY/ MANCHESTER ERROR RECEIVED	FORMAT ERROR; RT SUBADDRESS CONTROL WORD or RT MODE CODE (if selected): END OF MESSAGE

Table 131. RT Exception. Conditions				
	RT Response, Effect on RT Status Word Register Bits	**RT Block Status Word Bits (assuming Enhanced Mode)**	**RT Built-in-Test (BIT) Word Bits**	**Interrupt Conditions, Interrupt Status Register Bits (if enabled)**
ENHANCED MODE and Command Word Contents Error: **BROADCAST DISABLED is programmed to logic "0" and Command is a non-mode code transmit broadcast command,** **or** **BROADCAST DISABLED is programmed to logic "0" and message is a broadcasted -1553B mode code that is not permitted to be broadcast,** **or** **OVERRIDE MODE T/R* ERROR is logic "0" and a Command Word has a T/R* bit of 0, a SUBADDRESS /mode field of 00000 or 11111, and a mode code field between 00000 and 01111.**	No RT response. The Message Error bit is set to logic "1" in the internal RT Status Word. If the message was a broadcast command, the Broadcast Command Received bit is also set to logic "1" in the internal Status Word Register.	EOM, ERROR FLAG, RT-to-RT FORMAT, FORMAT ERROR, COMMAND WORD CONTENTS ERROR	COMMAND WORD CONTENTS ERROR	FORMAT ERROR; RT SUBADDRESS CONTROL WORD or RT MODE CODE (if selected): END OF MESSAGE
Superceded Message: **RT receives an incomplete message on one bus, followed by a gap with a maximum time of between 6 and 10 µs, followed by a new valid message on the same bus or alternate bus,** **or** **RT is responding to a transmit message on one bus and receives the start of a valid message on the alternate bus.**	The Enhanced Mini-ACE RT will abort processing of the first (superceded) message and respond in full to the second (superceding) message. If either message was broadcast, the Broadcast Command Received bit is set to logic "1" in the internal Status Word Register. If the second message was not a broadcast message, or a Transmit Status or Transmit Last Command mode code, the Broadcast Command Received bit in the internal RT Status Word Register is cleared to logic "0." If broadcast is enabled and the Enhanced Mini-ACE RT receives a broadcast Command Word (RT address 31), followed contiguously by a Transmit Command Word to the Enhanced Mini-ACE RT's own RTaddress, indicating an RT-to-RTs (broadcast) message, the broadcast Command Word will be superceded and the Enhanced Mini-ACE RT will respond to the transmit command.	The Block Status Word stored during the Start-of-Message (SOM) sequence for the first message remains stored in the block descriptor for that (superceded) message. This word will have an EOM bit of logic "0" and an SOM bit of logic "1." The Block Status Word for the second message will be stored at an address four locations above (modulo the stack size) that of the Block Status Word for the first message. Assuming that the second message is not itself superceded, its Block Status Word will have an EOM bit of logic "1," and an SOM bit of logic "0." All other bits will be valid for the second message.	None	There will be no interrupts following the first message. For the second message: RT SUBADDRESS CONTROL WORD or RT MODE CODE (if selected); END OF MESSAGE

6.37 Summary of Responses to Mode Code Messages

In the "1553B" Mode Codes configuration, the Enhanced Mini-ACE implements all MIL-STD-1553B mode codes applicable to dual redundant bus operation. The Enhanced Mini-ACE's responses to mode codes, including responses to various error conditions, is summarized in Table 132.

Table 132. Mode Code Summary

T/R Bit	Mode Code	Function	Data Word	Broadcast Allowed
0	00000-011111	Undefined (Note 1)	No	No
1	000000	Dynamic Bus Control	No	No
1	00001	Synchronize (Note 6)	No	Yes
1	00010	Transmit Status Word	No	No
1	00011	Initiate Self Test (Note 2)	No	Yes
1	00100	Transmitter Shutdown	No	Yes
1	00101	Override Transmitter Shutdown	No	Yes
1	00110	Inhibit Terminal Flag	No	Yes
1	00111	Override Inhibit Terminal Flag	No	Yes
1	01000	Reset Remote Terminal	No	Yes
1	01001-01111	RESERVED	No	TBD
1	10000	Transmit Vector Word (Note 6)	From Memory	No
0	10001	Synchronize with Data	To Memory (and, possibly, to Time Tag Register, see Note 3)	Yes
1	10010	Transmit Last Command	From Internal Register	No
1	10011	Transmit BIT Word	From Internal Register or RAM location (see Note 4)	No
0	10100	Selected Transmitter Shutdown (see Note 5)	To Memory	Yes
0	10101	Override Selected Transmitter Shutdown (see Note 5)	To Memory	Y
0	10110-11111	RESERVED	Yes	TBD
1	10110-11111	RESERVED	Yes	TBD

NOTES:

1. Receive mode commands 00000 through 01111 are undefined per MIL-STD-1553B. If the Enhanced Mini-ACE RT is not in ENHANCED MODE or if OVERRIDE MODE CODE T/R* BIT ERROR, bit 6 of Configuration Register #3, is programmed to logic "0," the Enhanced Mini-ACE RT will not respond and the Message Error bit will be set in the internal Status Word Register. If the Enhanced Mini-ACE is in ENHANCED MODE and OVERRIDE MODE CODE T/R* BIT ERROR is programmed to logic "1," the Enhanced Mini-ACE RT will treat the message as a RESERVED mode command. That is, it will respond with Status and a Message Error bit of logic "0" (unless the command has been illegalized).
2. If RT HALT ENABLE, bit 4 of Configuration Register #7 is logic “1,” the RT will automatically revert to its offline or (idle) BC mode. It will remain offline until either the host initiates self-test and self-test

completes, or if the host writes logic “1” to clear RT HALT, bit 11 of the Start/Reset Register. For further information, refer to the section on Enhanced Mini-ACE Built in Self-Test.
3. If LOAD TIME TAG ON SYNCHRONIZE, bit 5 of Configuration Register #2, is programmed to logic "1," the received Data Word is stored to the Time Tag Register. If Load Time Tag on Synchronize and Enhanced Time Tag Synchronize (Bit 2 of Configuration Record #7) are both programmed to logic “1,” the received data word will **only** be stored to the Time Tag Register if the LSB of the received data word is logic “0.”
4. In the non-ENHANCED mode, or if EXTERNAL BIT WORD ENABLE, bit 15 of Configuration Register #4, is programmed to logic "0," the BIT Word defined by Table 130 and stored in the Enhanced Mini-ACE's BIT Word Register is transmitted. If the Enhanced Mini-ACE is programmed for ENHANCED MODE and if EXTERNAL BIT WORD ENABLE is programmed to logic "1," the BIT Word transmitted will be read from a memory location. Refer to the section on the Transmit BIT Word mode command.
5. Terminal responds with Clear Status but no action is taken.
6. **See Appendix “F”** for important information regarding these Mode Codes if Clear Time Tag on Synchronize and Clear Service Request (i.e., bits 6 and 2 of Configuration Register #2 are Logic “1”) are used in conjunction with Interrupt Status Queue (i.e., bit 6 of Configuration Register #6 is Logic “1”).

6.38 Detailed Functional Description of Mode Codes ("1553B" Implementation)

6.38.1 Dynamic Bus Control (T/R* = 1; 00000)

Message Sequence = DBC Status

The Enhanced Mini-ACE responds with Status. If the host processor has written a logic "0" to the DB ACCEPT* bit in Configuration Register #1 (bit 11), the DYNAMIC BUS CONTROL ACCEPTANCE bit will be logic "1" in the RT Status Word. If the Enhanced Mini-ACE responds with the DYNAMIC BUS CONTROL ACCEPTANCE bit set, the Enhanced Mini-ACE **remains in RT mode** until directed to switch to BC mode by the PROCESSOR.

Error Conditions

Invalid Command. No response, command ignored.

Command Followed by Data Word. No Status response. Set Message error bit (Status Word), High Word Count (BIT Word).

T/R* bit set to zero. No Status response. Set Message Error bit (Status Word), Command Word Contents Error (BIT Word).

Zero T/R* bit and Broadcast Address. No Status response. Set Message Error and Broadcast Received bits (Status Word), Command Word Contents Error (BIT Word).

Broadcast Address. No Status response. Set Message Error and Broadcast Received bits (Status Word), Command Word Contents Error (BIT Word).

6.38.2 Synchronize Without Data Word (T/R* = 1; 00001)

Message Sequence = SYNC-Status

The Enhanced Mini-ACE responds with Status. If sent as a broadcast, the Broadcast Received bit will be set and Status response suppressed. If the CLEAR TIME TAG ON SYNCHRONIZE option is enabled (bit 6 in Configuration Register #2 programmed to logic "1") the Enhanced Mini-ACE will clear its internal time tag register to zero upon receipt of this mode code.

See Appendix "F" for important information **IF** bits 2 or 6 (Clear Service Request, Clear Time Tag on Synchronize) of Configuration Register #2 are enabled (Logic "1") **AND** Interrupt Status Queue is enabled (i.e., bit 6 of Configuration Register #6 is Logic "1") **AND** bits 6, 7 or 14 (Time Tag Rollover, RT Address Parity Error, or RAM Parity Error respectively) of Interrupt Mask Register #1 are enabled (Logic "1").

Invalid Command. No response, command ignored.

Error Conditions

Command Followed by Data Word. No Status response. Set Message Error bit (Status Word), High Word Count (BIT Word).

T/R* bit set to zero. No Status response. Set Message Error bit (Status Word), Command Word Contents Error (BIT Word).

Zero T/R* bit and Broadcast Address. No Status response. Set Message Error and Broadcast Received bits (Status Word), Command Word Contents Error (BIT Word).

6.38.3 Transmit Status Word (T/R* = 1; 00010)

Message Sequence = Transmit Status - Status

The Status register is not updated before it is transmitted and contains the resulting status from the previous command (assuming that it was not a Transmit status or Transmit last command mode command).

Error Conditions

Invalid Command. No response, command ignored.

Command Followed by Data Word. No Status response. Set Message Error bit (Status Word).

T/R* bit set to zero. No Status response. Set Message Error bit (Status Word), Command Word Contents Error (BIT Word).

Zero T/R* bit and Broadcast Address. No Status response. Set Message Error and Broadcast Received bits (Status Word), Command Word Contents Error (BIT Word).

Broadcast Address. No Status response. Set Message Error and Broadcast Command Received bits (Status Word), Command Contents Error (BIT Word).

6.38.4 Initiate Self-test (T/R* = 1; 00011)

Message Sequence = Self-Test – Status

The Enhanced Mini-ACE responds with Status. If the command was broadcast, the broadcast received bit is set and status transmission suppressed.

If RT HALT ENABLE (bit 4 of Configuration Register #7) has been programmed to logic "1" and the Enhanced Mini-ACE RT receives an Initiate self-test mode command, the RT will automatically go to an offline state (i.e., it will not receive or respond to messages from the 1553 bus). It is then up to the host to initiate the protocol or RAM self-test, via bits 7 or 9 respectively of the Start/Reset Register. Once the particular self-test completes, the Enhanced Mini-ACE RT will automatically go back online.

If the RT receives an Initiate self-test mode command and transitions to its offline state, the user (host) may “choose” to **not** perform the protocol self-test. To do this, the host should write a value of logic "1" to CLEAR RT HALT. Following this write operation, the RT will automatically **revert back to its online state**, and resume receiving and responding to messages from the 1553 bus.

Error Conditions

Invalid Command. No response, command ignored.

Command Followed by Data Word. No Status response. Set Message Error bit (Status Word), High Word Count (BIT Word).

T/R* bit set to zero. No status response. Set Message Error bit (Status Word), Command Word Contents Error (BIT Word).

Zero T/R* bit and Broadcast Address. No Status response. Set Message Error and Broadcast Command Received bits (Status word), Command Word Contents Error (BIT Word).

Loopback Test Fails. Set Terminal Flag bit in internal Status register (Status Word for next non-broadcast command), Current Channel (A or B) Loop Test Failure and CH A/B Loop Test Failure (BIT Word), assert Rt Fail output.

6.38.5 Transmitter Shutdown (T/R* = 1; 00100)

Message Sequence = Shutdown – Status

This command is only used with dual redundant bus systems. The Enhanced Mini-ACE responds with Status. Following the Status transmission, the Enhanced Mini-ACE inhibits any further transmission from the alternate redundant channel. Once shutdown, the transmitter can only be reactivated by an Override Transmitter Shutdown or Reset RT mode command, a Software Reset (writing logic "1" to bit 0 in the Start/Reset Register), or Hardware Reset (MSTRCLR input). Note that the receivers on both channels are always active, even when the transmitters are inhibited.

Error Conditions

Invalid Command. No response, command ignored.

Command Followed by Data Word. No Status response. Set Message Error bit (Status Word), High Word Count (BIT Word).

T/R* bit set to zero. No status response. Set Message Error bit (Status Word), Command Word Contents Error (BIT Word).

Zero T/R* bit and Broadcast Address. No Status response. Set Message Error and Broadcast Command Received bits (Status word), Command Word Contents Error (BIT Word).

6.38.6 Override Transmitter Shutdown (T/R* = 1; 00101)

Message Sequence = Override Shutdown – Status

This command is only used with dual redundant bus systems. The Enhanced Mini-ACE responds with Status. At the end of the Status transmission, the Enhanced Mini-ACE reactivates the transmitter of the alternate redundant bus. If the command was broadcast, the Broadcast Command Received Status Word bit is set and status transmission is suppressed.

Error Messages

Invalid Command. No response, command ignored.

Command Followed by Data Word. No Status response. Set Message Error bit (Status Word), High Word Count (BIT Word).

T/R* bit set to zero. No status response. Set Message Error bit (Status Word), Command Word Contents Error (BIT Word).

Zero T/R* bit and Broadcast Address. No Status response. Set Message Error and Broadcast Command Received bits (Status word), Command Word Contents Error (BIT Word).

6.38.7 Inhibit Terminal Flag Bit (T/R* = 1; 00110)

Message Sequence = Inhibit Terminal Flag – Status

The Enhanced Mini-ACE responds with Status and inhibits further setting of the Terminal Flag bit in its internal Status Word register. Once the Terminal Flag has been inhibited, it can only be reactivated by an Override Inhibit Terminal Flag or Reset RT mode code commands, or by Reset. If the command was broadcast, the Broadcast Received bit is set, the state of the Terminal Flag bit in the internal Status Word register remains unchanged and Status transmission is suppressed.

Error Conditions

Invalid Command. No response, command ignored.

Command Followed by Data Word. No Status response. Set Message Error bit (Status Word), High Word Count (BIT Word).

T/R* bit set to zero. No status response. Set Message Error bit (Status Word), Command Word Contents Error (BIT Word).

Zero T/R* bit and Broadcast Address. No Status response. Set Message Error and Broadcast Command Received bits (Status word), Command Word Contents Error (BIT Word).

6.38.8 Override Inhibit Terminal Flag Bit (T/R* = 1; 00111)

Message Sequence = Inhibit Terminal Flag – Status

The Enhanced Mini-ACE responds with Status and re-enables the Terminal Flag bit in its internal Status register. If the command was a broadcast, the Broadcast Command Received bit is set and status transmission is suppressed.

Error Conditions

Invalid Command. No response, command ignored.

Command Followed by Data Word. No Status response. Set Message Error bit (Status Word), High Word Count (BIT Word).

T/R* bit set to zero. No status response. Set Message Error bit (Status Word), Command Word Contents Error (BIT Word).

Zero T/R* bit and Broadcast Address. No Status response. Set Message Error and Broadcast Command Received bits (Status word), Command Word Contents Error (BIT Word).

6.38.9 Reset Remote Terminal (T/R* = 1; 01000)

Message Sequence = Reset Remote Terminal – Status

The Enhanced Mini-ACE responds with Status and internally resets. The Message Error and Broadcast Command Received bits of the internal Status register are reset to 0. The internal BIT Word Register is reset to 0. If either of the 1553 transmitters has been shut down, the shutdown condition is overridden. If the Terminal Flag bit has been inhibited, the inhibit is overridden. The receipt of this command **does not** reset any of the Enhanced Mini-ACE's host programmable registers.

If the command is received as a broadcast, the Broadcast Command Received bit is set and the Status Word is suppressed. Also, if the command is received as a broadcast and the Terminal Flag bit had been set as a result of the Loopback test of the previous message, the Terminal Flag bit is not reset to zero. The resulting operation is completed approximately 8 µs after the mid-parity bit crossing of the Reset mode code command.

If the Enhanced Mini-ACE is programmed for ENHANCED MODE (bit 15 of Configuration Register #3 is logic "1") **and** MODE CODE RESET/$\overline{\text{INCMD}}$, bit 0 of configuration register #7, has been programmed to logic "1," the Enhanced Mini-ACE will output a two clock cycle wide negative-going pulse on its $\overline{\text{INCMD}}$/$\overline{\text{MCRST}}$ output following receipt of a Reset RT mode command.

Error Conditions

Invalid Command. No response, command ignored.

Command Followed by Data Word. No Status response. Set Message Error bit (Status Word), High Word Count (BIT Word).

T/R* bit set to zero. No status response. Set Message Error bit (Status Word), Command Word Contents Error (BIT Word).

Zero T/R* bit and Broadcast Address. No Status response. Set Message Error and Broadcast Command Received bits (Status word), Command Word Contents Error (BIT Word).

6.38.10 Reserved Mode Codes (T/R*=1; 01001 - 01111)

Message Sequence = Reserved Mode Codes – Status

The Enhanced Mini-ACE responds with status. If the command has been illegalized by means of the illegalization table, the Message Error Status Word bit will be set.

Error Conditions

Invalid Command. No response, command ignored.

Command Followed by Data Word. No Status response. Set Message Error bit (Status Word), High Word Count (BIT Word).

T/R* bit set to zero. No status response. Set Message Error bit (Status Word), Command Word Contents Error (BIT Word).

Zero T/R* bit and Broadcast Address. No Status response. Set Message Error and Broadcast Command Received bits (Status word), Command Word Contents Error (BIT Word).

6.38.11 Transmit Vector Word (T/R* = 1; 10000)

Message Sequence = Transmit Vector Word – Status/Vector Word

The Enhanced Mini-ACE transmits a Status Word followed by a Vector Word. If the ENHANCED MODE CODES are enabled the contents of the Vector Word are obtained from RAM location 120 (hex). If ENHANCED MODE CODES are not enabled, the single word data block in the shared RAM that is referenced by the lookup table pointer for transmit subaddress 00000 or 11111.

See Appendix "F" for important information **IF** bits 2 or 6 (Clear Service Request, Clear Time Tag on Synchronize) of Configuration Register #2 are enabled (Logic "1") **AND** Interrupt Status Queue is enabled (i.e., bit 6 of Configuration Register #6 is Logic "1") **AND** bits 6, 7 or 14 (Time Tag Rollover, RT Address Parity Error, or RAM Parity Error respectively) of Interrupt Mask Register #1 are enabled (Logic "1").

Error Conditions

Invalid Command. No response, command ignored.

Correct Command Followed by Data Word. No Status response. Set Message Error bit (Status Word), High Word Count (BIT Word).

T/R* bit set to zero, no Data Word. No Status response. Set Message Error bit (Status Word), and Low Word Count (BIT Word).

T/R* bit set to zero plus one Data Word. The Enhanced Mini-ACE will respond with Status. The Data Word will be stored in RAM location 0110 (or single-word data block for subaddress 0000 or 1111).

Zero T/R* bit and Broadcast Address, no Data Word. No Status response. Set Message Error and Broadcast Command Received bits (Status Word), and Low Word Count (BIT word).

Zero T/R* bit and Broadcast Address, plus one Data Word. No Status response. Set Broadcast Command Received bits (Status Word).

Broadcast Address. No Status response. Set Message Error and Broadcast Command Received bits (Status Word), Command Word Contents Error (BIT word).

6.38.12 Synchronize with Data Word (T/R* = 0; 10001)

Message Sequence = Synchronize Command Data/Word – Status

If the ENHANCED MODE CODES are enabled the received data word is stored in RAM location 0111 (hex). If ENHANCED MODE CODES are not enabled, the word is stored in the single-word data block in the shared RAM referenced by receive subaddress 00000 or 11111 in the lookup table. If the LOAD TIME TAG ON SYNCHRONIZE option is enabled (bit 5 in Configuration Register #2 set to logic "1") **and** ENHANCED TIME TAG SYNCHRONIZE (bit 2 of Configuration Register #7) is logic “0,” the Enhanced Mini-ACE will load the received 16-bit data word into its internal Time Tag Register upon receipt of this mode command.

Also, if LOAD TIME TAG on SYNCHRONIZE is logic “1” **and** ENHANCED TIME TAG SYNCHRONIZE is logic “1,” the Enhanced Mini-ACE will load the received 16-bit data word into its internal Time Tag Register upon receipt of this command, but **only** if the LSB of the received data word is logic “0.”

Error Conditions

Invalid Command. No response, command ignored.

Correct Command not followed by Data Word. No Status response. Set Message Error bit (Status Word), Low Word Count (BIT Word).

Command Followed by too many data words. No Status response. Set Message Error bit (Status Word), High Word Count (BIT word).

Command T/R* bit set to one followed by Data Word. No Status response. Set Message Error bit (Status Word), and High Word Count (BIT Word).

Command T/R* bit set to one not followed by Data Word. The Enhanced Mini-ACE replies with Status plus one Data Word. The Data Word is read from RAM location 121 hex (or single-word data block for subaddress 0000 or 1111).

Command T/R* Bit set to one and Broadcast Address. No Status response. Set Message Error and Broadcast Command Received bits (Status Word); Set Command Word Contents Error (BIT word).

6.38.13 Transmit Last Command (T/R* = 1; 10010)

Message Sequence = Transmit Last Command – Status/Last Command

The Status register is not updated before transmission. It contains the Status from the previous command. The Data Word transmitted contains the previous valid command (providing it was not another TRANSMIT LAST COMMAND mode command).

Error Conditions

Invalid Command. No response, command ignored.

Correct Command followed by Data Word. No Status response. Set Message Error bit (Status Word), High Word Count Error (Bit Word).

T/R* Bit set to zero, no Data Word. No Status response. Set Message Error bit (Status Word), Low Word Count (BIT Word).

T/R* bit set to zero plus one Data Word. The Enhanced Mini-ACE will respond with Status. The Data Word is transferred to RAM location 0112 (or single-word data block for subaddress 0000 or 1111).

Zero T/R* Bit and Broadcast Address, no Data Word. No Status response. Set Message Error and Broadcast Received bits (Status Word), Low Word Count Error(BIT Word).

Zero T/R* bit and Broadcast Address, one Data Word. No Status response. Set Broadcast Received Bit (status word). The Data Word is transferred to RAM location 0132 (or single-word data block for subaddress 0000 or 1111).

Broadcast Address. No Status response. Set Message Error and Broadcast Command Received bits (Status Word), Command Word Contents Error (BIT Word).

6.39 Transmit BIT Word (T/R* = 1; 10011)

Message Sequence = Transmit Bit Word – Status/Bit Word

The Enhanced Mini-ACE responds with Status followed by the Built-in Test (BIT) word. In the NON-ENHANCED mode, or if EXTERNAL BIT WORD ENABLE, bit 15 of Configuration Register #4 is programmed to logic "0," the BIT Word transmitted is accessed from the Enhanced Mini-ACE's internal BIT Word register. This word is defined in Table 130.

If the Enhanced Mini-ACE is programmed for ENHANCED MODE **and** if EXTERNAL BIT WORD ENABLE is programmed to logic "1," the BIT Word transmitted will be read from a memory location. In this case, if ENHANCED MODE CODES are disabled (ENHANCED MODE disabled or ENHANCED MODE HANDLING disabled [bit 0 of Configuration Register #3 is programmed to logic "0"]), the location accessed for the external BIT Word will be the address referenced by the RT lookup table pointer for subaddress 00000 or subaddress 11111. In this case, it should be noted that for a given subaddress (00000 or 11111), the same Data Word will be transmitted in response to either a Transmit BIT Word or Transmit vector word mode command.

If ENHANCED MODE CODES are enabled (ENHANCED MODE and ENHANCED MODE HANDLING enabled (bits 15 and 0 of Configuration

Register #3 are programmed to logic "1"), the external BIT Word will be accessed from address location 0123.

Note that assuming that EXTERNAL BIT WORD ENABLE, BIT 15 of Configuration Register #4, is logic “0,” bit 8 of the transmitted bit word will reflect the result of the most recently performed built-in protocol self-test. That is, bit 8 will be logic “0” if the self-test passed or logic “1” if the self-test failed.

Error Conditions

Invalid Command. No response, command ignored.

Correct Command followed by Data Word. No Status response. Set Message Error bit (Status Word), High Word Count Error (Bit Word).

T/R* Bit set to zero, no Data Word. No Status response. Set Message Error bit (Status Word), Low Word Count (BIT Word).

T/R* bit set to zero plus one Data Word. The Enhanced Mini-ACE will respond with Status. The Data Word is transferred to RAM address 0113 (or single-word data block for subaddress 0000 or 1111).

Zero T/R* Bit and Broadcast Address, no Data Word. No Status response. Set Message Error and Broadcast Received bits (Status Word), Low Word Count Error(BIT Word).

Zero T/R* bit and Broadcast Address, one Data Word. No Status response. Set Broadcast Received Bit (status word). The Data Word is transferred to RAM location 0133 (or single-word data block for subaddress 0000 or 1111).

Broadcast Address. No Status response. Set Message Error and Broadcast Command received bits (Status Word), Command Word contents Error (BIT Word).

6.39.1 Selected Transmitter Shutdown (T/R* = 0; 10100)

Message Sequence = Transmitter Shutdown/Data/Status

The Data Word received is transferred to the RAM and Status is transmitted. If ENHANCED MODE CODES are not enabled, the Data Word is written to the single-word data block referenced by the lookup table pointer for subaddress 00000 or 11111. If ENHANCED MODE CODES are enabled, the Data Word is stored at hex location 0114. The Enhanced Mini-ACE takes no other action. No transmitters are shut down as a result of this mode command. This command is intended for use with RTs with more than one dual redundant channel. If the command was a broadcast, the Broadcast Command Received bit is set and Status transmission is suppressed.

Error Conditions

Invalid Command. No response, command ignored.

Correct Command not followed by Data Word. No Status response. Set Message Error bit (Status Word), and Low Word Count Bit (BIT Word).

Command followed by too many data words. No Status response. Set Message Error bit (Status Word), and High Word Count Bit (BIT Word).

Command T/R* bit Set to one followed by one Data Word. No Status response. Set Message Error bit (Status Word), and High Word Count (BIT Word).

Command T/R* bit set to one not followed by Data Word. The Enhanced Mini-ACE replies with Status plus one Data Word. The Data Word is read from hex RAM location 0124 (or single-word data block for subaddress 0000 or 1111).

Command T/R* Bit Set to One and Broadcast Address. No Status response. Set Message Error and Broadcast Command Received bits (Status Word), and Command Contents Error (bit word).

6.39.2 Override Selected Transmitter Shutdown (T/R* = 0; 10101)

Message Sequence = Transmitter Shutdown/Data – Status

The Data Word received is transferred to the RAM. If ENHANCED MODE CODES are disabled, the lookup table pointer for subaddress 00000 or 11111 references the single-word data block. If ENHANCED MODE CODES are enabled, the Data Word is stored in hex RAM location 0115. No transmitters that have been previously shut down are reactivated as a result of this command. The Enhanced Mini-ACE takes no other action. This command is intended for use with RTs with more than one dual redundant channel. If the command was a broadcast, the Broadcast Command Received bit is set and Status transmission is suppressed. Invalid Command. No response, command ignored.

Error Conditions

Command not followed by Data Word. No Status response. Set Message Error bit (Status Word), and Low Word Count (BIT Word).

Command followed by too many data words. No Status response. Set Message Error bit (Status Word), and High Word Count bit (BIT Word).

Command T/R* bit Set to one followed by Data Word. No Status response. Set Message Error bit (Status Word), and High Word Count (BIT Word).

Command T/R* bit Set to one not followed by Data Word. The Enhanced Mini-ACE replies with Status plus one Data Word. The Data Word is read from hex RAM location 0125 (or single-word data block for subaddress 0000 or 1111).

Command T/R* Bit Set to one and Broadcast Address. No Status response. Set Message Error and Broadcast Command Received bits (Status Word), Command Word Contents (BIT Word).

6.39.3 Reserved Mode Codes (T/R* = 0; 10110 - 11111)

Message Sequence = Reserved Mode Code (T/R = 1) – Status/Data = Reserved Mode Code (T/R = 0)/Data – Status

For a RESERVED receive Command, the Enhanced Mini-ACE stores the Data Word to the shared RAM. If the command was a broadcast, the Broadcast Command Received bit is set and Status transmission is suppressed. For a RESERVED transmit Command Word, the Enhanced Mini-ACE responds with Status plus a single Data Word. The Data Word is read from the shared RAM. The lookup table pointers for subaddresses 0 and 31 reference the shared RAM locations if ENHANCED MODE CODES are disabled. If ENHANCED MODE CODES are enabled, the RAM location accessed are 0116-001F for received mode codes, 0126-012F for transmit mode codes, or 0136-013F for broadcast mode codes.

Invalid Command. No response, command ignored.

Error Conditions

Command Followed by Data Word. No Status response. Set Message Error bit (Status Word), High Word Count (BIT Word).

Broadcast Command. No Status response. Set Message Error bit (status word), and Command Word Contents Error (BIT Word).

Error Conditions (T/R = 1)

Invalid Command. No response, command ignored.

Command not followed by contiguous Data Word. No Status response. Set Message Error bit (Status Word), and Low Word Count (BIT Word).

Command followed by too many data words. No Status response. Set Message Error bit (Status Word), and High Word Count (BIT word).

6.40 RT Software Initialization Procedure

The following software sequence is typical of the steps the host PROCESSOR should perform following power turn-on to configure the Enhanced Mini-ACE for RT operation. For most applications, it is possible to skip many of the steps indicated.

Perform a software reset, by writing 0001 (hex) to the Start/Reset Register.

If any of the Enhanced mode functions (e.g., subaddress double buffering) are to be used, invoke the Enhanced Mini-ACE RT's ENHANCED MODE by writing 8000 (hex) to Configuration Register #3.

Initialize Interrupt Mask Registers #1 and #2. For many RT applications, the EOM interrupt will generally be enabled. In other instances, the RT Subaddress CONTROL WORD, RT CIRCULAR BUFFER ROLLOVER, RT 50% CIRCULAR BUFFER ROLLOVER, RT MODE CODE and/or FORMAT ERROR Interrupt Requests may also be enabled. The RT Subaddress CONTROL WORD interrupt enables interrupt requests to be issued following messages to specified transmit, receive, or broadcast subaddresses. The RT MODE CODE interrupt enables interrupt requests to be programmed for individual mode code commands. The RT CIRCULAR BUFFER ROLLOVER and/or RT 50% CIRCULAR BUFFER ROLLOVER interrupts may be used to provide interrupt requests following a multi-message reception or transmission of a specified number of data words to/from a given subaddress.

Load the starting location of the Stack into the Active Area Stack Pointer location in RAM.

As an option, initialize the Active Area Stack. If there is a desire to poll the Stack RAM while 1553 messages are being processed, the Block Status Word locations for the respective message block descriptors (relative address locations 0, 4, 8 . . . [stack size -4] in the stack) should be cleared to 0000. A Block Status Word of 0000 (SOM = EOM = 0) indicates that a message has not yet been processed.

Initialize the Active Area Lookup Table. The Lookup Table address for each transmit, receive, and (optionally) broadcast subaddress should be initialized as the pointer value for each respective lookup table. If the RT is going to be used in the ENHANCED RT MEMORY MANAGEMENT mode, it will also be necessary to select the memory management and interrupt options for each subaddress by initializing the Subaddress Control Words for the Active Area. If there are several unused subaddresses for an RT, it is recommended that the Lookup Table pointers for these be initialized to the same value in order to conserve memory space.

If ENHANCED MODE CODE HANDLING (bit 0 of Configuration Register #4) is not used, the pointers for receive subaddresses 0 and 31 (for Synchronize with Data messages) generally get loaded with the same pointer value. Similarly, the Lookup Table addresses for transmit subaddresses 0 and 31 (for Transmit Vector Word messages) generally get loaded with the same pointer value.

If ENHANCED MODE CODE HANDLING is enabled, data words for these mode codes are stored in locations 0111 (for Synchronize with data) and 0130 (for Transmit Vector Word).

Initialize Configuration Register #2. This involves selecting use of the following functions: ENHANCED RT MEMORY MANAGEMENT should be selected if it is desirable to select the subaddress-specific and/or global circular buffer features, and/or subaddress double buffering features on an individual subaddress basis. SEPARATE BROADCAST should be set if it is necessary to comply with Notice 2 for broadcast messages. This enables separate lookup table pointers for non-broadcast received and broadcast receive messages.

For RT mode, 256-WORD BOUNDARY DISABLE should normally be programmed to logic "0." If this bit is programmed to logic "1," it should be noted that the size of all circular buffers becomes 64K words.

The three TIME TAG RESOLUTION bits should be programmed to select the desired resolution for the time tag register. The choices are 2, 4, 8, 16, 32, or 64 µs/LSB, or "EXTERNAL" (external clock). CLEAR TIME TAG ON SYNCHRONIZE should be programmed to logic "1" if it is desired to clear the time tag to 0000 following receipt of a synchronize (without data) mode code. Similarly, LOAD TIME TAG ON SYNCHRONIZE should be programmed to logic "1" if it is desired to load the time tag to the value of the received Data Word following receipt of a synchronize with data mode code.

See Appendix "F" for important information regarding these Mode Codes if Clear Time Tag On Synchronize and Clear Service Request (i.e., bits 6 and 2 of Configuration Register #2 are Logic "1") are used in conjunction with Interrupt Status Queue (i.e., bit 6 of Configuration Register #6 is Logic "1").

ENHANCED INTERRUPTS should be enabled if the processor needs to poll using the Interrupt Status Registers without causing actual interrupts and/or it is desired that one or more of the following conditions cause an interrupt: TRANSMITTER TIMEOUT, RT COMMAND STACK ROLLOVER, or RT MODE CODE interrupt. INTERRUPT STATUS AUTO CLEAR should be programmed to logic "1" if it is desired to automatically clear the Interrupt Status Register and the Enhanced Mini-ACE's INT* output (for a "level" type interrupt output) after the Interrupt Status

Register has been read. LEVEL/PULSE* INTERRUPT REQUEST should be programmed to logic "0" for a pulse type interrupt (500 ns) or to logic "1" for a level type interrupt.

CLEAR SERVICE REQUEST should be programmed to logic "1" if it is desired to automatically clear the Service Request Status Word bit following reception of a Transmit vector word mode command.

See Appendix "F" for important information regarding these Mode Codes if Clear Time Tag On Synchronize and Clear Service Request (i.e., bits 6 and 2 of Configuration Register #2 are Logic "1") are used in conjunction with Interrupt Status Queue (i.e., bit 6 of Configuration Register #6 is Logic "1").

OVERWRITE INVALID DATA should be set to logic "1" if the circular buffer mode is used with one or more subaddresses. Subaddress DOUBLE BUFFERING should be enabled, if desired. BUSY LOOKUP Table ENABLE should be logic "1" if there is a need for the Busy bit in the RT Status Word to be set for particular T/R*/Bcst subaddresses.

Initialize Configuration Register #3. If one or more of the ENHANCED MODE features are to be used, bit 15 must be maintained at logic "1." The RT Stacksize is programmable with choices of 256 words (default, 64 messages), 512, 1024, or 2048 words (512 messages) by bits 14 and 13. Other RT features that may be selected by this register include ILLEGALIZATION (default = "0" = enabled), ALTERNATE STATUS (allowing software programming of all 11 Status Word bits), the choice of storing or not storing words for illegal or "BUSY" messages, and ENHANCED MODE CODE HANDLING.

If enhanced mode code handling is selected, data words for mode codes are stored in address locations 0110-013F, and interrupt requests for individual mode codes may be enabled by means of a table in address locations 0108-010F. Other RT options selectable by Configuration Register #3 include 1553A MODE CODES ENABLED, and RTFAIL/RTFLAG* WRAP ENABLED. 1553A MODE CODES ENABLED causes only subaddress 00000 to be treated as a mode code subaddress. RTFAIL*/RTFLAG* WRAP ENABLE causes the RT FLAG Status bit to be automatically set following a failure of the loop test. OVERRIDE MODE CODE T/R ERROR should only be programmed to logic "1" if receive Mode Codes 0000 through 01111 are to be treated as defined mode codes.

Initialize Configuration Registers #4. If EXTERNAL BIT WORD ENABLE is logic "1," the Data Word for a Transmit BIT Word mode command is accessed from a shared RAM location, rather than from an internal register. If ENHANCED MODE CODES are not enabled, the RAM location for the external BIT Word is the location pointed to by the lookup table pointer for subaddress 0 or 31. If ENHANCED MODE CODES are enabled, the external BIT Word is stored in location 0123.

INHIBIT BIT WORD IF BUSY prevents the BIT Word from being transmitted if the RT is Busy. If MODE CODE OVERRIDE BUSY is logic "1," this enables the Enhanced Mini-ACE RT to transmit a Data Word in response to a Transmit Vector Word or Reserved transmit mode command, even if the RT is busy.

For all versions of the Enhanced Mini-ACE, bit 3 of Configuration Register #4, “LATCH RT ADDRESS WITH C.R. #5” allows the Enhanced Mini-ACE's RT address to be software programmable by means of bits 5 through 0 of Configuration Register #5. If bit 3 of Configuration Register #4, “LATCH RT ADDRESS WITH C.R. #5” is logic "1," performing a write cycle to Configuration #5 causes the RT address to be read from pins RTAD4-0 and RTADP and latched internally (refer to the programming of Configuration Register #6 in selection of the RT ADDRESS SOUCE). After the RT address has been programmed, it is suggested that “LATCH RT ADDRESS WITH C.R. #5” be cleared to logic "0" to prevent an erroneous overwrite.

The default clock frequency for the Enhanced Mini-ACE is 16 MHz. Refer to the programming of Configuration Register #5 in the Software Interface Section of this manual for additional details of the setting of clock frequency operation.

EXPANDED ZERO-CROSSING This read/writable bit provides legacy compatibility to the ACE and Mini-ACE (Plus) GENERATIONS. It defaults to a value of a Logic “0” and will update to Logic “1” if programmed so by the host. However, it is important to note that the Enhanced Mini-ACE’s Manchester decoders are **always** configured to sample using **both** edges of the clock input CLK_IN. That is, depending on the input clock frequency, the decoder sampling frequency doubles to either 20 (for a 10 MHz clock), 24 (for 12 MHz), 32 (for 16 MHz), or 40 MHz (for 20 MHz). The higher sampling frequency provides improved tolerance (about 30 to 40 ns) to input zero crossing distortion. RESPONSE TIMEOUT SELECT 1-0 selects the time value for

the RT-to-RT RESPONSE TIMEOUT FROM AMONG 18.5 µs (default), 22.5, 50.5, or 130 µs. If GAPCHECK ENABLED is programmed to Logic “1,” the RT verify for a minimum bus dead time of 2 µs prior to the transmitting RT’s response in an RT-to-RT transfer, where the Enhanced Mini-ACE RT is the receiving RT.

If RT Illegalization is used, the PROCESSOR should initialize the Illegalization Table, address locations 0300-03FF.

If the BUSY LOOKUP Table is enabled, select the desired subaddresses to be busy by programming the Busy table, address locations 0240 through 0247.

If ENHANCED INTERRUPTS are enabled and ENHANCED MODE CODE HANDLING is enabled, interrupts for selective mode code messages may be enabled by programming locations 0108 through 010F.

Data to be transmitted on the 1553 bus (in response to transmit commands) should be written into the appropriate data blocks. As an option, the locations for data words for anticipated receive data words may be initialized to zero.

To configure the Enhanced Mini-ACE as an on-line RT, write to Configuration Register #1, setting bit 15 (MSB) to logic "1" and bit 14 to logic "0.” The current active area is selected by the setting of bit 13 (0 for A, 1 for B). If ALTERNATE RT STATUS is not enabled, bits 11 through 8 should be initialized to select the values for the RT Status Word bits Dynamic Bus Control Acceptance, Busy, Service Request, and Subsystem Flag. Also, in the ENHANCED mode, the RT flag Status Word bit is programmable by bit 7. These bits must be programmed for the logical inverse of their desired values in the RT Status Word.

If ALTERNATE RT STATUS is enabled, bits 10 through 0 of the Enhanced Mini-ACE's RT Status Word are programmable via bits 11 through 1 of Configuration Register #1. In this case, the logical values (non-inverted) of the intended Status Word bit values must be programmed.

Initialize Configuration Register #6. To allow the host to intervene accesses when the RT is performing its SOM or EOM sequences, set Enhanced CPU ACCESS to logic "1." To cause the stack pointer to increment (by 4) during EOM rather than SOM sequence program COMMAND STACK POINTER ON EOM to logic "1."

To enable the global circular buffer feature, program GLOBAL CIRCULAR BUFFER ENABLE to logic "1." In addition, to specify the size of the global circular buffer, program GLOBAL CIRCULAR BUFFER SIZE 2-0 to the desired value.

To use the Interrupt Status Queue , program INTERRUPT STATUS QUEUE ENABLE to logic "1."

See Appendix "F" for important information **IF** this bit is enabled (logic "1") **AND** terminal is operating in RT Mode **AND** bits 6, 7 or 14 (Time Tag Rollover, RT Address Parity Error, or Ram Parity Error respectively) of Interrupt Mask Register #1 are enabled (logic "1").

To disable either invalid or valid messages from resulting in Interrupt Status Queue entries, program DISABLE INVALID MESSAGES TO INTERRUPT STATUS QUEUE and/or DISABLE VALID MESSAGES TO INTERRUPT STATUS QUEUE TO logic "1."

To enable the RT address to be software controllable (without connecting RTAD4-0 and RTADP to D5-D0), program RT address source to logic "1."

To enable access to built-in self-test register addresses 32 to 63, program 64-WORD REGISTER SPACE to logic "1."

To specify a clock frequency of either 10 Mhz, 12 Mhz or 20 Mhz, program CLOCK SELECT 1 and CLOCK SELECT 0 to the desired value.

Initialize Configuration Register #7. To relocate the addresses of the RT stack pointer, lookup table, and other "Fixed Address" data structures, program MEMORY MANAGEMENT BASE ADDRESS 15-10 to a non-zero value.

To cause the RT to automatically revert to its offline state following receipt of a initiate self-test mode command, program RT HALT ENABLE to logic "1."

If the LOAD TIME TAG ON SYNCHRONIZE feature is used (bit 5 of Configuration Register #2 is logic "1"), to configure the RT to load the time tag register **only** when the LSB of the received data word (for a synchronize (with data) mode command is logic "0," program ENHANCED TIME TAG SYNCHRONIZE to logic "1."

To configure the Enhanced Mini-ACE RT to output a two clock cycle wide pulse on its $\overline{\text{INCMD}}/\overline{\text{MCRST}}$ output signal following the receipt of a reset remote terminal , program MODE CODE RESET/ $\overline{\text{INCMD}}$ to a value of logic “1.”

6.41 RT Pseudo Code Example

The following example illustrates the programming steps necessary to initialize the Enhanced Mini-ACE Remote Terminal registers and memory, and place the RT in its on-line state. The example illustrates the initialization of four subaddresses plus mode codes.

The four subaddresses are:

Subaddress 1, transmitting; single message mode, enabling TX:EOM interrupt

Subaddress 7, receiving (and broadcast); 1024-word circular buffer mode, enabling RX:CIRCULAR BUFFER ROLLOVER and BCST:CIRCULAR BUFFER ROLLOVER interrupts

Subaddress 19, receiving (and broadcast); double buffered mode, enabling RX:EOM and BCST:EOM interrupts

Subaddress 30, receiving, broadcast, and transmitting (wraparound subaddress); single message mode, no interrupts enabled

-ENHANCED MODE will be enabled to allow use of the full Enhanced Mini-ACE RT functionality.

-ENHANCED INTERRUPTS are enabled. Interrupts for RT Subaddress CONTROL WORD, RT CIRCULAR BUFFER ROLLOVER, RT MODE CODE, and FORMAT ERROR are enabled.

-BROADCAST SEPARATION is implemented.

ENHANCED MEMORY MANAGEMENT and OVERWRITE INVALID DATA are enabled, and 256-WORD BOUNDARY DISABLED is disabled, allowing the proper use of circular buffers for subaddress 7.

Time Tag Resolution of 64 µs/LSB (default) is selected.

Busy by subaddress is enabled. However, all subaddresses are initially programmed as "not busy.”

A loopback test failure will cause the RTFLAG bit to become set.

Received data words will not be stored for non-mode messages, but will be stored for mode code messages.

ENHANCED MODE CODE HANDLING will be enabled. As such, individual address locations are allocated for data words for Synchronize with data and Transmit vector word mode commands. In addition, interrupts are enabled for the Synchronize (with and without data), Reset, and Self-test mode commands. Interrupts are also enabled for those commands received to the broadcast address.

The Enhanced Mini-ACE is initialized for a 16 MHz clock input, with GAP CHECKING and EXPANDED ZERO CROSSING enabled. An RT address of seven (7) is assigned. All used subaddresses, as well as all MIL-STD-1553B mode codes except Selected transmitter shutdown and override, are programmed as legal. This includes the associated broadcast commands, where appropriate. All unused subaddresses and mode codes, and undefined and reserved mode codes are illegalized.

The (single) 32-word Data Word Block for transmit subaddress 1 is initially loaded with a pattern of 0000, 0001, 001F. The values of all RT Status Word bits are initialized to 0. Table 133 illustrates the memory map to initialize for the subaddresses, mode codes, and other conditions described on the previous page.

Table 133 Memory Map For RT Example Pseudo Code			
Address	**Data**	**Description**	**Portion of Memory, Comment**
0000 0004 . . . 00FC	0000 0000 . . . 0000	Block Status Word location for Message #0 . . . . Block Status Word location for Message #63	Stack Area. Note that the locations allocated for anticipated Block Status Words, stored by the Enhanced Mini-ACE in every fourth location (0000, 0004, ..00FC) at the start and end of messages, are initialized to 0000.
100	0	Area A (active area) Stack Pointer	Fixed Location
108	0	No interrupts for receive mode codes 0-15	**Mode code interrupts**
109	2	Enable interrupts for receive mode code: Synchronize with data	
010A	010A	Enable interrupts for transmit mode codes: Synchronize (without data), Reset RT, Self-Test	
010B	0	No interrupts for transmit mode codes 16-31	
010C	0	No interrupts for broadcast receive mode codes 0-15	
010D	0	Enable interrupts for broadcast receive mode code: Synchronize with data	
10	010A	Enable interrupts for broadcast transmit mode codes: Synchronize without data, Reset RT, Self-test	
010F	0	No interrupts for transmit broadcast mode codes 16-31	
111	0	Reserved for received Data Word for Synchronize with data mode command	Mode code data words (since ENHANCED MODE CODES are enabled)
120	1234	Data Word for Transmit vector word mode code initialized to 1234	
147	800	Receive subaddress 7	RT lookup table. Note that for the wraparound subaddress, (30, in accordance with the recommendation in MIL-STD-1553B Notice 2), the same pointer value (0480) is used for transmit, receive, and broadcast receive messages. Also, note that a pointer value of 04E0 should be assigned for all unused subaddresses (not shown).
153	440	Receive subaddress 19	
161	400	Transmit subaddress 1	
15	480	Receive subaddress 30	
17	480	Transmit subaddress 30	
187	0C00	Broadcast receive subaddress 7	
193	04A0	Broadcast receive subaddress 19	
19	480	Broadcast receive subaddress 30	
01A1	4000	Subaddress 1. Programmed for single message transmit buffer. TX:EOM interrupt enabled.	RT Subaddress Control Words. Note that a value of 0000 should be assigned to the Subaddress Control Words for all unused subaddresses not shown).
01A7	018C	Subaddress 7. 1024-word circular buffer programmed for receive and broadcast receive. RX:CIRCULAR BUFFER ROLLOVER and BCST:CIRCULAR BUFFER ROLLOVER interrupts enabled.	
01B3	8210	Subaddress 19. Programmed for double buffered receive and broadcast receive operation. RX:EOM and BCST:EOM interrupts enabled.	
01BE	0	Subaddress 30. Data wraparound subaddress. Programmed for single message operation for transmit, receive, and broadcast receive operation. No interrupts enabled.	
0240 . . 0247	0000 . . 0000	All subaddresses initialized as “not busy”	Subaddress Busy Table
300	FFFF	Subaddress 0, broadcast receive mode codes. Only Synchronize (with data) is legal.	Command illegalization Table. Note that only used subaddress and mode codes are legalized. All unused subaddresses and mode codes are illegalized
301	FFFD		
0302-030D	FFFF	Broadcast receive subaddress 1-6 illegal	
030E-030F	0	Broadcast receive subaddress 7 legal	
0310-0325	FFFF	Broadcast receive subaddress 8-18 illegal	
0326-0327	0	Broadcast receive subaddress 19 legal	
0328-033B	FFFF	Broadcast receive subaddress 20-29 illegal	
033C-033D	0	Broadcast receive subaddress 30 legal	
33	FFFF	Subaddress 31, broadcast receive mode codes. Only Synchronize (without data) is legal.	
033F	FFFD		

Table 133 Memory Map For RT Example Pseudo Code			
Address	**Data**	**Description**	**Portion of Memory, Comment**
340	FE05	Subaddress 0, broadcast transmit mode codes. Synchronize (without data), Initiate self-test, Transmitter shutdown, Override transmitter shutdown, Inhibit terminal flag bit, Override inhibit terminal flag bit, and Reset remote terminal are legal.	
341	FFFF		
0342-037D	Don't need to program (non-mode code broadcast transmit commands)		
37	FE05	Subaddress 31, broadcast transmit mode codes. Synchronize (without data), Initiate self-test, Transmitter shutdown, Override transmitter shutdown, Inhibit terminal flag bit, Override inhibit terminal flag bit, and Reset remote terminal are legal.	Command illegalization Table. Note that only used subaddress and mode codes are legalized. All unused subaddresses and mode codes are illegalized.
037F	FFFF		
380	FFFF	Subaddress 0, non-broadcast receive mode codes. Only Synchronize (with data) is legal.	
381	FFFD		
0382-038D	FFFF	Nonbroadcast subaddresses 1-6 illegal.	
038E-038F	0	Receive subaddress 7 legal	
0390-03A5	FFFF	Nonbroadcast receive subaddresses 8-18 illegal.	
03A6-03A7	0	Nonbroadcast receive subaddress 19 legal	
03A8-03BB	FFFF	Nonbroadcast subaddresses 1-6 illegal.	
03BC-03BD	0	Receive subaddress 30 legal	
03BE	FFFF	Subaddress 31, non-broadcast receive mode codes. Only Synchronize (with data) is legal.	
03BF	FFFD		
03C0	FE00	Subaddress 0, non-broadcast transmit mode.	
03C1	FFF2	codes. Dynamic bus control, Synchronize (without data), Transmit status word, Initiate self-test, Transmitter shutdown, Override transmitter shutdown, Inhibit terminal flag bit, Override inhibit terminal flag bit, Reset remote terminal, Transmit vector word, Transmit last command, and Transmit BIT word are legal.	
03C2-03C3	0	Nonbroadcast transmit subaddress 1 legal	
03C4-03FB	FFFF	Nonbroadcast transmit subaddresses 2-29 illegal	
03FC-03FD	0	Transmit subaddress 30 legal	
03FE	FE00	Subaddress 31, non-broadcast transmit mode codes. Dynamic bus control, Synchronize (without data), Transmit status word, Initiate self-test, Transmitter shutdown, Override transmitter shutdown, Inhibit terminal flag bit, Override inhibit terminal flag bit, Reset remote terminal, Transmit vector word, Transmit last command, and Transmit BIT word are legal.	
03FF	FFF2		
0400 0401 0402 . . 041F	0000 0001 0002 . . 001F	data words stored ("walking pattern" 0000 to 001F) to be transmitted for transmit subaddress 1.	RT Data Word tables.
0440-045F	----	Reserved for "Block 0" (double buffered) for receive subaddress 19	
0460-047F	----	Reserved for "Block 1" (double buffered) for receive subaddress 19	

Table 133 Memory Map For RT Example Pseudo Code			
Address	**Data**	**Description**	**Portion of Memory, Comment**
0480-049F	----	Reserved for subaddress 30 (data wraparound subaddress) transmit, receive, and broadcast receive data words	
04A0-04BF	----	Reserved for “Block 0” (double buffered) for receive subaddress 19	
04C0-04DF	----	Reserved for “Block 1” (double buffered) for receive subaddress 19	
04E0-04FF	----	Reserved for all unused subaddresses.	
0800-0BFF	----	Reserved for 1024-word circular buffer for receive subaddress 7	
0C00-0FFF	----	Reserved for 1024-word circular buffer for receive subaddress 7	

6.42 Pseudo Code

The following pseudo code is the series of register and memory write transfers required to initiate the Enhanced Mini-ACE RT as described above. The notation "Rxy □"represents a write access to Enhanced Mini-ACE register address xy. The notation "Mwxyz <" represents a write access to Enhanced Mini-ACE shared RAM address wxyz.

R03←0001	Software reset via the Start/Reset Register
R07←8000	Set ENHANCED MODE bit in Configuration Register #3 to enable enhanced RT features (busy by subaddress, enhanced mode code handling, enhanced interrupts, etc.)
R000←0036	Interrupt Mask Register: Enable interrupts for RT CIRCULAR BUFFER ROLLOVER, RT SUBADDRESS CONTROL WORD, FORMAT ERROR, and RT MODE CODE
R02←B803	Configuration Register #2: Enable ENHANCED INTERRUPTS, BUSY LOOKUP TABLE, RECEIVE SUBADDRESS DOUBLE BUFFERING, OVERWRITE INVALID DATA, ENHANCED RT MEMORY MANAGEMENT, and SEPARATE BROADCAST DATA.
R07←801D	Configuration Register #3: Keep ENHANCED MODE enabled. Disable ILLEGAL RECEIVE DATA TRANSFERS and ILLEGAL BUSY DATA TRANSFERS (by programming the respective bits to logic "1"). Enable RTFAIL-RTFLAG WRAP and ENHANCED MODE CODE HANDLING.
R08←2008	Configuration Register #4: Enable MODE CODE OVERRIDE BUSY and LATCH RT ADDRESS WITH CONFIGURATION REGISTER # 5.
R09←000E	Configuration Register #5: EXPANDED ZERO CROSSING, and GAP CHECK. Program RT address to 7 (parity bit = 0)
M0000←0000	Initialize Block Status Word locations in stack to 0000
M00FC←0000	
M0100←0000	Initialize Stack Pointer to top of stack

M0108←0000	Program mode code interrupts
M0109←0002	
M010A←010A	
M010B←0000	
M010C←0000	Program mode code interrupts (continued)
M010D←0000	
M010E←010A	
M010F←0000	
M0111←0000	Reserved for received Data Word for Synchronize (with data) mode code
M0120←1234	Programmed value for vector word (to be transmitted)
M0147←0800	RT Lookup table
M0153←0440	
M0161←0400	
M015E←0480	
M017E←0480	
M0187←0C00	
M0193←04A0	
M019E←4080	
M01A1←4000	RT Subaddress Control Words

M01A7←018C	
M01B3←8210	
M01BE←0000	
M0240←0000	Subaddress Busy Table
M0247←0000	
Pseudo Code (Cont)	
M0300←0000	Command Illegalization Table
M0301←FFFD	
M0302-030D←FFFF	
M030E-030F←0000	
M0310-0325←FFFF	
M0326-0327←0000	
M0328-033B←FFFF	
M033C-033D←0000	
M033E←FFFF	
M033F←FFFD	
M0340←FE05	
M0341←FFFF	
M037E←FE05	

M037F←FFFF	
M0380←FFFF	
M0381←FFFD	
M0382-038D←FFFF	
M038E-038F←0000	
M0390-03A5←FFFF	
M03A6-03A7←0000	
M03A8-03BB←FFFF	
M03BC-03BD←0000	
M03BE←FFFF	
M03BF←FFFD	
M03C0←FE00	
M03C0←FE00	
M03C1←FFF2	
M03C2-03C3←0000	
M03C4-03FB←0000	
M03FC-03FD←0000	
M03FE←FE00	
M03FF←FFF2	
M0400←0000	Data words for transmit subaddress 1
M0401←0001	

M041F←001F	
R01←8F80	Configuration Register #1: Configure Enhanced Mini-ACE for RT mode. Clear DYNAMIC BUS CONTROL, BUSY, SERVICE REQUEST, SUBSYSYTEM FLAG, and RTFLAG RT status Word Bits (by programming the respective bits to logic “1”).

6.43 Servicing Completed RT Messages

The Enhanced Mini-ACE RT provides a number of techniques for determining when a message has been processed. These methods support both polling-driven and interrupt-driven software.

There are several polling methods that may be used which include:

In the ENHANCED mode, the host may continuously poll RT MESSAGE IN PROGRESS, bit 0 of Configuration Register #1. This bit will return logic "0" while the Enhanced Mini-ACE RT is not processing a message. During the time that the Enhanced Mini-ACE RT is servicing a message (after the receipt of a Command Word), RT MESSAGE IN PROGRESS will return logic "1." When the message completes, RT MESSAGE IN PROGRESS will once again return logic "0."

The PROCESSOR can poll the contents of the Stack Pointer RAM location. The active area Stack Pointer increments by four **at the beginning** of each message being processed (after receipt of a Command Word).

If the host needs to determine the occurrence of a **particular** Command Word, it may do so by polling the RT Last Command Register. It should be noted that the contents of this register are updated at the **beginning** of a message being processed. The PROCESSOR may then poll the EOM (End-of-Message) bit of the Interrupt Status Register to determine when the message has been completed. See explanation below.

If the Enhanced Mini-ACE is programmed for the ENHANCED mode **and** ENHANCED INTERRUPTS (bit 15 of Configuration Register #2) are enabled, the PROCESSOR may poll the Interrupt Status Register. In this mode, the various bits in the Interrupt Status Register will become set, **regardless** of the programming of the corresponding bits in the Interrupt Mask register.

In this mode, the Enhanced Mini-ACE may determine that a message has been **completed** by polling the Interrupt Status Register until the EOM (End-of-Message) bit returns logic "1."

In this mode, the host processor may also poll to determine when a message has been processed for a **particular** transmit, receive, or broadcast subaddress. In order to perform this function, ENHANCED RT MEMORY MANAGEMENT (bit 1 of Configuration Register #2) must be invoked. To cause the bit to be set for a particular Tx, Rx or Bcst subaddress, it is then necessary to set the appropriate bit ([TX:, RX:, or BCST:] INT on EOM) in the desired Subaddress Control Word to logic "1." All other Subaddress Control Word ([TX:, RX:, or BCST:] INT on EOM) bits should be programmed to logic "0." This will cause the RT Subaddress CONTROL WORD EOM bit in the Interrupt Status Register to be set to logic "1" after completion of the desired message.

Similarly, the host may poll for receipt of a **particular** mode code message. This feature is enabled by invoking ENHANCED MODE CODE HANDLING (bit 0 of Configuration Register #3). The desired mode code may be selected by setting the

appropriate bit in the Mode Code Selective Interrupt Table (address range 0108-010F). When the specific mode code message has been completed, the RT MODE CODE bit of the Interrupt Status Register will return logic "1."

Similarly, the Interrupt Status Register may be polled to determine the occurrence of FORMAT ERROR, CIRCULAR BUFFER ROLLOVER, 50% CIRCULAR BUFFER ROLLOVER, and/or COMMAND STACK ROLLOVER conditions. FORMAT ERROR indicates any error in a received message, other than an invalid Command Word: sync or Manchester encoding, parity, bit count, word count, or RT-to-RT transfer errors. CIRCULAR BUFFER ROLLOVER may be used to signal completion of a multi-message bulk data transfer. COMMAND STACK ROLLOVER occurs when the Stack rolls over at an address boundary of 256, 512, 1024, or 2048 words, as programmed in Configuration Register #3.

If interrupts are used, the normal procedure would be to **not** invoke ENHANCED INTERRUPTS. This allows the Interrupt Mask Register to be used to enable interrupts and the corresponding Interrupt Status Register bits for only **selected** condition(s), as discussed above.

6.44 RT Error Handling

As discussed above, the preferred method for handling erroneous messages is to make use of the circular buffer and/or double buffering techniques. In the case of the circular buffer mode, the OVERWRITE INVALID DATA bit should be set to logic "1." With these techniques, the Enhanced Mini-ACE RT will automatically overwrite data words received and stored from invalid messages. In most systems, the bus controller will retry failed messages. By so doing, the occurrence of errors and message retries is transparent to the RT's host processor.

If necessary, the RT's host processor may ascertain the occurrence of failed messages by several methods:

Determine, by polling or interrupt techniques, when a FORMAT ERROR condition occurs.

Read the Block Status Words for all messages processed. Bits 12-9 and 6-0 all indicate error conditions in received messages.

6.45 RT Auto-Boot Option

If utilized, the RT pin-programmable auto-boot option allows the Enhanced Mini-ACE RT to automatically initialize as an active remote terminal with the Busy status word bit set to logic “1” immediately following power turn-on. This is a useful feature for MIL-STD-1760 applications, in which the RT is required to be responding within 150 ms after power-up. This feature is available for versions of the Enhanced Mini-ACE with 4K words of RAM.

If UPPADREN is connected to logic “0,” then address line A12 functions as RTBOOT*. If RTBOOT* is connected to logic “0,” the Enhanced Mini-ACE will initialize in RT mode with the Busy status word bit set following power turn-on. If RTBOOT* is hardwired to logic “1,” the Enhanced Mini-ACE will initialize in either Idle Mode (for an RT-only part) or in BC mode (for a BC/RT/MT part).

If RT Auto-boot is enabled, then Configuration Register #1 will be set to 0x8B80 and Configuration Register #3 will be set to 0x8088 following either a hardware or software reset.

6.46 Other RT Features

The Enhanced Mini-ACE includes options for the Terminal flag status word bit to be set either under software control and/or automatically following a failure of the loopback self-test. Other software programmable RT options include software programmable RT status and RT BIT words, automatic clearing of the Service Request bit following receipt of a Transmit vector word mode command, options regarding Data Word transfers for the Busy and Message error (illegal) Status word bits, and options for the handling of 1553A and reserved mode codes.

7 MONITOR OPERATION

The Enhanced Mini-ACE terminals provide three different bus monitor modes: (1) Word Monitor, (2) Selective Message Monitor, (3) combined RT/Selective Message Monitor mode. When the Enhanced Mini-ACE is in Non-Enhanced Mode, the Monitor operates the same as the previous generation product, BUS-61559 Advanced Integrated Mux Hybrid with Enhanced RT features (AIM-HY'er). In ENHANCED MODE, both Selective Message Monitor and Combined RT/Selective Message Monitor modes may be activated. ENHANCED MODE also enables the Monitor triggering capability for the Word Monitor mode.

In Enhanced mode, the Word Monitor provides a programmable Trigger Word. The Trigger Word, which defines a specific Command Word, may be used to start and stop the Monitor or generate an interrupt. You may also start the Word Monitor by means of an external trigger.

The Selective Message Monitor supports message filtering, based on RT Address/T-R* bit/Subaddress, and provides separate Command and Data Stacks. The Message Monitor also stores the contents of the 16-bit Time Tag Register (see Time Tag Register for resolution programming).

The RT/Selective Message Monitor mode provides full RT capability for the Enhanced Mini-ACE terminal's own RT address **PLUS** selective monitoring for all other RT addresses. When using the Enhanced Mini-ACE runtime library some post processing is performed which merges the discrete RT and MT stacks into a combined RT/MT stack that contains all selectively monitored activity on the 1553 data bus. For more information on this operation see the BU-69090 Enhanced Mini-ACE Runtime Library Software Manual. Similar to RT mode, the Selective Monitor's Command Stack stores all command words, Time Tag words, Block Status words, and Data block pointers for each monitored message. The Command and Data Stacks are programmable via bits 12-8 in Configuration Register 3.

Note : *For an RT-RT transfer command where the Enhanced Mini-ACE device is in RT/MT mode and is the* ***receiving*** *RT in the data transfer.*

1.The Monitor does not log any data as the device is busy servicing the receive command. The RT stack has the RT-RT transfer bit set in the Block Status Word of the receiving RT indicating that the received command is part of an RT-RT transfer command initiated by the BC.

Note : *For an RT-RT transfer command where the Enhanced Mini-ACE device is in RT/MT mode and is the* ***transmitting*** *RT in the data transfer.*

2.The Monitor stack contains a command with the block status word set to 0x4000, which indicates a SOM. The RT-RT transfer bit is **not** set in the Block Status Word for this command. The monitor sees this as a transmit command in the command word part of the stack entry. A second entry is placed in the monitor command stack for this one RT-RT

command. This entry has the following bits set in the Block Status Word : EOM, Error Flag, Format Error, Command Word Contents Error and the RT-RT transfer bit is **not** set in the Block Status Word for this command.

7.1 Word Monitor Mode

In Word Monitor Terminal mode, the Enhanced Mini-ACE monitors both 1553 buses. After the software initialization and MONITOR START sequences, the Enhanced Mini-ACE stores all Command, Status, and Data Words received from both buses. For each word received from either bus, **a pair** of words are stored to the Enhanced Mini-ACE's shared RAM. The first word is the 16 bits of data from the received word. The second word is the Monitor Identification (ID), or "Tag" word. The ID Word contains information relating to bus channel, word validity, and interword time gaps. The data and ID words are stored in a circular buffer in the shared RAM address space.

7.2 Word Monitor Memory Map

A typical word monitor memory map is illustrated in Table 134. Table 134 assumes that the full 64K words of shared RAM address space is available for the Enhanced Mini-ACE's monitor. The Active Area Stack pointer provides the address where the first monitored word is stored. In the example, it is assumed that the Active Area Stack Pointer for Area A (location 0100) is initialized to 0000. The first received data word is stored in location 0000, the ID word for the first word is stored in location 0001, etc.

The current Monitor address is maintained by means of an internal counter register. This value may be read by the CPU by means of the Data Stack Address Register. It is important to note that when the counter reaches the Stack Pointer address of 0100 (for active area A) or 0104 (for active area B), the initial pointer value stored in this shared RAM location **will be overwritten** by the monitored data and ID Words. When the internal address counter reaches an address of FFFF (or 0FFF, if only the Enhanced Mini-ACE's 4K of internal RAM is used), the counter rolls over to 0000.

Table 134. Typical Word MT Memory Map

Hex Address	Function
0	First Received 1553 Word
1	First Identification Word
2	Second Received 1553 Word
3	Second Identification Word
4	Third Received 1553 Word
0005..	Third Identification Word..
0100..FFFF	Stack Pointer (Fixed Location)...

To initialize the Enhanced Mini-ACE for Word Monitor mode, the host processor should program bits 15, 14, and 12 of Configuration Register #1 to logic "0," logic "1," and logic "0" respectively. Next, the Stack Pointer for the active area should be loaded with the starting location of the monitor stack in the Enhanced Mini-ACE shared RAM address space. Finally, to start the monitor, a "Start" command should be issued by means of the Start/Reset Register. Note that in ENHANCED MODE, the Word Monitor may also be started via the external trigger (EXT_TRIG) input.

The Monitor ID Word contains a Word Flag bit (always Logic “1”) plus information relating to bus channel, word validity, Command-Status/Data* sync type, and inter-word gap time information. This latter field includes a "Contiguous Data" bit as well as an 8-bit gap time field, indicating 0 to 127 µs with a resolution of 0.5 µs per LSB.

In order to take the Enhanced Mini-ACE monitor off-line, the host CPU must issue a RESET command to the Start/Reset Register.

The Enhanced Mini-ACE Identification Word is defined in Table 135.

Table 135. Word Monitor Identification Word

Bit	Description
15(MSB)	GAP TIME
•	•
•	•
•	•
8	GAP TIME
7	WORD FLAG
6	THIS_RT*
5	BROADCAST*
4	ERROR
3	COMMAND/DATA*
2	CHANNEL B/A*
1	CONTIGUOUS DATA/GAP*
0(LSB)	MODE_CODE*

Gap Time: If the CONTIGUOUS DATA bit is high, these 8 bits are not used. If CONTIGUOUS DATA is low, GAP TIME indicates the time gap between the end of the previous word to the start of the current word in 0.5 us/LSB resolution, up to 127.5 us. For inter-word time gaps greater than 127.5 us, the GAP time field will indicate FF (hex). It should be noted that if the current word was received on the **alternate** bus from the previous word, the GAP TIME field will indicate approximately **20 us greater** than the actual gap time from the word on the first bus. That is, if the current word is received on the alternate bus from the previous word and the current GAP TIME is a time of less than 20 µs, this indicates that the current word **overlapped** the previous word (received on the alternate bus).

Word Flag: Always set to logic "1" for every Identification Word. Each location in the shared RAM where an ID Word is anticipated being stored should be initialized by the CPU to logic "0."

This RT*: If this bit is low, it indicates that the received word was valid, contained a Command/Status sync type, had an RT Address field matching the address on inputs RTAD4-RTAD0 and that correct odd parity was presented on RTADP. This bit will be high otherwise.

Broadcast*: If this bit is low, it indicates that the received word was valid, contained a Command/Status sync type and an RT Address field of 31. This bit will be high otherwise.

Note: *that if the Enhanced Mini-ACE is programmed for ENHANCED MODE and Broadcast has been disabled by programming bit 7 of Configuration Register #5 to logic "1," Broadcast will always return logic "1."*

Error: If this bit is low, it indicates that the received word passed all of the MIL-STD-1553 validation criteria. If this bit is high, it indicates an error in the word: either Manchester II encoding, sync, bit count or parity.

Command/data* Sync: If this bit is high, it indicates the word contained a Command/Status type sync. If this bit is low, it indicates that the word contained a Data type sync.

Channel B/A*: If this bit is low, it indicates that the word was received on Channel A. If the bit is high, it indicates that the word was received on Channel B.

Contiguous Data/Gap*: If this bit is high, it indicates either no gap or less than 2 µs of dead time on the bus from the end of the previous word to the start of the current word. In this case, the GAP TIME field is not used. If this bit is low, it indicates a gap time of more than 2 µs from the end of the previous word to the start of the current word. In this case, the GAP TIME field **does** contain valid bus dead time information.

Mode Code*: If this bit is low, it indicates that the received word was valid, had a Command/Status sync type and contained a subaddress field of either 0 or 31. This bit will be high otherwise. However, if the MONITOR TAG GAP OPTION bit , bit 4 of Configuration Register #4(01000h, Read/Write) is set to logic “1,” the MODE CODE* bit indicates the occurrence of a handshake failure. A hand shake failure occurs in the transparent mode when an external arbitration circuit withholds the data transfer grant signal beyond the specified timeout period. When a timeout occurs, the monitored 1553 word and tag word will be lost and the Enhanced Mini-ACE will assert the MODE CODE* bit in the tag word of the NEXT monitored word to indicate that a timeout occurred and a word was lost. Note that this feature is not implemented in some versions of the ACE family. However, this feature is implemented in all Mini-ACE (Plus) series terminals.

7.3 Word Monitor Initialization

In Word MT mode, the active area stack pointer provides the address where the first monitored word is stored. This pointer must be written by the CPU prior to issuing a MT START command. The data for the first received word will be stored in the location pointed to by the Active Area Stack Pointer.

IMPORTANT NOTE**:** *Both stack pointers (area A and B) will be overwritten by received data or identification words*. *(See Figure 25 and Figure 26)*

7.3.1 Word Monitor Start and Stop

To start the Enhanced Mini-ACE Monitor, write the value 0002 to the Start/Reset Register (BC/MT START). To stop the Monitor from storing further words from the 1553 bus, write the value 0001 to the Start/Reset Register (RESET).

7.3.2 Word Monitor Software Initialization Sequence

1. The software procedure for initializing the Enhanced Mini-ACE in Monitor mode is outlined as follows:

2. Issue a software RESET by writing a value of 0001 to the Start/Reset Register.

3. Initialize the Enhanced Mini-ACE to MT mode with Active Area A (the Active Area selection doesn't matter in MT mode) by writing a value of 5000 to Configuration Register #1.

4. Write the desired location to start storing received words to the Area A Stack Pointer location, 0100.

5. Optionally, clear the area of shared RAM where received data and ID words are anticipated to be received to values of 0000. This allows the host processor to easily determine the location of the last word received by means of the WORD FLAG bit in the ID Word.

6. To initiate the Monitor to start storing received words, write the value 0002 to the Start/Reset Register (BC/MT START).

7. To subsequently cause the Monitor to stop storing received words, write the value 0001 to the Start/Reset Register (RESET).

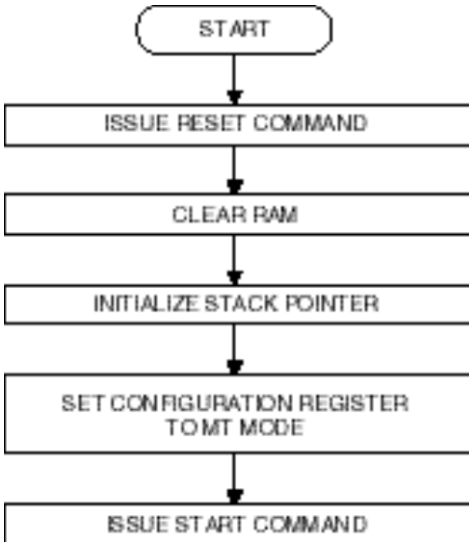


Figure 25. Stack Pointer Area "A"

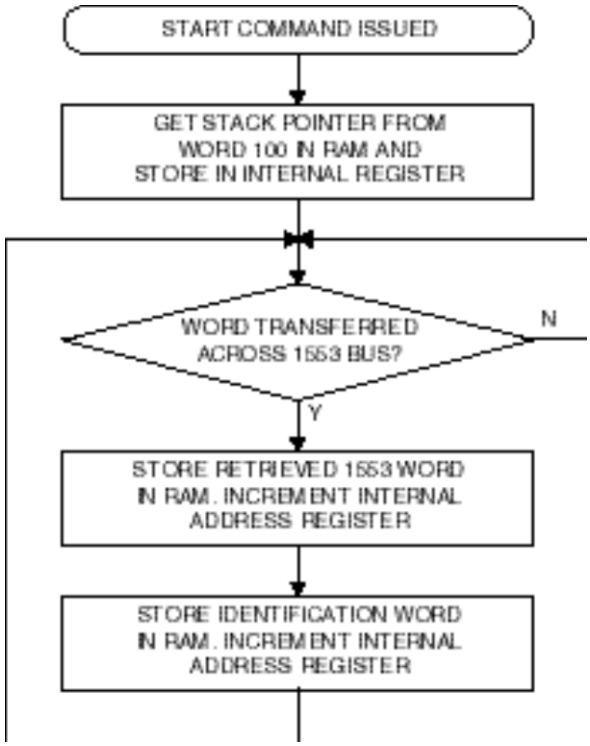


Figure 26. Stack Pointer Area "B"

7.4 Distinguishing Command Words From Status Words : Message Reconstruction

In the Word Monitor mode, message reconstruction entails determining when individual messages received from the 1553 bus begin and end. A critical part of this process, which must be implemented in software (either in real time or off-line), is to distinguish between Command Words and Status Words.

There probably is no universal algorithm for making an absolute "100%" determination between Command and Status Words. This would have to take into account superseding and bus switching command sequences in addition to a multiplicity of message error conditions. However, the rules listed below will prove useful in making the command/status determination for the **vast majority (greater than 99.99%)** of all "real-world" MIL-STD-1553B applications.

1. A word containing a Command/Status sync and any subaddress field (bits 9 (MSB) through 5 (LSB)) other than 0 or 8 is a Command Word.

2. A word with a Command/Status sync preceded by a gap time of longer than the "response timeout" time is a Command Word. For most applications, 14 µs is probably a good starting value for the "response timeout" parameter. For applications entailing very long lengths of bus cable (several hundred feet), a longer period for the "bus timeout" parameter may be required.

3. A word with a Command/Status type of sync received on the alternate bus from the last previous received word may be considered to be a Command Word.

4. Two contiguous (no intervening gap time) words with Command/Status sync types, with the first of the two words preceded by a gap, are the two Command Words for an RT-to-RT transfer or RT-to-Broadcast transfer.

5. A word with a Command/Status sync and a value of 31 (11111) for the RT Address field (bits 15 [MSB] through 11 [LSB]) is a Command Word to the Broadcast address.

6. The next noncontiguous word with a Command/Status sync following a Command Word to the Broadcast address is a Command Word.

7. The principal purpose of the CPU's Monitor software will be to reconstruct the 1553 messages. Once the parsing routine encounters a Command Word, marking the beginning of a new message, it should continue to search through the message, verifying that it conforms to one of the MIL-STD-1553B message formats (reference FIGURE 3 of MIL-STD-1553B). If the "message reconstructor" software is parsing through a received message that is not an RT-to-RT transfer, a word with a Command/Status sync, and a different RT address than the previous word with a command/status sync may be considered to be the Command Word for the next message.

8. If the message reconstructor software is parsing through a stream of Data Words and determines the end of a complete, valid message followed by a gap time (possibly less than the "response timeout" value), the next word with a command/status sync type will be a Command Word. This is regardless of whether the word contains the same RT address or a different RT address than the previous Command/Status word.

7.5 Word Monitor Trigger

In the Word Monitor mode, there is a pattern recognition trigger and a pattern recognition interrupt. The 16-bit compare word for both the trigger and the interrupt is stored in the MT TRIGGER WORD register. The pattern recognition interrupt is enabled by setting the MT PATT TRIG bit (bit 9) in the Interrupt Mask Register. The pattern recognition trigger is enabled by setting the TRIGGER ENABLE bit (bit 11) in Configuration Register #1 and selecting either the START-ON-TRIGGER (bit 10) or the STOP-ON-TRIGGER (bit 9) bit in Configuration Register #1.

Table 136. Word Monitor With Trigger Truth Table (Configuration Register #1 Bits)

Start On Trigger (Bit 10)	Stop On Trigger (Bit 9)	External Trigger (Bit 7)	Word MT Start and Store Operation
0	0	0	Software Start, MT stores all data on the bus.
0	0	1	Software or External Trigger Start, MT stores all data on the BUS
0	1	0	Software Start, MT stores all data until the Command Word matches the word stored in the MT Trigger Register (MTR). This Command Word is the last word stored in the MT Stack.
0	1	1	Software or External Trigger Start stores all data until the Command Word matches the word stored in the MT Trigger Register (MTR). This Command Word is the last word stored in the MT Stack.
1	0	0	Software Start, stores all data after a valid Command Word matches the word stored in the MT Trigger Register (MTR). This Command Word is stored in the MT Stack.
1	0	1	Software or External Trigger Start, stores all data after a valid Command Word matches the word stored in the MT Trigger Register (MTR). This Command Word is stored in the MT Stack.
1	1	0	Software Start, stores ONLY the Command Word that matches the word stored in the MT Trigger Register.
1	1	1	Software or External Trigger Start, stores ONLY the Command Word that matches the word stored in the MT Trigger Register.

Note: The Word Monitor with Trigger truth table above assumes the following:
1. User is in the ENHANCED MODE.
2. Word Monitor is selected in Config Reg #1 (Bit 15=0 14=1 12=0).
3. User programs the "Trigger Word" in the MT Trigger Register.
4. Trig Enable Bit (bit 11 in Config Reg # 1) is set to a Logic “1.”

7.6 Selective Message Monitor Mode

The Enhanced Mini-ACE provides a flexible interface that allows selective monitoring of 1553 messages based on RT Address, T/R, and Subaddress with very little host processor intervention. The Message Monitor mode of the Enhanced Mini-ACE recreates all command/response messages on the 1553 bus on channels A and B, and stores them into the shared RAM based on a user programmable filter (RT Address, T/R, and Subaddress). This monitor can be used as a monitor alone or in a combined RT/Monitor mode. The Message Monitor contains two stacks (a command stack and a data stack) that are independent from the BC/RT command stack. The pointers for these stacks are located in fixed locations in the RAM.

The Message Monitor is enabled in the RT/Monitor mode by setting the ENHANCED MODE bit (bit 15) in Configuration Register bit #3 to a logic "1," RT/BC_L (bit 15) to logic "0," and setting MT (bit 14) and MESSAGE MONITOR ENABLE (bit 12) bits in Configuration Register #1 to logic "1."

It should be noted that an MT START command (setting bit 1 of the START/RESET REGISTER) is **required** to start the Selective Message Monitor in the monitor only mode. However, in the combined RT/Selective Message Monitor mode, an MT START command is **not** required.

7.6.1 Monitor Selection Function

While operating in Selective Message Monitor mode, upon receipt of a valid command, the Enhanced Mini-ACE will reference the selective monitor lookup table (a fixed block of RAM) to determine if this command is enabled. The address for this location is determined by using the RT Address, T/R* bit, and Subaddress bit 4, of the current command, and adding it to the base address 0280(hex) (Figure 27). The bit location within this 16-bit word is determined by subaddress bits 3..0 of the current Command Word.

If the specified bit in the lookup table is logic "0" the command is not enabled and the Enhanced Mini-ACE will abort processing this message and will begin looking for new command words. It should be noted that an RT status word may be interpreted by the Enhanced Mini-ACE as a new command word. If the bit in the monitor look up table is logic "1," the command is enabled and the Enhanced Mini-ACE will create an entry on the monitor command stack (based on the monitor command stack pointer) and store the data associated with this command into sequential locations in the monitor data stack.

The address definition for the Selective Monitor Lookup Table is illustrated in Table 137 .

Table 137. Message Monitor Selection Table Address

Bit	Description
15(MSB)	LOGIC “0”
14	LOGIC “0”
13	LOGIC “0”
12	LOGIC “0”
11	LOGIC “0”
10	LOGIC “0”
9	LOGIC “1”
8	LOGIC “0”
7	LOGIC “1”
6	RTAD_4
5	RTAD_3
4	RTAD_2
3	RTAD_1
2	RTAD_0
1	T/R*
0(LSB)	Subaddress_4

For even-numbered addresses in the Selective Monitor Lookup Table (Subaddress_4 = A0 = 0), bit 15 enables monitoring for subaddress 15, bit 14 enables monitoring for subaddress 14, . . . bit 0 enables subaddress 0. For odd-numbered addresses in the Selective Monitor Lookup Table (Subaddress_4 = A0 = 1), bit 15 enables monitoring for subaddress 31, bit 14 enables monitoring for subaddress 30, . . . bit 0 enables subaddress 16. Programming a bit to logic "0" **disables** monitoring for the respective RT Address-T/R* bit-subaddress; i.e., a message will be ignored. Programming a bit to logic "1" **enables** monitoring for the respective RT Address-T/R* bit-subaddress; that is, the message will be stored.

7.6.2 Message Monitor Formats

The format of the information in the data stack depends on the type of message that was processed. A BC-to-RT command transfer (receive) will store the Command Word in the monitor Command Word stack, the N-Data Words followed by the receiving RT's status response in the monitor data stack.

IMPORTANT NOTE: If the Enhanced Mini-ACE selects the **receive** command in a RT-to-RT transfer, the RT-RT TRANSFER FORMAT bit (bit 11) of the Block Status Word will be set regardless of whether the transmit command was selected. In the case where the Enhanced Mini-ACE selects only the transmit Command Word in an RT-to-RT transfer, the first word stored in the monitor data stack entry will be the second (transmit) Command Word, followed by Txstatus, data and Rx status, i.e., the Enhanced Mini-ACE will ignore the receive command word and status word.

Reading a monitored message from the Enhanced Mini-ACE, requires the use of:

1. The Block Status Word to determine if the message was an RT-to-RT transfer.

2. The Command Word to determine the message format (transmit, receive, mode code, broadcast, etc) and word count.

3. The data pointer to the data block entry. Refer to Figure 27 or a complete listing of all message monitor data stack message formats.

BC-to-RT Transfer (Receive)		**RT-to-BC Transfer (Transmit)**		**RT-to-RT Transfer**
Data Word #1		Status Received		Transmit Command
Data Word #2		Data Word #1		Transmit RT Status
•		Data Word #2		Data Word #1
•		•		Data Word #2
•		•		•
Last Data Word		•		•
Status Received		Last Data Word		•
				Last Data Word
		Mode Command Without Data		Receive RT Status
		Status Word		
RT-to-RT Broadcast		**Broadcast**		**Rx Mode Code With Data**
Transmit Command		Data Word #1		Data Word
Transmit RT Status		Data Word #2		Status Received
Data Word #1		•		
Data Word #2		•		
•		•		
•		Last Data Word		
•				
Last Data Word				
		Broadcast Mode Code With Data		Tx Mode Code With Data
		Data Word		Status Received
				Data Word

Figure 27. Selective Monitor Data Block Formats

A typical memory map for the Enhanced Mini-ACE in the Selective Message Monitor mode is illustrated in Table 138. This mode of operation defines several fixed locations in the RAM. These locations are allocated in a manner in which none of them overlap with the reserved RT locations. This allows for a combined RT/Selective Message Monitor mode. Refer to Table 139 for an example of a typical RT/Selective Message Monitor Memory Map.

The fixed memory map consists of two Monitor Command Stack Pointers (locations 102 and 106 hex), two Monitor Data Stack Pointers (locations 103 and 107 hex), and a Selective Message Monitor Lookup Table (locations 0280 through 02FF hex) based on RT Address, T/R*, and subaddress. The Monitor Command Stack size is assumed to be 1K words, and the Monitor Data Stack size is assumed to be 2K words.

Table 138. Typical Selective Message Monitor Memory Map (shown for 4K RAM for "Monitor Only" Mode.)	
Address (Hex)	**Description**
0101	Not Used
102	Monitor Command Stack Pointer A (fixed location)
103	Monitor Data Stack Pointer A (fixed location)
104.105	Not Used
106	Monitor Command Stack Pointer B (fixed location)
107	Monitor Data Stack Pointer B (fixed location)
0108-027F	Not Used
0280-02FF	Selective Monitor Lookup Table (fixed area)
0300-03FF	Not Used
0400-07FF	Monitor Command Stack A
0800-0FFF	Monitor Data Stack A

NOTE: Stack B is not used in this example

Table 139. Typical RT/Selective Message Monitor Memory Map (shown for 64K RAM for combined RT/MT mode)	
Address (Hex)	**Description**
0000-00FF	RT Command Stack A (256 words)
100	RT Command Stack Pointer A (fixed location)
101	RESERVED
102	Monitor Command Stack Pointer A (fixed location)
103	Monitor Data Stack Pointer A (fixed location)
104	Stack Pointer B (fixed location)
105	RESERVED
106	Monitor Command Stack Pointer B (fixed location)
107	Monitor Data Stack Pointer B (fixed location)
0108-010F	Mode Code Selective Interrupt Table (fixed area)
0110-013F	Mode Code data (fixed area)
0140-01BF	Lookup Table A (fixed area)
01C0-023F	Lookup Table B (fixed area)
240.0247	Busy Bit Lookup Table (fixed area)
0248-025F	(not used)
0260-027F	RT Data Block 0
0280-02FF	Selective Monitor Lookup Table (fixed area)
0300-03FF	Command Illegalizing Table (fixed area)
0400-07FF	Monitor Command Stack A (1024 words)
0800-081F	RT Data Block 0
0820-083F	RT Data Block 1
•	•
7FE0-7FFF	RT Data Block 959
8000-FFFF	Monitor Data Stack (32,768 words)

The size of the monitor command stack is programmable to 256, 1K, 4K, or 16K by bits 11 and 12 of Configuration Register #3. The Monitor Data Stack size is programmable to 512, 1K, 2K, 4K, 8K, 16K, 32K or 64K by use of bits 8 through 10 in Configuration Register #3. Refer to Figure 28 for an illustration of the Selective Message Monitor operation. Upon receipt of a valid Command Word, the Enhanced

Mini-ACE will reference the Selective Monitor Lookup Table (a fixed block of addresses) to determine if the current command is enabled. If the current command is disabled, the Enhanced Mini-ACE will ignore (and not store) the current message.

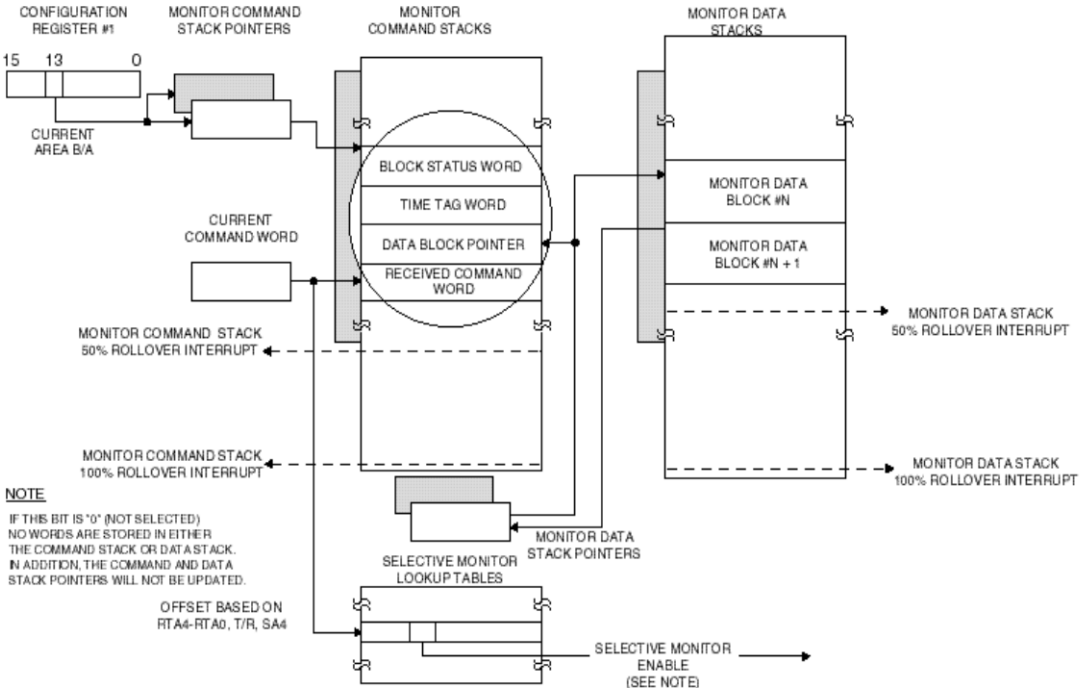


Figure 28. Selective Message Monitor Operation

If the command is enabled, the Enhanced Mini-ACE will create an entry in the Monitor Command Stack at the address location referenced by the Monitor Command Stack Pointer.

As indicated in Figure 28, the host may utilize the 50% and 100% stack rollover interrupts. These are done when the command stack pointer and/or the data stack pointer cross the 50% and/or 100% “rollover” points. Note that the “rollover” addresses are based on modulo (0.5* stack size) or modulo (stack size), and **not** on the starting (initialized) values for the two stack pointers.

7.7 Message Monitor Block Status Word

The bit map and bit descriptions for the Message Monitor Block Status Word are indicated on the following page.

Table 140. Selective Message Monitor Mode Block Status Word	
BIT	**DESCRIPTION**
15(MSB)	EOM
14	SOM
13	CHANNEL B/A*
12	ERROR FLAG
11	RT-RT TRANSFER
10	FORMAT ERROR
9	NO RESPONSE TIMEOUT
8	GOOD DATA BLOCK TRANSFER
7	DATA STACK ROLLOVER
6	RESERVED (logic “0”)
5	WORD COUNT ERROR
4	INCORRECT DATA SYNC
3	INVALID WORD
2	RT-RT GAP/SYNC/ADDRESS ERROR
1	RT-RT- 2ND COMMAND ERROR
0(LSB)	COMMAND WORD CONTENTS ERROR

END-OF-MESSAGE (EOM)(bit 15): Set at the completion of a monitored message, regardless of whether or not there were any errors in the message.

START-OF-MESSAGE (SOM)(bit 14): Set approximately 3-4 µs following the receipt (mid-parity bit) of the Command Word and cleared at the end of the message.

CHANNEL B/A*(bit 13): This bit will be low if the message was monitored from Channel A or high if the message was monitored on Channel B.

ERROR FLAG (bit 12): If this bit is high and bit 10 and/or bit 9 is high, this indicates that either a format error, no response error occurred in the message. If this bit is high, the Enhanced Mini-ACE is configured for its transparent mode of processor interface, and bits 10 and 9 are both logic "0," this indicates that a handshake failure has occurred. A handshake failure occurs when the input signal DTGRT* is either not asserted low or is asserted low too late (later than 4.4µs in 20 MHz mode, 4µs in 16 MHz mode, 3.5µs in 12 MHz mode, or 3.2 µs in 10 MHz) after the time that the output signal DTREQ* is asserted low. Alternatively, a handshake failure will occur if the host CPU fails to clear STRBD* (high) within 4 µs after the Enhanced Mini-ACE has asserted its READYD* output (low). If a handshake failure occurs, a received message should be considered invalid.

RT-to-RT TRANSFER (bit 11): This bit indicates that the message was an RT-to-RT transfer. The receive Command Word must be selected, and is stored in the Monitor Command Stack. The transmit Command Word is stored in the Monitor Data Stack in the location referenced by the Data Block Pointer Word in the Monitor Command Stack.

FORMAT ERROR (bit 10): If set, indicates that a message contained one or more violations of the 1553 message validation criteria (sync, encoding, parity, bit count, word count, etc.).

RESPONSE TIMEOUT (bit 9): If set, indicates that an RT has either not responded or has responded later than the programmed No Response Timeout time. The Enhanced Mini-ACE's No Response Timeout Time is defined per MIL-STD-1553B as the time from the mid-bit crossing of the parity bit to the mid-sync crossing of the RT Status Word. The value of the No Response Timeout value is programmable from among the nominal values (±1 µs) 18.5, 22.5, 50.5, and 130 µs by means of bits 10 and 9 of Configuration Register #5.

GOOD DATA BLOCK TRANSFER (bit 8): Set to logic "1" following completion of a valid (error-free) message, set to logic "0" following completion of an erroneous (invalid) message.

DATA STACK ROLLOVER (bit 7): If DATA STACK ROLLOVER is logic "1," indicates that the current message resulted in the value of the Monitor Data Stack Pointer rolling over, from the bottom to the top of its range. The size of the Monitor Data Stack is programmable from among 512, 1K, 2K, 4K, 8K, 16K, 32K, and 64K words by means of bits 10, 9, and 8 of Configuration Register #3.

WORD COUNT ERROR (bit 5): If set, indicates that either a BC or a responding RT did not transmit with the correct number of Data Words.

INCORRECT SYNC TYPE (bit 4): If set, indicates that a BC transmitted a Data sync with a Command Word or a Command/Status sync with a Data Word, or a responding RT responded with a Data sync in a Status Word and/or a Command/Status sync in a Data Word.

INVALID WORD (bit 3): Indicates a BC transmitted, or an RT responded with one or more words containing one or more of the following error types: sync field error, Manchester encoding error, parity error, and/or bit count error.

RT-to-RT GAP/SYNC/ADDRESS ERROR (bit 2): This bit is set if one or more of the following occur: (1) If the GAP CHECK ENABLED bit (bit 8) of Configuration Register #5 is set to logic "1" **and** the transmitting RT responds with a response time of less than 4 µs, per MIL-STD-1553B (mid-parity bit to mid-sync); i.e., less than 2 µs dead time; and/or (2) A responding RT for an RT-to-RT transfer responds with an invalid Status Word (encoding, bit count, and/or parity error) or a Data Word sync in its Status Word and/or; (3) The RT Address field of the command word does not match the RT address in the RT status response.

RT-to-RT SECOND COMMAND ERROR (bit 1): For an RT-to-RT transfer, this bit set to logic "1" indicates one or more of the following error conditions in the second of two contiguous Command Words: (1) T/R bit = logic "0"; (2) subaddress = 00000 or 11111; (3) The RT Address in the transmit Command Word is the same as the RT Address in the receive Command Word.

COMMAND WORD CONTENTS ERROR (bit 0): Indicates that a received Command Word is not defined in accordance with MIL-STD-1553B. This includes the following undefined Command Words: (1) BROADCAST DISABLED, bit 7 of Configuration Register #5 is logic "0" **and** the Command Word is a non-mode code, broadcast, transmit command; (2) The OVERRIDE MODE T/R* ERROR bit, bit 6 of Configuration Register #3, is logic "0" **and** a message with a the Command Word had

a T/R* bit of "0," a subaddress/mode field of 00000 or 11111 and a mode code field between 00000 and 01111; (3) BROADCAST DISABLED, bit 7 of Configuration Register #5 is logic "0" **and** the Command Word is a broadcast command of

a mode code that is not permitted to be broadcast to the broadcast address (11111).

Monitor Interrupts. Selective monitor interrupts may be issued for End-of-message and for conditions relating to the monitor command stack pointer and monitor data stack pointer. The latter, which are shown in Figure 9, include Command Stack 50% Rollover, Command Stack 100% Rollover, Data Stack 50% Rollover, and Data Stack 100% Rollover.

The 50% rollover interrupts may be used to inform the host processor when the command stack or data stack is half full. At that time, the host may proceed to read the received messages in the upper half of the respective stack, while the Enhanced Mini-ACE monitor writes messages to the lower half of the stack. Later, when the monitor issues a 100% stack rollover interrupt, the host can proceed to read the received data from the lower half of the stack, while the Enhanced Mini-ACE monitor continues to write received data words to the upper half of the stack.

7.8 Interrupt Status Queue

Like the Enhanced Mini-ACE RT, the Selective Monitor and combined RT/Selective Monitor modes include the capability for generating an interrupt status queue. As illustrated in Figure 29 this provides a chronological history of interrupt generating conditions and events.

In addition to the Interrupt Mask Register, the Interrupt Status Queue provides additional filtering capability, such that only valid messages and/or only invalid messages may result in the creation of an entry to the Interrupt Status Queue. Queue entries for invalid and/or valid messages may be individually disabled by means of bits 8 and 7 of Configuration Register #6. The interrupt status queue is 64 words deep, providing the capability to store entries for up to 32 monitored messages.

The pointer to the Interrupt Status Queue is stored in the INTERRUPT VECTOR QUEUE POINTER REGISTER (register address 1F). This register must be initialized by the host, and is subsequently incremented by the RT message processor. The interrupt status queue is 64 words deep, providing the capability to store entries for up to 32 messages.

The queue rolls over at addresses of modulo 64. The events that result in queue entries include both message-related and non-message related events. Note that the Interrupt Vector Queue Pointer Register will always point to the next location (modulo 64) **following** the last vector/pointer pair written by the Enhanced Mini-ACE RT, Monitor, or RT/Monitor.

Each event that causes an interrupt results in a two-word entry to be written to the queue. The first word of the entry is the interrupt vector. The vector indicates which interrupt event(s)/condition(s) caused the interrupt.

The interrupt events are classified into two categories: message interrupt events and non-message interrupt events. Message-based interrupt events include End-of-Message, Selected mode code, Format error, Subaddress control word interrupt, RT Circular buffer Rollover, Handshake failure, RT Command stack rollover, transmitter timeout, MT data stack rollover, MT command stack rollover, RT Command stack 50% rollover, MT data stack 50% rollover, MT command stack 50% rollover, and RT

Circular buffer 50% rollover. Non-message interrupt events/conditions include time tag rollover, RT address parity error, RAM parity error, and BIT completed.

Bit 0 of the interrupt vector (interrupt status) word indicates whether the entry is for a message interrupt event (if bit 0 is logic "1") or a non-message interrupt event (if bit 0 is logic "0"). It is **not** possible for one entry on the queue to indicate both a message interrupt and a non-message interrupt.

For a message interrupt event, the parameter word is a pointer. The pointer will reference the first word of the RT or MT command stack descriptor (i.e., the Block Status Word).

For a RAM Parity Error non-message interrupt, the parameter will be the RAM address where the parity check failed. For the RT address Parity Error, Protocol Self-test Complete, and Time Tag Rollover non-message interrupts, the parameter is not used; it will have a value of 0000.

If enabled, an INTERRUPT STATUS QUEUE ROLLOVER interrupt will be issued when the value of the queue pointer address rolls over at a 64-word address boundary.

Table 141 defines the RT/Monitor Interrupt status word for message and non-message interrupt events. Detailed bit descriptions are listed following the table.

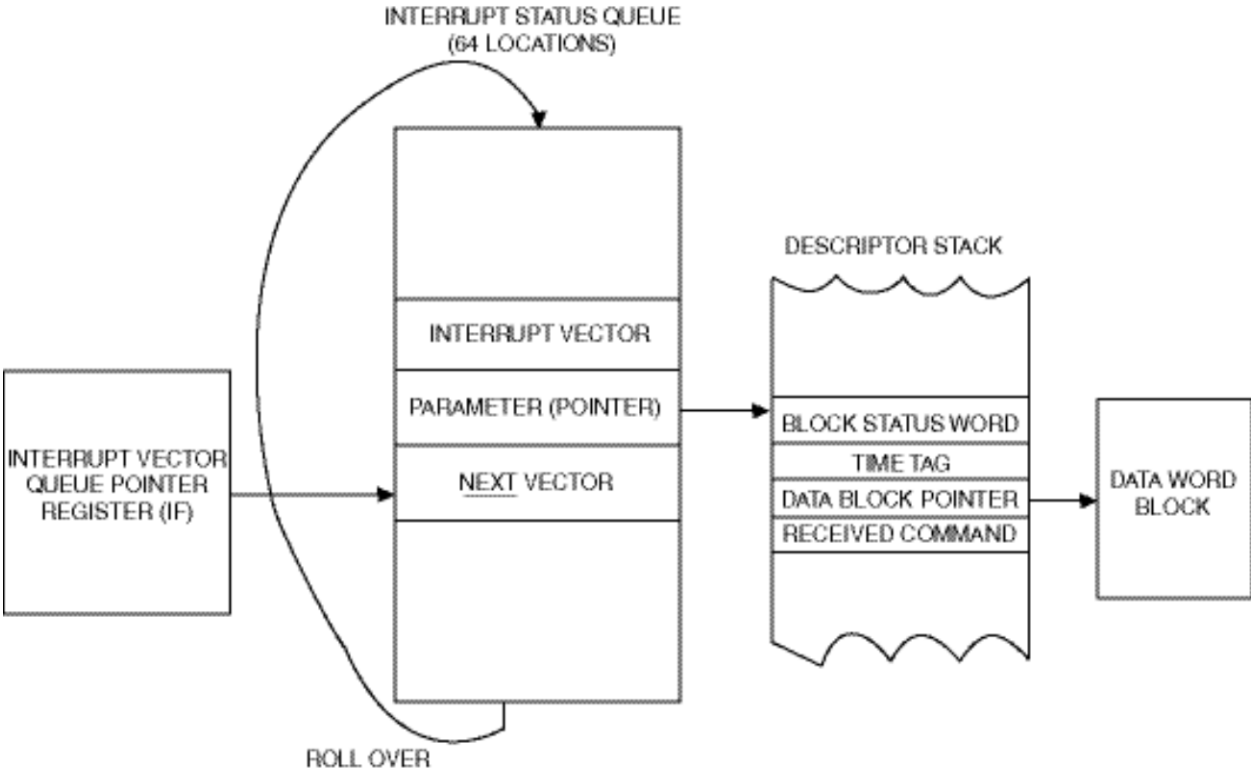


Figure 29. RT (and Monitor) Interrupt Status Queue (shown message interrupt event)

Table 141. RT/Monitor Interrupt Status Word (for interrupt status queue)		
Bit	**Definition For Message Interrupt Event**	**Definition For Non-Message Interrupt Event**
15	TRANSMITTER TIMEOUT	NOT USED
14	ILLEGAL COMMAND	NOT USED
13	MONITOR DATA STACK 50% ROLLOVER	NOT USED
12	MONITOR DATA STACK ROLLOVER	NOT USED
11	RT CIRCULAR BUFFER 50% ROLLOVER	NOT USED
10	RT CIRCULAR BUFFER ROLLOVER	NOT USED
9	MONITOR COMMAND (DESCRIPTOR) STACK 50% ROLLOVER	NOT USED
8	MONITOR COMMAND (DESCRIPTOR) STACK ROLLOVER	NOT USED
7	RT COMMAND (DESCRIPTOR) STACK 50% ROLLOVER	NOT USED
6	RT COMMAND (DESCRIPTOR) STACK ROLLOVER	NOT USED
5	HANDSHAKE FAIL	NOT USED
4	FORMAT ERROR	TIME TAG ROLLOVER
3	MODE CODE INTERRUPT	RT ADDRESS PARITY ERROR
2	SUBADDRESS CONTROL WORD EOM	PROTOCOL SELF-TEST COMPLETE
1	END-OF-MESSAGE (EOM)	RAM PARITY ERROR
0	“1” FOR MESSAGE INTERRUPT EVENT; “0” FOR NON-MESSAGE INTERRUPT EVENT	

7.8.1 Message INTERRUPT EVENT BIT DESCRIPTIONS

RT TRANSMITTER TIMEOUT (bit 15): Applicable only in the ENHANCED mode (ENHANCED MODE ENABLE, bit 15 of Configuration Register #3 set to logic "1") and ENHANCED INTERRUPTS ENABLED (bit 15 of Configuration Register #2 set to logic "1"). If this bit is set to logic "1," this indicates that the Enhanced Mini-ACE's transmitter watchdog timer has timed out. This occurs if the Enhanced Mini-ACE's encoder attempts to transmit for longer than 660.5 µs.

MONITOR DATA STACK 50% ROLLOVER (bit 13): For Selective Monitor mode, this bit indicates that the Monitor data stack pointer has crossed an address boundary which is an exact multiple of half of the programmed value of the Monitor Data Stack size. If the data stack pointer was initialized at an address which is an exact multiple of its programmed size, then this interrupt will indicate that the data stack is half full. Note that this interrupt will occur at the end of the message in which the 50% rollover occurred.

MONITOR DATA STACK ROLLOVER (bit 12): Applicable only in the ENHANCED mode (ENHANCED MODE ENABLE, bit 15 of Configuration Register #3 set to logic "1") and ENHANCED INTERRUPTS ENABLED (bit 15 of Configuration Register #2 set to logic "1"). If this bit returns a value of logic "1," it indicates a rollover of the Word Monitor or Message Monitor Data Stack. The size of the Data Stack is programmable from among 512, 1024, 2048, 4096, 8192, 16,384, 32,768, or 65,536 words by means of bits 10, 9, and 8 of Configuration Register #3.

RT CIRCULAR BUFFER 50% ROLLOVER (bit 11): For RT mode, this bit indicates that an RT circular buffer (either for an individual transmit, receive(/broadcast), or broadcast subaddress, or the global circular buffer) has crossed an address boundary which is an exact multiple of half of the programmed value of the circular buffer size. If the circular buffer lookup table pointer was initialized at an address which is an exact multiple of its programmed size, then this interrupt will indicate that the stack is half full. Note that this interrupt will occur at the end of the message in which the 50% rollover occurred.

RT CIRCULAR BUFFER ROLLOVER (bit 10) : This bit will be set at the end of a message in RT mode, provided that the Enhanced Mini-ACE is in the ENHANCED RT Memory Management mode (bit 2 of Configuration Register #2 = logic “1”) and the "Interrupt at Rollover" bit is set in the Subaddress Control Word for the Tx/Rx/Bcst subaddress of the just completed message and the current message caused the data block Lookup Table address pointer to cross the lower boundary of the respective circular buffer, resulting in a rollover. This interrupt is applicable for rollovers of either a subaddress-specific circular buffer, or the global circular buffer.

Note that if OVERWRITE INVALID DATA (bit 11 of Configuration Register #2) is logic "0, "this interrupt request will occur immediately when the address location at the upper boundary of a circular buffer is accessed. If OVERWRITE INVALID DATA is logic "1," the interrupt request will occur at the end of a valid message in which the last location in the circular buffer was accessed. If OVERWRITE INVALID DATA is logic "1," an RT CIRCULAR BUFFER ROLLOVER will not occur following an invalid received message

MONITOR COMMAND STACK 50% ROLLOVER (bit 9): For Selective Monitor mode, this bit indicates that the Monitor descriptor stack (command stack) pointer has crossed an address boundary which is an exact multiple of half of the programmed value of the Monitor Command Stack size. If the command stack pointer was initialized at an address that is an exact multiple of its programmed size, then this interrupt will indicate that the command stack is half full. The timing for this interrupt request depends on the programming of COMMAND STACK POINTER INCREMENT ON EOM, bit 13 of Configuration Register #6. If COMMAND STACK POINTER INCREMENT ON EOM is logic "0" (default), then the command stack 50% rollover interrupt will occur during the SOM (start-of-message) sequence for the message in which the 50% rollover occurred. This happens following receipt of the command word. However, if COMMAND STACK POINTER INCREMENT ON EOM has been programmed to logic "1,” then the command stack 50% rollover interrupt will occur at the end of the EOM (END-of-message) sequence, for the message in which the value of the stack pointer incremented past the 50% point of the command stack. The “50% rollover” address will be an exact multiple of half of the programmed stack size.

MT COMMAND STACK ROLLOVER (bit 8): Applicable only in the ENHANCED mode (ENHANCED MODE ENABLE, bit 15 of Configuration Register #3 set to logic "1") and ENHANCED INTERRUPTS ENABLED (bit 15 of Configuration Register #2 set to logic "1"). If this bit returns a value of logic "1," it indicates an interrupt following a rollover of the Message Monitor Command Stack. This is applicable for both the Message Monitor as well as the combined RT/Message Monitor modes. The size of the MT Command Stack is programmable from among 256 (64 messages), 1024, 4096, and 16,384 words (4096 messages) by means of bits 12 and 11 of Configuration Register #3.

RT COMMAND STACK 50% ROLLOVER (bit 7): For RT mode, this bit indicates that the RT descriptor stack (command stack) pointer has crossed an address boundary which is an exact multiple of half of the programmed value of the Command Stack size. If the stack pointer was initialized at an address that is an exact multiple of its programmed size, then this interrupt will indicate that the stack is half full.

The timing for this interrupt request depends on the programming of COMMAND STACK POINTER INCREMENT ON EOM, bit 13 of Configuration Register #6. If COMMAND STACK POINTER INCREMENT ON EOM is logic "0" (default), then the command stack 50% rollover interrupt will occur during the SOM (start-of-message) sequence for the message in which the 50% rollover occurred, which occurs following receipt of the command word. However, if COMMAND STACK POINTER INCREMENT ON EOM has been programmed to logic "1," then the command stack 50% rollover interrupt will occur at the end of the EOM (END-of-message) sequence, for the message in which the value of the stack pointer incremented past the 50% point of the command stack. The “50% rollover” address will be an exact multiple of half of the programmed stack size.

RT COMMAND STACK ROLLOVER (bit 6): If this bit returns a value of logic "1," it indicates a rollover of the BC/RT Command Stack. The size of the BC/RT Command Stack 1 is programmable from among 256 words (64 messages), 512, 1024, and 2048 words (512 messages) by means of bits 14 and 13 of Configuration Register #3.

HANDSHAKE FAILURE (bit 5): This bit indicates an interrupt has occurred following a handshake timeout during a transfer between the 1553 protocol section and the RAM. A Handshake Failure can only occur in the transparent configuration of the Enhanced Mini-ACE host interface. There are two conditions that can cause a Handshake Failure. For both conditions, the maximum allotted time is 10.5 μs for a 20 MHz clock input, 10.0 μs for a 16 MHz clock input, 9.0 μs for a 12 MHz clock input, and 8.5 μs for a 10 MHz clock input:

Condition 1 occurs when the Data Transfer Grant (DTGRT*) input is not asserted within the allotted time after the Enhanced Mini-ACE's Data Transfer Request (DTREQ*) output has been asserted.

Condition 2 occurs when the STRBD* input signal is held low too long at the end of a processor transfer cycle (as indicated by the falling edge of READYD*).

Note : STRBD* asserted low for too long will **not** result in a HANDSHAKE-FAILURE condition in the buffered mode configuration.

FORMAT ERROR (bit 4): *Indicates that a completed message contained one or more of the following errors:*

Loop Test Failure: A loopback test is performed on all messages transmitted by the RT (except broadcast messages in RT mode). The received version of all transmitted words is checked for validity and correct sync type. In addition, a 16-bit comparison is performed on the last word transmitted by the RT. If any of these checks or comparisons do not verify, the loopback test is considered to have failed. Loop Test Failure is not applicable in Monitor mode.

Message Error: A received message contained a violation of the 1553 message validation criteria (encoding, parity, bit count, word count, etc.).

Response Timeout: In RT mode, if the Enhanced Mini-ACE is the receiving RT in an RT-to-RT transfer and the transmitting RT has not responded with its Status Word within the programmed value of the RT-to-RT Response Timeout time after the Transmit Command Word.

RT Mode Code Interrupt (bit 3): This interrupt can only occur in the ENHANCED mode and if Enhanced Mode Code Handling is enabled (bit 0 of Configuration Register #3 is set to logic “1”). If these two bits are set, mode code interrupts for individual broadcast- T/R bit mode codes may be enabled by setting the appropriate bit(s) in address location 0108-010F in the shared RAM. Reception of an enabled mode code message will then cause a MODE CODE interrupt at the end of the message.

RT Subaddress CONTROL WORD EOM (bit 2): For RT mode, if this bit is set and the Enhanced Mini-ACE is in the Enhanced Memory Management RT mode and the "Interrupt at EOM" bit is set in the Subaddress Control Word for the respective Transmit, Receive or Broadcast subaddress, an interrupt will occur at the end of the current message.

END OF MESSAGE (EOM) (bit 1): Indicates the completion of the message (regardless of validity)

NON-MESSAGE INTERRUPT EVENT BITS

TIME TAG ROLLOVER (bit 4): If set, enables an interrupt if the 16-bit Time Tag Register rolls over from FFFF to 0000.

RT ADDRESS PARITY ERROR (bit 3): Indicates that the parity sum of the internal RTAD4-RTAD0 and RTADP signals is even, rather than odd, as required for the Enhanced Mini-ACE to respond to messages directed to its own RT address in RT mode. If the input signal RT_AD_LAT is connected to logic “0,” or if RT_AD_LAT is connected to logic “1” and RT ADDRESS SOURCE (bit 5 of Configuration Register #6) has been programmed to logic “0,” then the internal RTAD4-RTAD0 and RTADP logic levels are derived directly from the RTAD4-RTAD0 and RTADP input signals.

However, if the input signal RT_AD_LAT is connected to logic “1” and RT ADDRESS SOURCE (bit 5 of Configuration Register #6) has been programmed to logic “1,” then the internal RTAD4-RTAD0 and RTADP logic levels are programmed by the host processor by means of Configuration Register #5.

It should be noted that if an RT ADDRESS PARITY ERROR condition occurs, the respective Interrupt Status Register bit will clear to logic "0" after the Interrupt Status Register has been read (if AUTO CLEAR is enabled) or after INTERRUPT RESET, bit 2 of the Start/Reset Register, has been written as logic "1." The RT ADDRESS PARITY ERROR bit will remain at logic "0" and will not return to logic "1" until either of the following two sequences has occurred: (1) the RT Address parity error condition goes away and then re-occurs, or (2) the RT ADDRESS PARITY ERROR bit in Interrupt Mask Register #1 is cleared (either by writing "0" to the register bit or by means of either a hardware or software reset to the Enhanced Mini-ACE) and is then set back to logic "1," assuming that the address parity error condition persists.

BIT TEST COMPLETE (bit 2): This bit indicates that the protocol built-in self-test or the RAM built-in self-test has been completed. The result of the test may be determined by reading the BIT Test Status Register.

RAM PARITY ERROR (bit 1): Applicable only in the ENHANCED mode (ENHANCED MODE ENABLE, bit 15 of Configuration Register #3 set to logic "1") and ENHANCED INTERRUPTS ENABLED (bit 15 of Configuration Register #2 set to logic "1"). If set to logic "1," this indicates a RAM parity error. This bit is only applicable for the 64K X 17 RAM versions of Enhanced Mini-ACE. It is not applicable for the 4K X 16 RAM versions. By programming RAM PARITY ENABLE, bit 14 of Configuration Register #2 to logic "1," the 64K X 17 RAM versions of the Enhanced Mini-ACE can be programmed to generate a parity bit on all write accesses to 17-bit RAM. A parity check is then performed on all read accesses to the 17-bit RAM. A RAM PARITY ERROR interrupt indicates a failure of this parity check.

The RAM address where the parity error was detected is stored on the Interrupt Status Queue.

7.9 Superceding Commands

A superseded message sequence occurs when a valid message begins on one bus, followed by a time gap, followed by a new command on the alternate bus. If both the old and the new command are to the same RT Address, the RT **must** stop processing the first command, and begin processing the new command. If the commands are to different RT Addresses, the terminal responding to the first command **must** complete processing the message and ignore the activity on the alternate bus.

The Enhanced Mini-ACE selective message monitor will abort processing the first message and begin processing the new message. The only exception to this is when the Enhanced Mini-ACE is operating in the combined RT/Selective Message and the first command is to the Enhanced Mini-ACE's RT Address **and** the second command is to different, nonbroadcast, RT Address. As an RT, the Enhanced Mini-ACE must continue processing the first command (in compliance with MIL-STD-1553), and ignore the new command to a different terminal on the alternate bus.

The Enhanced Mini-ACE selective message monitor will supersede a message on the same bus except when the superseding command may be interpreted as a status word. Hence, a RT status response with the wrong RT address in the status word will NOT appear to the Enhanced Mini-ACE selective message monitor as a new command, but rather will appear to be a bad status word.

When a message is superseded, a normal Start Of Message (SOM) sequence is performed on the new (superseding) message. Note that an End Of Message (EOM) sequence is NOT executed on the original (superseded) message. This will result in a command stack entry with the Start Of Message (SOM) bit in the block status word set to logic "1" and the End Of Message (EOM) bit set to logic "0."

The host processor can distinguish between a message in progress and a superseded message by the value of the monitor command stack pointer. If the monitor command stack pointer has incremented beyond the command stack entry in question and the block status word indicates an SOM state, then the message must have been superseded.

7.10 Selective Message Monitor SOM and EOM Transfer Sequences

Approximately 1.25 µs following the mid-parity bit crossing of a received Command Word, the Enhanced Mini-ACE performs the Selective Monitor Start-of-Message (SOM) sequence. After the first two steps of the SOM sequence, the Enhanced Mini-ACE determines if the message is "selected" (to be stored); this is a function of the RT address, T/R bit, and Subaddress fields of the received Command Word. Approximately 6 µs after the end of the last word received for a selected message, the Enhanced Mini-ACE performs the MT End-of-Message (EOM) Sequence. The MT SOM and EOM sequences consist of sequences of words read from and written to the ACE's shared RAM. The Monitor SOM and EOM sequences are summarized below:

7.10.1 MT Start-of-Message (SOM) Sequence

1. Corresponding to the RT address, T/R* bit, and subaddress of the received Command Word, the appropriate Monitor Selection word is read from the Monitor Selection table.

2. The Monitor Command Stack Pointer is read from the active area Monitor Command Stack Pointer location. This address is used to locate the first word of message's block descriptor in the Monitor Command Stack. If the result of step 1 indicated that the message is "selected" (to be stored), continue to step 3. If the message is not "selected," the SOM sequence is terminated.

3. The Monitor Data Stack Pointer is read from the active area Monitor Data Stack Pointer location (either memory location 103h or 107h, depending upon the state of the CURRENT AREA B/A* bit in configuration register #1).

4. The Command Word is written to the fourth location in the current descriptor block.

5. The Data Stack Pointer is written to the third word of the current descriptor block. This value is used for locating the first location for the current message in the Monitor Data Stack.

6. The Time Tag word is written to the second location in the current descriptor block.

7. The Block Status Word is written to the first location in the current descriptor block.

8. The value of the Command Stack Pointer read in step 2 is incremented by four and written to the active area Stack Pointer.

7.10.2 MT End-of-Message (EOM) Sequence

1. The address of the last word stored in the Data Stack is incremented by one (modulo the Data Stack size) and written to the active area Data Stack Pointer location.

2. The Time Tag word is written to the second location in the block descriptor.

3. The Block Status Word is written to the first location in the block descriptor. Selective Message Monitor Programming Sequence (assuming 4K RAM using End-of-Message (EOM) interrupt)

7.10.3 Initialization

1. Write 0001h to START/RESET Register to reset the device.

2. Write 8000h to CONFIGURATION REGISTER #3 to enable ENHANCED MODE features.

3. Write 8D00h to CONFIGURATION REGISTER #3 to configure the device for ENHANCED MODE enabled, a 1K Monitor Command Stack size and a 2K Monitor Data Stack size.

4. Write 5000h to CONFIGURATION REGISTER #1 to place the device in the Selective Message Monitor mode.

5. Write 0400h to RAM location 0102h to initialize the Monitor Command Stack Pointer.

6. Write 0800h to RAM location 0103h to initialize the Monitor Data Stack Pointer.

7. Initialize the Selective Monitor Lookup Table in RAM locations 0280h to 02FFh. Note that programming FFFFh in all 128 locations will program the Enhanced Mini-ACE to monitor ALL commands.

8. Write 0010h to CONFIGURATION REGISTER #2 to enable interrupt auto clear function.

9. Write 0001h to INTERRUPT MASK register to enable End Of Message (EOM interrupt.

10. Initialize the software variable stkptr to 0400h. This will act as an indicator of the next message that is to be serviced.

Write 0002h to START/RESET register to start the monitor.

Note : The order in which steps 3-10 are executed does not matter. This example is for a 1K-monitor command stack and a 2K-monitor data stack. If larger stack sizes are used, the initial stack pointer values written to RAM locations 102h and 103h have to be left shifted to compensate for the larger stack pointer counter width. As the stack pointers increment the lower bits are overwritten by the actual counters and the upper bits remain in the initial values written 102h and 103h.

In the previous example, the 10-bit counter selected via configuration register #3 determines the 1K-monitor command stack. The counter will not overwrite the base of the initial command stack pointer because the set bits of the base (0400h) start at bit 11. If the monitor command stack size were increased to 2K via configuration register #3, the initial command stack pointer would have to be adjusted. For example, writing 0800h to the RAM location 0102h would prevent the 2K-stack pointer counter (now 11-bits wide) from overwriting the 0800h base (bit 12-set) when the counter wraps around. In, addition, the base of the monitor data stack would have to be adjusted accordingly and the actual amount of RAM in the part would have to be considered.

7.10.4 Servicing Technique

Define an Interrupt Service Routine that will do the following

1. Read and save value of INTERRUPT STATUS register.

2. Verify that Interrupt Status is 0001h (EOM occurred).

3. Read and store value of RAM location 0102h (Monitor Command Stack Pointer). This value will be referred to as MTCMDPTR.

4. Repeat the following sequence until (stkptr = MTCMDPTR) or [(((stkptr + 4) mod stack size) = MTCMDPTR) and (Block status word has som set)]:

- Block Status Word = RAM location stkptr.

- Time Tag = RAM location stkptr + 1.

- Data pointer = RAM location stkptr + 2.

- Command Word = RAM location stkptr + 3.

- Status and Data words are stored sequentially in RAM locations starting at the value of data pointer, the number of words and message format is determined by reading bit 11 of the Block Status Word and the contents of the Command Word. If bit 11 of the Block Status Word is logic "1," the message was an RT-to-RT transfer. In addition, you must check for a 2K data stack rollover when reading words from the data stack.

- Store and/or use message information must be based on application requirements.

• stkptr = (stkptr + 4) modulo 1024. Increment to next message to be serviced, with a 1k rollover.

5. Exit Interrupt Service Routine.

Note : The initial value of the ‘STKPTR’ variable is set to the initial value of ‘MTCMDPTA’ at location 102/106h. Superceding Commands.

8 ENHANCED MINI-ACE BUILT-IN SELF-TEST

8.1 Introduction

Self-test is a common system level requirement for MIL-STD-1553 terminals. The design of the Enhanced Mini-ACE satisfies these requirements by incorporating a number of built-in self-test capabilities. These includes highly autonomous, comprehensive self-tests of the protocol logic and internal RAM, which may be initiated by command from the host processor. In addition, the Enhanced Mini-ACE implements the BC/RT online loop test and BC offline loop test that were provided by the previous generation ACE and Mini-ACE (Plus). The Enhanced Mini-ACE also include a method for testing the transmitter watchdog timer.

The protocol self-test consists of a functional test of the terminal's logic. The RAM built-in test exercises the Enhanced Mini-ACE's 4K X 16 or 64K X 17 internal shared RAM. Like the previous generation ACE and Mini-ACE's (Plus) BC and RT modes, there is a also continuous on-line loopback self-test performed for each message transmitted.

The Enhanced Mini-ACE will **automatically** perform its built-in protocol self-test following power turn-on. That is, the test will be initiated following a hardware reset; i.e., after the MSTCLR* (reset) input transitions from logic "0" to logic "1." There exists a ball programmable option "RSTBITEN" on BU-61740B RT, and BU-61840B/61860B BC/RT/MT Micro-ACE and BU-64840B/64843B/64860B/64863B BC/RT/MT Micro-ACE-TE, and BU-64843T Total-ACE components which is used to disable both the automatic, power-up built-in protocol self-test and manually initiated protocol self-test. Note that the self-test will **not** automatically be performed following a software reset; that is, after the host writes a value of logic "1" to bit 0 of the Start/Reset Register (Write 03H). If the host attempts a **write access** to the Enhanced Mini-ACE registers or internal RAM (e.g., to perform initialization) while the self-test is being performed, the register or RAM transfer will **not** be completed correctly.

In addition to performing the protocol self-test following power turn-on, the protocol and RAM self-tests may be initiated by the host processor at any time as long as the Enhanced Mini-ACE is "off-line," by means of the Start/Reset Register-Specifically, in BC mode if the BC is currently processing messages, the BC frame in progress will continue and self-test will not be performed. Similarly, if the Enhanced Mini-ACE is online in Word Monitor mode, a command to initiate self-test will be ignored. In addition, in RT, Message Monitor or RT/Monitor modes, a write to the Start/Reset Register to initiate a protocol or RAM self-test will be ignored, any message in progress will be completed, and the self-test will not be performed.

The results of these tests are then made available to the host by means of a BIT Test Status Register and/or interrupts. For RT mode, if the protocol self-test fails, the Terminal flag status word bit, along with a bit in the RT's BIT word, will be set to indicate the failure.

8.2 Differences from ACE and Mini-ACE (Plus)

One important feature of the Enhanced Mini-ACE is its software compatibility with DDC's previous generation terminals, the ACE and Mini-ACE (Plus). In terms of architectural functionality, the Enhanced Mini-ACE is basically a superset of the older ACE and Mini-ACE. The only exceptions have to do with a few items involving self-test. These are:

(1) Immediately following power turn-on, the Enhanced Mini-ACE will automatically perform its built-in protocol self-test. Depending on clock frequency, this test takes approximately 2 ms to complete (reference Table 142). If the host processor tries to access the Enhanced Mini-ACE's memory or registers during this time, the user is likely to encounter unexpected results.

(2) For the ACE or Mini-ACE (Plus), bit 8 of the RT BIT Word Register and the BIT word transmitted to the BC is CHANNEL B/A*. With the Enhanced Mini-ACE, bit 8 is BIT TEST FAIL. It will become set to a value of logic "1" if there is a failure of the Enhanced Mini-ACE's built-in protocol self-test.

(3) With the ACE or Mini-ACE (Plus), in order to run the protocol self-test, it is necessary for the host processor to write and read/verify approximately 4,000 test vectors. With the Enhanced Mini-ACE, all the host processor needs to do is to write a register bit. The self-test vectors, which are stored in on-chip ROM, are then run autonomously by the Enhanced Mini-ACE. When the self-test is complete, an interrupt request will be issued to the host (if enabled) and the results of the self-test will be readable via the BIT Test Status Register. In addition, the Enhanced Mini-ACE provides a separate autonomous self-test for the 4K or 64K internal RAM.

8.3 Protocol Logic Test

The protocol built-in self-test includes a comprehensive test of the Enhanced Mini-ACE's registers, Manchester decoders, protocol logic, and memory management logic. The test consists of a set of about 4,000 test vectors stored in on-chip ROM which are written to, and read and verified from individual Enhanced Mini-ACE registers and RAM locations.

With respect to the Enhanced Mini-ACE internal registers and RAM, the protocol test is almost entirely "non-destructive." That is, when the self-test is performed, the values of internal registers are temporarily stored into memory. Assuming that the protocol self-test is run to completion, the contents of most registers will then be restored to their original values.

Therefore, it is advised that the host processor **not** perform a register or memory write cycle to the Enhanced Mini-ACE during its self-test, since this would abort the test prior to the registers' restoration.

The only registers that are not restored are the Command Stack Register, RT/Monitor Data Stack Register, the Subaddress Control Word Register, and the Time Tag Register. The values of the first three of these registers clear to 0000 as the result of

protocol self-test. The value of the Time Tag Register will continue to increment during the self-test.

In addition, assuming that the protocol self-test passes, all of the shared RAM locations will be restored to their state prior to the self-test, *with the exception of the 60 RAM address locations **0342-037D***. Note that for RT mode, these locations map to the illegalization lookup table for “broadcast transmit subaddresses 1 through 30” (non-mode code broadcast transmit subaddresses). Since MIL-STD-1553 does not define these as valid command words, this section of the RT command illegalization lookup table is normally not used.

Also, if the Enhanced Mini-ACE’s INT* (interrupt request) output was asserted low prior to the start of self-test, it will clear during self-test, and **not** become re-asserted. Of course, the exception to this is for the BIT TEST COMPLETE interrupt, bit 1 of

Interrupt Mask and Status Register #2. That is, assuming this interrupt is enabled, INT* will assert low following self-test. However, note that the contents of Interrupt Status Register #1 and Interrupt Status Register #2 will automatically be restored to their previous values (plus (possibly) BIT TEST COMPLETE) following the protocol self-test.

Note that the Enhanced Mini-ACE BC will not process any messages, and the RT will not respond to any messages while the protocol or RAM self-tests are being performed. Therefore (for example), the RT busy bit is irrelevant during this time.

8.4 RAM Self-Test

For Enhanced Mini-Ace’s with 64K X 17 RAM, the 17th bit is used for implementing RAM parity. However, for purposes of the RAM built-in self-test, the RAM is treated as two separate sections: a 4K X 16 section and a 64K X 16 section (with no parity). Therefore, you will never get a RAM parity error during RAM self-test.

The built-in RAM self-test consists of writing and then reading/verifying the walking pattern “data = address,” followed by the walking pattern “data = address inverted.” At the end of the test, the data test pattern is left resident in the RAM. That is, unlike the protocol self-test, the RAM test is "destructive" of system data. As a result, following the RAM self-test, regardless of whether the test passes or fails, the data in shared RAM is not automatically restored to its previous values.

Note that for an Enhanced Mini-ACE with 64K X 17 of RAM, the 4K X 16 RAM (used for RAM parity) is tested at the same time that the lower 4K of the 64K X 16 RAM is tested.

8.5 Test Time

The Enhanced Mini-ACE protocol self-test consists of approximately 4,000 test vectors. It takes 8 clock cycles to execute each test vector, for a total of approximately 32,000 clock cycles.

The RAM test takes a total of 10 clock cycles per RAM location. That is, for each word location, it takes 5 clocks to write and read/verify the "data = address" pattern, and another 5 clocks to write and read/verify the "data = inverted address" pattern. This breaks down to 3 clock cycles to perform each write operation, and two clock cycles for each read operation. Therefore, for an Enhanced Mini-ACE hybrid with 4K RAM locations, it takes a total of 40,960 clock cycles to perform the RAM self-test. For an Enhanced Mini-ACE with 64K RAM locations, it takes a total of 655,360 clock cycles to perform the RAM self-test.

Table 142 provides the test times, in milliseconds, for the protocol and RAM self-tests for 10, 12, 16, and 20 MHz operation of the Enhanced Mini-ACE.

Table 142. Test Time (in ms)

		10 MHz	12 MHz	16 MHz	20 MHz
Protocol Self-Test		3.2	2.7	2.0	1.6
RAM Self-Test	4K RAM	4.1	3.4	2.6	2.0
	64K RAM	65.5	54.6	42.0	32.8

8.6 Power-on Self-Test

The Enhanced Mini-ACE will automatically perform its built-in protocol self-test following power turn-on. That is, the test will be initiated following a hardware reset; i.e., after the MSTCLR* (reset) input transitions from logic "0" to logic "1." Note that the self-test will *not* automatically be performed following a software reset; that is, after the host writes a value of "1" to bit 0 of the Start/Reset Register.

If the host attempts a write access to the Enhanced Mini-ACE registers or RAM (e.g., to perform initialization) while the self-test is being performed, the register or RAM transfer will *not* be completed correctly.

Note: *Therefore, when porting software to the Enhanced Mini-ACE that was used for a previous ACE or Mini-ACE (Plus) application, it is recommended that software initialization be delayed until after the completion of the power-on self-test.*

Incorrect parity for the Enhanced Mini-ACE's RT address input will have **no effect** on self-test.

To determine when the power-up protocol self-test has been completed, the host may poll the value of the BIT Test Status Register (register address 1Ch, read only; reference Table 143). While the test is in progress, this register should return a value of 4800h. After a successful completion of the test, this register will return a value of A800h (PROTOCOL SELF-TEST COMPLETED and PASSED).

If the self-test fails, this register will return a value of 8800h. If the register continues to return a value of 4800h after the time that the test should have been completed (e.g., after significantly more than 2.0 ms following the rising edge of MSTCLR*, assuming a 16 MHz clock input – reference Table 142), then the test has probably hung. This indicates a likely problem with the Enhanced Mini-ACE's internal self-test logic.

The value of the BIT Test Status Register may be cleared to 0000 by writing a value of logic "1" to bit 10, CLEAR SELF-TEST REGISTER, of the Start/Reset Register.

8.7 Register Bits

The following register bits are applicable to initiating and monitoring the Enhanced Mini-ACE built-in self-tests:

Start/Reset Register (register address 03h (write only)):

CLEAR RT HALT (bit 11): If RT HALT ENABLE (bit 4 of Configuration Register #7) has been programmed to logic "1" and the Enhanced Mini-ACE RT receives an Initiate self-test mode command, the RT will automatically go to an offline state (i.e., it will not receive or respond to messages from the 1553 bus). It is then up to the host to initiate the protocol or RAM self-test, via bits 7 or 9 respectively of the Start/Reset Register. Once the particular self-test completes, the Enhanced Mini-ACE RT will *automatically* go back online.

However, if the RT receives an Initiate self-test mode command, the user (host) may "choose" to *not* perform the protocol self-test. To do this, the host should write a value of logic "1" to CLEAR RT HALT. Following this write operation, the RT will automatically *revert back to its online state*, and resume receiving and responding to messages from the 1553 bus.

CLEAR SELF-TEST REGISTER (bit 10): Writing logic "1" to this bit will clear the value of the BIT TEST STATUS REGISTER (register address 1Ch) to a value of 0000h.

INITIATE RAM SELF-TEST (bit 9): If the Enhanced Mini-ACE is in BC mode and not transmitting messages, Word Monitor mode (but not online), or RT HALT, SELECTIVE MONITOR HALT, or Idle mode, writing logic "1" to this bit will initiate the self-test of the Enhanced Mini-ACE's internal 4K X 16 or 64K X 16 internal RAM. If the Enhanced Mini-ACE is online in BC or Word Monitor mode; or in the RT, Message Monitor, or combined RT/Monitor modes, the write to the Start/Reset Register to initiate RAM self-test will be *ignored*.

INITIATE PROTOCOL SELF-TEST (bit 7): If the Enhanced Mini-ACE is in BC mode (and not transmitting messages), Word Monitor mode (but not online), or RT HALT, SELECTIVE MONITOR HALT, or Idle mode, writing logic "1" to this bit will initiate the autonomous self-test of the Enhanced Mini-ACE's protocol logic. This test exercises the internal registers, decoders, protocol logic, and memory management logic. If the Enhanced Mini-ACE is online in BC or Word Monitor mode; or in the RT, Message Monitor, or combined RT/Monitor modes, the write to the Start/Reset Register to initiate protocol self-test will be *ignored*.

For a given write operation to the Start/Reset Register, the host should **never** write logic "1" to INITIATE RAM SELF-TEST **and** INITIATE PROTOCOL SELF-TEST simultaneously. If this is done, the Enhanced Mini-ACE will attempt to run **both** self-tests, and **both** will fail. For the same reason, the host should never attempt to initiate one of the two self-tests while the other one is being performed.

Configuration Register #3 (register address 19h, read/write):

ENHANCED MODE ENABLE (bit 15): This bit must be set to logic "1" by programming this register to a value of 8000h *before* attempting any ENHANCED MODE operations, including the protocol logic or RAM built-in tests. Note that in order to keep the Enhanced Mini-ACE in ENHANCED MODE (and thus allow the self-tests to be performed), this bit to remain set to logic "1" as the result of any subsequent write operations to Configuration Register #3.

Configuration Register #6 (register address 18h, read/write):

64-WORD REGISTER SPACE (bit 2): To provide compatibility with ACE/Mini-ACE (Plus), the default size of the Enhanced Mini-ACE register space is 32 words. In order for the host to be able to access test registers above register address 1Fh, it is necessary to program this bit to logic "1." For example, following a failed protocol test, this is necessary in order to determine the first failed test vector. Note that in order to initiate self-test, it is **not** necessary to set this bit.

Configuration Register #7 (register address 19h, read/write):

RT HALT ENABLE (bit 4): If this bit has been programmed to logic "1," the Enhanced Mini-ACE RT will automatically go off-line – to the RT HALT state -- following reception of an Initiate self-test mode command. When this occurs, the host may then initiate protocol or RAM self-test by means of the Start/Reset Register.

8.8 Initiating Self-Test

As explained above, the Enhanced Mini-ACE protocol logic and RAM built-in self-tests are initiated by writing to specific bits in the Start/Reset Register. However, if the Enhanced Mini-ACE is online in BC or Word Monitor mode; or in the RT, Monitor, or combined RT/Monitor modes, the write to the Start/Reset Register to initiate a protocol or RAM self-test will be *ignored*.

Specifically, in BC mode if the BC is currently processing messages, the BC frame in progress will continue and self-test will *not* be performed. Similarly, if the Enhanced Mini-ACE is online in Word Monitor mode, a command to initiate self-test will be ignored. In addition, in RT, Message Monitor or RT/Monitor modes, a write to the Start/Reset Register to initiate a protocol or RAM self-test will be ignored, any message in progress will be completed, and the self-test will *not* be performed.

In BC mode, a protocol or RAM self-test may be initiated while the BC is currently *not* processing messages (i.e., it is already offline). It is possible to determine that there is no BC frame in progress by polling the value of BC FRAME IN PROGRESS, bit 1 of Configuration Register #1. If this bit is logic "0," then the BC is idle, and the Enhanced Mini-ACE *will* respond to a command to initiate self-test.

Similarly, in Word Monitor mode, it is only possible to initiate self-test if the monitor is not online. That is, prior to the host writing to BC/MT START (bit 1 of the Start/Reset Register) or after the Word Monitor has been taken offline by writing to RESET, bit 0 of the Start/Reset Register.

In RT mode, there are two methods for initiating built-in self-test. These are:

(1) Set the RT HALT ENABLE register bit (bit 4 of Configuration Register #7) to logic "1." This will cause the RT to automatically go offline following receipt of an Initiate self-test mode command from the BC. This will put the Enhanced Mini-ACE into its RT HALT state. At this time, the host may then initiate protocol or RAM self-test by writing to the Start/Reset Register. *This is the preferred method* for initiating self-test from RT mode.

(2) Alternatively, for a BC/RT/MT terminal the host can direct the Enhanced Mini-ACE to transition from RT mode to (offline) BC or Word Monitor mode, by means of Configuration Register #1, before initiating the self-test. For an RT-only terminal, the host can direct the Enhanced Mini-ACE to transition to Idle mode, by means of Configuration Register #1, before initiating the self-test. *Note that this method must also be used for initiating self-test from the Enhanced Mini-ACE's Message Monitor mode.*

To switch from RT, Message Monitor, or combined RT/Monitor mode to BC or Idle mode in order to initiate self-test, the upper two bits (15 and 14) of Configuration Register #1 must both be programmed to logic "0." Alternatively, for a BC/RT/MT terminal, the Enhanced Mini-ACE may be programmed to Word Monitor mode, by programming Configuration Register #1 as follows: bit 15 to logic "0," bit 14 to logic "1," and bit 12 to logic "0." To initiate self-test, it does **not** matter what value Configuration Register #1 bits 13, and 11-0 are programmed to.

However, if this method is used from RT, Message Monitor, or combined RT/Monitor mode, it is important to note that if the RT or Monitor is servicing a message at that time, that the message reception and/or response will be *aborted immediately*. The host may determine if the RT is currently processing a message by polling the read-only bit RT MESSAGE IN PROGRESS (or MONITOR ACTIVE), bit 0 of Configuration Register #1. If this bit is logic "1," this indicates that the RT or Message Monitor is currently processing a message.

If the switch from RT and/or Monitor mode to BC or Word Monitor mode takes place between the SOM (Start-of-Message) and EOM (End-of-Message) sequences for a particular message, then the message in progress will *not* be completed. This will likely result in an invalid message, *unless* the switch took place between the end of the last transmitted or received word and the end of the EOM sequence, in which case the EOM sequence will **not** occur. For the latter scenario, the result will be that the SOM bit in the Block Status Word will remain logic "1," the EOM bit will remain logic "0"; and the Time Tag word in the message descriptor will reflect the time of the start-of-message, rather than the time of the end-of-message.

8.9 Terminating Self-Test

The protocol logic or RAM self-test may be terminated as the result of a host processor write operation at any time during the test. Note that a read operation (for example, of the BIT Test Status Register) will *not* abort the self-test; however, *any* write operation will. Also, such an intended write operation itself will not be completed. Note that if the protocol logic self-test is terminated prematurely, bit 12 of the BIT Test Status Register, PROTOCOL BUILT-IN TEST ABORT, will be set to logic "1." Also, note that there is *no* corresponding register bit to denote the termination of a RAM self-test.

8.10 Determining BIT Test Completion and Results

The Enhanced Mini-ACE includes a number of mechanisms for the host processor, along with the BC (for the Enhanced Mini-ACE RT mode), to determine when the built-in self-test has been completed, along with the test results. These include:

1. Interrupt Mask Register #2 and Interrupt Status Register #2.

2. The BIT Test Status Register.

3. The Terminal flag RT status word bit.

4. The RT BIT word (bit 8), and the RT BIT Word Register.

In the case of RT mode, methods (3) and/or (4) may be used to report the test results to the bus controller.

There are three methods for the host to determine when the protocol or RAM self-test has been completed: (1) by means of an interrupt; (2) by polling Interrupt Status Register #2; or (3) by polling the BIT Test Status Register.

To use an interrupt to determine when the self-test has completed, the host must enable the BIT TEST COMPLETE interrupt, by programming the value of bit 1 of Interrupt Mask Register #2 (register address 1Dh, RD/WR) to logic "1." After the host has initiated self-test and an interrupt request has been issued, it may then read Interrupt Status Register #2 (register address 1Eh, read-only) following the issuance of an Interrupt Request. If enabled, BIT TEST COMPLETE will be set following completion of the protocol **or** RAM self-test.

For a system that does not use interrupts -- at least for 1553 self-test -- the host may still poll Interrupt Status Register #2 to determine when a self-test has completed. To enable this, the host must: (1) enable ENHANCED INTERRUPTS, by programming bit 15 of Configuration Register #2 to logic "1"; (2) program the value of bit 1 of Interrupt Mask Register #2 to logic **"0."** This second step will allow the host to poll bit 1 of Interrupt Status Register #2 (BIT TEST COMPLETE) *without* having to deal with the issuance of an interrupt request.

Any host write operation during self-test will terminate the test. An aborted self-test has the effect of a software reset. That is, the value of all configuration registers will clear to 0000; and, in the case of RT mode (prior to running self-test), the transmitters are re-enabled (if inhibited); Terminal Flag bit re-enabled (if inhibited); and the Message Error and Broadcast Command Received RT Status Word bits are cleared to logic "0."

8.11 BIT Test Status Register

Table 143 provides the bit mapping and bit descriptions for the BIT Test Status Register. Note that this register initializes to a value of 0000h immediately following power turn-on. While the protocol self-test is in progress, a read of this register will return a value of 4800h. After a successful completion of the test, this register should return a value of A800h (PROTOCOL SELF-TEST COMPLETED and PASSED). The host may reset the value of this register to 0000h by writing a value of logic "1" to CLEAR SELF-TEST REGISTER, bit 10 of the Start/Reset Register.

Table 143. BIT Test Status Register (register address 1Ch, read-only)		
BIT	**BIT NAME**	**BIT DESCRIPTION**
15 (MSB)	PROTOCOL BUILT-IN TEST COMPLETE	Following power turn-on and MSTCLR* going high, this bit initializes to a value of logic "0." Normally, it will change to logic "1" after the Enhanced Mini-ACE completes its power turn-on protocol self-test. It will remain at logic "1" until a value of logic "1" is written to CLEAR SELF-TEST REGISTER, bit 10 of the Start/Reset register, or until the host initiates a subsequent protocol self-test. PROTOCOL SELF-TEST COMPLETE will clear to a value of logic "0" at the start of a new self-test.
14	PROTOCOL BUILT-IN TEST IN PROGRESS	If this bit is logic "1," it indicates that the Enhanced Mini-ACE is currently running its protocol self-test. This bit will clear to logic "0" upon completion of the test. If this bit persists in returning a value of logic "1" after the time that the test should have been completed (e.g., after much more than 2.0 ms following the initiation of the test, assuming a 16 MHz clock input - reference Table 1), then the test has probably hung. This indicates a likely problem in the Enhanced Mini-ACE's internal self-test logic.
13	PROTOCOL BUILT-IN TEST PASSED	If this bit is logic "1, this indicates that the built-in protocol self-test has passed. This bit will remain logic "1" until a value of logic "1" has been written to CLEAR SELF-TEST REGISTER, or the host initiates a subsequent protocol self-test. The start of a subsequent protocol self-test clears PROTOCOL BUILT-IN TEST PASSED to "0."
12	PROTOCOL BUILT-IN TEST ABORT	This bit indicates that the protocol self-test has been terminated. The self-test will immediately abort if the host processor writes to any Enhanced Mini-ACE register or RAM while the protocol self-test is being performed.
11	PROTOCOL BUILT-IN TEST IN PROGRESS OR COMPLETE	Following hardware reset (MSTCLR* low), this bit initializes to logic "0." However, when the power turn-on protocol self-test begins, PROTOCOL BUILT-IN TEST IN PROGRESS OR COMPLETE transitions to logic "1," and remains at logic "1" after the test completes. It is cleared to logic "0" by clearing the BIT Test Status Register, by means of CLEAR SELF-TEST REGISTER. Otherwise, it will stay at logic "1." If cleared to "0," it will go back to "1" after another protocol self-test is initiated. PROTOCOL BUILT-IN TEST IN PROGRESS OR COMPLETE is **not** cleared to "0" by software reset.
10	LOGIC "0"	
9	LOGIC "0"	
8	LOGIC "0"	
7	RAM BUILT-IN TEST COMPLETE	If this bit is logic "1, this indicates that the RAM self-test has completed. Following power turn-on and MSTCLR* going high, this bit initializes to a value of logic "0." It will return a value of "0" while a RAM self-test is being performed, and will only return logic "1" following completion of the RAM self-test. The host may clear this bit by writing logic "1" to CLEAR SELF-TEST REGISTER, or by initiating a subsequent RAM self-test. The host may clear this bit to "0" by writing logic "1" to CLEAR SELF-TEST REGISTER, by initiating a subsequent RAM self-test or initiating a PROTOCOL SELF-TEST.
6	RAM BUILT-IN TEST IN PROGRESS	If this bit is logic "1," it indicates that the Enhanced Mini-ACE is currently running its built-in RAM self-test. This bit will clear to logic "0" upon completion of the test. If this bit persists in returning a value of logic "1" after the time that the test should have been completed (e.g., after much more than 2.6 ms following the initiation of the test, assuming a 4K RAM Enhanced Mini-ACE and a 16 MHz clock input - reference Table 1), then the test has probably hung. This indicates a likely problem in the Enhanced Mini-ACE's internal self-test logic.
5	RAM BUILT-IN TEST PASSED	If this bit is logic "1, this indicates that the built-in RAM self-test has completed and passed. The host may clear this bit to "0" by writing logic "1" to CLEAR SELF-TEST

Table 143. BIT Test Status Register (register address 1Ch, read-only)		
BIT	**BIT NAME**	**BIT DESCRIPTION**
		REGISTER, by initiating a subsequent RAM self-test or initiating a PROTOCOL SELF-TEST. This bit will remain logic “1” until a value of logic “1” has been written to CLEAR SELF-TEST REGISTER, or the host initiates a subsequent RAM self-test. The start of a subsequent RAM self-test clears RAM BUILT-IN TEST PASSED to “0.”
4	LOGIC “0”	
3	LOGIC “0”	
2	LOGIC “0”	
1	LOGIC “0”	
0 (LSB)	LOGIC “0”	

8.12 RT BIT Word

The Enhanced Mini-ACE provides two options for the RT BIT (Built-in Test) Word: (1) The default configuration is for the internally formulated BIT Word (reference Table 144); (2) a version which is software programmable by the host processor. To enable the second option, the host must write a value of logic “1” to EXTERNAL BIT WORD ENABLE, bit 15 of Configuration Register #4. In this case, the RT BIT word will be read from a RAM location rather than from the RT BIT Word Register.

It is recommended that the internally formulated RT BIT word be used. Table 144 illustrates the bit mapping for the internal RT BIT word and the read-only RT BIT Word Register. The contents of this register are transmitted to the BC in response to a Transmit BIT word mode command.

Table 144. RT BIT Word	
BIT	**DESCRIPTION**
15 (MSB)	TRANSMITTER TIMEOUT
14	LOOP TEST FAILURE B
13	LOOP TEST FAILURE A
12	HANDSHAKE FAILURE
11	TRANSMITTER SHUTDOWN B
10	TRANSMITTER SHUTDOWN A
9	TERMINAL FLAG INHIBITED
8	BIT TEST FAIL
7	HIGH WORD COUNT
6	LOW WORD COUNT
5	INCORRECT SYNC RECEIVED
4	PARITY/MANCHESTER ERROR RECEIVED
3	RT-RT GAP/SYNC/ADDRESS ERROR
2	RT-RT NO RESPONSE ERROR
1	RT-RT 2ND COMMAND WORD ERROR
0 (LSB)	COMMAND WORD CONTENTS ERROR

NOTE:

Bits 15 through 9 are cleared only following a MSTCLR* input, a software reset via the Start/Reset Register, or reception of a Reset Remote Terminal mode command. Bits 7 through 0 are updated as a result of every message processed by the RT.

Bit 8 of the internally formulated RT BIT word represents the result of the Enhanced Mini-ACE RT's most recent built-in protocol self-test. A value of logic "0" for bit 8, BIT TEST FAIL, indicates that the test passed. The bit will return a value of logic "1" if the Enhanced Mini-ACE has failed its most recent protocol self-test. If a subsequent performing of the protocol self-test passes, bit 8 will clear to "0." Also, note that the RAM self-test has no effect on bit 8.

8.13 Terminal Flag Status Word bit

If RTFAIL-TO-TERMINAL FLAG WRAP ENABLE, bit 2 of Configuration Register #3, has been programmed to logic "1" *and* the protocol logic built-in self-test fails, the RT Terminal flag status bit will be set to logic "1."

Consequently, the result of the last loop test performed prior to protocol self-test becomes "lost." That is, if the loop test fails for the last message before the protocol self-test has been performed (e.g., for the response to an Initiate Self-test mode command) and the self-test passes, the Terminal flag bit will then be logic "0" starting

with the first message following the self-test. If the protocol self-test fails, note that RT FAIL (and Terminal Flag) will **remain set** regardless of the subsequent loop test results, until the protocol test is re-run and passes, or the host writes logic "1" to CLEAR SELF-TEST REGISTER, bit 10 of the Start/Reset Register.

If the protocol self-test passes however, a subsequent failure of the loop test will still result in the setting of the Terminal flag bit.

8.14 Self-Test Registers

If there is a failure of the protocol self-test, it is possible to access information about the first failed vector. This may be done by means of the Enhanced Mini-ACE's upper registers (register addresses 20h through 3Fh).

It should be noted that the protocol and RAM self-tests do **not** stop when an individual vector fails. That is, the tests **will** continue to completion.

In order to enable access to these upper 32 registers, it is first necessary to program 64-WORD REGISTER SPACE, bit 2 of Configuration Register #6, to logic "1." By means of these registers, it is possible to determine the self-test ROM address of the first failed vector, the expected response data pattern (from the ROM), the register or memory address, and the actual (incorrect) data value read from register or memory.

The on-chip self-test ROM is 4K X 24.

For reference, Table 145 provides an address map of (a subset) of the self-test registers, while Tables 148 through 154 provide the bit descriptions for those self-test registers. All of these registers are read/writable. However, like the non-test registers, these registers should **not** be written while self-test is being performed. If this is done, the test will be aborted immediately.

Table 145. Self-Test Registers

Register Address (hex)	Register Name
36	Self-Test ROM Address Register
37	Test Vector (RAM or register) Address Register
38	Test Vector (RAM or register) Data Register
39	Self-Test ROM Data Register (lower 16 bits)
3A	Self-Test ROM Data Register (upper 8 bits)
3B	ROM Address Register
3E	RAM/Register Address Register (upper 10 bits)

Table 146. Self-Test ROM Address Register (36h)		
BIT	**BIT NAME**	**BIT DESCRIPTION**
15 (MSB)	READ/WRITE*	If this bit is logic "0," this indicates that the current test vector is to be written to a register or RAM location. If this bit is logic "1," this indicates that the current test vector is to be read from an Enhanced Mini-ACE register or RAM location, and verified to match the data pattern from ROM. If there is a protocol test failure, the contents of this bit will be latched, reflecting the value of the READ/WRITE* bit for the **first** failed test vector.
14	MEMORY/REGISTER*	If this bit is logic "0," this indicates that a test vector is to be written to, or read/verified from an Enhanced Mini-ACE register. If this bit is logic "1," this indicates that a test vector is to be written to, or read/verified from an Enhanced Mini-ACE RAM location. If there is a protocol test failure, the contents of this bit will be latched, reflecting the value of the MEMORY/REGISTER* bit for the **first** failed test vector.
13	LOGIC "0"	
12		
11	SELF-TEST ROM ADDRESS 11 (MSB)	Self-test ROM address (12 bits). If there is a protocol test failure, the contents of this address will be latched, reflecting the value of the self-test ROM address for the **first** failed test vector.
*	*	
*	*	
*	*	
0 (LSB)	SELF-TEST ROM ADDRESS 0 (LSB)	

Table 147. Test Vector (RAM or Register) Address Register (37h)		
BIT	**BIT NAME**	**BIT DESCRIPTION**
15 (MSB)	RAM/REGISTER ADDRESS 15 (MSB)	This register stores the address of the Enhanced Mini-ACE register or RAM location being accessed for the current test vector. If there is a protocol test failure, the contents of these bits will be latched, reflecting the value of the self-test register or RAM address for the **first** failed test vector.
*	*	
*	*	
*	*	
0 (LSB)	RAM/REGISTER ADDRESS 0 (LSB)	

Table 148. Test Vector (Ram or Register) Data (Latched on Failure) Register (38h)		
BIT	**BIT NAME**	**BIT DESCRIPTION**
15 (MSB)	RAM/REGISTER DATA 15 (MSB)	This register stores the data written to or read from the Enhanced Mini-ACE register or RAM being accessed for the current test vector. If there is a protocol test failure, the contents of this register will be latched, reflecting the value of the self-test register or RAM data for the **first** failed test vector.
*	*	
*	*	
*	*	
0 (LSB)	RAM/REGISTER DATA 0 (LSB)	

Table 149. Self-Test-ROM-Data (lower 16-Bits) Register (39h)		
BIT	**BIT NAME**	**BIT DESCRIPTION**
15 (MSB)	ROM DATA (VECTOR) 15 (MSB)	This register represents the value of data bits 15-0 (the lower 16 data bits) from the current self-test ROM location. This is the data pattern written to, or the "expected value" to be read and verified from the specified Enhanced Mini-ACE RAM or register. In the case of a protocol self-test failure, the host may determine the "expected (data) value" for a particular test vector by first writing the Self-Test ROM Address Register (register address 3Bh), and then reading the contents of the Self-Test ROM Data (lower 16 bits) Register.
*	*	
*	*	
*	*	
0 (LSB)	ROM DATA (VECTOR) 0 (LSB)	

Table 150. Self-Test-ROM-Data (Upper 8-Bits) Register (3Ah)		
BIT	**BIT NAME**	**BIT DESCRIPTION**
15	LOGIC "0"	
*		
*		
*		
8		
7 (MSB)	READ/WRITE*	Data bit 23 (MSB) from the current self-test ROM location. If this bit is logic "0," this indicates that the current test vector is to be written to an Enhanced Mini-ACE register or RAM location. If this bit is logic "1," this indicates that the current test vector is to be read from register or RAM, and verified to match the ROM data pattern.
6	MEMORY/REGISTER*	Data bit 22 from the current self-test ROM location. If this bit is logic "0," this indicates a test vector written to or read/verified from an Enhanced Mini-ACE register. If this bit is logic "1," this indicates a test vector written to or read/verified from an Enhanced Mini-ACE RAM location.
5	RAM/REGISTER ADDRESS 5	Data bits 21-16 from the current self-test ROM location. These bits represent the lower 6 bits of the address of the Enhanced Mini-ACE register or RAM being accessed for the current test vector.
*	*	
*	*	
*	*	
0	RAM/REGISTER ADDRESS 0 (LSB)	

Table 151. ROM Address Register (38h)		
BIT	**BIT NAME**	**BIT DESCRIPTION**
15 (MSB)	LOGIC "0"	
*		
*		
*		
12		
11	ROM ADDRESS 11 (MSB)	This is the current 12-bit self-test ROM address. In the case of a protocol self-test failure, the host may determine the expected data value for a particular test vector by first writing this register and then reading the contents of the Self-Test ROM Data (lower 16 bits) Register (register address 39h).
*	*	
*	*	
*	*	
0 (LSB)	ROM ADDRESS 0 (LSB)	

Table 152. RAM/Register-Address-Register-(Upper-19 –bits)(3Eh)		
BIT	**BIT NAME**	**BIT DESCRIPTION**
15 (MSB)	RAM/Register Address 15 (MSB)	Upper 10 bits of the Enhanced Mini-ACE RAM/Register address for the current vector. This register gets written by the Enhanced Mini-ACE during self-test. These are concatenated with the lower 6 RAM/Register address bits, which are accessible via Register 3Ah, the Self-Test ROM Data (upper 8 bits) Register.
* * *	* * *	
6	RAM/Register Address 6	
5	LOGIC “0”	
* * *		
0 (LSB)		

The final ROM address for the protocol self-test is 0FC6. The last vector of the protocol self-test is a write operation to register address 003F, with a data value of 0001. The data values for the self-test registers following a completed, passed protocol self-test are listed in Table 153.

Table 153. Final Values of Self Test Registers Following Passed Protocol Self Test		
Register Address (hex)	**Register Name**	**Value Following Passed Protocol Self-Test**
36	Self-Test ROM Address Register	0F36
37	Test Vector (RAM or register) Address Register	003F
38	Test Vector (RAM or register) Data Register	0001
39	Self-Test ROM Data Register (lower 16 bits)	0001
3A	Self-Test ROM Data Register (upper 8 bits)	003F
3B	ROM Address Register	0FC6
3E	RAM/Register Address Register (upper 10 bits)	0000

Following a passed protocol self-test, the host may run an additional check of the Enhanced Mini-ACE test logic by reading the seven test registers and verifying for the contents listed in Table 155.

After a failed protocol self-test, the self-test ROM address, Enhanced Mini-ACE RAM/register address, and RAM/register data (that was actually read) for the **first** failed may be read from register addresses 36h, 37h, and 38h respectively. In addition, it is possible to determine the “expected value” ROM data for the first failed test vector by:

(1) Reading the failed ROM address of the first failed vector from the 12 LSBs of the Self-Test ROM Address Register (36h);

(2) Writing the value read during step (1) to the 12 LSBs of ROM Address Register (3B);

(3) Reading the “expected” data value from the Self-Test ROM Data (lower 16 bits) Register (39h).

Another possible concern involving the self-test logic is the possibility that the protocol and/or RAM self-test flag(s) are stuck in the “passed” state. To verify that this is *not* the case, the host can: (1) check the final values in the self-test registers (see above); and/or (2) poll the "PROTOCOL SELF-TEST PASSED" bit (bit 12) or "RAM BUILT-IN SELF-TEST PASSED" bit (bit 5) of the BIT Test Status Register *while the respective self-test is being performed*. If the "PASSED" bit for the active test returns a value of logic "1" *while the test is being performed*, this indicates that the bit is stuck high. If the BIT Test Status Register indicates “passed” but either of these checks fails, this indicates a fault in the Enhanced Mini-ACE self-test logic.

8.15 BC/RT Online Loop Test

In addition to the built-in protocol and RAM self-tests, the Enhanced Mini-ACE provides an online loop test for *every* message transmitted by the BC and *every* non-broadcast message processed by the RT. For this test, the received versions of all words transmitted by the BC or RT are checked for validity (sync, Manchester encoding, bit count, parity), *and* there is a bit-by-bit comparison performed on the received version of the last transmitted word. If either of these tests fail, the loop test is considered to have failed.

The online loop test is a true internal/external wraparound test. It is performed on the received digital version of each word; i.e., the word sent out of the transmitter to the isolation transformer, reflected back to the receiver, and decoded by the Manchester decoder.

There are a number of conditions that can result in a loop test failure. For example, a shorted isolation transformer winding or stub will almost certainly result in a loop test failure. That is, if one of the transformer stub connections is shorted, the transceiver power supply current will increase from less than 500 ma to greater than 1.8 amps. Since the Enhanced Mini-ACE transceiver's idle (non-transmitting) current is about 100 ma, a power supply current of 1.8 amps indicates an instantaneous primary current (one transformer leg to center tap) of about 1.7 amps, which indicates - based on the transformer turns ratio of 1:1.79 - a current of about 475 ma across the (shorted) transformer secondary (stub).

In addition to a shorted isolation transformer, a loop test failure in a system can indicate a fault in one of several other areas (both internal and external): the Enhanced Mini-ACE Manchester encoder or decoder, transceiver, P.C. board traces, system connector, cable connector, stub cable; coupling box connector, transformer or isolation resistors; bus cable, or bus terminating resistors.

The Enhanced Mini-ACE provides the following indications of a loop test failure:

(1) In both BC and RT modes, bit 12 - ERROR FLAG, and bit 8 – LOOP TEST FAIL of the block status word, will both be logic “1.”

(2) In RT mode, the transmitted value of the Terminal flag status word bit will be logic "1" if RTFAIL/RTFLAG AUTOWRAP ENABLE, bit 2 of Configuration Register #3, has been programmed to logic "1" *and* the loop test failed for the *previous* non-broadcast message processed by the RT. In addition, if RTFAIL/RTFLAG AUTOWRAP ENABLE is set, a transmitter timeout condition will also result in the setting of the Terminal flag bit.

A transmitter timeout condition occurs when the Enhanced Mini-ACE's 660.5 µs transmitter watchdog timer times out and aborts the current BC or RT transmission on the 1553 bus. The latter indicates a fault in the Manchester II encoder, RT state machine, or word count logic. Note that if the protocol logic built-in self-test has been performed since the processing of the previous non-broadcast message, that the value of the Terminal flag bit will reflect the result of the protocol self-test (“0” = pass; “1” = fail), rather than the result of the previous loop test (or transmitter timeout).

Note that the transmitted Terminal flag status word bit will also be set to logic “1” if the host has programmed TERMINAL FLAG*, bit 7 of Configuration Register #1, to a value of logic “0.”

(3) In RT mode, assuming that the internally formulated BIT word is used, bit 14 of the RT BIT word (and BIT Word Register) will be set if the loop test failed for a message on bus channel B, while bit 13 will be set if the loop test failed for a message on bus channel A. If either of these bits becomes set, they will only be cleared following a MSTCLR* input, a software reset via the Start/Reset Register, or reception of a Reset remote terminal mode command.

(4) If bit 2 of Interrupt Mask Register #1, FORMAT ERROR, has been set, this will result in an interrupt request and the setting of bit 2 of Interrupt Status Register #1.

8.16 BC Offline Loop Test

In addition to the online loop test, the Enhanced Mini-ACE BC includes capability for performing an offline loop test. For any individual message, the BC offline loop test may be activated by setting OFF-LINE SELF-TEST, bit 6 of the BC Control Word, to logic “1.” This test involves the “transmission” of an internal message in which the serial output of the Manchester encoder is routed to the input of the Manchester decoder. For this test, *no* message is transmitted on the external 1553 bus. A failure of this loop test would indicate a failure of the Manchester encoder or decoder, parallel or serial data paths, or BC state machine logic. Similar to the online loop test, the result of this test is host accessible by means of the message’s block status word, the BC loopback word (stored in RAM), and/or Interrupt Status Register #1.

8.17 Transmitter Watchdog (failsafe) Timer Test

The purpose of the Enhanced Mini-ACE’s transmitter watchdog timer is to mitigate against a “babbling” Manchester encoder by automatically shutting down the channel A or channel B transmitter. The watchdog timer logic operates independently of the Manchester encoder logic. Specifically, its purpose is to automatically shut down the active encoder and transmitter if it attempts to transmit for longer than 660.5 µs. The longest valid MIL-STD-1553 transmission is 660 µs.

To test the transmitter watchdog timer, it is necessary to induce a timeout condition, which will not occur under normal operation. To induce a transmitter timeout condition, the host should set the lower three bits (TEST MODE) of Configuration Register #4 to a value of 4 (100). This configures the Enhanced Mini-ACE test mode for "FAILSAFE TIMER" test mode.

When this is done, the Enhanced Mini-ACE will transmit until a time-out condition occurs for *every* BC or RT transmission regardless of the message's correct word count. That is, for every BC message or every RT response, the active bus channel will transmit until the watchdog timer terminates the transmission. This will occur following a transmission of approximately 660.5 µs. To resume correct BC, RT, or Monitor operation following this test, the host should select "NORMAL OPERATION" mode by programming the lower three bits of Configuration Register #4 to a value of 000.

8.18 Channel A-to-Channel B Wraparound Self-Test (BC/RT/MT Versions Only)

The Channel A-to-Channel B wraparound test provides a method to exercise the Enhanced Mini-ACE's Channel A and Channel B front end circuitry, including the respective transceivers and isolation transformers.

This test involves the simultaneous use of the Enhanced Mini-ACE's Word Monitor Mode **and** its Test Mode. Note that this test is **only applicable for the BC/RT/MT versions** of the Enhanced Mini-ACE. This test is **not** possible for the RT-only versions, since these don't provide the Word Monitor function, which is required to perform the test.

Please note that a valid RT-ADDRESS/PARITY BIT combination must be supplied otherwise Bit #6 "THIS_RT*" of the "Word Monitor Identification Word" will indicate a fault condition.

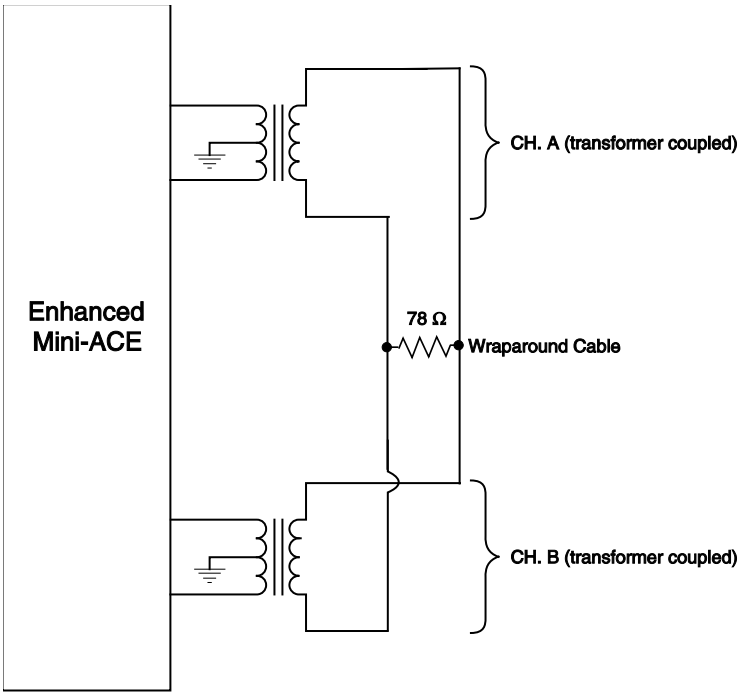


Figure 30. Connection Diagram for CH. A-to-CH. B Wraparound Self-Test

In order to perform this test, there needs be a wraparound connection between the 1553 A and B bus channels, as shown in Figure 30. This connection must include a termination resistor connected between the DATA-A(B) and DATA-A(B)* wires. Assuming that the transformer-coupled (stub-coupled) taps (usually the inner taps) of the isolation transformers are used, the value of this resistor should be 78 ohms. If the outer (direct coupled) taps are used -- which are required to include 55 ohm series resistors in each leg – then the value of the termination resistor should be 39 ohms.

The software programming steps required to perform the wraparound test are as follows:

1. Program the Enhanced Mini-ACE for ENHANCED MODE, by writing bit 15 of Configuration Register #3 to logic "1."

2. Program the Enhanced Mini-ACE for Encoder Test Mode, by writing the lower three bits of Configuration Register #4 to values of 010.

3. Program the Enhanced Mini-ACE for Word Monitor mode by programming Configuration Register #1 to a value of 4000. Initialize the value of the Monitor Stack Pointer (shared RAM address 0100) to a known value – a value of 0000 is suggested. Then, to start the Word Monitor, write a value of 0002 (BC/MONITOR START) to the Start/Reset Register.

4. Write the 16-bit data pattern for the 1553 “command,” “status,” or “data” word to be transmitted to Register address 0D (which is the BC Frame Time/RT Last Command/MT Trigger Word Register in non-test mode).

5. Write to test register address 11 (hex), the "ETEST" Register, as follows:

bit 15 - E_CHA: "0" = CH. B, "1" = CH. A

bit 14 - logic "0"

bit 13 - E_TXENA: logic "1"

bit 12 - E_ENCENA: logic "1"

bit 11 - E_SYNC: "1" = command/status word sync, "0" = data word sync

bit 10 - In order to receive transmitted words on both receivers/decoders (into the Monitor stack), it is necessary to assign a value of logic "1" for this bit. If this bit is logic "0," the transmitted word will **only** be stored for the version received by the **alternate bus** from which it was sent.

bits 9-6: logic "0"

bit 5 - Flip ENC (15:0) mux to AUX1 (15:0): logic "1"

bits 4-0: logic "0"

This write operation will cause the word with data from step 4 and sync type defined by bit 11 to be transmitted on the 1553 bus specified by bit 15.

6. Immediately after step 5, depending on which bus the word was transmitted on, start polling bit 1 or bit 0 of Register address 0011. These two bits are:

bit 1: A_TBUSY_L

bit 0: B_TBUSY_L

Some time after step 5 (immediately, in the case of the first word transmitted by the BC or an RT), the respective TBUSY bit (A or B) will transition from logic "1" to logic "0." It will stay at logic "0" for approximately 4 µs. During this time, which indicates the start of transmission of the word just loaded in steps 4 and 5 (that is, **before** the respective TBUSY bit transitions back to logic "1"), if it is desired to transmit a subsequent contiguous word, then steps 4, 5, and 6 must be repeated for that next word.

7. Following the loading of the **last** test word to be sent, transmission must be halted by disabling the respective encoder. To do this, after the last word has been written, poll the respective TBUSY bit until it returns a value of logic "0." At this time, write to register 11 (hex) one more time. This time, write the same value as during the previous step 5, **except** that the value of bit 12 (E_ENCENA) must be logic "0" rather

than logic "1." This will shut down the respective encoder (and therefore the respective 1553 transmitter) at the end of the current word.

8. To verify that data was correctly transmitted from Channel A to Channel B (or visa versa), it is necessary to read the words received by the Enhanced Mini-ACE Word Monitor. For each word transmitted on either channel, it is possible to read the received version of the data, along with the respective Monitor Tag (ID) word. That is, assuming that bit 10 of the "ETEST" register was assigned a value of logic "1," there should be a total of four (4) words stored in the Word Monitor RAM, starting at the monitor stack pointer address (e.g., 0000) for each word transmitted. These are, for each word transmitted:

(i) Word Data (CHANNEL A(B)) – The 16-bit word data written in step (4).

(ii) Tag Word (ID Word). This will indicate bus channel, word validity, command/status, data sync type, and some timing information and other bits for the **first** received version of the transmitted word. This word will **usually** indicate for the most recent bus channel transmitted from (A or B). However, there's no guarantee of that. That is, it's theoretically possible for the test word to be received on the alternate (non-transmitting) channel first.

(iii) Word Data (CHANNEL B(A) – Like step (i), verify that this word matches the 16-bit word data written in step (4).

(iv Tag Word (ID Word). --- This word should be the same pattern as read in step (ii), except that it will indicate the alternate bus channel from the word represented by verification steps (i) and (ii). In addition, the timing information may be different.

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