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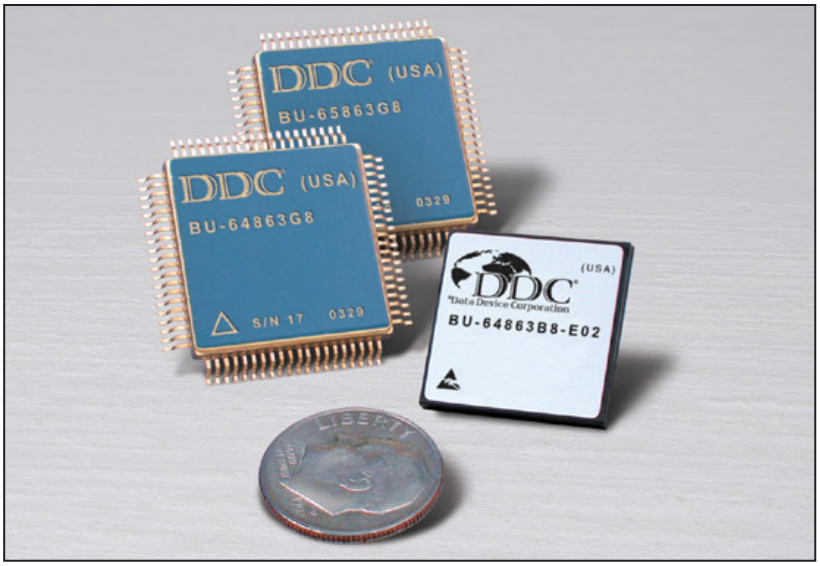
BU-6474X/6484X/6486X

MINI-ACE® MARK3/MICRO-ACE®*-TE



DESCRIPTION

The Mini-ACE Mark3 and Micro-ACE-TE are the world's first MIL-STD-1553 terminals which can be powered entirely by +3.3 volts, thus eliminating the need for a +5 volt power supply. With a package body of 0.880 inches square and a gull wing "toe-to-toe" dimension of 1.110 inches, the Mini-ACE Mark3 is the industry's smallest ceramic gull-lead 1553 terminal. At 0.815 inches square, the Micro-ACE-TE (BGA package) provides the smallest industry footprint, enabling its use in applications where PC board space is at a premium.

These devices integrate dual 3.3 or 5 volt transceivers, 3.3 or 5.0 volt protocol logic, and either 4K or 64K words of internal RAM. The architecture is identical to that of the Enhanced Mini-ACE, and most features are functionally and software compatible with the previous Mini-ACE (Plus) and ACE generations.

A salient feature of the Mini-ACE Mark3 and Micro-ACE-TE is the advanced bus controller architecture. This provides methods to control message scheduling, the means to minimize host overhead for asynchronous message insertion, facilitate bulk data transfers and double buffering, and support various message retry and bus switching strategies.

The remote terminal architecture provides flexibility in meeting all common MIL-STD-1553 protocols. The choice of RT data buffering and interrupt options provides robust support for synchronous and asynchronous messaging, while ensuring data sample consistency and supporting bulk data transfers. The monitor mode provides true message monitoring, and supports filtering on an RT address/T-R bit/subaddress basis.

The Mini-ACE Mark3 and Micro-ACE-TE incorporate fully autonomous built-in self-tests of internal protocol logic and RAM. The terminals provide the same flexibility in host interface configurations as the ACE/Mini-ACE, along with a reduction in the host processor's worst case holdoff time.

FEATURES

- Fully Integrated 3.3 or 5.0 Volt, 1553 A/B Notice 2 Terminal
- World's First all 3.3 Volt Terminal
- Transceiver Power-Down Options
- World's Smallest CQFP MIL-STD-1553 Device
- 80-pin Ceramic Flat/Gull Wing Package or 324-Ball BGA Package
- Enhanced Mini-ACE Architecture
- Multiple Configurations:
  - RT-only, 4K RAM
  - BC/RT/Monitor, 4K RAM
  - BC/RT/Monitor, 64K RAM
- Supports 1553A/B Notice 2, McAir, STANAG 3838 Protocols
- MIL-STD-1553, McAir, and MIL-STD-1760 Transceiver Options
- Highly Flexible Host Side Interface
- Compatible With Mini-ACE and ACE Generations
- Highly Autonomous BC with Built-In Message Sequence Controller
- Choice of Single, Double, and Circular RT Buffering Options
- Selective Message Monitor
- Comprehensive Built-In Self-Test
- Choice Of 10, 12, 16, or 20 MHz Clock Inputs
- Software Libraries and Drivers available for Windows® 9x/2000/XP, Windows NT®, VxWorks® and Linux
- Available with Full Military Temperature Range and Screening

FOR MORE INFORMATION CONTACT:

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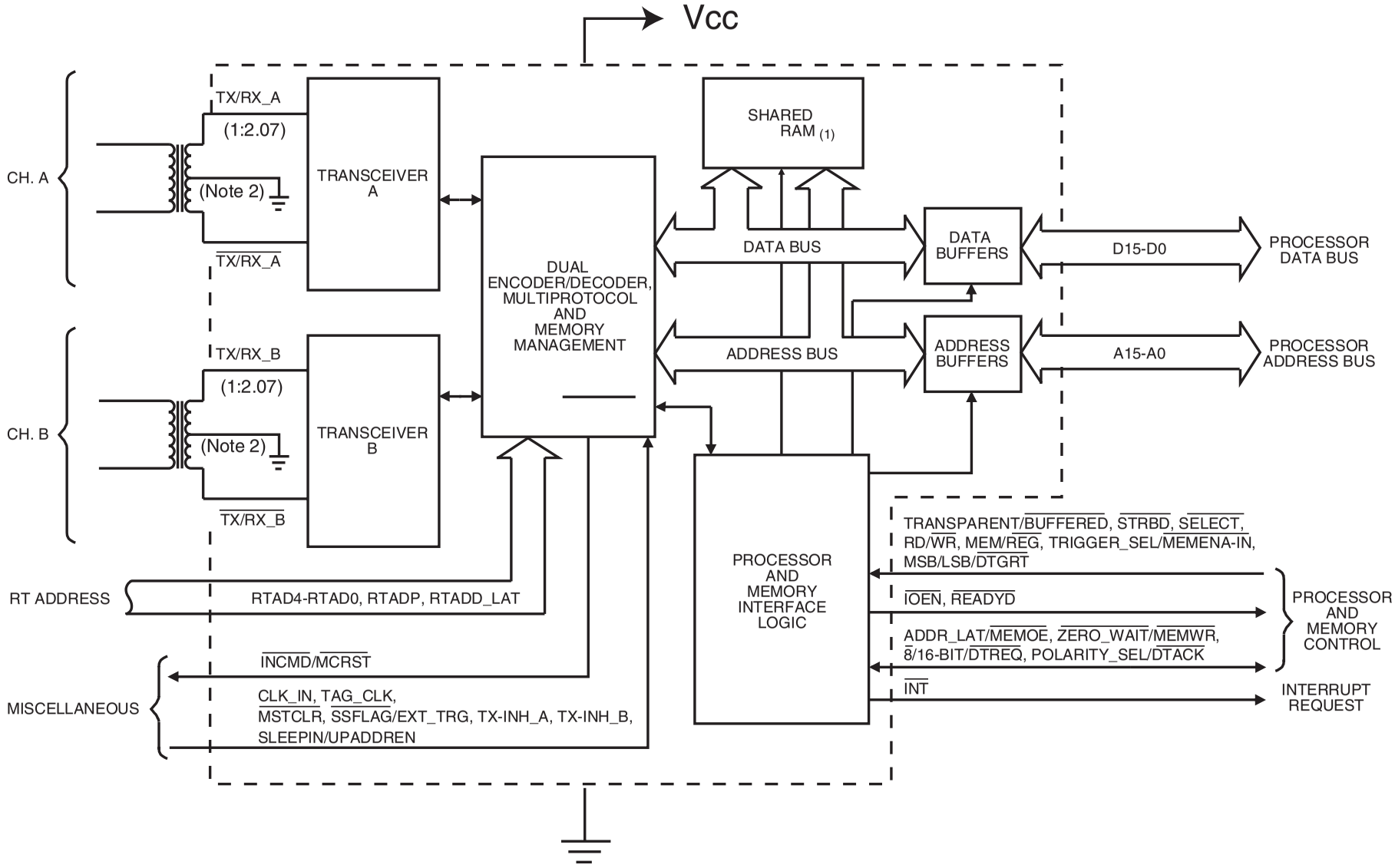
* The technology used in DDC's Micro-ACE series of products may be subject to one or more patents pending.



Notes:
1. See Ordering Information for Available Memory Options.
2. Transformer-coupled configuration and ratio shown.

FIGURE 1. MINI-ACE MARK3 AND MICRO-ACE-TE BLOCK DIAGRAM

TABLE 1. MINI-ACE MARK3 SERIES SPECIFICATIONS

PARAMETER	MIN	TYP	MAX	UNITS
ABSOLUTE MAXIMUM RATING				
Supply Voltage (Note 12)				
• Logic +5V	-0.3		6.0	V
• Logic +3.3V	-0.3		4.1	V
• RAM +5V	-0.3		6.0	V
• Transceivers +5V	-0.3		7.0	V
• Transceivers +3.3V (not during transmit)	-0.3		6.0	V
• Transceivers +3.3V (during transmit)	-0.3		4.5	V
Logic				
• +5V Logic Input Range	-0.3		6.0	V
• +3.3V Logic Input Range	-0.3		6.0	V
MIL-STD-1553 Transceiver Signals				
• BU-64XXXX3/4				
Powered Input Range (Note 17)	-5V_XCVR - 0.3		5V_XCVR + 0.3	V
Unpowered Input Range	-1.5		+1.5	V
• BU-64XXXXC/D				
Powered Input Range (Note 18)	-3.3V_XCVR - 0.3		3.3V_XCVR + 0.3	V
Unpowered Input Range	-1		+1	V
RECEIVER				
Differential Input Resistance (Notes 1-6)				
+5.0V	2.5			kΩ
+3.3V	2.0			kΩ
Differential Input Capacitance (Notes 1-6)				
+5.0V			25	pF
+3.3V			40	pF
Threshold Voltage, Transformer Coupled, Measured on Stub	0.200		0.860	Vp-p
Common-Mode Voltage (Note 7)			10	Vpeak
TRANSMITTER				
Differential Output Voltage				
• Direct Coupled Across 35 Ω, Measured on Bus	6	7	9	Vp-p
• Transformer Coupled Across 70 Ω, Measured on Bus				
BU-64XXXXX-XX0	18	20	27	Vp-p
BU-64XXXXX-XX2 (Note 13)	20	21.5	27	Vp-p
Output Noise, Differential (Direct Coupled)			10	mVp-p
Output Offset Voltage, Transformer Coupled Across 70 Ω	-250		250	mVp
Rise/Fall Time				
BU-64XXXX8/3/C	100	150	300	nsec
BU-64XXXX9/4/D	200	250	300	nsec
LOGIC				
V_{IH}				
All signals except CLK_IN	2.1			V
CLK_IN	0.8•V_{cc}			V
V_{IL}				
All signals except CLK_IN			0.7	V
CLK_IN			0.2•Vcc	V
Schmidt Hysteresis				
All signals except CLK_IN	0.4			V
CLK_IN	1.0			V
I_{IH}, I_{IL}				
All signals except CLK_IN				
I_{IH} (Vcc=3.6V, V_{IN}=Vcc)	-10		10	µA
I_{IH} (Vcc=3.6V, V_{IN}=2.7V)	-350		-33	µA
I_{IL} (Vcc=3.6V, V_{IN}=0.4V)	-350		-33	µA
I_{IH}, I_{IL}				
All signals except CLK_IN				
I_{IH} (Vcc=5.25V, Vin=Vcc)	-10		10	µA
I_{IH} (Vcc=5.25V, I_{IH} Vin=2.7V)	-350		-50	µA
I_{IL} (Vcc=5.25V, Vin=0.4V)	-350		-50	µA
V_{OH} (Vcc=3.0V, V_{IH}=2.7V, V_{IL}=0.2V, I_{OH}=max)	2.4			V
V_{OL} (Vcc=3.0V, V_{IH}=2.7V, V_{IL}=0.2V, I_{OL}=max)			0.4	V
V_{OH} (Vcc=4.5V, V_{IH}=2.7V, V_{IL}=0.2V, I_{OH}=max)	2.4			V
V_{OL} (Vcc=4.5V, V_{IH}=2.7V, V_{IL}=0.2V, I_{OL}=max)			0.4	V

TABLE 1. MINI-ACE MARK3 SERIES SPECIFICATIONS (CONT.)

PARAMETER	MIN	TYP	MAX	UNITS
LOGIC (CONT.)				
CLK_IN				
I_{IH}	-10		10	µA
I_{IL}	-10		10	µA
I_{OL} (Vcc = 4.5V)	3.4			mA
I_{OH} (Vcc = 4.5V)			-3.4	mA
I_{OL} (Vcc = 3.0V)	2.2			mA
I_{OH} (Vcc = 3.0V)			-2.2	mA
C_I (Input Capacitance)		50		pF
C_{IO} (Bi-directional signal input capacitance)		50		pF
POWER SUPPLY REQUIREMENTS				
Voltages/Tolerances (Note 12)				
• Logic +3.3V	3.00	3.3	3.60	V
• Logic +5.0V	4.5	5.0	5.5	V
• RAM +5.0V	4.5	5.0	5.5	V
• Transceivers +3.3V	3.14	3.3	3.46	V
• Transceivers +5.0V	4.75	5.0	5.25	V
Current Drain (Total Hybrid) (Note 14)				
BU-64743X8/9-XX0, BU-64843X8/9-XX0 (1553&McAir)				
• Idle		56	95	mA
• 25% Duty Transmitter Cycle		246	300	mA
• 50% Duty Transmitter Cycle		436	500	mA
• 100% Duty Transmitter Cycle		816	900	mA
BU-64743F/G3/4-XX0, BU-64843F/G3/4-XX0 (1553&McAir)				
+5V (Ch. A, Ch. B)				
• Idle		65	100	mA
• 25% Duty Transmitter Cycle		169	205	mA
• 50% Duty Transmitter Cycle		273	310	mA
• 100% Duty Transmitter Cycle		481	520	mA
• +3.3V (Logic)		25	40	mA
BU-64745F/G3/4-XX0, BU-64845F/G3/4-XX0 (1553&McAir)				
+5V (Logic, RAM, Ch. A, Ch. B)				
• Idle		116	160	mA
• 25% Duty Transmitter Cycle		222	265	mA
• 50% Duty Transmitter Cycle		328	370	mA
• 100% Duty Transmitter Cycle		540	580	mA
BU-64745F/G3-XX2, BU-64845F/G3-XX2 (1760)				
+5V (Logic, RAM, Ch. A, Ch. B)				
• Idle		116	160	mA
• 25% Duty Transmitter Cycle		233	276	mA
• 50% Duty Transmitter Cycle		350	392	mA
• 100% Duty Transmitter Cycle		584	625	mA
BU-64863X8/9-XX0 (1553&McAir)				
• Idle w/ transceiver SLEEPIN enabled		31	69	mA
• Idle w/ transceiver SLEEPIN disabled		77	110	mA
• 25% Duty Transmitter Cycle		267	315	mA
• 50% Duty Transmitter Cycle		457	515	mA
• 100% Duty Transmitter Cycle		837	915	mA
BU-64863F/G3/4-XX0 (1553&McAir)				
+5V (Ch. A, Ch. B)				
• Idle		65	100	mA
• 25% Duty Transmitter Cycle		169	205	mA
• 50% Duty Transmitter Cycle		273	310	mA
• 100% Duty Transmitter Cycle		481	520	mA
• +3.3V (Logic, 64K RAM)		21	55	mA
BU-64743X8-XX2, BU-64843X8-XX2 (1760)				
• Idle		55	95	mA
• 25% Duty Transmitter Cycle		216	315	mA
• 50% Duty Transmitter Cycle		377	535	mA
• 100% Duty Transmitter Cycle		699	975	mA

TABLE 1. MINI-ACE MARK3 SERIES SPECIFICATIONS (CONT.)

PARAMETER	MIN	TYP	MAX	UNITS
POWER SUPPLY REQUIREMENTS (CONT.)				
BU-64743F/G3-XX2, BU-64843F/G3-XX2 (1760)				
+5V (Ch. A, Ch. B)				
• Idle		65	100	mA
• 25% Duty Transmitter Cycle		180	216	mA
• 50% Duty Transmitter Cycle		295	332	mA
• 100% Duty Transmitter Cycle		525	565	mA
• +3.3V (Logic)		25	40	mA
BU-64840B3-X02 (1760)				
+5V (Logic, Ch. A, Ch. B)				
• Idle		116	160	mA
• 25% Duty Transmitter Cycle		233	276	mA
• 50% Duty Transmitter Cycle		350	392	mA
• 100% Duty Transmitter Cycle		584	625	mA
BU-64840B3-X02 (1760)				
+5V (Ch. A, Ch. B)				
• Idle		65	100	mA
• 25% Duty Transmitter Cycle		180	216	mA
• 50% Duty Transmitter Cycle		295	332	mA
• 100% Duty Transmitter Cycle		525	565	mA
• +3.3V (Logic)		25	40	mA
BU-64863X8-XX2 (1760)				
• Idle w/ transceiver SLEEPIN enabled		27	69	mA
• Idle w/ transceiver SLEEPIN disabled		76	110	mA
• 25% Duty Transmitter Cycle		237	330	mA
• 50% Duty Transmitter Cycle		398	550	mA
• 100% Duty Transmitter Cycle		720	990	mA
BU-64863F/G3-XX2 (1760)				
+5V (Ch. A, Ch. B)				
• Idle		65	100	mA
• 25% Duty Transmitter Cycle		180	216	mA
• 50% Duty Transmitter Cycle		295	332	mA
• 100% Duty Transmitter Cycle		525	565	mA
• +3.3V (Logic, 64K RAM)		21	55	mA
BU-64860B(R)3-X02 (1760)				
+5V (Logic, 64K RAM, Ch. A, Ch. B)				
• Idle		116	180	mA
• 25% Duty Transmitter Cycle		228	296	mA
• 50% Duty Transmitter Cycle		340	412	mA
• 100% Duty Transmitter Cycle		563	645	mA
BU-64860B(R)3-X02 (1760)				
+5V (64K RAM, Ch. A, Ch. B)				
• Idle		66	120	mA
• 25% Duty Transmitter Cycle		174	236	mA
• 50% Duty Transmitter Cycle		282	352	mA
• 100% Duty Transmitter Cycle		498	585	mA
• +3.3V (Logic)		25	40	mA
BU-64743X0-XX0, BU-64843X0-XX0 (Xcvrless)		25	40	mA
BU-64863X0-XX0 (Xcvrless)		21	55	mA
BU-64X43XC/D-XXX				
• Idle		25	51	mA
• 25% Duty Transmitter Cycle		158	225	mA
• 50% Duty Transmitter Cycle		316	399	mA
• 100% Duty Transmitter Cycle		608	747	mA
BU-64863XC/D-XXX				
• Idle		46	66	mA
• 25% Duty Transmitter Cycle		179	240	mA
• 50% Duty Transmitter Cycle		337	414	mA
• 100% Duty Transmitter Cycle		629	762	mA

TABLE 1. MINI-ACE MARK3 SERIES SPECIFICATIONS (CONT.)

PARAMETER	MIN	TYP	MAX	UNITS
POWER DISSIPATION				
TOTAL HYBRID (NOTES 14 AND 15)				
BU-64743X8/9-XX0, BU-64843X8/9-XX0 (1553&McAir)				
• Idle		0.18	0.31	W
• 25% Duty Transmitter Cycle		0.57	0.69	W
• 50% Duty Transmitter Cycle		0.91	1.04	W
• 100% Duty Transmitter Cycle		1.58	1.74	W
BU-64743F/G3/4-XX0, BU-64843F/G3/4-XX0 (1553&McAir)				
+3.3V (Logic) +5.0V (Ch. A, Ch. B)				
• Idle		0.41	0.63	W
• 25% Duty Transmitter Cycle		0.70	0.85	W
• 50% Duty Transmitter Cycle		0.94	1.07	W
• 100% Duty Transmitter Cycle		1.40	1.51	W
BU-64745F/G3/4-XX0, BU-64845F/G3/4-XX0 (1553&McAir)				
• Idle		0.64	0.88	W
• 25% Duty Transmitter Cycle		0.93	1.11	W
• 50% Duty Transmitter Cycle		1.22	1.33	W
• 100% Duty Transmitter Cycle		1.81	1.97	W
BU-64745F/G3-XX2, BU-64845F/G3-XX2 (1760)				
• Idle		0.64	0.88	W
• 25% Duty Transmitter Cycle		0.99	1.17	W
• 50% Duty Transmitter Cycle		1.34	1.46	W
• 100% Duty Transmitter Cycle		2.04	2.05	W
BU-64863X8/9-XX0 (1553&McAir)				
• Idle w/ transceiver SLEEPIN enabled		0.10	0.23	W
• Idle w/ transceiver SLEEPIN disabled		0.25	0.36	W
• 25% Duty Transmitter Cycle		0.62	0.73	W
• 50% Duty Transmitter Cycle		0.97	1.09	W
• 100% Duty Transmitter Cycle		1.64	1.79	W
BU-64863F/G3/4-XX0 (1553&McAir)				
+3.3V (Logic, 64K RAM) +5.0V (Ch. A, Ch. B)				
• Idle		0.44	0.68	W
• 25% Duty Transmitter Cycle		0.74	0.90	W
• 50% Duty Transmitter Cycle		0.99	1.12	W
• 100% Duty Transmitter Cycle		1.44	1.56	W
BU-64743X8-XX2, BU-64843X8-XX2 (1760)				
• Idle		0.18	0.31	W
• 25% Duty Transmitter Cycle		0.49	0.71	W
• 50% Duty Transmitter Cycle		0.76	1.08	W
• 100% Duty Transmitter Cycle		1.31	1.83	W
BU-64743F/G3-XX2, BU-64843F/G3-XX2 (1760)				
+3.3V (Logic) +5.0V (Ch. A, Ch. B)				
• Idle		0.41	0.63	W
• 25% Duty Transmitter Cycle		0.72	0.86	W
• 50% Duty Transmitter Cycle		0.97	1.09	W
• 100% Duty Transmitter Cycle		1.45	1.56	W
BU-64840B3-X02 (1760)				
+5.0V (Logic, Ch. A, Ch. B)				
• Idle		0.58	0.80	W
• 25% Duty Transmitter Cycle		0.87	1.03	W
• 50% Duty Transmitter Cycle		1.13	1.26	W
• 100% Duty Transmitter Cycle		1.62	1.73	W
BU-64840B3-X02 (1760)				
+3.3V (Logic) +5.0V (Ch. A, Ch. B)				
• Idle		0.41	0.63	W
• 25% Duty Transmitter Cycle		0.72	0.86	W
• 50% Duty Transmitter Cycle		0.97	1.09	W
• 100% Duty Transmitter Cycle		1.45	1.56	W
BU-64X43XC/D-XXX				
• Idle		0.08	0.19	W
• 25% Duty Transmitter Cycle		0.22	0.33	W
• 50% Duty Transmitter Cycle		0.32	0.47	W
• 100% Duty Transmitter Cycle		0.45	0.62	W

TABLE 1. MINI-ACE MARK3 SERIES SPECIFICATIONS (CONT.)

PARAMETER	MIN	TYP	MAX	UNITS
POWER DISSIPATION (CONT)				
TOTAL HYBRID (NOTES 14 AND 15)				
BU-64863X8-XX2 (1760)				
• Idle w/ transceiver SLEEPIN enabled		0.09	0.23	W
• Idle w/ transceiver SLEEPIN disabled		0.25	0.36	W
• 25% Duty Transmitter Cycle		0.53	0.74	W
• 50% Duty Transmitter Cycle		0.93	1.12	W
• 100% Duty Transmitter Cycle		1.36	1.87	W
BU-64863F/G3-XX2 (1760)				
+3.3V (Logic, 64K RAM) +5.0V (Ch. A, Ch. B)				
• Idle		0.44	0.68	W
• 25% Duty Transmitter Cycle		0.76	0.91	W
• 50% Duty Transmitter Cycle		1.01	1.14	W
• 100% Duty Transmitter Cycle		1.50	1.61	W
BU-64860B(R)3-X02 (1760)				
+5.0V (Logic, Ch. A, Ch. B, 64K RAM)				
• Idle		0.64	0.90	W
• 25% Duty Transmitter Cycle		0.87	1.13	W
• 50% Duty Transmitter Cycle		1.12	1.36	W
• 100% Duty Transmitter Cycle		1.60	1.83	W
BU-64860B(R)3-X02 (1760)				
+3.3V (Logic) +5.0V (Ch. A, Ch. B, 64K RAM)				
• Idle		0.40	0.73	W
• 25% Duty Transmitter Cycle		0.71	0.96	W
• 50% Duty Transmitter Cycle		0.95	1.19	W
• 100% Duty Transmitter Cycle		1.41	1.66	W
BU-64743X0-XX0, BU-64843X0-XX0 (Xcvrless)		0.08	0.132	W
BU-64863X0-XX0 (Xcvrless)		0.07	0.182	W
BU-64863XC/D-XXX				
• Idle		0.15	0.24	W
• 25% Duty Transmitter Cycle		0.29	0.38	W
• 50% Duty Transmitter Cycle		0.39	0.52	W
• 100% Duty Transmitter Cycle		0.52	0.67	W
HOTTEST DIE				
BU-64XXXX8/9-XX0 (1553&McAir)				
• Idle w/ transceiver SLEEPIN enabled (BU-64863 only)		0.01	0.02	W
• Idle w/ transceiver SLEEPIN disabled		0.05	0.09	W
• 25% Duty Transmitter Cycle		0.39	0.47	W
• 50% Duty Transmitter Cycle		0.72	0.82	W
• 100% Duty Transmitter Cycle		1.38	1.52	W
BU-64XXXX3/4-XX0 (1553&McAir)				
• Idle		0.16	0.25	W
• 25% Duty Transmitter Cycle		0.39	0.47	W
• 50% Duty Transmitter Cycle		0.61	0.69	W
• 100% Duty Transmitter Cycle		1.06	1.13	W
BU-64XXXX8-XX2 (1760)				
• Idle w/ transceiver SLEEPIN enabled (BU-64863 only)		0.01	0.02	W
• Idle w/ transceiver SLEEPIN disabled		0.05	0.09	W
• 25% Duty Transmitter Cycle		0.39	0.49	W
• 50% Duty Transmitter Cycle		0.60	0.85	W
• 100% Duty Transmitter Cycle		1.15	1.61	W
HOTTEST DIE				
BU-64XXXX3-XX2 (1760)				
• Idle		0.16	0.25	W
• 25% Duty Transmitter Cycle		0.40	0.48	W
• 50% Duty Transmitter Cycle		0.63	0.71	W
• 100% Duty Transmitter Cycle		1.11	1.18	W
BU-64XX3X0-XX0 (Xcvrless)		0.08	0.13	W
BU-64XX3XC/D-XXX				
• Idle		0.07	0.11	W
• 25% Duty Transmitter Cycle		0.20	0.25	W
• 50% Duty Transmitter Cycle		0.30	0.39	W
• 100% Duty Transmitter Cycle		0.42	0.54	W

TABLE 1. MINI-ACE MARK3 SERIES SPECIFICATIONS (CONT.)

PARAMETER	MIN	TYP	MAX	UNITS
CLOCK INPUT				
• Frequency:				
Nominal Values				
Default Mode		16.0		MHz
Option		12.0		MHz
Option		10.0		MHz
Option		20.0		MHz
• Long Term Tolerance				
1553A Compliance	0.01		-0.01	%
1553B Compliance	0.10		-0.10	%
• Short Term Tolerance, 1 second				
1553A Compliance	-0.001		0.001	%
1553B Compliance	-0.01		0.01	%
Duty Cycle	40		60	%
1553 MESSAGE TIMING				
Completion of CPU Write (BC Start)-to-Start of First Message for Non-enhanced BC Mode		2.5		µs
BC Intermessage Gap (Note 8)				
Non-enhanced (Mini-ACE compatible) BC mode		9.5		µs
Enhanced BC mode (Note 9)		10 to 10.5		µs
BC/RT/MT Response Timeout (Note 10)				
• 18.5 nominal	17.5	18.0	19.5	µs
• 22.5 nominal	21.5	22.5	23.5	µs
• 50.5 nominal	49.5	50.5	51.5	µs
• 128.0 nominal	127	129.5	131	µs
RT Response Time (mid-parity to mid-sync) (Note 11)	4		7	µs
Transmitter Watchdog Timeout		660.5		µs
THERMAL				
FLAT PACK/GULL WING				
80-pin Ceramic Package Thermal Resistance, Junction-to-Case, Hottest Die (θ_{JC}) Note 16		9	11	°C/W
MICRO-ACE-TE BGA				
324-ball BGA Package			15	°C/W
(See Thermal Management Section)				
Active Transceiver (Hottest Die)				
• Junction-to-Ambient (θ_{JA} via simulation)				
- Per JESD 51-2 standard at 25°C				
θ_{JA} in Still Air		55.0		°C/W
- Per JESD 51-6 standard at 25°C				
θ_{JA} @1M/S		44.5		°C/W
θ_{JA} @2M/S		41.8		°C/W
• Junction-to-Case (θ_{JC} via simulation)				
- Per JESD 51-12 standard at 25°C				
θ_{JC}		20.8		°C/W
• Junction-to-Board (θ_{JB} via simulation)				
- Per JESD 51-2 standard at 25°C				
θ_{JB}		31.1		°C/W
ALL PACKAGES				
Operating Case/Ball Temperature				
-1XX, -4XX	-55		+125	°C
-2XX, -5XX	-40		+85	°C
-3XX, -8XX	0		+70	°C
-EXX	-40		+100	°C
Operating Junction Temperature				
• Transceiver	-55		+150	°C
• Protocol	-55		+135	°C
• Memory	-55		+140	°C
Storage Temperature	-65		+150	°C

TABLE 1. MINI-ACE MARK3 SERIES SPECIFICATIONS (CONT.)

PARAMETER	MIN	TYP	MAX	UNITS
SOLDERING/MOUNTING				
FLAT PACK/GULL WING				
Lead Temperature (soldering, 10 sec.)		+300		°C
324-BALL BGA PACKAGE				
The reflow profile detailed in IPC/JEDEC J-STD-020 is applicable for both leaded and lead-free products		+250		°C
Refer to DDC's Application Note #A/N49 "BGA User's Guide" for additional important mounting information.				
PHYSICAL CHARACTERISTICS				
Package Body Size				
80-pin Ceramic Flat pack or Gull Wing		0.880 X 0.880 X 0.13 (22.35 X 22.35 X 3.3)		in. (mm)
324-ball BGA		0.815 X 0.815 X 0.12 (20.7 X 20.7 X 3.05)		in. (mm)
Micro-ACE-TE				
Moisture Sensitivity Level		MSL-3		
Electrostatic Discharge Sensitivity		ESD Class 0		
Lead Toe-to-Toe Distance 80-pin Gull Wing		1.110 (28.194)		in. (mm)
Weight				
80-pin Ceramic Flat pack or Gull Wing		0.353 (10)		oz (g)
324-ball BGA		.088 (2.5)		oz (g)

TABLE 1 Notes:

Notes 1 through 6 are applicable to the Receiver Differential Resistance and Receiver Differential Input Capacitance specifications:

(1) Specifications include both transmitter and receiver (tied together internally).

(2) Impedance parameters are specified directly between pins TX/RX_A(B) and $\overline{\text{TX/RX\_A(B)}}$ of the Mini-ACE Mark3 hybrid.

(3) It is assumed that all power and ground inputs to the hybrid are connected.

(4) The specifications are applicable for both unpowered and powered conditions.

(5) The specifications assume a 2 volt rms balanced, differential, sinusoidal input. The applicable frequency range is 75 kHz to 1 MHz.

(6) Minimum resistance and maximum capacitance parameters are guaranteed over the operating range, but are not tested.

(7) Assumes a common-mode voltage within the frequency range of dc to 2 MHz, applied to pins of the isolation transformer on the stub side (either direct or transformer coupled), and referenced to hybrid ground. Transformer must be a DDC recommended transformer or other transformer that provides an equivalent minimum CMRR.

(8) Typical value for minimum intermessage gap time. Under software control, this may be lengthened (to 65,535 ms - message time) in increments of 1 µs. If ENHANCED CPU ACCESS, bit 14 of Configuration Register #6, is set to logic "1", then host accesses during BC Start-of-Message (SOM) and End-of-Message (EOM) transfer sequences could have the effect of lengthening the intermessage gap time. For each host access during an SOM or EOM sequence, the intermessage gap time will be lengthened by 6 clock cycles. Since there are 7 internal transfers during SOM and 5 during EOM, this could theoretically lengthen the intermessage gap by up to 72 clock cycles; i.e., up to 7.2 ms with a 10 MHz clock, 6.0 µs with a 12 MHz clock, 4.5 µs with a 16 MHz clock, or 3.6 µs with a 20 MHz clock.

(9) For Enhanced BC mode, the typical value for intermessage gap time is approximately 10 clock cycles longer than for the non-enhanced BC mode. That is, an addition of 1.0 µs at 10 MHz, 833 ns at 12 MHz, 625 ns at 16 MHz, or 500 ns at 20 MHz.

TABLE 1 Notes (Cont.):

(10) Software programmable (4 options). Includes RT-to-RT Timeout (measured mid-parity of transmit Command Word to mid-sync of transmitting RT Status Word).

(11) Measured from mid-parity crossing of Command Word to mid-sync crossing of RT's Status Word.

(12) External 10 µF tantalum and 0.1 µF capacitors should be located as close as possible to the voltage input pins/balls.

(13) MIL-STD-1760 requires a 20 Vp-p minimum output on the stub connection.

(14) Current drain and power dissipation specs are preliminary and subject to change.

(15) Power dissipation is the input power minus the power delivered to the 1553 fault isolation resistors, the power delivered to the bus termination resistors, and the copper losses in the transceiver isolation transformer and the bus coupling transformer. An illustration of external power dissipation for transformer coupled configuration (while transmitting) is: 0.14 watts for the active isolation transformer, 0.08 watts for the active bus coupling transformer, 0.45 watts for each of the two bus isolation resistors and 0.15 watts for each of the two bus termination resistors.

(16) θJC is measured to bottom of ceramic case.

(17) Assuming the use of isolation transformers with the turns ratios shown in Figure 16 and in the absence of common mode signal on the 1553 stub, this equates to a nominal stub voltage of 38 Volts$_{PK\text{-}to\text{-}PK}$ transformer-coupled, or 53 Volts$_{PK\text{-}to\text{-}PK}$ direct-coupled.

(18) Assuming the use of isolation transformers with the turns ratios shown in Figure 16 and in the absence of common mode signal on the 1553 stub, this equates to a nominal stub voltage of 29.8 Volts$_{PK\text{-}to\text{-}PK}$ transformer-coupled, or 38.2 Volts$_{PK\text{-}to\text{-}PK}$ direct-coupled."

INTRODUCTION

The Mini-ACE Mark3 is the world's first MIL-STD-1553 terminal which can be powered entirely by 3.3 volts, thus eliminating the need for a 5 volt power supply. The BU-6474X RT only, and BU-6484X/6486X BC/RT/MT Mini-ACE Mark3 family of MIL-STD-1553 terminals comprise a complete integrated interface between a host processor and a MIL-STD-1553 bus. The Mini-ACE Mark3 is available in a 0.88 square inch flat pack or gull wing package with a "toe-to-toe" dimension of 1.110 inches, as well as a 324-ball BGA. The Mini-ACE Mark3 is the industry's smallest ceramic gull-lead 1553 terminal, enabling its use in applications where PC board space is at a premium. At 0.815 inches square, the Micro-ACE-TE provides the smallest MIL-STD-1553 footprint in the industry. The Mark3's architecture is identical to that of the Enhanced Mini-ACE, and most features are functionally and software compatible with the previous Mini-ACE (Plus) and ACE generations.

The Mini-ACE Mark3 provides complete multiprotocol support of MIL-STD-1553A/B/McAir and STANAG 3838. The Mark3 integrates dual transceiver, protocol logic, and either 4K or 64K words of internal RAM. The BU-6486X BC/RT/MT terminal includes 64K words of internal RAM, with built-in parity checking.

The Mini-ACE Mark3 includes dual 3.3 volt or 5.0 volt voltage source transceivers for improved line driving capability, with options for MIL-STD-1760 and McAir compatibility. Mark3 versions with 64K x 17 RAM and all versions of the Micro-ACE-TE with the 8/9 transceiver option offer an additional transceiver power-down (SLEEPIN) option to further reduce device power consumption. To provide further flexibility, the Mini-ACE Mark3 may operate with a choice of 10, 12, 16, or 20 MHz clock inputs.

One of the new salient features of the Mark3 is its Enhanced bus controller architecture. The Enhanced BC's highly autonomous message sequence control engine provides a means for offloading the host processor for implementing multiframe message scheduling, message retry schemes, data double buffering, and asynchronous message insertion. For the purpose of performing messaging to the host processor, the Enhanced BC mode includes a General Purpose Queue, along with user-defined interrupts.

A second major new feature of the Mark3 is the incorporation of a fully autonomous built-in self-test. This test provides comprehensive testing of the internal protocol logic. A separate test verifies the operation of the internal RAM. Since the self-tests are fully autonomous, they eliminate the need for the host to write and read stimulus and response vectors.

The Mini-ACE Mark3 RT offers the same choices of single, double, and circular buffering for individual subaddresses as the ACE, Mini-ACE (Plus) and Enhanced Mini-ACE. New enhancements to the RT architecture include a global circular buffering option for multiple (or all) receive subaddresses, a 50% rollover interrupt for circular buffers, an interrupt status queue for logging up to 32 interrupt events, and an option to automatically initialize to RT mode with the Busy bit set. The interrupt status queue and 50% rollover interrupt features are also included as improvements to the Mark3's Monitor architecture.

To minimize board space and "glue" logic, the Mini-ACE Mark3 terminals provide the same wide choice of host interface configurations as the ACE, Mini-ACE (Plus) and Enhanced Mini-ACE. This includes support of interfaces to 16-bit or 8-bit processors, memory or port type interfaces, and multiplexed or non-multiplexed address/data buses. In addition, with respect to ACE/Mini-ACE (Plus), the worst case processor wait time has been significantly reduced. For example, assuming a 16 MHz clock, this time has been reduced from 2.8 µs to 632 ns for read accesses, and to 570 ns for write accesses.

The Mini-ACE Mark3 series terminals operate over the full military temperature range of -55 to +125°C and are available screened to MIL-PRF-38534C. The terminals are ideal for military and industrial processor-to-1553 applications powered by 3.3 volts only.

MICRO-ACE-TE IN SIMPLE SYSTEM RT (SSRT) MODE

The Micro-ACE-TE with 4K RAM (BU-64843B(R)8), MIL-STD-1553 terminal can provide a complete interface between a simple system and a MIL-STD-1553 bus when configured as an SSRT. These terminals integrate dual transceiver, protocol logic, and a FIFO memory for received messages in a 324-ball BGA. The internal architecture is identical to that of the original BU-61703/61705 Simple System RT (SSRT).

The SSRT configured Micro-ACE-TE incorporates a built-in self-test (BIT). This BIT, which is processed following power turn-on or after receipt of an Initiate self-test mode command, provides a comprehensive test of the encoders, decoders, protocol, transmitter watchdog timer, and protocol section. The SSRT configured, Micro-ACE-TE also includes an auto-configuration feature.

The Micro-ACE-TE when configured as an SSRT is ideal for munitions stores and other simple systems that do not require a microprocessor. To streamline the interface to simple systems it includes an internal 32-word FIFO for received data words. This serves to ensure that only complete, consistent blocks of validated data words are transferred to a system.

Detailed SSRT configuration information can be found in Application Note AN/B-37.

TEST COMPONENTS

Daisy chain mechanical samples of the Micro-ACE-TE, 324-ball BGA (BU-64863B8-600) are available. These are used to verify both the electrical and mechanical integrity of the solder joints between the BGA package and the board. Ball pairs are internally wired so that the user can test for electrical continuity between balls. Refer to TABLE 70 for interconnection details.

Although these units are inert, they are fully populated with silicon die so that they closely match the thermal and mechanical characteristics of standard production units. Internal daisy chain interconnections are made by copper PWB traces.

TRANSCEIVERLESS "COMPATIBLE" VERSION OF MICRO-ACE-TE

All versions of the Micro-ACE-TE, 324-ball BGA are transceiverless "Compatible". These devices contain fully functional, dual-redundant, MIL-STD-1553 transceivers with internal / intermediate connections brought out to balls. These intermediate connections allow devices to be used in transceiverless mode for direct interfacing to MIL-STD-1773 (fiber optic) transceivers. Mandatory Additional Connections (See TABLE 59) are required if these devices are **not** utilized in their transceiverless mode.

BU-61860E3 +5.0V µ-ACE (MICRO-ACE) & TRANSFORMER EVALUATION BOARD

The BU-61860E3 board is intended to support customers who are interested in electrically connecting and evaluating the performance of +5.0V Enhanced Mini-ACE and/or +5.0V µ-ACE series of products. The user will be able to quickly perform functional tests and run their system software utilizing this relatively small (2.0" x 2.5") evaluation board.

The BU-61860E3 (see FIGURE 19) consists of a PC board incorporating a +5.0V µ-ACE (BU-61860B3, BC / RT / MT with 64K x 17 RAM), necessary decoupling capacitors, and associated isolation transformers. The MIL-STD-1760 outputs are user configurable as either Stub (transformer) or Direct coupling. The board supports the signal fan-out (see TABLE 72) of the +5.0V µ-ACE to 112 pins subdivided into (4) dual inline, berg type pin rows. These pins (0.025" square max) and their row placement adhere to standard 0.100" vector board spacing.

BU-64863E8 MINI-ACE MARK3 (+3.3V) & TRANSFORMER EVALUATION BOARD

The BU-64863E8 board is intended to support customers who are interested in electrically connecting and evaluating the performance of the +3.3V Mini-ACE Mark3 and/or +3.3V Micro-ACE-TE series of products. The user will be able to quickly perform functional tests and run their system software utilizing this relatively small (2.0" x 2.5") evaluation board.

The BU-64863E8 (see FIGURE 20) consists of a PC board incorporating a +3.3V Mini-ACE Mark3 (BU-64863G8, BC / RT / MT with 64K x 17 RAM), necessary decoupling capacitors, and associated isolation transformers. The MIL-STD-1553 outputs have been factory configured for Stub (transformer) coupling. The board supports the signal fan-out (see TABLE 71) of the +3.3V Mini-ACE Mark3 to 112 pins subdivided into (4) dual inline, berg type pin rows. These pins (0.025" square max) and their row placement adhere to standard 0.100" vector board spacing.

TRANSCEIVERS

The transceivers in the Mini-ACE Mark3 series terminals are fully monolithic, requiring only a +3.3 or 5.0 volt power input. The transmitters are voltage sources, providing improved line driving capability over current sources. This serves to improve performance on long buses with many taps. Mark3 versions with 64K x 17 RAM and all versions of tthe Micro-ACE-TE with the 8/9 transceiver option offer an additional transceiver power-down (SLEEPIN) option to further reduce device power consumption. The transmitters also offer an option that satisfies the MIL-STD-1760 requirement for a minimum of 20 volts peak-to-peak, transformer coupled output.

Besides eliminating the demand for an additional power supply, the use of a +3.3 volt only transceiver (5.0 volt available) requires the use of a step-up, rather than a step-down, isolation transformer. This provides the advantage of a higher terminal input impedance than is possible for a 15V, 12V or 5V transmitter. As a result, there is a greater margin for the input impedance test, mandated for the 1553 validation test. This allows for longer cable lengths between a system connector and the isolation transformers of an embedded 1553 terminal.

To provide compatibility to McAir specs, the Mini-ACE Mark3 is available with an option for transmitters with increased rise and fall times.

The receiver sections of the Mini-ACE Mark3 are fully compliant with MIL-STD-1553B Notice 2 in terms of front end overvoltage protection, threshold, common-mode rejection, and word error rate.

REGISTER AND MEMORY ADDRESSING

The software interface of the Mini-ACE Mark3 to the host processor consists of 24 internal operational registers for normal operation, an additional 24 test registers, plus 64K words of shared memory address space. The Mini-ACE Mark3's 4K X 16 or 64K X 17 internal RAM resides in this address space.

For normal operation, the host processor only needs to access the lower 32 register address locations (00-1F). The next 32 locations (20-3F) should be reserved, since many of these are used for factory test.

INTERNAL REGISTERS

The address mapping for the Mini-ACE Mark3 registers is illustrated in TABLE 2.

TABLE 2. ADDRESS MAPPING

ADDRESS LINES					REGISTER DESCRIPTION/ACCESSIBILITY
A4	A3	A2	A1	A0	
0	0	0	0	0	Interrupt Mask Register #1 (RD/WR)
0	0	0	0	1	Configuration Register #1 (RD/WR)
0	0	0	1	0	Configuration Register #2 (RD/WR)
0	0	0	1	1	Start/Reset Register (WR)
0	0	0	1	1	Non-Enhanced BC/RT Command Stack Pointer / Enhanced BC Instruction List Pointer Register (RD)
0	0	1	0	0	BC Control Word / RT Subaddress Control Word Register (RD/WR)
0	0	1	0	1	Time Tag Register (RD/WR)
0	0	1	1	0	Interrupt Status Register #1 (RD)
0	0	1	1	1	Configuration Register #3 (RD/WR)
0	1	0	0	0	Configuration Register #4 (RD/WR)
0	1	0	0	1	Configuration Register #5 (RD/WR)
0	1	0	1	0	RT / Monitor Data Stack Address Register (RD)
0	1	0	1	1	BC Frame Time Remaining Register (RD)
0	1	1	0	0	BC Time Remaining to Next Message Register (RD)
0	1	1	0	1	Non-Enhanced BC Frame Time / Enhanced BC Initial Instruction Pointer / RT Last Command / MT Trigger Word Register (RD/WR)
0	1	1	1	0	RT Status Word Register (RD)
0	1	1	1	1	RT BIT Word Register (RD)
1	0	0	0	0	Test Mode Register 0
1	0	0	0	1	Test Mode Register 1
1	0	0	1	0	Test Mode Register 2
1	0	0	1	1	Test Mode Register 3
1	0	1	0	0	Test Mode Register 4
1	0	1	0	1	Test Mode Register 5
1	0	1	1	0	Test Mode Register 6
1	0	1	1	1	Test Mode Register 7
1	1	0	0	0	Configuration Register #6 (RD/WR)
1	1	0	0	1	Configuration Register #7 (RD/WR)
1	1	0	1	0	RESERVED
1	1	0	1	1	BC Condition Code Register (RD)
1	1	0	1	1	BC General Purpose Flag Register (WR)
1	1	1	0	0	BIT Test Status Register (RD)
1	1	1	0	1	Interrupt Mask Register #2 (RD/WR)
1	1	1	1	0	Interrupt Status Register #2 (RD)
1	1	1	1	1	BC General Purpose Queue Pointer / RT-MT Interrupt Status Queue Pointer Register (RD/WR)

TABLE 3. INTERRUPT MASK REGISTER #1 (READ/WRITE 00H)

BIT	DESCRIPTION
15(MSB)	RESERVED
14	RAM PARITY ERROR
13	BC/RT TRANSMITTER TIMEOUT
12	BC/RT COMMAND STACK ROLLOVER
11	MT COMMAND STACK ROLLOVER
10	MT DATA STACK ROLLOVER
9	HANDSHAKE FAIL
8	BC RETRY
7	RT ADDRESS PARITY ERROR
6	TIME TAG ROLLOVER
5	RT CIRCULAR BUFFER ROLLOVER
4	BC CONTROL WORD/RT SUBADDRESS CONTROL WORD EOM
3	BC END OF FRAME
2	FORMAT ERROR
1	BC STATUS SET/RT MODE CODE/MT PATTERN TRIGGER
0(LSB)	END OF MESSAGE

TABLE 4. CONFIGURATION REGISTER #1 (READ/WRITE 01H)				
BIT	**BC FUNCTION (Bits 11-0 Enhanced Mode Only)**	**RT WITHOUT ALTERNATE STATUS**	**RT WITH ALTERNATE STATUS (Enhanced Only)**	**MONITOR FUNCTION (Enhanced mode only bits 12-0)**
15 (MSB)	RT/$\overline{\text{BC-MT}}$ (logic 0)	(logic 1)	(logic 1)	(logic 0)
14	MT/$\overline{\text{BC-RT}}$ (logic 0)	(logic 0)	(logic 0)	(logic 1)
13	CURRENT AREA B/$\overline{\text{A}}$	CURRENT AREA B/$\overline{\text{A}}$	CURRENT AREA B/A	CURRENT AREA B/A
12	MESSAGE STOP-ON-ERROR	MESSAGE MONITOR ENABLED (MMT)	MESSAGE MONITOR ENABLED	MESSAGE MONITOR ENABLED
11	FRAME STOP-ON-ERROR	$\overline{\text{DYNAMIC BUS CONTROL ACCEPTANCE}}$	S10	TRIGGER WORD ENABLED
10	STATUS SET STOP-ON-MESSAGE	$\overline{\text{BUSY}}$	S09	START-ON-TRIGGER
9	STATUS SET STOP-ON-FRAME	$\overline{\text{SERVICE REQUEST}}$	S08	STOP-ON-TRIGGER
8	FRAME AUTO-REPEAT	$\overline{\text{SSFLAG}}$	S07	NOT USED
7	EXTERNAL TRIGGER ENABLED	$\overline{\text{RTFLAG}}$ (Enhanced Mode Only)	S06	EXTERNAL TRIGGER ENABLED
6	INTERNAL TRIGGER ENABLED	NOT USED	S05	NOT USED
5	INTERMESSAGE GAP TIMER ENABLED	NOT USED	S04	NOT USED
4	RETRY ENABLED	NOT USED	S03	NOT USED
3	DOUBLED/$\overline{\text{SINGLE}}$ RETRY	NOT USED	S02	NOT USED
2	BC ENABLED (Read Only)	NOT USED	S01	MONITOR ENABLED (Read Only)
1	BC FRAME IN PROGRESS (Read Only)	NOT USED	S00	MONITOR TRIGGERED (Read Only)
0 (LSB)	BC MESSAGE IN PROGRESS (Read Only)	RT MESSAGE IN PROGRESS (Enhanced mode only, Read Only)	RT MESSAGE IN PROGRESS (Read Only)	MONITOR ACTIVE (Read Only)

TABLE 5. CONFIGURATION REGISTER #2 (READ/WRITE 02H)	
BIT	**DESCRIPTION**
15(MSB)	ENHANCED INTERRUPTS
14	RAM PARITY ENABLE
13	BUSY LOOKUP TABLE ENABLE
12	RX SA DOUBLE BUFFER ENABLE
11	OVERWRITE INVALID DATA
10	256-WORD BOUNDARY DISABLE
9	TIME TAG RESOLUTION 2
8	TIME TAG RESOLUTION 1
7	TIME TAG RESOLUTION 0
6	CLEAR TIME TAG ON SYNCHRONIZE
5	LOAD TIME TAG ON SYNCHRONIZE
4	INTERRUPT STATUS AUTO CLEAR
3	LEVEL/$\overline{\text{PULSE}}$ INTERRUPT REQUEST
2	CLEAR SERVICE REQUEST
1	ENHANCED RT MEMORY MANAGEMENT
0(LSB)	SEPARATE BROADCAST DATA

TABLE 6. START/RESET REGISTER (WRITE 03H)	
BIT	**DESCRIPTION**
15(MSB)	RESERVED
14	RESERVED
13	RESERVED
12	RESERVED
11	CLEAR RT HALT
10	CLEAR SELF-TEST REGISTER
9	INITIATE RAM SELF-TEST
8	RESERVED
7	INITIATE PROTOCOL SELF-TEST
6	BC/MT STOP-ON-MESSAGE
5	BC STOP-ON-FRAME
4	TIME TAG TEST CLOCK
3	TIME TAG RESET
2	INTERRUPT RESET
1	BC/MT START
0(LSB)	RESET

TABLE 7. BC/RT COMMAND STACK POINTER REG. (READ 03H)	
BIT	**DESCRIPTION**
15(MSB)	COMMAND STACK POINTER 15
•	•
•	•
•	•
0(LSB)	COMMAND STACK POINTER 0

TABLE 8. BC CONTROL WORD REGISTER (READ/WRITE 04H)	
BIT	**DESCRIPTION**
15(MSB)	TRANSMIT TIME TAG FOR SYNCHRONIZE MODE COMMAND
14	MESSAGE ERROR MASK
13	SERVICE REQUEST BIT MASK
12	BUSY BIT MASK
11	SUBSYSTEM FLAG BIT MASK
10	TERMINAL FLAG BIT MASK
9	RESERVED BITS MASK
8	RETRY ENABLED
7	BUS CHANNEL A/B
6	OFF-LINE SELF-TEST
5	MASK BROADCAST BIT
4	EOM INTERRUPT ENABLE
3	1553A/B SELECT
2	MODE CODE FORMAT
1	BROADCAST FORMAT
0(LSB)	RT-to-RT FORMAT

TABLE 9. RT SUBADDRESS CONTROL WORD (READ/WRITE 04H)	
BIT	**DESCRIPTION**
15(MSB)	RX: DOUBLE BUFFER ENABLE
14	TX: EOM INT
13	TX: CIRC BUF INT
12	TX: MEMORY MANAGEMENT 2 (MM2)
11	TX: MEMORY MANAGEMENT 1 (MM1)
10	TX: MEMORY MANAGEMENT 0 (MM0)
9	RX: EOM INT
8	RX: CIRC BUF INT
7	RX: MEMORY MANAGEMENT 2 (MM2)
6	RX: MEMORY MANAGEMENT 1 (MM1)
5	RX: MEMORY MANAGEMENT 0 (MM0)
4	BCST: EOM INT
3	BCST: CIRC BUF INT
2	BCST: MEMORY MANAGEMENT 2 (MM2)
1	BCST: MEMORY MANAGEMENT 1 (MM1)
0(LSB)	BCST: MEMORY MANAGEMENT 0 (MM0)

TABLE 10. TIME TAG REGISTER (READ/WRITE 05H)	
BIT	**DESCRIPTION**
15(MSB)	TIME TAG 15
•	•
•	•
•	•
0(LSB)	TIME TAG 0

TABLE 11. INTERRUPT STATUS REGISTER #1 (READ 06H)	
BIT	**DESCRIPTION**
15(MSB)	MASTER INTERRUPT
14	RAM PARITY ERROR
13	TRANSMITTER TIMEOUT
12	BC/RT COMMAND STACK ROLLOVER
11	MT COMMAND STACK ROLLOVER
10	MT DATA STACK ROLLOVER
9	HANDSHAKE FAIL
8	BC RETRY
7	RT ADDRESS PARITY ERROR
6	TIME TAG ROLLOVER
5	RT CIRCULAR BUFFER ROLLOVER
4	BC CONTROL WORD/RT SUBADDRESS CONTROL WORD EOM
3	BC END OF FRAME
2	FORMAT ERROR
1	BC STATUS SET / RT MODE CODE / MT PATTERN TRIGGER
0(LSB)	END OF MESSAGE

TABLE 12. CONFIGURATION REGISTER #3 (READ/WRITE 07H)	
BIT	**DESCRIPTION**
15(MSB)	ENHANCED MODE ENABLE
14	BC/RT COMMAND STACK SIZE 1
13	BC/RT COMMAND STACK SIZE 0
12	MT COMMAND STACK SIZE 1
11	MT COMMAND STACK SIZE 0
10	MT DATA STACK SIZE 2
9	MT DATA STACK SIZE 1
8	MT DATA STACK SIZE 0
7	ILLEGALIZATION DISABLED
6	OVERRIDE MODE T/$\overline{R}$ ERROR
5	ALTERNATE STATUS WORD ENABLE
4	ILLEGAL RX TRANSFER DISABLE
3	BUSY RX TRANSFER DISABLE
2	$\overline{\text{RTFAIL}}$ / $\overline{\text{RTFLAG}}$ WRAP ENABLE
1	1553A MODE CODES ENABLE
0(LSB)	ENHANCED MODE CODE HANDLING

TABLE 13. CONFIGURATION REGISTER #4 (READ/WRITE 08H)	
BIT	**DESCRIPTION**
15(MSB)	EXTERNAL BIT WORD ENABLE
14	INHIBIT BIT WORD IF BUSY
13	MODE COMMAND OVERRIDE BUSY
12	EXPANDED BC CONTROL WORD ENABLE
11	BROADCAST MASK ENA/$\overline{\text{XOR}}$
10	RETRY IF -A AND M.E.
9	RETRY IF STATUS SET
8	1ST RETRY ALT/$\overline{\text{SAME}}$ BUS
7	2ND RETRY ALT/$\overline{\text{SAME}}$ BUS
6	VALID M.E./NO DATA
5	VALID BUSY/NO DATA
4	MT TAG GAP OPTION
3	LATCH RT ADDRESS WITH CONFIG #5
2	TEST MODE 2
1	TEST MODE 1
0(LSB)	TEST MODE 0

TABLE 14. CONFIGURATION REGISTER #5 (READ/WRITE 09H)	
BIT	**DESCRIPTION**
15(MSB)	12 / $\overline{16}$ MHZ CLOCK SELECT
14	SINGLE-ENDED SELECT
13	EXTERNAL TX INHIBIT A
12	EXTERNAL TX INHIBIT B
11	EXPANDED CROSSING ENABLED
10	RESPONSE TIMEOUT SELECT 1
9	RESPONSE TIMEOUT SELECT 0
8	GAP CHECK ENABLED
7	BROADCAST DISABLED
6	RT ADDRESS LATCH/$\overline{\text{TRANSPARENT}}$
5	RT ADDRESS 4
4	RT ADDRESS 3
3	RT ADDRESS 2
2	RT ADDRESS 1
1	RT ADDRESS 0
0(LSB)	RT ADDRESS PARITY

TABLE 15. RT / MONITOR DATA STACK ADDRESS REGISTER (READ/WRITE 0AH)	
BIT	**DESCRIPTION**
15(MSB)	RT / MONITOR DATA STACK ADDRESS 15
•	•
•	•
•	•
0(LSB)	RT / MONITOR DATA STACK ADDRESS 0

TABLE 16. BC FRAME TIME REMAINING REGISTER (READ/WRITE 0BH)	
BIT	**DESCRIPTION**
15(MSB)	BC FRAME TIME REMAINING 15
•	•
•	•
•	•
0(LSB)	BC FRAME TIME REMAINING 0

Note: resolution = 100 μs per LSB

TABLE 17. BC MESSAGE TIME REMAINING REGISTER (READ/WRITE 0CH)	
BIT	**DESCRIPTION**
15(MSB)	BC MESSAGE TIME REMAINING 15
•	•
•	•
•	•
0(LSB)	BC MESSAGE TIME REMAINING 0

Note: resolution = 1 μs per LSB

TABLE 18. BC FRAME TIME / RT LAST COMMAND / MT TRIGGER REGISTER (READ/WRITE 0DH)	
BIT	**DESCRIPTION**
15(MSB)	BIT 15
•	•
•	•
•	•
0(LSB)	BIT 0

TABLE 19. RT STATUS WORD REGISTER (READ/WRITE 0EH)	
BIT	**DESCRIPTION**
15(MSB)	LOGIC “0”
14	LOGIC “0”
13	LOGIC “0”
12	LOGIC “0”
11	LOGIC “0”
10	MESSAGE ERROR
9	INSTRUMENTATION
8	SERVICE REQUEST
7	RESERVED
6	RESERVED
5	RESERVED
4	BROADCAST COMMAND RECEIVED
3	BUSY
2	SSFLAG
1	DYNAMIC BUS CONTROL ACCEPT
0(LSB)	TERMINAL FLAG

TABLE 20. RT BIT WORD REGISTER (READ 0FH)	
BIT	**DESCRIPTION**
15(MSB)	TRANSMITTER TIMEOUT
14	LOOP TEST FAILURE B
13	LOOP TEST FAILURE A
12	HANDSHAKE FAILURE
11	TRANSMITTER SHUTDOWN B
10	TRANSMITTER SHUTDOWN A
9	TERMINAL FLAG INHIBITED
8	BIT TEST FAIL
7	HIGH WORD COUNT
6	LOW WORD COUNT
5	INCORRECT SYNC RECEIVED
4	PARITY / MANCHESTER ERROR RECEIVED
3	RT-to-RT GAP / SYNC / ADDRESS ERROR
2	RT-to-RT NO RESPONSE ERROR
1	RT-to-RT 2ND COMMAND WORD ERROR
0(LSB)	COMMAND WORD CONTENTS ERROR

TABLE 21. CONFIGURATION REGISTER #6 (READ/WRITE 18H)	
BIT	**DESCRIPTION**
15(MSB)	ENHANCED BUS CONTROLLER
14	ENHANCED CPU ACCESS
13	COMMAND STACK POINTER INCREMENT ON EOM (RT, MT)
12	GLOBAL CIRCULAR BUFFER ENABLE
11	GLOBAL CIRCULAR BUFFER SIZE 2
10	GLOBAL CIRCULAR BUFFER SIZE 1
9	GLOBAL CIRCULAR BUFFER SIZE 0
8	DISABLE INVALID MESSAGES TO INTERRUPT STATUS QUEUE
7	DISABLE VALID MESSAGES TO INTERRUPT STATUS QUEUE
6	INTERRUPT STATUS QUEUE ENABLE
5	RT ADDRESS SOURCE
4	ENHANCED MESSAGE MONITOR
3	RESERVED
2	64-WORD REGISTER SPACE
1	CLOCK SELECT 1
0(LSB)	CLOCK SELECT 0

TABLE 22. CONFIGURATION REGISTER #7 (READ/WRITE 19H)	
BIT	**DESCRIPTION**
15(MSB)	MEMORY MANAGEMENT BASE ADDRESS 15
14	MEMORY MANAGEMENT BASE ADDRESS 14
13	MEMORY MANAGEMENT BASE ADDRESS 13
12	MEMORY MANAGEMENT BASE ADDRESS 12
11	MEMORY MANAGEMENT BASE ADDRESS 11
10	MEMORY MANAGEMENT BASE ADDRESS 10
9	RESERVED
8	RESERVED
7	RESERVED
6	RESERVED
5	RESERVED
4	RT HALT ENABLE
3	1553B RESPONSE TIME
2	ENHANCED TIMETAG SYNCHRONIZE
1	ENHANCED BC WATCHDOG TIMER ENABLED
0(LSB)	MODE CODE RESET / INCMD SELECT

TABLE 23. BC CONDITION REGISTER (READ 1BH)	
BIT	**DESCRIPTION**
15(MSB)	LOGIC “1”
14	RETRY 1
13	RETRY 0
12	BAD MESSAGE
11	MESSAGE STATUS SET
10	GOOD BLOCK TRANSFER
9	FORMAT ERROR
8	NO RESPONSE
7	GENERAL PURPOSE FLAG 7
6	GENERAL PURPOSE FLAG 6
5	GENERAL PURPOSE FLAG 5
4	GENERAL PURPOSE FLAG 4
3	GENERAL PURPOSE FLAG 3
2	GENERAL PURPOSE FLAG 2
1	EQUAL FLAG / GENERAL PURPOSE FLAG 1
0(LSB)	LESS THAN FLAG / GENERAL PURPOSE FLAG 1

Note: If the Mini-ACE Mark3 is not online in enhanced BC mode (i.e., processing instructions), the BC condition code register will always return a value of 0000.

TABLE 24. BC GENERAL PURPOSE FLAG REGISTER (WRITE 1BH)	
BIT	**DESCRIPTION**
15(MSB)	CLEAR GENERAL PURPOSE FLAG 7
14	CLEAR GENERAL PURPOSE FLAG 6
13	CLEAR GENERAL PURPOSE FLAG 5
12	CLEAR GENERAL PURPOSE FLAG 4
11	CLEAR GENERAL PURPOSE FLAG 3
10	CLEAR GENERAL PURPOSE FLAG 2
9	CLEAR GENERAL PURPOSE FLAG 1
8	CLEAR GENERAL PURPOSE FLAG 0
7	SET GENERAL PURPOSE FLAG 7
6	SET GENERAL PURPOSE FLAG 6
5	SET GENERAL PURPOSE FLAG 5
4	SET GENERAL PURPOSE FLAG 4
3	SET GENERAL PURPOSE FLAG 3
2	SET GENERAL PURPOSE FLAG 2
1	SET GENERAL PURPOSE FLAG 1
0(LSB)	SET GENERAL PURPOSE FLAG 0

TABLE 25. BIT TEST STATUS FLAG REGISTER (READ 1CH)	
BIT	**DESCRIPTION**
15(MSB)	PROTOCOL BUILT-IN TEST COMPLETE
14	PROTOCOL BUILT-IN TEST IN-PROGRESS
13	PROTOCOL BUILT-IN TEST PASSED
12	PROTOCOL BUILT-IN TEST ABORT
11	PROTOCOL BUILT-IN-TEST COMPLETE / IN-PROGRESS
10	LOGIC “0”
9	LOGIC “0”
8	LOGIC “0”
7	RAM BUILT-IN TEST COMPLETE
6	RAM BUILT-IN TEST IN-PROGRESS
5	RAM BUILT-IN TEST IN-PASSED
4	LOGIC “0”
3	LOGIC “0”
2	LOGIC “0”
1	LOGIC “0”
0(LSB)	LOGIC “0”

TABLE 26. INTERRUPT MASK REGISTER #2 (READ/WRITE 1DH)	
BIT	**DESCRIPTION**
15(MSB)	NOT USED
14	BC OP CODE PARITY ERROR
13	RT ILLEGAL COMMAND/MESSAGE MT MESSAGE RECEIVED
12	GENERAL PURPOSE QUEUE / INTERRUPT STATUS QUEUE ROLLOVER
11	CALL STACK POINTER REGISTER ERROR
10	BC TRAP OP CODE
9	RT COMMAND STACK 50% ROLLOVER
8	RT CIRCULAR BUFFER 50% ROLLOVER
7	MONITOR COMMAND STACK 50% ROLLOVER
6	MONITOR DATA STACK 50% ROLLOVER
5	ENHANCED BC IRQ3
4	ENHANCED BC IRQ2
3	ENHANCED BC IRQ1
2	ENHANCED BC IRQ0
1	BIT TEST COMPLETE
0(LSB)	NOT USED

TABLE 27. INTERRUPT STATUS REGISTER #2 (READ 1EH)	
BIT	**DESCRIPTION**
15(MSB)	MASTER INTERRUPT
14	BC OP CODE PARITY ERROR
13	RT ILLEGAL COMMAND/MESSAGE MT MESSAGE RECEIVED
12	GENERAL PURPOSE QUEUE / INTERRUPT STATUS QUEUE ROLLOVER
11	CALL STACK POINTER REGISTER ERROR
10	BC TRAP OP CODE
9	RT COMMAND STACK 50% ROLLOVER
8	RT CIRCULAR BUFFER 50% ROLLOVER
7	MONITOR COMMAND STACK 50% ROLLOVER
6	MONITOR DATA STACK 50% ROLLOVER
5	ENHANCED BC IRQ3
4	ENHANCED BC IRQ2
3	ENHANCED BC IRQ1
2	ENHANCED BC IRQ0
1	BIT TEST COMPLETE
0(LSB)	INTERRUPT CHAIN BIT

TABLE 28. BC GENERAL PURPOSE QUEUE POINTER REGISTER RT, MT INTERRUPT STATUS QUEUE POINTER REGISTER (READ/WRITE1FH)	
BIT	**DESCRIPTION**
15(MSB)	QUEUE POINTER BASE ADDRESS 15
14	QUEUE POINTER BASE ADDRESS 14
13	QUEUE POINTER BASE ADDRESS 13
12	QUEUE POINTER BASE ADDRESS 12
11	QUEUE POINTER BASE ADDRESS 11
10	QUEUE POINTER BASE ADDRESS 10
9	QUEUE POINTER BASE ADDRESS 9
8	QUEUE POINTER BASE ADDRESS 8
7	QUEUE POINTER BASE ADDRESS 7
6	QUEUE POINTER BASE ADDRESS 6
5	QUEUE POINTER ADDRESS 5
4	QUEUE POINTER ADDRESS 4
3	QUEUE POINTER ADDRESS 3
2	QUEUE POINTER ADDRESS 2
1	QUEUE POINTER ADDRESS 1
0(LSB)	QUEUE POINTER ADDRESS 0

NOTE: TABLES 29 TO 35 ARE NOT REGISTERS, BUT THEY ARE WORDS STORED IN RAM.

TABLE 29. BC MODE BLOCK STATUS WORD

BIT	DESCRIPTION
15(MSB)	EOM
14	SOM
13	CHANNEL B/$\overline{A}$
12	ERROR FLAG
11	STATUS SET
10	FORMAT ERROR
9	NO RESPONSE TIMEOUT
8	LOOP TEST FAIL
7	MASKED STATUS SET
6	RETRY COUNT 1
5	RETRY COUNT 0
4	GOOD DATA BLOCK TRANSFER
3	WRONG STATUS ADDRESS / NO GAP
2	WORD COUNT ERROR
1	INCORRECT SYNC TYPE
0(LSB)	INVALID WORD

TABLE 30. RT MODE BLOCK STATUS WORD

BIT	DESCRIPTION
15(MSB)	EOM
14	SOM
13	CHANNEL B/$\overline{A}$
12	ERROR FLAG
11	RT-to-RT FORMAT
10	FORMAT ERROR
9	NO RESPONSE TIMEOUT
8	LOOP TEST FAIL
7	DATA STACK ROLLOVER
6	ILLEGAL COMMAND WORD
5	WORD COUNT ERROR
4	INCORRECT DATA SYNC
3	INVALID WORD
2	RT-to-RT GAP / SYNC / ADDRESS ERROR
1	RT-to-RT 2ND COMMAND ERROR
0(LSB)	COMMAND WORD CONTENTS ERROR

TABLE 31. 1553 COMMAND WORD

BIT	DESCRIPTION
15(MSB)	REMOTE TERMINAL ADDRESS BIT 4
14	REMOTE TERMINAL ADDRESS BIT 3
13	REMOTE TERMINAL ADDRESS BIT 2
12	REMOTE TERMINAL ADDRESS BIT 1
11	REMOTE TERMINAL ADDRESS BIT 0
10	TRANSMIT / $\overline{\text{RECEIVE}}$
9	SUBADDRESS / MODE BIT 4
8	SUBADDRESS / MODE BIT 3
7	SUBADDRESS / MODE BIT 2
6	SUBADDRESS / MODE BIT 1
5	SUBADDRESS / MODE BIT 0
4	DATA WORD COUNT / MODE CODE BIT 4
3	DATA WORD COUNT / MODE CODE BIT 3
2	DATA WORD COUNT / MODE CODE BIT 2
1	DATA WORD COUNT / MODE CODE BIT 1
0(LSB)	DATA WORD COUNT / MODE CODE BIT 0

TABLE 32. WORD MONITOR IDENTIFICATION WORD

BIT	DESCRIPTION
15(MSB)	GAP TIME (MSB)
•	•
•	•
•	•
8	GAP TIME (LSB)
7	WORD FLAG
6	$\overline{\text{THIS RT}}$
5	$\overline{\text{BROADCAST}}$
4	ERROR
3	COMMAND / $\overline{\text{DATA}}$
2	CHANNEL B/$\overline{A}$
1	CONTIGUOUS DATA / $\overline{\text{GAP}}$
0(LSB)	$\overline{\text{MODE\_CODE}}$

TABLE 33. MESSAGE MONITOR MODE BLOCK STATUS WORD	
BIT	**DESCRIPTION**
15(MSB)	EOM
14	SOM
13	CHANNEL B/$\overline{A}$
12	ERROR FLAG
11	RT-to-RT TRANSFER
10	FORMAT ERROR
9	NO RESPONSE TIMEOUT
8	GOOD DATA BLOCK TRANSFER
7	DATA STACK ROLLOVER
6	RESERVED
5	WORD COUNT ERROR
4	INCORRECT SYNC
3	INVALID WORD
2	RT-to-RT GAP / SYNC / ADDRESS ERROR
1	RT-to-RT 2ND COMMAND ERROR
0(LSB)	COMMAND WORD CONTENTS ERROR

TABLE 34. RT/MONITOR INTERRUPT STATUS WORD (FOR INTERRUPT STATUS QUEUE)		
BIT	**DEFINITION FOR MESSAGE INTERRUPT EVENT**	**DEFINITION FOR NON-MESSAGE INTERRUPT EVENT**
15	TRANSMITTER TIMEOUT	NOT USED
14	ILLEGAL COMMAND	NOT USED
13	MONITOR DATA STACK 50% ROLLOVER	NOT USED
12	MONITOR DATA STACK ROLLOVER	NOT USED
11	RT CIRCULAR BUFFER 50% ROLLOVER	NOT USED
10	RT CIRCULAR BUFFER ROLLOVER	NOT USED
9	MONITOR COMMAND (DESCRIPTOR) STACK 50% ROLLOVER	NOT USED
8	MONITOR COMMAND (DESCRIPTOR) STACK ROLLOVER	NOT USED
7	RT COMMAND (DESCRIPTOR) STACK 50% ROLLOVER	NOT USED
6	RT COMMAND (DESCRIPTOR) STACK ROLLOVER	NOT USED
5	HANDSHAKE FAIL	NOT USED
4	FORMAT ERROR	TIME TAG ROLLOVER
3	MODE CODE INTERRUPT	RT ADDRESS PARITY ERROR
2	SUBADDRESS CONTROL WORD EOM	PROTOCOL SELF-TEST COMPLETE
1	END-OF-MESSAGE (EOM)	RAM PARITY ERROR
0	“1” FOR MESSAGE INTERRUPT EVENT “0” FOR NON-MESSAGE INTERRUPT EVENT	

TABLE 35. 1553B STATUS WORD	
BIT	**DESCRIPTION**
15(MSB)	REMOTE TERMINAL ADDRESS BIT 4
14	REMOTE TERMINAL ADDRESS BIT 3
13	REMOTE TERMINAL ADDRESS BIT 2
12	REMOTE TERMINAL ADDRESS BIT 1
11	REMOTE TERMINAL ADDRESS BIT 0
10	MESSAGE ERROR
9	INSTRUMENTATION
8	SERVICE REQUEST
7	RESERVED
6	RESERVED
5	RESERVED
4	BROADCAST COMMAND RECEIVED
3	BUSY
2	SSFLAG
1	DYNAMIC BUS CONTROL ACCEPTANCE
0(LSB)	TERMINAL FLAG

NON-TEST REGISTER FUNCTION SUMMARY

A summary of the Mini-ACE Mark3 24 non-test registers follows.

INTERRUPT MASK REGISTERS #1 AND #2

Interrupt Mask Registers #1 and #2 are used to enable and disable interrupt requests for various events and conditions.

NOTE: Please see Appendix “F” of the Enhanced Mini-ACE Users Guide for important information applicable only to RT MODE operation, enabling of the interrupt status queue and use of specific non-message interrupts.

CONFIGURATION REGISTERS #1 AND #2

Configuration Registers #1 and #2 are used to select the Mini-ACE Mark3’s mode of operation, and for software control of RT Status Word bits, Active Memory Area, BC Stop-On-Error, RT Memory Management mode selection, and control of the Time Tag operation.

START/RESET REGISTER

The Start/Reset Register is used for "command" type functions such as software reset, BC/MT Start, Interrupt reset, Time Tag Reset, Time Tag Register Test, Initiate protocol self-test, Initiate RAM self-test, Clear self-test register, and Clear RT Halt. The Start/Reset Register also includes provisions for stopping the BC in its auto-repeat mode, either at the end of the current message or at the end of the current BC frame.

BC/RT COMMAND STACK REGISTER

The BC/RT Command Stack Register allows the host CPU to determine the pointer location for the current or most recent message.

BC INSTRUCTION LIST POINTER REGISTER

The BC Instruction List Pointer Register may be read to determine the current location of the Instruction List Pointer for the Enhanced BC mode.

BC CONTROL WORD/RT SUBADDRESS CONTROL WORD REGISTER

In BC mode, the BC Control Word/RT Subaddress Control Word Register allows host access to the current word or most recent BC Control Word. The BC Control Word contains bits that select the active bus and message format, enable off-line self-test, masking of Status Word bits, enable retries and interrupts, and specify MIL-STD-1553A or -1553B error handling. In RT mode, this register allows host access to the current or most recent Subaddress Control Word. The Subaddress Control Word is used to select the memory management scheme and enable interrupts for the current message.

TIME TAG REGISTER

The Time Tag Register maintains the value of a real-time clock. The resolution of this register is programmable from among 2, 4, 8, 16, 32, and 64 µs/LSB. The Start-of-Message (SOM) and End-of-Message (EOM) sequences in BC, RT, and Message Monitor modes cause a write of the current value of the Time Tag Register to the stack area of the RAM.

INTERRUPT STATUS REGISTERS #1 AND #2

Interrupt Status Registers #1 and #2 allow the host processor to determine the cause of an interrupt request by means of one or two read accesses. The interrupt events of the two Interrupt Status Registers are mapped to correspond to the respective bit positions in the two Interrupt Mask Registers. Interrupt Status Register #2 contains an INTERRUPT CHAIN bit, used to indicate an interrupt event from Interrupt Status Register #1.

CONFIGURATION REGISTERS #3, #4, AND #5

Configuration Registers #3, #4, and #5 are used to enable many of the Mini-ACE Mark3's advanced features that were implemented by the prior generation products, the ACE and Mini-ACE (Plus). For BC, RT, and MT modes, use of the Enhanced Mode enables the various read-only bits in Configuration Register #1. For BC mode, Enhanced Mode features include the expanded BC Control Word and BC Block Status Word, additional Stop-On-Error and Stop-On-Status Set functions, frame auto-repeat, programmable intermessage gap times, automatic retries, expanded Status Word Masking, and the capability to generate interrupts following the completion of any selected message. For RT mode, the Enhanced Mode features include the expanded RT Block Status Word, combined RT/Selective Message Monitor mode, automatic setting of the TERMINAL FLAG Status Word bit following a loop test failure; the double buffering scheme for individual receive (broadcast) subaddresses, and the alternate (fully software programmable) RT Status Word. For MT mode, use of the Enhanced Mode enables the Selective Message Monitor, the combined RT/Selective Monitor modes, and the monitor triggering capability.

RT/MONITOR DATA STACK ADDRESS REGISTER

The RT/Monitor Data Stack Address Register provides a read/writable indication of the last data word stored for RT or Monitor modes.

BC FRAME TIME REMAINING REGISTER

The BC Frame Time Remaining Register provides a read-only indication of the time remaining in the current BC frame. In the enhanced BC mode, this timer may be used for minor or major frame control, or as a watchdog timer for the BC message sequence control processor. The resolution of this register is 100 µs/LSB.

BC TIME REMAINING TO NEXT MESSAGE REGISTER

The BC Time Remaining to Next Message Register provides a read-only indication of the time remaining before the start of the next message in a BC frame. In the enhanced BC mode, this timer may also be used for the BC message sequence control processor's Delay (DLY) instruction, or for minor or major frame control. The resolution of this register is 1 µs/LSB.

BC FRAME TIME/ RT LAST COMMAND /MT TRIGGER WORD REGISTER

In BC mode, this register is used to program the BC frame time, for use in the frame auto-repeat mode. The resolution of this register is 100 µs/LSB, with a range up to 6.55 seconds. In RT mode, this register stores the current (or most previous) 1553 Command Word processed by the Mini-ACE Mark3 RT. In the Word Monitor mode, this register is used to specify a 16-bit Trigger (Command) Word. The Trigger Word may be used to start or stop the monitor, or to generate interrupts.

BC INITIAL INSTRUCTION LIST POINTER REGISTER

The BC Initial Instruction List Pointer Register enables the host to assign the starting address for the enhanced BC Instruction List.

RT STATUS WORD REGISTER AND BIT WORD REGISTERS

The RT Status Word Register and BIT Word Registers provide read-only indications of the RT Status and BIT Words.

CONFIGURATION REGISTERS #6 AND #7:

Configuration Registers #6 and #7 are used to enable the Mini-ACE Mark3 features that extend beyond the architecture of the ACE/Mini-ACE (Plus). These include the Enhanced BC mode; RT Global Circular Buffer (including buffer size); the RT/MT Interrupt Status Queue, including valid/invalid message filtering; enabling a software-assigned RT address; clock frequency selection; a base address for the "non-data" portion of Mini-ACE Mark3 memory; LSB filtering for the Synchronize (with data) time tag operations; and enabling a watchdog timer for the Enhanced BC message sequence control engine.

NOTE: Please see Appendix "F" of the Enhanced Mini-ACE User's Guide for important information applicable only to RT MODE operation, enabling of the interrupt status queue and use of specific non-message interrupts.

BC CONDITION CODE REGISTER

The BC Condition Code Register is used to enable the host processor to read the current value of the Enhanced BC Message Sequence Control Engine's condition flags.

BC GENERAL PURPOSE FLAG REGISTER

The BC General Purpose Flag Register allows the host processor to be able to set, clear, or toggle any of the Enhanced BC Message Sequence Control Engine's General Purpose condition flags.

BIT TEST STATUS REGISTER

The BIT Test Status Register is used to provide read-only access to the status of the protocol and RAM built-in self-tests (BIT).

BC GENERAL PURPOSE QUEUE POINTER

The BC General Purpose Queue Pointer provides a means for initializing the pointer for the General Purpose Queue, for the Enhanced BC mode. In addition, this register enables the host to determine the current location of the General Purpose Queue pointer, which is incremented internally by the Enhanced BC message sequence control engine.

RT/MT INTERRUPT STATUS QUEUE POINTER

The RT/MT Interrupt Status Queue Pointer provides a means for initializing the pointer for the Interrupt Status Queue, for RT, MT, and RT/MT modes. In addition, this register enables the host to determine the current location of the Interrupt Status Queue pointer, which is incremented by the RT/MT message processor.

BUS CONTROLLER (BC) ARCHITECTURE

The BC functionality for the Mini-ACE Mark3 includes two separate architectures: (1) the older, non-Enhanced Mode, which provides complete compatibility with the previous ACE and Mini-ACE (Plus) generation products; and (2) the newer, Enhanced BC mode. The Enhanced BC mode offers several new powerful architectural features. These include the incorporation of a highly autonomous BC message sequence control engine, which greatly serves to offload the operation of the host CPU.

The Enhanced BC's message sequence control engine provides a high degree of flexibility for implementing major and minor frame scheduling; capabilities for inserting asynchronous messages in the middle of a frame; to separate 1553 message data from control/status data for the purpose of implementing double buffering and performing bulk data transfers; for implementing message retry schemes, including the capability for automatic bus channel switchover for failed messages; and for reporting various conditions to the host processor by means of four user-defined interrupts and a general purpose queue.

In both the non-Enhanced and Enhanced BC modes, the Mini-ACE Mark3 BC implements all MIL-STD-1553B message formats. Message format is programmable on a message-by-message basis by means of the BC Control Word and the T/R bit of the Command Word for the respective message. The BC Control

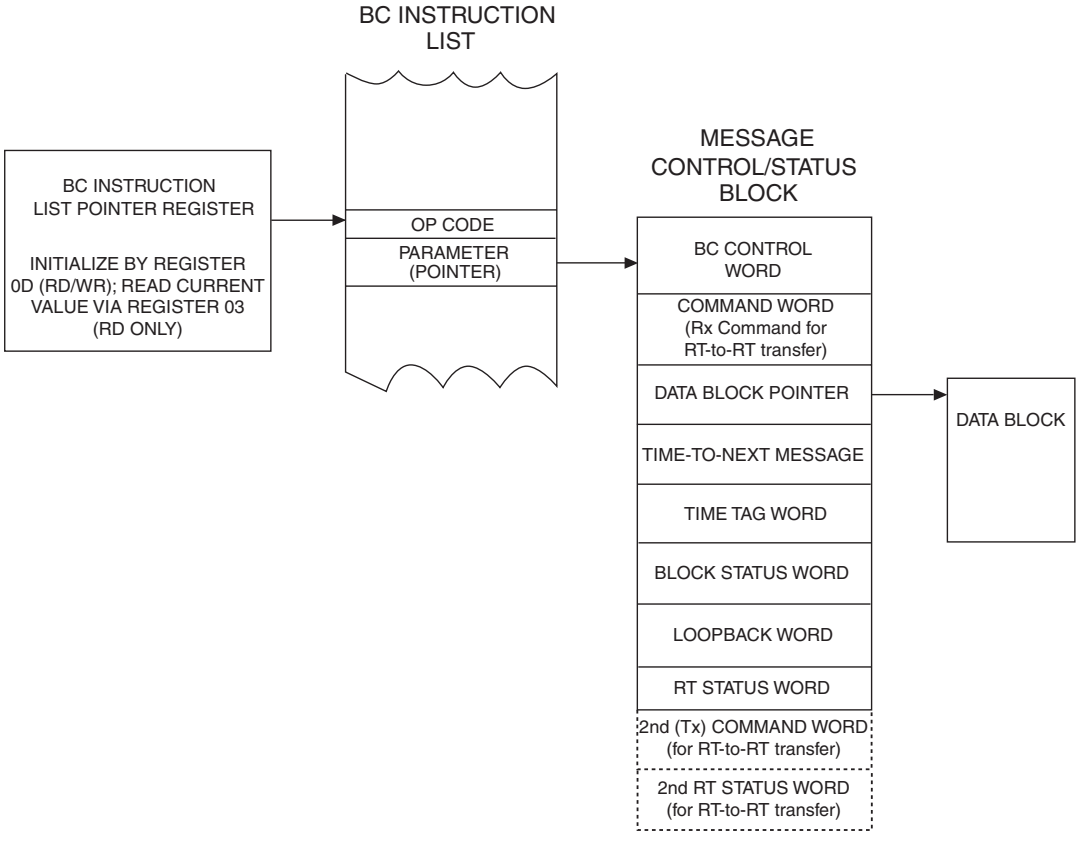


FIGURE 2. BC MESSAGE SEQUENCE CONTROL

Word allows 1553 message format, 1553A/B type RT, bus channel, self-test, and Status Word masking to be specified on an individual message basis. In addition, automatic retries and/or interrupt requests may be enabled or disabled for individual messages. The BC performs all error checking required by MIL-STD-1553B. This includes validation of response time, sync type and sync encoding, Manchester II encoding, parity, bit count, word count, Status Word RT Address field, and various RT-to-RT transfer errors. The Mini-ACE Mark3 BC response timeout value is programmable with choices of 18, 22, 50, and 130 µs. The longer response timeout values allow for operation over long buses and/or the use of repeaters.

In its non-Enhanced Mode, the Mini-ACE Mark3 may be programmed to process BC frames of up to 512 messages with no processor intervention. In the Enhanced BC mode, there is no explicit limit to the number of messages that may be processed in a frame. In both modes, it is possible to program for either single frame or frame auto-repeat operation. In the auto-repeat mode, the frame repetition rate may be controlled either internally, using a programmable BC frame timer, or from an external trigger input.

ENHANCED BC MODE: MESSAGE SEQUENCE CONTROL

One of the major new architectural features of the Mini-ACE Mark3 series is its advanced capability for BC message sequence control. The Mini-ACE Mark3 supports highly autonomous BC operation, which greatly offloads the operation of the host processor.

The operation of the Mini-ACE Mark3's message sequence control engine is illustrated in FIGURE 2. The BC message sequence control involves an instruction list pointer register; an instruction list which contains multiple 2-word entries; a message control/status stack, which contains multiple 8-word or 10-word descriptors; and data blocks for individual messages.

The initial value of the instruction list pointer register is initialized by the host processor (via Register 0D), and is incremented by the BC message sequence processor (host readable via Register 03). During operation, the message sequence control processor fetches the operation referenced by the instruction list pointer register from the instruction list.

Note that the pointer parameter referencing the first word of a message's control/status block (the BC Control Word) must contain an address value that is **modulo 8**. Also, note that if the message is an RT-to-RT transfer, the pointer parameter must contain an address value that is **modulo 16**.

OP CODES

The instruction list pointer register references a pair of words in the BC instruction list: an op code word, followed by a parameter word. The format of the op code word, which is illustrated in FIGURE 3, includes a 5-bit op code field and a 5-bit condition code field. The op code identifies the instruction to be executed by the BC message sequence controller.

Most of the operations are conditional, with execution dependent on the contents of the condition code field. Bits 3-0 of the condition code field identifies a particular condition. Bit 4 of the condition code field identifies the logic sense ("1" or "0") of the selected condition code on which the conditional execution is dependent. TABLE 36 lists all the op codes, along with their respective mnemonic, code value, parameter, and description. TABLE 37 defines all the condition codes.

Eight of the condition codes (8 through F) are set or cleared as the result of the most recent message. The other eight are defined as "General Purpose" condition codes GP0 through GP7. There are three mechanisms for programming the values of the General Purpose Condition Code bits: (1) They may be set, cleared, or toggled by the host processor, by means of the BC GENERAL PURPOSE FLAG REGISTER; (2) they may be set, cleared, or toggled by the BC message sequence control processor, by means of the GP Flag Bits (FLG) instruction; and (3) GP0 and GP1 only (but none of the others) may be set or cleared by means of the BC message sequence control processor's Compare Frame Timer (CFT) or Compare Message Timer (CMT) instructions.

The host processor also has read-only access to the BC condition codes by means of the BC CONDITION CODE REGISTER.

Note that four (4) instructions are **unconditional**. These are Compare to Frame Timer (CFT), Compare to Message Timer (CMT), GP Flag Bits (FLG), and Execute and Flip (XQF). For these instructions, the Condition Code Field is "don't care". That is, these instructions are **always** executed, regardless of the result of the condition code test.

All of the other instructions are conditional. That is, they will only be executed if the condition code specified by the condition code field in the op code word tests true. If the condition code field tests false, the instruction list pointer will skip down to the next instruction.

FIGURE 3. BC OP CODE FORMAT

As shown in TABLE 36, many of the operations include a single-word parameter. For an XEQ (execute message) operation, the parameter is a pointer to the start of the message's Control / Status block. For other operations, the parameter may be an address, a time value, an interrupt pattern, a mechanism to set or clear general purpose flag bits, or an immediate value. For several op codes, the parameter is "don't care" (not used).

As described above, some of the op codes will cause the message sequence control processor to execute messages. In this case, the parameter references the first word of a message Control/Status block. With the exception of RT-to-RT transfer messages, all message status/control blocks are eight words long: a block control word, time-to-next-message parameter, data block pointer, command word, status word, loopback word, block status word, and time tag word.

In the case of an RT-to-RT transfer message, the size of the message control/status block increases to 16 words. However, in this case, the last six words are not used; the ninth and tenth words are for the second command word and second status word.

The third word in the message control/status block is a pointer that references the first word of the message's data word block. Note that the data word block stores only data words, which are to be either transmitted or received by the BC. By segregating data words from command words, status words, and other control and "housekeeping" functions, this architecture enables the use of convenient, usable data structures, such as circular buffers and double buffers.

Other operations support program flow control; i.e., jump and call capability. The call capability includes maintenance of a call stack which supports a maximum of four (4) entries; there is also a return instruction. In the case of a call stack overrun or underrun, the BC will issue a CALL STACK POINTER REGISTER ERROR interrupt, if enabled.

Other op codes may be used to delay for a specified time; start a new BC frame; wait for an external trigger to start a new frame; perform comparisons based on frame time and time-to-next message; load the time tag or frame time registers; halt; and issue host interrupts. In the case of host interrupts, the message control processor passes a 4-bit user-defined interrupt vector to the host, by means of the Mini-ACE Mark3's Interrupt Status Register.

The purpose of the FLG instruction is to enable the message sequence controller to set, clear, or toggle the value(s) of any or all of the eight general purpose condition flags.

The op code parity bit encompasses all sixteen bits of the op code word. This bit must be programmed for odd parity. If the message sequence control processor fetches an undefined op code word, an op code word with even parity, or bits 9-5 of an op code word do not have a binary pattern of 01010, the message sequence control processor will immediately halt the BC's operation. In addition, if enabled, a BC TRAP OP CODE interrupt will be issued. Also, if enabled, a parity error will result in an OP CODE PARITY ERROR interrupt. TABLE 37 describes the Condition Codes.

TABLE 36. BC OPERATIONS FOR MESSAGE SEQUENCE CONTROL

INSTRUCTION	MNEMONIC	OP CODE (HEX)	PARAMETER	CONDITIONAL OR UNCONDITIONAL	DESCRIPTION
Execute Message	XEQ	0001	Message Control / Status Block Address	Conditional (See Note)	Executes the message at the specified Message Control/Status Block Address if the condition flag tests TRUE, otherwise continue execution at the next OpCode in the instruction list.
Jump	JMP	0002	Instruction List Address	Conditional	Jump to the OpCode specified in the Instruction List if the condition flag tests TRUE, otherwise continue execution at the next OpCode in the instruction list.
Subroutine Call	CAL	0003	Instruction List Address	Conditional	Jump to the OpCode specified by the Instruction List Address and push the Address of the Next OpCode on the Call Stack if the condition flag tests TRUE, otherwise continue execution at the next OpCode in the instruction list. Note that the maximum depth of the subroutine call stack is **four**.
Subroutine Return	RTN	0004	Not Used (Don't Care)	Conditional	Return to the OpCode popped off the Call Stack if the condition flag tests TRUE, otherwise continue execution at the next OpCode in the instruction list.
Interrupt Request	IRQ	0006	Interrupt Bit Pattern in 4 LS bits	Conditional	Generate an interrupt if the condition flag tests TRUE, otherwise continue execution at the next OpCode in the instruction list. The passed parameter (Interrupt Bit Pattern) specifies which of the ENHANCED BC IRQ bit(s) (bits 5-2) will be set in Interrupt Status Register #2. Only the four LSBs of the passed parameter are used. A parameter where the four LSBs are logic "0" will **not** generate an interrupt.
Halt	HLT	0007	Not Used (Don't Care)	Conditional	Stop execution of the Message Sequence Control Program until a new BC Start is issued by the host if the condition flag tests TRUE, otherwise continue execution at the next OpCode in the instruction list.
Delay	DLY	0008	Delay Time Value (Resolution = 1µS / LSB)	Conditional	Delay the time specified by the Time parameter before executing the next OpCode if the condition flag tests TRUE, otherwise continue execution at the next OpCode without delay. The delay generated will use the Time to Next Message Timer.
Wait Until Frame Timer = 0	WFT	0009	Not Used (Don't Care)	Conditional	Wait until Frame Time counter is equal to Zero before continuing execution of the Message Sequence Control Program if the condition flag tests TRUE, otherwise continue execution at the next OpCode without delay.
Compare to Frame Timer	CFT	000A	Delay Time Value (Resolution = 100µS / LSB)	Unconditional	Compare Time Value to Frame Time Counter. The LT/GP0 and EQ/GP1 flag bits are set or cleared based on the results of the compare. If the value of the CFT's parameter is less than the value of the frame time counter, then the LT/GP0 and NE/$\overline{GP1}$ flags will be set, while the GT-EQ/$\overline{GP0}$ and EQ/GP1 flags will be cleared. If the value of the CFT's parameter is equal to the value of the frame time counter, then the GT-EQ/$\overline{GP0}$ and EQ/GP1 flags will be set, while the LT/GP0 and NE/$\overline{GP1}$ flags will be cleared. If the value of the CFT's parameter is greater than the current value of the frame time counter, then the GT-EQ/$\overline{GP0}$ and NE/$\overline{GP1}$ flags will be set, while the LT/GP0 and EQ/GP1 flags will be cleared.
Compare to Message Timer	CMT	000B	Delay Time Value (Resolution = 1µS / LSB)	Unconditional	Compare Time Value to Message Time Counter. The LT/GP0 and EQ/GP1 flag bits are set or cleared based on the results of the compare. If the value of the CMT's parameter is less than the value of the message time counter, then the LT/GP0 and NE/$\overline{GP1}$ flags will be set, while the GT-EQ/$\overline{GP0}$ and EQ/GP1 flags will be cleared. If the value of the CMT's parameter is equal to the value of the message time counter, then the GT-EQ/$\overline{GP0}$ and EQ/GP1 flags will be set, while the LT/GP0 and NE/$\overline{GP1}$ flags will be cleared. If the value of the CMT's parameter is greater than the current value of the message time counter, then the GT-EQ/$\overline{GP0}$ and NE/$\overline{GP1}$ flags will be set, while the LT/GP0 and EQ/GP1 flags will be cleared.

NOTE: While the XEQ (Execute Message) instruction is conditional, not all condition codes may be used to enable its use. The ALWAYS and NEVER condition codes may be used. The eight general purpose flag bits, GP0 through GP7, may also be used. However, if GP0 through GP7 are used, it is imperative that the host processor not modify the value of the specific general purpose flag bit that enabled a particular message while that message is being processed. Similarly, the LT, GT-EQ, EQ, and NE flags, which the BC only updates by means of the CFT and CMT instructions, may also be used. However, these two flags are dual use. Therefore, if these are used, it is imperative that the host processor not modify the value of the specific flag (GP0 or GP1) that enabled a particular message while that message is being processed. The NORESP, FMT ERR, GD BLK XFER, MASKED STATUS SET, BAD MESSAGE, RETRY0, and RETRY1 condition codes are not available for use with the XEQ instruction and should not be used to enable its execution.

TABLE 36. BC OPERATIONS FOR MESSAGE SEQUENCE CONTROL (CONT.)

INSTRUCTION	MNEMONIC	OP CODE (HEX)	PARAMETER	CONDITIONAL OR UNCONDITIONAL	DESCRIPTION
GP Flag Bits	FLG	000C	Used to set, clear, or toggle GP (General Purpose) Flag bits (See description)	Unconditional	Used to set, toggle, or clear any or all of the eight general purpose flags. The table below illustrates the use of the GP Flag Bits instruction for the case of GP0 (General Purpose Flag 0). Bits 1 and 9 of the parameter byte affect flag GP1, bits 2 and 10 effect GP2, etc., according to the following rules:
Load Time Tag Counter	LTT	000D	Time Value. Resolution (µs/LSB) is defined by bits 9, 8, and 7 of Configuration Register #2.	Conditional	Load Time Tag Counter with Time Value if the condition flag tests TRUE, otherwise continue execution at the next OpCode in the instruction list.
Load Frame Timer	LFT	000E	Time Value (resolution = 100 µs/LSB)	Conditional	Load Frame Timer Register with the Time Value parameter if the condition flag tests TRUE, otherwise continue execution at the next OpCode in the instruction list.
Start Frame Timer	SFT	000F	Not Used (Don't Care)	Conditional	Start Frame Time Counter with Time Value in Time Frame register if the condition flag tests TRUE, otherwise continue execution at the next OpCode in the instruction list.
Push Time Tag Register	PTT	0010	Not Used (Don't Care)	Conditional	Push the value of the Time Tag Register on the General Purpose Queue if the condition flag tests TRUE, otherwise continue execution at the next OpCode in the instruction list.
Push Block Status Word	PBS	0011	Not Used (Don't Care)	Conditional	Push the Block Status Word for the most recent message on the General Purpose Queue if the condition flag tests TRUE, otherwise continue execution at the next OpCode in the instruction list.
Push Immediate Value	PSI	0012	Immediate Value	Conditional	Push Immediate data on the General Purpose Queue if the condition flag tests TRUE, otherwise continue execution at the next OpCode in the instruction list.
Push Indirect	PSM	0013	Memory Address	Conditional	Push the data stored at the specified memory location on the General Purpose Queue if the condition flag tests TRUE, otherwise continue execution at the next OpCode in the instruction list.
Wait for External Trigger	WTG	0014	Not Used (Don't Care)	Conditional	Wait for a logic "0"-to-logic "1" transition on the EXT_TRIG input signal before proceeding to the next OpCode in the instruction list if the condition flag tests TRUE, otherwise continue execution at the next OpCode without delay.
Execute and Flip	XQF	0015	Message Control / Status Block Address	Unconditional	Execute (unconditionally) the message referenced by the Message Control/Status Block Address. Following the processing of this message, if the condition flag tests TRUE, the BC will toggle bit 4 in the Message Control/Status Block Address, and store the new Message Block Address as the updated value of the parameter following the XQF instruction code. As a result, the **next** time that this line in the instruction list is executed, the Message Control/Status Block at the **updated** address (**old address XOR 0010h**), rather than the old address, will be processed. If the condition flag tests FALSE, the value of the Message Control/Status Block Address parameter will not change.

Bit 8	Bit 0	Effect on GP0
0	0	No Change
0	1	Set Flag
1	0	Clear Flag
1	1	Toggle Flag

TABLE 37. BC CONDITION CODES

BIT CODE	NAME (BIT 4 = 0)	INVERSE (BIT 4 = 1)	FUNCTIONAL DESCRIPTION
0	LT/GP0	GT-EQ/ $\overline{\text{GP0}}$	Less than or GP0 flag. This bit is set or cleared based on the results of the compare. If the value of the CMT's parameter is less than the value of the message time counter, then the LT/GP0 and NE/$\overline{\text{GP1}}$ flags will be set, while the GT-EQ/$\overline{\text{GP0}}$ and EQ/GP1 flags will be cleared. If the value of the CMT's parameter is equal to the value of the message time counter, then the GT-EQ/$\overline{\text{GP0}}$ and EQ/GP1 flags will be set, while the LT/GP0 and NE/$\overline{\text{GP1}}$ flags will be cleared. If the value of the CMT's parameter is greater than the current value of the message time counter, then the GT-EQ/$\overline{\text{GP0}}$ and NE/$\overline{\text{GP1}}$ flags will be set, while the LT/GP0 and EQ/GP1 flags will be cleared. Also, General Purpose Flag 1 may be also be set or cleared by a FLG operation.
1	EQ/GP1	NE/$\overline{\text{GP1}}$	Equal Flag. This bit is set or cleared after CFT or CMT operation. If the value of the CMT's parameter is equal to the value of the message time counter, then the EQ/GP1 flag will be set and the NE/$\overline{\text{GP1}}$ bit will be cleared. If the value of the CMT's parameter is not equal to the value of the message time counter, then the NE/$\overline{\text{GP1}}$ flag will be set and the EQ/GP1bit will be cleared. Also, General Purpose Flag 1 may be also be set or cleared by a FLG operation.
2 3 4 5 6 7	GP2 GP3 GP4 GP5 GP6 GP7	$\overline{\text{GP2}}$ $\overline{\text{GP3}}$ $\overline{\text{GP4}}$ $\overline{\text{GP5}}$ $\overline{\text{GP6}}$ $\overline{\text{GP7}}$	General Purpose Flags may be set, cleared, or toggled by a FLG operation. The host processor can set, clear, or toggle these flags in the same way as the FLG instruction by means of the BC GENERAL PURPOSE FLAG REGISTER.
8	NORESP	$\overline{\text{RESP}}$	NORESP indicates that an RT has either not responded or has responded later than the BC No Response Timeout time. The Mini-ACE Mark3's No Response Timeout Time is defined per MIL-STD-1553B as the time from the mid-bit crossing of the parity bit of the last word transmitted by the BC to the mid-sync crossing of the RT Status Word. The value of the No Response Timeout value is programmable from among the nominal values 18.5, 22.5, 50.5, and 130 µs (±1 µs) by means of bits 10 and 9 of Configuration Register #5.
9	FMT ERR	$\overline{\text{FMT ERR}}$	FMT ERR indicates that the received portion of the most recent message contained one or more violations of the 1553 message validation criteria (sync, encoding, parity, bit count, word count, etc.), or the RT's status word received from a responding RT contained an incorrect RT address field.
A	GD BLK XFER	$\overline{\text{GD BLK XFER}}$	For the most recent message, GD BLK XFER will be set to logic "1" following completion of a valid (error-free) RT-to-BC transfer, RT-to-RT transfer, or transmit mode code with data message. This bit is set to logic "0" following an invalid message. GOOD DATA BLOCK TRANSFER is **always** logic "0" following a BC-to-RT transfer, a mode code with data, or a mode code without data. The Loop Test has **no effect** on GOOD DATA BLOCK TRANSFER. GOOD DATA BLOCK TRANSFER may be used to determine if the transmitting portion of an RT-to-RT transfer was error free.
B	MASKED STATUS BIT	$\overline{\text{MASKED STATUS BIT}}$	Indicates that one or both of the following conditions have occurred for the most recent message: (1) If one (or more) of the Status Mask bits (14 through 9) in the BC Control Word is logic "0" **and** the corresponding bit(s) is (are) set (logic "1") in the received RT Status Word. In the case of the RESERVED BITS MASK (bit 9) set to logic "0," any or all of the 3 Reserved Status Word bits being set will result in a MASKED STATUS SET condition; and/or (2) If BROADCAST MASK ENABLED/$\overline{\text{XOR}}$ (bit 11 of Configuration Register #4) is logic "1" **and** the MASK BROADCAST bit of the message's BC Control Word is logic "0" and the BROADCAST COMMAND RECEIVED bit in the received RT Status Word is logic "1."
C	BAD MESSAGE	GOOD MESSAGE	BAD MESSAGE indicates either a format error, loop test fail, or no response error for the most recent message. Note that a "Status Set" condition has **no effect** on the "BAD MESSAGE/GOOD MESSAGE" condition code.
D E	RETRY0 RETRY1	$\overline{\text{RETRY0}}$ $\overline{\text{RETRY1}}$	These two bits reflect the retry status of the most recent message. The number of times that the message was retried is delineated by these two bits as shown below: RETRY COUNT 1 (bit 14) / RETRY COUNT 0 (bit 13) / Number of Message Retries 0 / 0 / 0 0 / 1 / 1 1 / 0 / N/A 1 / 1 / 2
F	ALWAYS	NEVER	The ALWAYS flag should be set (bit 4 = 0) to designate an instruction as unconditional. The NEVER bit (bit 4 = 1) can be used to implement a NOP or "skip" instruction.

BC MESSAGE SEQUENCE CONTROL

The Mini-ACE Mark3 BC message sequence control capability enables a high degree of offloading of the host processor. This includes using the various timing functions to enable autonomous structuring of major and minor frames. In addition, by implementing conditional jumps and subroutine calls, the message sequence control processor greatly simplifies the insertion of asynchronous, or "out-of-band" messages.

EXECUTE AND FLIP OPERATION

The Mini-ACE Mark3 BC's XQF, or "Execute and Flip" operation, provides some unique capabilities. Following execution of this unconditional instruction, if the condition code tests TRUE, the BC will modify the value of the current XQF instruction's pointer parameter by toggling bit 4 of the pointer. That is, if the selected condition flag tests true, the value of the parameter will be **updated** to the value = **old address XOR 0010h**. As a result, the next time that this line in the instruction list is executed, the Message Control/Status Block at the updated address (old address XOR 0010h) will be processed, rather than the one at the old address. The operation of the XQF instruction is illustrated in FIGURE 4.

There are multiple ways of utilizing the "execute and flip" instruction. One is to facilitate the implementation of a double buffering data scheme for individual messages. This allows the message sequence control processor to "ping-pong" between a pair of data buffers for a particular message. By doing so, the host processor can access one of the two Data Word blocks, while the BC reads or writes the alternate Data Word block.

A second application of the "execute and flip" capability is in conjunction with message retries. This allows the BC to not only switch buses when retrying a failed message, but to automatically switch buses **permanently** for all future times that the same message is to be processed. This not only provides a high degree of autonomy from the host CPU, but saves BC bandwidth, by eliminating the need for future attempts to process messages on an RT's failed channel.

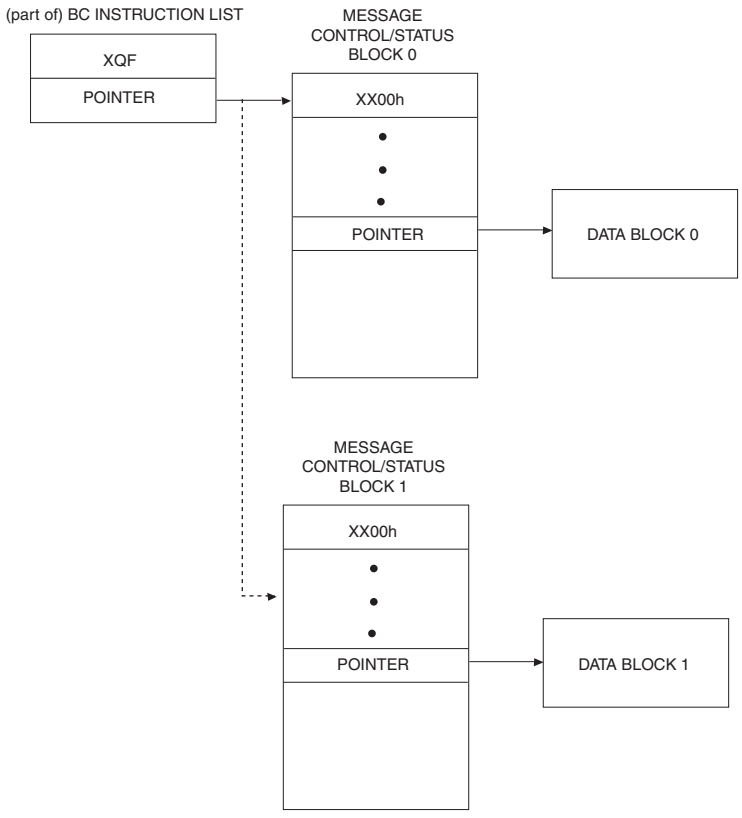


FIGURE 4. EXECUTE and FLIP (XQF) OPERATION

GENERAL PURPOSE QUEUE

The Mini-ACE Mark3 BC allows for the creation of a general purpose queue. This data structure provides a means for the message sequence processor to convey information to the BC host. The BC op code repertoire provides mechanisms to push various items on this queue. These include the contents of the Time Tag Register, the Block Status Word for the most recent message, an immediate data value, or the contents of a specified memory address.

FIGURE 5 illustrates the operation of the BC General Purpose Queue. Note that the BC General Purpose Queue Pointer Register will always point to the **next** address location (modulo 64); that is, the location **following** the last location written by the BC message sequence control engine.

If enabled, a BC GENERAL PURPOSE QUEUE ROLLOVER interrupt will be issued when the value of the queue pointer address rolls over at a 64-word boundary. The rollover will always occur at a modulo 64 address.

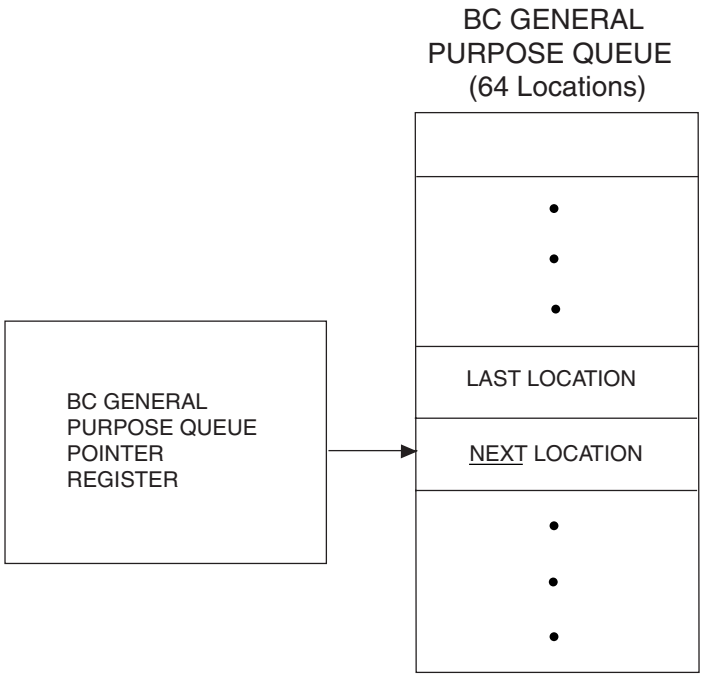


FIGURE 5. BC GENERAL PURPOSE QUEUE

REMOTE TERMINAL (RT) ARCHITECTURE

The Mini-ACE Mark3's RT architecture builds upon that of the ACE and Mini-ACE. The Mini-ACE Mark3 provides multiprotocol support, with full compliance to all of the commonly used data bus standards, including MIL-STD-1553A, MIL-STD-1553B Notice 2, STANAG 3838, General Dynamics 16PP303, and McAir A3818, A5232, and A5690. For the Mini-ACE Mark3 RT mode, there is programmable flexibility enabling the RT to be configured to fulfill any set of system requirements. This includes the capability to meet the MIL-STD-1553A response time requirement of 2 to 5 µs, and multiple options for mode code subaddresses, mode codes, RT status word, and RT BIT word.

The Mini-ACE Mark3 RT protocol design implements all of the MIL-STD-1553B message formats and dual redundant mode codes. The design has passed validation testing for MIL-STD-1553B compliance. The Mini-ACE Mark3 RT performs comprehensive error checking including word and format validation, and checks for various RT-to-RT transfer errors. One of the main features of the Mini-ACE Mark3 RT is its choice of memory management options. These include single buffering by subaddress, double buffering for individual receive subaddresses, circular buffering by individual subaddresses, and global circular buffering for multiple (or all) subaddresses.

Other features of the Mini-ACE Mark3 RT include a set of interrupt conditions, a flexible status queue with filtering based on valid and/or invalid messages, flexible command illegalization, programmable busy by subaddress, multiple options on time tagging, and an "auto-boot" feature which allows the RT to initialize as an online RT with the busy bit set following power turn-on.

TABLE 38. TYPICAL RT MEMORY MAP (SHOWN FOR 4K RAM)

ADDRESS (HEX)	DESCRIPTION
0000-00FF	Stack A
0100	**Stack Pointer A**
0101	**Global Circular Buffer A Pointer**
0102-0103	RESERVED
0104	**Stack Pointer B**
0105	**Global Circular Buffer B Pointer**
0106-0107	RESERVED
0108-010F	**Mode Code Selective Interrupt Table**
0110-013F	**Mode Code Data**
0140-01BF	**Lookup Table A**
01C0-023F	**Lookup Table B**
0240-0247	**Busy Bit Lookup Table**
0248-025F	(not used)
0260-027F	Data Block 0
0280-02FF	Data Block 1-4
0300-03FF	**Command Illegalizing Table**
0400-041F	Data Block 5
0420-043F	Data Block 6
•	•
•	•
•	•
0FE0-0FFF	Data Block 100

RT MEMORY ORGANIZATION

TABLE 38 illustrates a typical memory map for an Mini-ACE Mark3 RT with 4K RAM. The two Stack Pointers reside in fixed locations in the shared RAM address space: address 0100 (hex) for the Area A Stack Pointer and address 0104 for the Area B Stack Pointer. In addition to the Stack Pointer, there are several other areas of the shared RAM address space that are designated as fixed locations (all shown in **bold**). These are for the Area A and Area B lookup tables, the illegalization lookup table, the busy lookup table, and the mode code data tables.

The RT lookup tables (reference TABLE 39) provide a mechanism for allocating data blocks for individual transmit, receive, or broadcast subaddresses. The RT lookup tables include subaddress control words as well as the individual data block pointers. If command illegalization is used, address range 0300-03FF is used for command illegalizing. The descriptor stack RAM area, as well as the individual data blocks, may be located in any of the non-fixed areas in the shared RAM address space.

Note that in TABLE 38, there is no area allocated for "Stack B". This is shown for purpose of simplicity of illustration. Also, note that in TABLE 38, the allocated area for the RT command stack is 256 words. However, larger stack sizes are possible. That is, the RT command stack size may be programmed for 256 words (64 messages), 512, 1024, or 2048 words (512 messages) by means of bits 14 and 13 of Configuration Register 3.

RT MEMORY MANAGEMENT

The Mini-ACE Mark3 provides a variety of RT memory management capabilities. As with the ACE and Mini-ACE, the choice of memory management scheme is fully programmable on a transmit/receive/broadcast subaddress basis.

In compliance with MIL-STD-1553B Notice 2, received data from broadcast messages may be optionally separated from non-broadcast received data. For each transmit, receive or broadcast subaddress, either a single-message data block, a double buffered configuration (two alternating Data Word blocks), or a vari-

TABLE 39. RT LOOK-UP TABLES

AREA A	AREA B	DESCRIPTION	COMMENT
0140 • • • 015F	01C0 • • • 01DF	Rx(/Bcst) SA0 • • • Rx(/Bcst) SA31	Receive (/Broadcast) Lookup Pointer Table
0160 • • • 017F	01E0 • • • 01FF	Tx SA0 • • • Tx SA31	Transmit Lookup Pointer Table
0180 • • • 019F	0200 • • • 021F	Bcst SA0 • • • Bcst SA31	Broadcast Lookup Pointer Table (Optional)
01A0 • • • 01BF	0220 • • • 023F	SACW SA0 • • • SACW SA31	Subaddress Control Word Lookup Table (Optional)

able-sized (128 to 8192 words) subaddress circular buffer may be allocated for data storage. The memory management scheme for individual subaddresses is designated by means of the subaddress control word (reference TABLE 40).

For received data, there is also a global circular buffer mode. In this configuration, the data words received from multiple (or all) subaddresses are stored in a common circular buffer structure. Like the subaddress circular buffer, the size of the global circular buffer is programmable, with a range of 128 to 8192 data words.

The double buffering feature provides a means for the host processor to easily access the most recent, complete received block of valid Data Words for any given subaddress. In addition to helping ensure data sample consistency, the circular buffer options provide a means for greatly reducing host processor overhead for multi-message bulk data transfer applications.

End-of-message interrupts may be enabled either globally (following all messages), following error messages, on a transmit/receive/broadcast subaddress or mode code basis, or when a circular buffer reaches its midpoint (50% boundary) or lower (100%) boundary. A pair of interrupt status registers allow the host processor to determine the cause of all interrupts by means of a single read operation.

SINGLE BUFFERED MODE

The operation of the single buffered RT mode is illustrated in FIGURE 6. In the single buffered mode, the respective lookup table entry must be written by the host processor. Received data words are written to, or transmitted data words are read from the data word block with starting address referenced by the lookup table pointer. In the single buffered mode, the current lookup table pointer is not updated by the Mini-ACE Mark3 memory management logic. Therefore, if a subsequent message is received for the same subaddress, the **same** Data Word block will be overwritten or overread.

SUBADDRESS DOUBLE BUFFERING MODE

The Mini-ACE Mark3 provides a double buffering mechanism for received data, that may be selected on an individual subaddress basis for any or all receive (and/or broadcast) subaddresses. This is illustrated in FIGURE 7. It should be noted that the Subaddress Double Buffering mode is applicable for receive data only, **not for transmit data.** Double buffering of transmit messages may be easily implemented by software techniques.

The purpose of the subaddress double buffering mode is to provide data sample consistency to the host processor. This is accomplished by allocating **two** 32-word data word blocks for each individual receive (and/or broadcast receive) subaddress. At any given time, one of the blocks will be designated as the "active" 1553 block while the other will be considered as "inactive". The data words for the next receive command to that subaddress will be stored in the active block. Following receipt of a valid message, the Mini-ACE Mark3 will automatically switch the active and inactive blocks for that subaddress. As a result, the latest, valid, complete data block is always accessible to the host processor.

CIRCULAR BUFFER MODE

The operation of the Mini-ACE Mark3's circular buffer RT memory management mode is illustrated in FIGURE 8. As in the single buffered and double buffered modes, the individual lookup table entries are initially loaded by the host processor. At the start of each message, the lookup table entry is stored in the third position of the respective message block descriptor in the descriptor stack area of RAM. Receive or transmit data words are transferred to (from) the circular buffer, starting at the location referenced by the lookup table pointer.

In general, the location after the last data word written or read (modulo the circular buffer size) during the message is written to the respective lookup table location during the end-of-message sequence. By so doing, data for the next message for the respec-

TABLE 40. RT SUBADDRESS CONTROL WORD - MEMORY MANAGEMENT OPTIONS

DOUBLE-BUFFERED OR GLOBAL CIRCULAR BUFFER (bit 15)	SUBADDRESS CONTROL WORD BITS			MEMORY MANAGEMENT SUBADDRESS BUFFER SCHEME DESCRIPTION	
	MM2	MM1	MM0		
0	0	0	0	Single Message	
1	0	0	0	For Receive or Broadcast: Double Buffered For Transmit: Single Message	
0	0	0	1	128-Word	Subaddress - specific circular buffer of specified size.
0	0	1	0	256-Word	
0	0	1	1	512-Word	
0	1	0	0	1024-Word	
0	1	0	1	2048-Word	
0	1	1	0	4096-Word	
0	1	1	1	8192-Word	
1	1	1	1	(for receive and / or broadcast subaddresses only) Global Circular Buffer: The buffer size is specified by Configuration Register #6, bits 11-9. The pointer to the global circular buffer is stored at address 0101 (for Area A) or address 0105 (for Area B)	

tive transmit, receive(/broadcast), or broadcast subaddress will be accessed from the next lower contiguous block of locations in the circular buffer.

For the case of a receive (or broadcast receive) message with a data word error, there is an option such that the lookup table pointer will only be updated following receipt of a **valid** message. That is, the pointer will **not** be updated following receipt of a message with an error in a data word. This allows failed messages in a bulk data transfer to be retried without disrupting the circular buffer data structure, and without intervention by the RT's host processor.

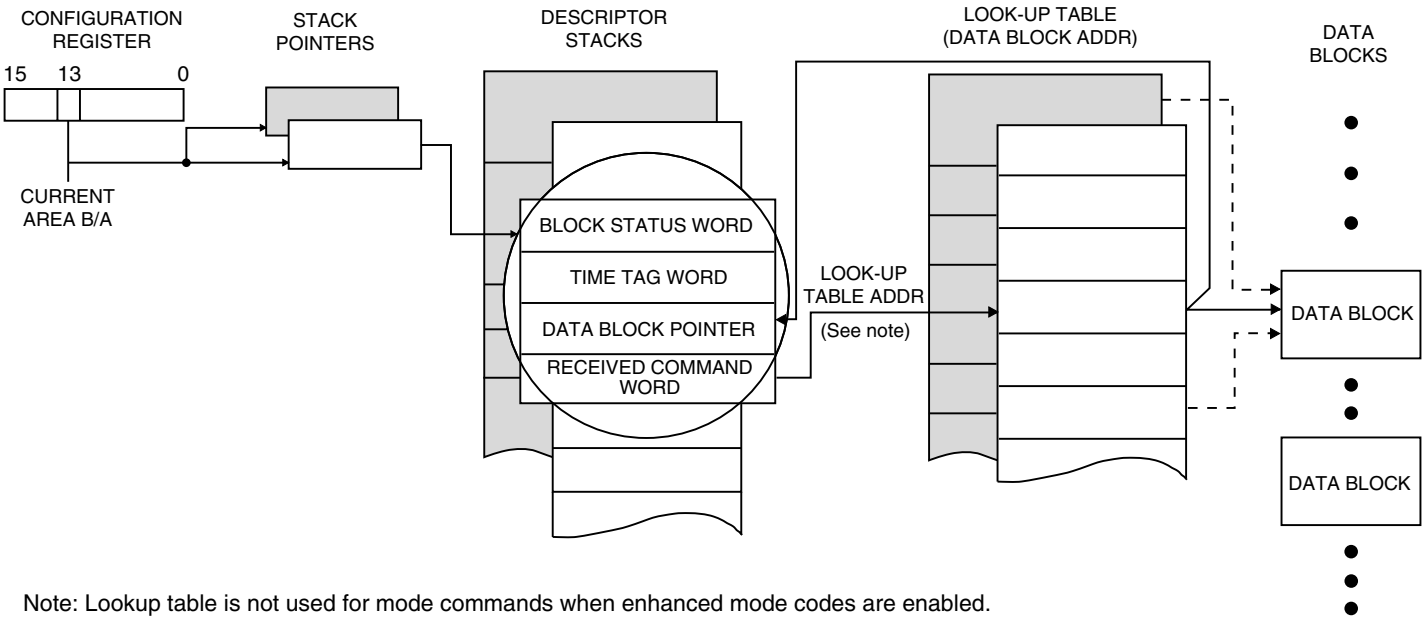
GLOBAL CIRCULAR BUFFER

Beyond the programmable choice of single buffer mode, double buffer mode, or circular buffer mode, programmable on an individual subaddress basis, the Mini-ACE Mark3 RT architecture provides an additional option, a variable sized **global** circular buffer. The Mini-ACE Mark3 RT allows for a mix of single buffered, double buffered, and individually circular buffered subaddresses, **along with** the use of the global double buffer for any arbitrary group of receive(/broadcast) or broadcast subaddresses.

In the global circular buffer mode, the data for **multiple** receive subaddresses is stored in the same circular buffer data structure. The size of the global circular buffer may be programmed for 128, 256, 512, 1024, 2048, 4096, or 8192 words, by means of bits 11, 10, and 9 of Configuration Register #6. As shown in TABLE 40, individual subaddresses may be mapped to the global circular buffer by means of their respective subaddress control words.

The pointer to the Global Circular Buffer will be stored in location 0101 (for Area A), or location 0105 (for Area B).

The global circular buffer option provides a highly efficient method for storing received message data. It allows for frequently used subaddresses to be mapped to individual data blocks, while also providing a method for asynchronously received messages to infrequently used subaddresses to be logged to a common area. Alternatively, the global circular buffer provides an efficient means for storing the received data words for all subaddresses. Under this method, all received data words are stored chronologically, regardless of subaddress.



Note: Lookup table is not used for mode commands when enhanced mode codes are enabled.

FIGURE 6. RT SINGLE BUFFERED MODE

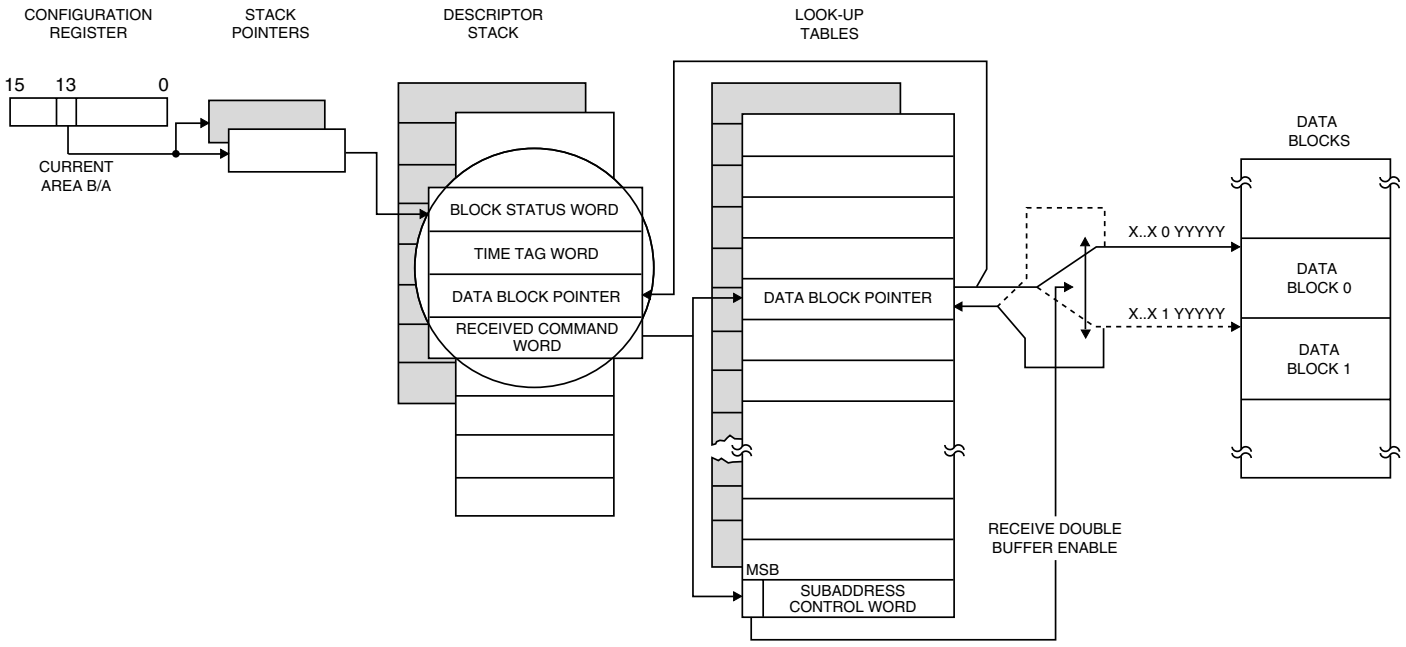
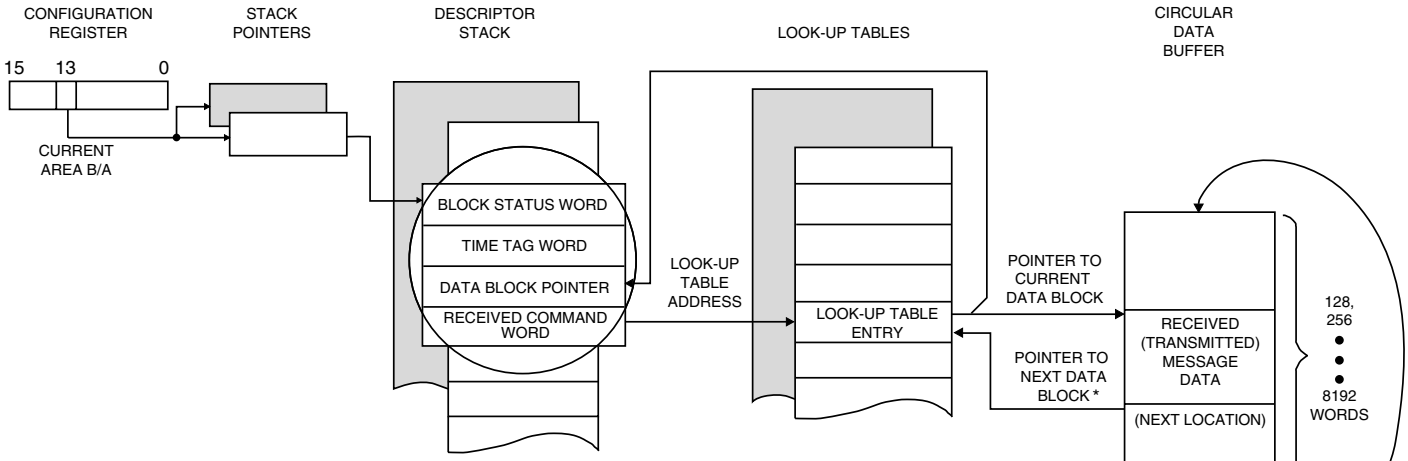


FIGURE 7. RT DOUBLE BUFFERED MODE



Notes:

1. TX/RS/BCST_SA look-up table entry is updated following valid receive (broadcast) message or following completion of transmit message
2. For the Global Circular Buffer Mode, the pointer is read from and re-written to Address 0101 (for Area A) or Address 0105 (for Area B).

FIGURE 8. RT CIRCULAR BUFFERED MODE

RT DESCRIPTOR STACK

The descriptor stack provides a chronology of all messages processed by the Mini-ACE Mark3 RT. Reference FIGURES 6, 7, and 8. Similar to BC mode, there is a four-word block descriptor in the Stack for each message processed. The four entries to each block descriptor are the Block Status Word, Time Tag Word, the pointer to the start of the message's data block, and the 16-bit received Command Word.

The RT Block Status Word includes indications of whether a particular message is ongoing or has been completed, what bus channel it was received on, indications of illegal commands, and flags denoting various message error conditions. For the double buffering, subaddress circular buffering, and global circular buffering modes, the data block pointer may be used for locating the data blocks for specific messages. Note that for mode code commands, there is an option to store the transmitted or received data word as the third word of the descriptor, in place of the data block pointer.

The Time Tag Word provides a 16-bit indication of relative time for individual messages. The resolution of the Mini-ACE Mark3's time tag is programmable from among 2, 4, 8, 16, 32, or 64 µs/LSB. There is also a provision for using an external clock input for the time tag. If enabled, there is a time tag rollover interrupt, which is issued when the value of the time tag rolls over from FFFF(hex) to 0. Other time tag options include the capabilities to clear the time tag register following receipt of a Synchronize (without data) mode command and/or to set the time tag following receipt of a Synchronize (with data) mode command. For the latter, there is an added option to filter the "set" capability based on the LSB of the received data word being equal to logic "0".

RT INTERRUPTS

The Mini-ACE Mark3 offers a great deal of flexibility in terms of RT interrupt processing. By means of the Mini-ACE Mark3's two Interrupt Mask Registers, the RT may be programmed to issue interrupt requests for the following events/conditions: End-of-(every)Message, Message Error, Selected (transmit or receive) Subaddress, 100% Circular Buffer Rollover, 50% Circular Buffer Rollover, 100% Descriptor Stack Rollover, 50% Descriptor Stack Rollover, Selected Mode Code, Transmitter Timeout, Illegal Command, and Interrupt Status Queue Rollover.

Interrupts for 50% Rollovers of Stacks and Circular Buffers. The Mini-ACE Mark3 RT and Monitor are capable of issuing host interrupts when a subaddress circular buffer pointer or stack pointer crosses its mid-point boundary. For RT circular buffers, this is applicable for both transmit and receive subaddresses. Reference FIGURE 9. There are four interrupt mask and interrupt status register bits associated with the 50% rollover function:

(1) RT circular buffer;
(2) RT command (descriptor) stack;
(3) Monitor command (descriptor) stack; and
(4) Monitor data stack.

The 50% rollover interrupt is beneficial for performing bulk data transfers. For example, when using circular buffering for a particular receive subaddress, the 50% rollover interrupt will inform the host processor when the circular buffer is half full. At that time, the host may proceed to read the received data words in the upper half of the buffer, while the Mini-ACE Mark3 RT writes received data words to the lower half of the circular buffer. Later, when the RT issues a 100% circular buffer rollover interrupt, the host can proceed to read the received data from the lower half of the buffer, while the Mini-ACE Mark3 RT continues to write received data words to the upper half of the buffer.

Interrupt status queue. The Mini-ACE Mark3 RT, Monitor, and combined RT/Monitor modes include the capability for generating an interrupt status queue. As illustrated in FIGURE 10, this provides a chronological history of interrupt generating events and conditions. In addition to the Interrupt Mask Register, the Interrupt Status Queue provides additional filtering capability, such that only valid messages and/or only invalid messages may result in the creation of an entry to the Interrupt Status Queue. Queue entries for invalid and/or valid messages may be disabled by means of bits 8 and 7 of configuration register #6.

The interrupt status queue is 64 words deep, providing the capability to store entries for up to 32 messages. These events and conditions include both message-related and non-message related events. Note that the Interrupt Vector Queue Pointer Register will always point to the next location (modulo 64) following the last vector/pointer pair written by the Mini-ACE Mark3 RT.

The pointer to the Interrupt Status Queue is stored in the INTERRUPT VECTOR QUEUE POINTER REGISTER (register address 1F). This register must be initialized by the host, and is subsequently incremented by the RT message processor. The interrupt status queue is 64 words deep, providing the capability to store entries for up to 32 messages.

The queue rolls over at addresses of modulo 64. The events that result in queue entries include both message-related and non-message-related events. Note that the Interrupt Vector Queue Pointer Register will always point to the next location (modulo 64) **following** the last vector/pointer pair written by the Mini-ACE Mark3 RT, Monitor, or RT/Monitor.

Each event that causes an interrupt results in a two-word entry to be written to the queue. The first word of the entry is the interrupt vector. The vector indicates which interrupt event(s)/condition(s) caused the interrupt.

The interrupt events are classified into two categories: message interrupt events and non-message interrupt events. Message-based interrupt events include End-of-Message, Selected mode code, Format error, Subaddress control word interrupt, RT Circular buffer Rollover, Handshake failure, RT Command stack rollover, transmitter timeout, MT Data Stack rollover, MT Command Stack rollover, RT Command Stack 50% rollover, MT Data Stack 50% rollover, MT Command Stack 50% rollover, and RT Circular buffer 50% rollover. Non-message interrupt events/conditions include time tag rollover, RT address parity error, RAM parity error, and BIT completed.

Bit 0 of the interrupt vector (interrupt status) word indicates whether the entry is for a message interrupt event (if bit 0 is logic "1") or a non-message interrupt event (if bit 0 is logic "0"). It is **not** possible for one entry on the queue to indicate both a message interrupt and a non-message interrupt.

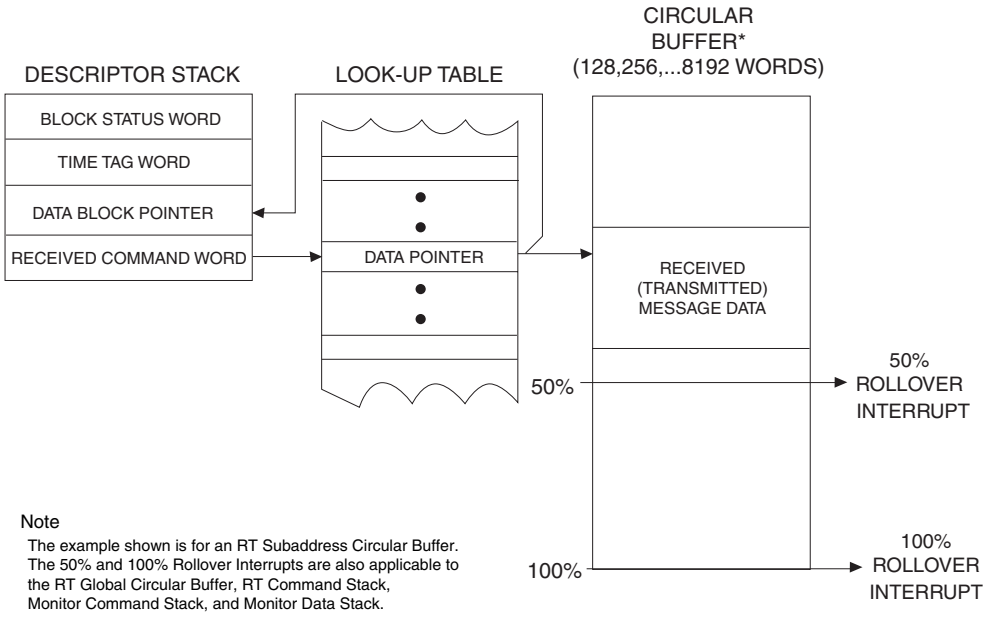


FIGURE 9. 50% and 100% ROLLOVER INTERRUPTS

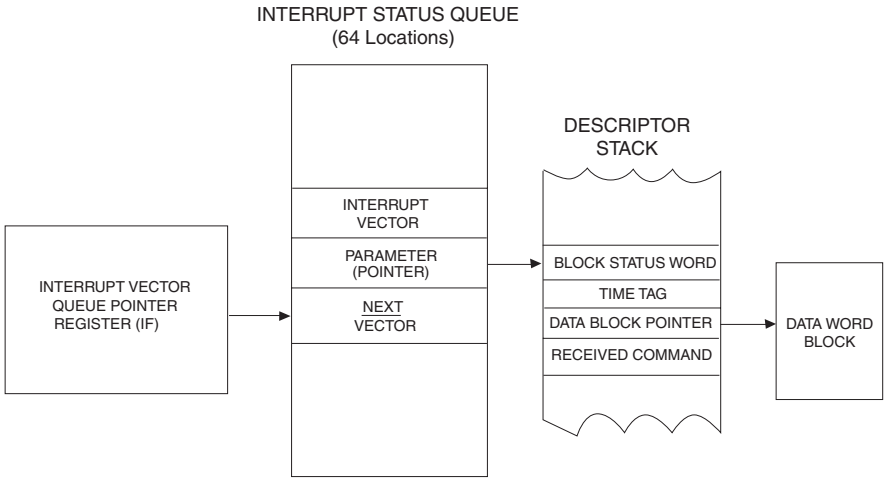


FIGURE 10. RT (and MONITOR) INTERRUPT STATUS QUEUE (shown for message Interrupt event)

As illustrated in FIGURE 10, for a message interrupt event, the parameter word is a pointer. The pointer will reference the first word of the RT or MT command stack descriptor (i.e., the Block Status Word).

For a RAM Parity Error non-message interrupt, the parameter will be the RAM address where the parity check failed. For the RT address Parity Error, Protocol Self-test Complete, and Time Tag rollover non-message interrupts, the parameter is not used; it will have a value of 0000.

If enabled, an INTERRUPT STATUS QUEUE ROLLOVER interrupt will be issued when the value of the queue pointer address rolls over at a 64-word address boundary.

NOTE: Please see Appendix "F" of the Enhanced Mini-ACE User's Guide for important information applicable only to RT MODE operation, enabling of the interrupt status queue and use of specific non-message interrupts.

RT COMMAND ILLEGALIZATION

The Mini-ACE Mark3 provides an internal mechanism for RT Command Word illegalizing. By means of a 256-word area in shared RAM, the host processor may designate that any message be illegalized, based on the command word T/$\overline{R}$ bit, subaddress, and word count/mode code fields. The Mini-ACE Mark3 illegalization scheme provides the maximum in flexibility, allowing any subset of the 4096 possible combinations of broadcast/own address, T/$\overline{R}$ bit, subaddress, and word count/mode code to be illegalized.

The address map of the Mini-ACE Mark3's illegalizing table is illustrated in TABLE 41.

BUSY BIT

The Mini-ACE Mark3 RT provides two different methods for setting the Busy status word bit: (1) globally, by means of Configuration Register #1; or (2) on a T/R-bit/subaddress basis, by means of a RAM lookup table. If the host CPU asserts the $\overline{BUSY}$ bit to logic "0" in Configuration Register #1, the Mini-ACE Mark3 RT will

TABLE 41. ILLEGALIZATION TABLE MEMORY MAP

ADDRESS	DESCRIPTION
300	Brdcst / Rx, SA 0. MC15-0
301	Brdcst / Rx, SA 0. MC31-16
302	Brdcst / Rx, SA 1. WC15-0
303	Brdcst / Rx, SA 1. WC31-16
• • •	• • •
33F	Brdcst / Rx, SA 31. MC31-16
340	Brdcst / Tx, SA 0. MC15-0
341	Brdcst / Tx, SA 0. MC31-16
342	Brdcst / Tx, SA 1. WC15-0
• • •	• • •
37D	Brdcst / Tx, SA 30. WC31-16
37E	Brdcst / Tx, SA 31. MC15-0
37F	Brdcst / Tx, SA 31. MC31-16
380	Own Addr / Rx, SA 0. MC15-0
381	Own Addr / Rx, SA 0. MC31-16
382	Own Addr / Rx, SA 1. WC15-0
383	Own Addr / Rx, SA 1. WC31-16
• • •	• • •
3BE	Own Addr / Rx, SA 31. MC15-0
3BF	Own Addr / Rx, SA 31. MC31-16
3C0	Own Addr / Tx, SA 0. MC15-0
3C1	Own Addr / Tx, SA 0. MC31-16
3C2	Own Addr / Tx, SA 1. WC15-0
3C3	Own Addr / Tx, SA 1. WC31-16
• • •	• • •
3FC	Own Addr / Tx, SA 30. WC15-0
3FD	Own Addr / Tx, SA 30. WC31-16
3FE	Own Addr / Tx, SA 31. MC15-0
3FF	Own Addr / Tx, SA 31. MC31-16

respond to **all** non-broadcast commands with the Busy bit set in its RT Status Word.

Alternatively, there is a Busy lookup table in the Mini-ACE Mark3 shared RAM. By means of this table, it is possible for the host processor to set the busy bit for any selectable subset of the 128 combinations of broadcast/own address, T/$\overline{R}$ bit, and subaddress.

If the busy bit is set for a transmit command, the Mini-ACE Mark3 RT will respond with the busy bit set in the status word, but will not transmit any data words. If the busy bit is set for a receive command, the RT will also respond with the busy status bit set. There are two programmable options regarding the reception of data words for a non-mode code receive command for which the RT is busy: (1) to transfer the received data words to shared RAM; or (2) to **not** transfer the data words to shared RAM.

RT ADDRESS

The Mini-ACE Mark3 offers several different options for designating the Remote Terminal address. These include the following: (1) hardwired, by means of the 5 RT ADDRESS inputs, and the RT ADDRESS PARITY input; (2) by means of the RT ADDRESS (and PARITY) inputs, but latched via hardware, on the rising edge of the RT_AD_LAT input signal; (3) input by means of the RT ADDRESS (and PARITY) inputs, but latched via host software; and (4) software programmable, by means of an internal register. In all four configurations, the RT address is readable by the host processor.

RT BUILT-IN-TEST (BIT) WORD

The bit map for the Mini-ACE Mark3's internal RT Built-in-Test (BIT) Word is indicated in TABLE 42.

RT AUTO-BOOT OPTION

If utilized, the RT pin-programmable auto-boot option allows the Mini-ACE Mark3 RT to automatically initialize as an active remote terminal with the Busy status word bit set to logic "1" immediately following power turn-on. This is a useful feature for MIL-STD-1760 applications, in which the RT is required to be responding within 150 ms after power-up. This feature is available for versions of the Mini-ACE Mark3 with 4K words of RAM.

TABLE 42. RT BIT WORD

BIT	DESCRIPTION
15(MSB)	TRANSMITTER TIMEOUT
14	LOOP TEST FAILURE B
13	LOOP TEST FAILURE A
12	HANDSHAKE FAILURE
11	TRANSMITTER SHUTDOWN B
10	TRANSMITTER SHUTDOWN A
9	TERMINAL FLAG INHIBITED
8	BIT TEST FAILURE
7	HIGH WORD COUNT
6	LOW WORD COUNT
5	INCORRECT SYNC RECEIVED
4	PARITY / MANCHESTER ERROR RECEIVED
3	RT-to-RT GAP / SYNC ADDRESS ERROR
2	RT-to-RT NO RESPONSE ERROR
1	RT-to-RT 2ND COMMAND WORD ERROR
0 (LSB)	COMMAND WORD CONTENTS ERROR

OTHER RT FEATURES

The Mini-ACE Mark3 includes options for the Terminal flag status word bit to be set either under software control and/or automatically following a failure of the loopback self-test. Other software programmable RT options include software programmable RT status and RT BIT words, automatic clearing of the Service Request bit following receipt of a Transmit vector word mode command, options regarding Data Word transfers for the Busy and Message error (illegal) Status word bits, and options for the handling of 1553A and reserved mode codes.

MONITOR ARCHITECTURE

The Mini-ACE Mark3 includes three monitor modes:

(1) A Word Monitor mode

(2) A selective message monitor mode

(3) A combined RT/message monitor mode

For new applications, it is recommended that the selective message monitor mode be used, rather than the word monitor mode. Besides providing monitor filtering based on RT address, T/$\overline{R}$ bit, and subaddress, the message monitor eliminates the need to determine the start and end of messages by software.

WORD MONITOR MODE

In the Word Monitor Terminal mode, the Mini-ACE Mark3 monitors both 1553 buses. After the software initialization and Monitor Start sequences, the Mini-ACE Mark3 stores all Command, Status, and Data Words received from both buses. For each word received from either bus, a pair of words is stored to the Mini-ACE Mark3's shared RAM. The first word is the word received from the 1553 bus. The second word is the Monitor Identification (ID), or "Tag" word. The ID word contains information relating to bus channel, word validity, and inter-word time gaps. The data and ID words are stored in a circular buffer in the shared RAM address space.

WORD MONITOR MEMORY MAP

A typical word monitor memory map is illustrated in TABLE 43. TABLE 43 assumes a 64K address space for the Mini-ACE Mark3's monitor. The Active Area Stack pointer provides the address where the first monitored word is stored. In the example, it is assumed that the Active Area Stack Pointer for Area A (location 0100) is initialized to 0000. The first received data word is stored in location 0000, the ID word for the first word is stored in location 0001, etc.

The current Monitor address is maintained by means of a counter register. This value may be read by the CPU by means of the Data Stack Address Register. It is important to note that when the counter reaches the Stack Pointer address of 0100 or 0104, the initial pointer value stored in this shared RAM location **will be overwritten** by the monitored data and ID Words. When the internal counter reaches an address of FFFF (or 0FFF, for an Mini-ACE Mark3 with 4K RAM), the counter rolls over to 0000.

TABLE 43. TYPICAL WORD MONITOR MEMORY MAP	
HEX ADDRESS	**FUNCTION**
0000	First Received 1553 Word
0001	First Identification Word
0002	Second Received 1553 Word
0003	Second Identification Word
0004	Third Received 1553 Word
005	Third Identification Word
• • •	• • •
0100	Stack Pointer (Fixed Location - gets overwritten)
• • • FFFF	• • • Received 1553 Words and Identification Word

WORD MONITOR TRIGGER

In the Word Monitor mode, there is a pattern recognition trigger and a pattern recognition interrupt. The 16-bit compare word for both the trigger and the interrupt is stored in the Monitor Trigger Word Register. The pattern recognition interrupt is enabled by setting the MT Pattern Trigger bit in Interrupt Mask Register #1. The pattern recognition trigger is enabled by setting the Trigger Enable bit in Configuration Register #1 and selecting either the Start-on-trigger or the Stop-on-trigger bit in Configuration Register #1.

The Word Monitor may also be started by means of a low-to-high transition on the EXT_TRIG input signal.

SELECTIVE MESSAGE MONITOR MODE

The Mini-ACE Mark3 Selective Message Monitor provides monitoring of 1553 messages with filtering based on RT address, T/$\overline{R}$ bit, and subaddress with no host processor intervention. By autonomously distinguishing between 1553 command and status words, the Message Monitor determines when messages begin and end, and stores the messages into RAM, based on a programmable filter of RT address, T/$\overline{R}$ bit, and subaddress.

The selective monitor may be configured as just a monitor, or as a **combined RT/Monitor.** In the combined RT/Monitor mode, the Mini-ACE Mark3 functions as an RT for one RT address (including broadcast messages), and as a selective message monitor for the other 30 RT addresses. The Mini-ACE Mark3 Message Monitor contains two stacks, a command stack and a data stack, that are independent from the RT command stack. The pointers for these stacks are located at fixed locations in RAM.

MONITOR SELECTION FUNCTION

Following receipt of a valid command word in Selective Monitor mode, the Mini-ACE Mark3 will reference the selective monitor lookup table to determine if the particular command is enabled. The address for this location in the table is determined by means of an offset based on the RT Address, T/$\overline{R}$ bit, and Subaddress bit 4 of the current command word, and concatenating it to the monitor lookup table base address of 0280 (hex). The bit location within this word is determined by subaddress bits 3-0 of the current command word.

If the specified bit in the lookup table is logic "0", the command is not enabled, and the Mini-ACE Mark3 will ignore this command. If this bit is logic "1", the command is enabled and the Mini-ACE Mark3 will create an entry in the monitor command descriptor stack (based on the monitor command stack pointer), and store the data and status words associated with the command into sequential locations in the monitor data stack. In addition, for an RT-to-RT transfer in which the receive command is selected, the second command word (the transmit command) is stored in the monitor data stack.

The address definition for the Selective Monitor Lookup Table is illustrated in TABLE 44.

TABLE 44. MONITOR SELECTION TABLE LOOKUP ADDRESS	
BIT	**DESCRIPTION**
15(MSB)	Logic “0”
14	Logic “0”
13	Logic “0”
12	Logic “0”
11	Logic “0”
10	Logic “0”
9	Logic “1”
8	Logic “0”
7	Logic “1”
6	RTAD_4
5	RTAD_3
4	RTAD_2
3	RTAD_1
2	RTAD_0
1	TRANSMIT / $\overline{\text{RECEIVE}}$
0(LSB)	SUBADDRESS 4

SELECTIVE MESSAGE MONITOR MEMORY ORGANIZATION

A typical memory map for the Mini-ACE Mark3 in the Selective Message Monitor mode, assuming a 4K RAM space, is illustrated in TABLE 45. This mode of operation defines several fixed locations in the RAM. These locations are allocated in a way in which none of them overlap with the fixed RT locations. This allows for the combined RT/Selective Message Monitor mode.

The fixed memory map consists of two Monitor Command Stack Pointers (locations 102 and 106 hex), two Monitor Data Stack Pointers (locations 103 and 107 hex), and a Selective Message Monitor Lookup Table (locations 0280 through 02FF hex). For this example, the Monitor Command Stack size is assumed to be 1K words, and the Monitor Data Stack size is assumed to be 2K words.

FIGURE 11 illustrates the Selective Message Monitor operation. Upon receipt of a valid Command Word, the Mini-ACE Mark3 will reference the Selective Monitor Lookup Table to determine if the current command is enabled. If the current command is disabled, the Mini-ACE Mark3 monitor will ignore (and not store) the current message. If the command is enabled, the monitor will create

an entry in the Monitor Command Stack at the address location referenced by the Monitor Command Stack Pointer, and an entry in the monitor data stack starting at the location referenced by the Monitor Data Stack Pointer.

The format of the information in the data stack depends on the format of the message that was processed. For example, for a BC-to-RT transfer (receive command), the monitor will store the command word in the monitor command descriptor stack, with the data words and the receiving RT's status word stored in the monitor data stack.

The size of the monitor command stack is programmable, with choices of 256, 1K, 4K, or 16K words. The monitor data stack size is programmable with choices of 512, 1K, 2K, 4K, 8K, 16K, 32K or 64K words.

MONITOR INTERRUPTS

Selective monitor interrupts may be issued for End-of-message and for conditions relating to the monitor command stack pointer and monitor data stack pointer. The latter, as shown in FIGURE 9, include Command Stack 50% Rollover, Command Stack 100% Rollover, Data Stack 50% Rollover, and Data Stack 100% Rollover.

The 50% rollover interrupts may be used to inform the host processor when the command stack or data stack is half full. At that time, the host may proceed to read the received messages in the upper half of the respective stack, while the Mini-ACE Mark3 monitor writes messages to the lower half of the stack. Later, when the monitor issues a 100% stack rollover interrupt, the host can proceed to read the received data from the lower half of the stack, while the Mini-ACE Mark3 monitor continues to write received data words to the upper half of the stack.

INTERRUPT STATUS QUEUE

Like the Mini-ACE Mark3 RT, the Selective Monitor mode includes the capability for generating an interrupt status queue. As illustrated in FIGURE 10, this provides a chronological history of interrupt generating events. Besides the two Interrupt Mask Registers, the Interrupt Status Queue provides additional filtering capability, such that only valid messages and/or only invalid messages may result in entries to the Interrupt Status Queue. The interrupt status queue is 64 words deep, providing the capability to store entries for up to 32 monitored messages.

TABLE 45. TYPICAL SELECTIVE MESSAGE MONITOR MEMORY MAP (shown for 4K RAM for "Monitor only" mode)

ADDRESS (HEX)	DESCRIPTION
0000-0101	Not Used
0102	Monitor Command Stack Pointer A (fixed location)
0103	Monitor Data Stack Pointer A (fixed location)
0104-0105	Not Used
0106	Monitor Command Stack Pointer B (fixed location)
0107	Monitor Data Stack Pointer B (fixed location)
0108-027F	Not Used
0280-02FF	Selective Monitor Lookup Table (fixed location)
0300-03FF	Not Used
0400-07FF	Monitor Command Stack A
0800-0FFF	Monitor Data Stack A

MISCELLANEOUS

CLOCK INPUT

The Mini-ACE Mark3 decoder is capable of operating from a 10, 12, 16, or 20 MHz clock input. Depending on the configuration of the specific model Mini-ACE Mark3 terminal, the selection of the clock input frequency may be chosen by one of either two methods. For all versions, the clock frequency may be specified by means of the host processor writing to Configuration Register #6. With the second method, which is applicable only for the versions incorporating 4K (but not 64K) words of internal RAM, the clock frequency may be specified by means of the input signals that are otherwise used as the A15 and A14 address lines.

ENCODER/DECODERS

For the selected clock frequency, there is internal logic to derive the necessary clocks for the Manchester encoder and decoders. For all clock frequencies, the decoders sample the receiver outputs on **both** edges of the input clock. By in effect doubling the decoders' sampling frequency, this serves to widen the tolerance to zero-crossing distortion, and reduce the bit error rate.

For interfacing to fiber optic transceivers (e.g., for MIL-STD-1773 applications), the decoders are capable of operating with single-ended, rather than double-ended, input signals. The standard transceiverless version (BU-64XXXX0) of the Mini-ACE Mark3 is internally strapped for single-ended input signals. For applications involving the use of double-ended transceivers, it is suggested that you contact the factory at DDC regarding a double-ended transceiverless version of the Mini-ACE Mark3.

TIME TAG

The Mini-ACE Mark3 includes an internal read/writable Time Tag Register. This register is a CPU read/writable 16-bit counter with a programmable resolution of either 2, 4, 8, 16, 32, or 64 µs per LSB. Another option allows software controlled incrementing of the Time Tag Register. This supports self-test for the Time Tag Register. For each message processed, the value of the Time Tag Register is loaded into the second location of the respective descriptor stack entry ("TIME TAG WORD") for both the BC and RT modes.

The functionality involving the Time Tag Register that's compatible with ACE/Mini-ACE (Plus) includes: the capability to issue an interrupt request and set a bit in the Interrupt Status Register when the Time Tag Register rolls over FFFF to 0000; for RT mode, the capability to automatically clear the Time Tag Register following reception of a Synchronize (without data) mode command, or to load the Time Tag Register following a Synchronize (with data) mode command.

Additional time tag features supported by the Mini-ACE Mark3 include the capability for the BC to transmit the contents of the Time Tag Register as the data word for a Synchronize (with data) mode command; the capability for the RT to "filter" the data word for the Synchronize with data mode command, by only loading the Time Tag Register if the LSB of the received data word is "0"; an instruction enabling the BC Message Sequence Control engine to load the Time Tag Register with a specified value; and an instruction enabling the BC Message Sequence Control engine to write the value of the Time Tag Register to the General Purpose Queue.

INTERRUPTS

The Mini-ACE Mark3 series terminals provide many programmable options for interrupt generation and handling. The interrupt output pin ($\overline{INT}$) has three software programmable modes of operation: a pulse, a level output cleared under software control, or a level output automatically cleared following a read of the Interrupt Status Register (#1 or #2).

Individual interrupts are enabled by the two Interrupt Mask Registers. The host processor may determine the cause of the interrupt by reading the two Interrupt Status Registers, which provide the current state of interrupt events and conditions. The Interrupt Status Registers may be updated in two ways. In one interrupt handling mode, a particular bit in Interrupt Status Register #1 or #2 will be updated only if the event occurs **and** the corresponding bit in Interrupt Mask Register #1 or #2 is enabled. In the enhanced interrupt handling mode, a particular bit in one of the Interrupt Status Registers will be updated if the event/condition occurs regardless of the value of the corresponding Interrupt Mask Register bit. In either case, the respective Interrupt Mask Register (#1 or #2) bit is used to enable an interrupt for a particular event/condition.

The Mini-ACE Mark3 supports all the interrupt events from ACE/Mini-ACE (Plus), including RAM Parity Error, Transmitter Timeout, BC/RT Command Stack Rollover, MT Command Stack and Data Stack Rollover, Handshake Error, BC Retry, RT Address Parity Error, Time Tag Rollover, RT Circular Buffer Rollover, BC Message, RT Subaddress, BC End-of-Frame, Format Error, BC Status Set, RT Mode Code, MT Trigger, and End-of-Message.

For the Mini-ACE Mark3's Enhanced BC mode, there are four user-defined interrupt bits. The BC Message Sequence Control Engine includes an instruction enabling it to issue these interrupts at any time.

For RT and Monitor modes, the Mini-ACE Mark3 architecture includes an Interrupt Status Queue. This provides a mechanism for logging messages that result in interrupt requests. Entries to the Interrupt Status Queue may be filtered such that only valid and/or invalid messages will result in entries on the queue.

The Mini-ACE Mark3 incorporates additional interrupt conditions beyond the ACE/Mini-ACE (Plus), based on the addition of Interrupt Mask Register #2 and Interrupt Status Register #2. This is accomplished by chaining the two Interrupt Status Registers using the INTERRUPT CHAIN BIT (bit 0) in Interrupt Status Register #2 to indicate that an interrupt has occurred in Interrupt Status Register #1. Additional interrupts include "Self-Test Completed", masking bits for the Enhanced BC Control Interrupts, 50% Rollover interrupts for RT Command Stack, RT Circular Buffers, MT Command Stack, and MT Data Stack; BC Op Code Parity Error, (RT) Illegal Command, (BC) General Purpose Queue or (RT/MT) Interrupt Status Queue Rollover, Call Stack Pointer Register Error, BC Trap Op Code, and the four User-Defined interrupts for the Enhanced BC mode.

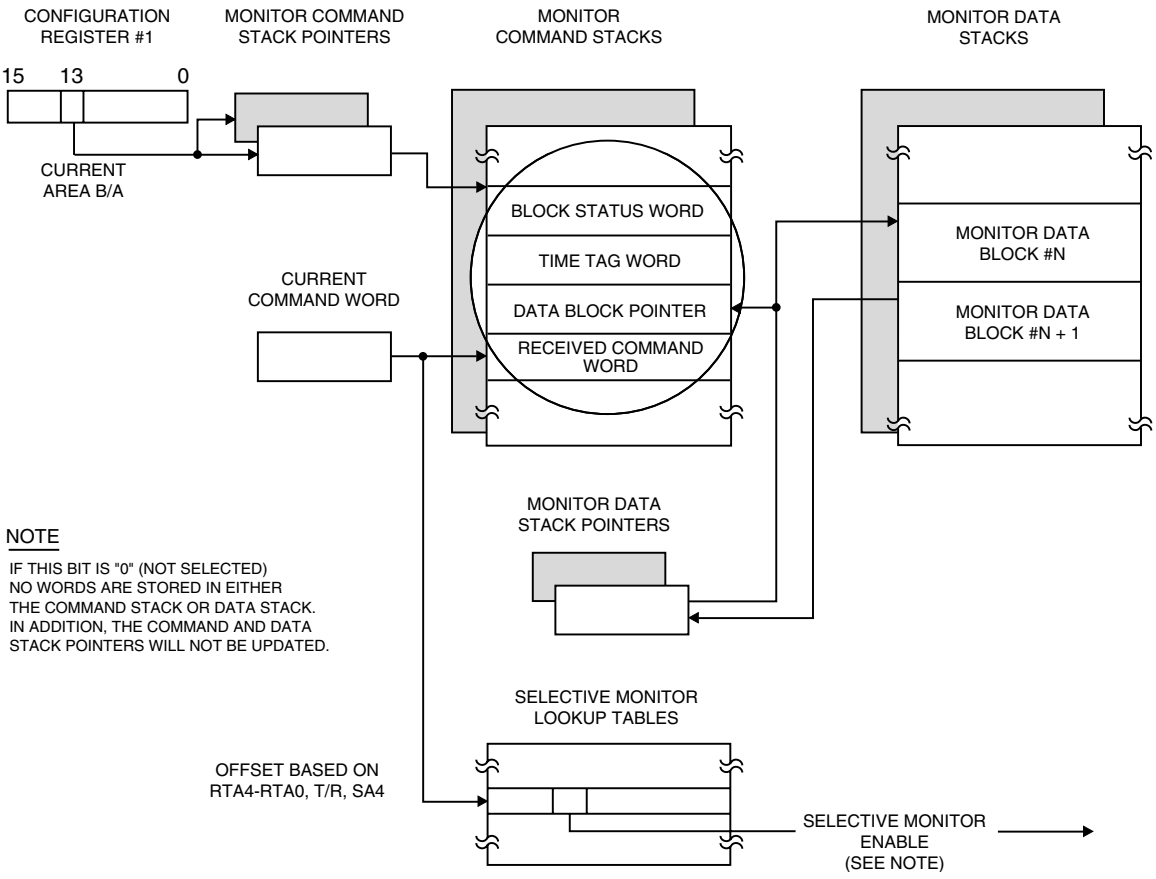


FIGURE 11. SELECTIVE MESSAGE MONITOR MEMORY MANAGEMENT

BUILT-IN TEST

A salient feature of the Mini-ACE Mark3 is its highly autonomous self-test capability. This includes both protocol and RAM self-tests. Either or both of these self-tests may be initiated by command(s) from the host processor.

The protocol test consists of a comprehensive toggle test of the terminal's logic. The test includes testing of all registers, Manchester decoders, protocol logic, and memory management logs. This test is completed in approximately 32,000 clock cycles. That is, about 1.6 ms with a 20 MHz clock, 2.0 ms at 16 MHz, 2.7 ms at 12 MHz, and 3.2 ms at 10 MHz.

There is also a separate built-in test (BIT) for the Mini-ACE Mark3's 4K X 16 or 64K X 16 shared RAM. This test consists of writing and then reading/verifying the two walking patterns "data = address" and "data = address inverted". This test takes 10 clock cycles per word. For a Mini-ACE Mark3 with 4K words of RAM, this is about 2.0 ms with a 20 MHz clock, 2.6 ms at 16 MHz, 3.4 ms at 12 MHz, or 4.1 ms at 10 MHz. For an Mini-ACE Mark3 with 64K words of RAM, this test takes about 32.8 ms with a 20 MHz clock, 40.1 ms at 16 MHz, 54.6 ms at 12 MHz, or 65.6 ms at 10 MHz.

The Mini-ACE Mark3 built-in protocol test is performed automatically at power-up. In addition, the protocol or RAM self-tests may be initiated by a command from the host processor, via the START/RESET REGISTER. For RT mode, this may include the host processor invoking self-test following receipt of an Initiate self-test mode command. The results of the self-test are host accessible by means of the BIT status register. For RT mode, the result of the self-test may be communicated to the bus controller via bit 8 of the RT BIT word ("0" = pass, "1" = fail).

Assuming that the protocol self-test passes, all of the register and shared RAM locations will be restored to their state prior to the self-test, with the exception of the 60 RAM address locations 0342-037D and the TIME TAG REGISTER. Note that for RT mode, these locations map to the illegalization lookup table for "broadcast transmit subaddresses 1 through 30" (non-mode code subaddresses). Since MIL-STD-1553 does not define these as valid command words, this section of the illegalization lookup table is normally not used during RT operation. The TIME TAG REGISTER will continue to increment during the self-test.

If there is a failure of the protocol self-test, it is possible to access information about the first failed vector. This may be done by means of the Mini-ACE Mark3's upper registers (register addresses 32 through 63). Through these registers, it is possible to determine the self-test ROM address of the first failed vector, the expected response data pattern (from the ROM), the register or memory address, and the actual (incorrect) data value read from register or memory. The on-chip self-test ROM is 4K X 24.

Note that the RAM self-test is destructive. That is, following the RAM self-test, regardless of whether the test passes or fails, the shared RAM is **not** restored to its state prior to this test. Following a failed RAM self-test, the host may read the internal RAM to determine which location(s) failed the walking pattern test.

RAM PARITY

The BC/RT/MT version of the Mini-ACE Mark3 is available with options of 4K or 64K words of internal RAM. For the 64K option, the RAM is 17 bits wide. The 64K X 17 internal RAM allows for parity generation for RAM write accesses, and parity checking for RAM read accesses. This includes host RAM accesses, as well as accesses by the Mini-ACE Mark3's internal logic. When the Mini-ACE Mark3 detects a RAM parity error, it reports it to the host processor by means of an interrupt and a register bit. Also, for the RT and Selective Message Monitor modes, the RAM address where a parity error was detected will be stored on the Interrupt Status Queue (if enabled).

RELOCATABLE MEMORY MANAGEMENT LOCATIONS

In the Mini-ACE Mark3's default configuration, there is a *fixed* area of shared RAM addresses, 0000h-03FF, that is allocated for storage of the BC's or RT's pointers, counters, tables, and other "non-message" data structures. As a means of reducing the overall memory address space for using multiple Mini-ACE Mark3's in a given system (e.g., for use with the DMA interface configuration), the Mini-ACE Mark3 allows this area of RAM to be relocated by means of 6 configuration register bits. To provide backwards compatibility to ACE and Mini-ACE, the default for this RAM area is 0000h-03FFh.

HOST PROCESSOR INTERFACE

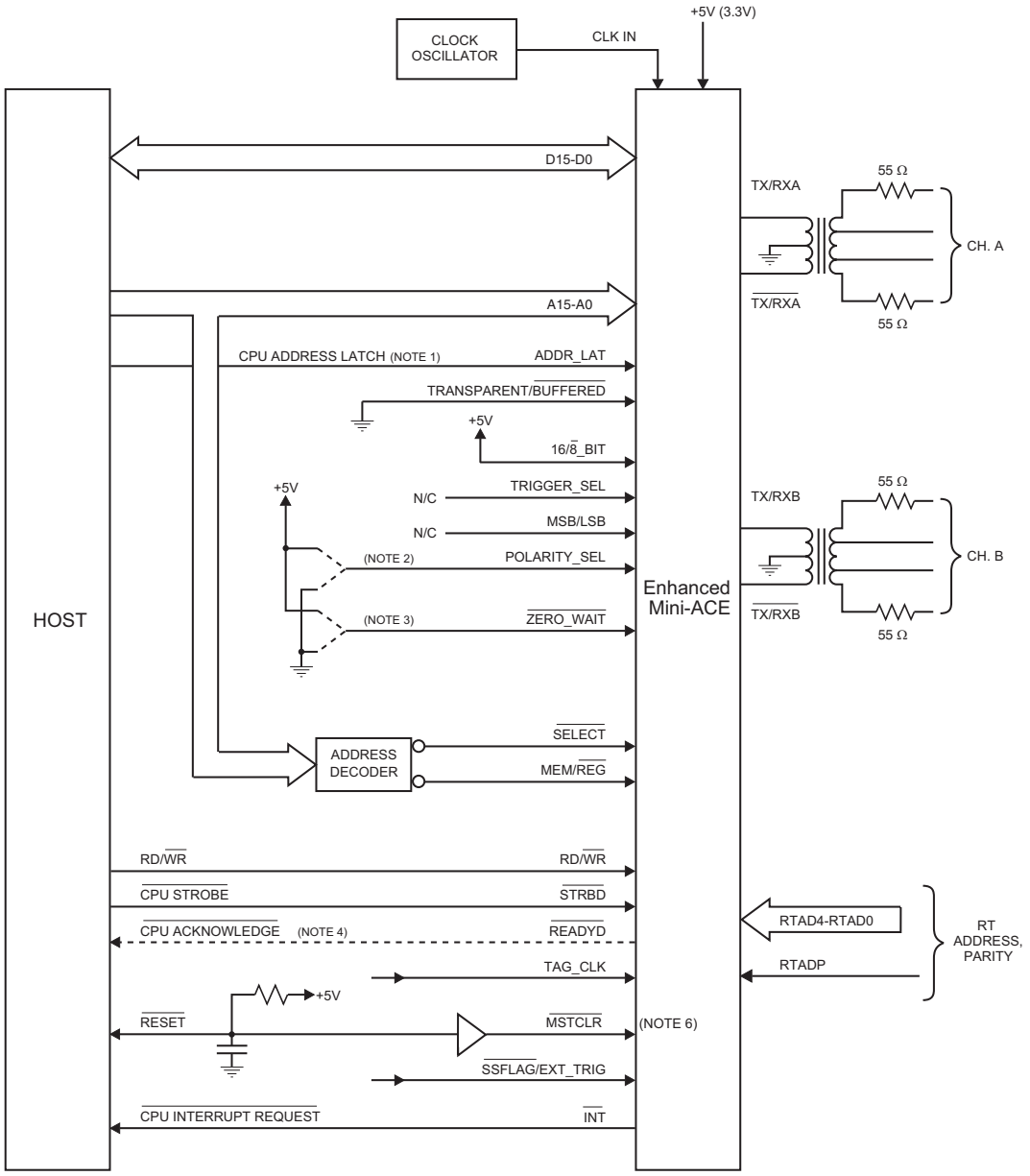
The Mini-ACE Mark3 supports a wide variety of processor interface configurations. These include shared RAM and DMA configurations, straightforward interfacing for 16-bit and 8-bit buses, support for both non-multiplexed and multiplexed address/data buses, non-zero wait mode for interfacing to a processor address/data buses, and zero wait mode for interfacing (for example) to microcontroller I/O ports. In addition, with respect to the ACE/Mini-ACE, the Mini-ACE Mark3 provides two major improvements: (1) reduced maximum host access time for shared RAM mode; and (2) increased maximum DMA grant time for the transparent/DMA mode.

The Mini-ACE Mark3's maximum host holdoff time (time prior to the assertion of the $\overline{\text{READYD}}$ handshake signal) has been significantly reduced. For ACE/Mini-ACE, this maximum holdoff time is 17 internal word transfer cycles, resulting in an overall holdoff time of approximately 4.6 µs, using a 16 MHz clock. By comparison, using the Mini-ACE Mark3's ENHANCED CPU ACCESS feature, this worst-case holdoff time is reduced significantly, to a single internal transfer cycle. For example, when operating the Mini-ACE Mark3 in its 16-bit buffered, non-zero wait configuration with a 16 MHz clock input, this results in a maximum overall host transfer cycle time of 632 ns for a read cycle, or 570 ns for a write cycle.

In addition, when using the ACE or Mini-ACE in the transparent/DMA configuration, the maximum request-to-grant time, which occurs prior to an RT start-of-message sequence, is 4.0 µs with a 16 MHz clock, or 3.5 µs with a 12 MHz clock. For the Mini-ACE Mark3 functioning as a MIL-STD-1553B RT, this time has been increased to 8.5 µs at 10 MHz, 9 µs at 12 MHz, 10 µs at 16 MHz, and 10.5 µs at 20MHz. This provides greater flexibility, particularly for systems in which a host has to arbitrate among multiple DMA requestors.

By far, the most commonly used processor interface configuration is the 16-bit buffered, non-zero wait mode. This configuration may be used to interface between 16-bit or 32-bit microprocessors and an Mini-ACE Mark3. In this mode, only the Mini-ACE Mark3's internal 4K or 64K words of internal RAM are used for storing 1553 message data and associated "housekeeping" functions. That is, in this configuration, the Mini-ACE Mark3 will never attempt to access memory on the host bus.

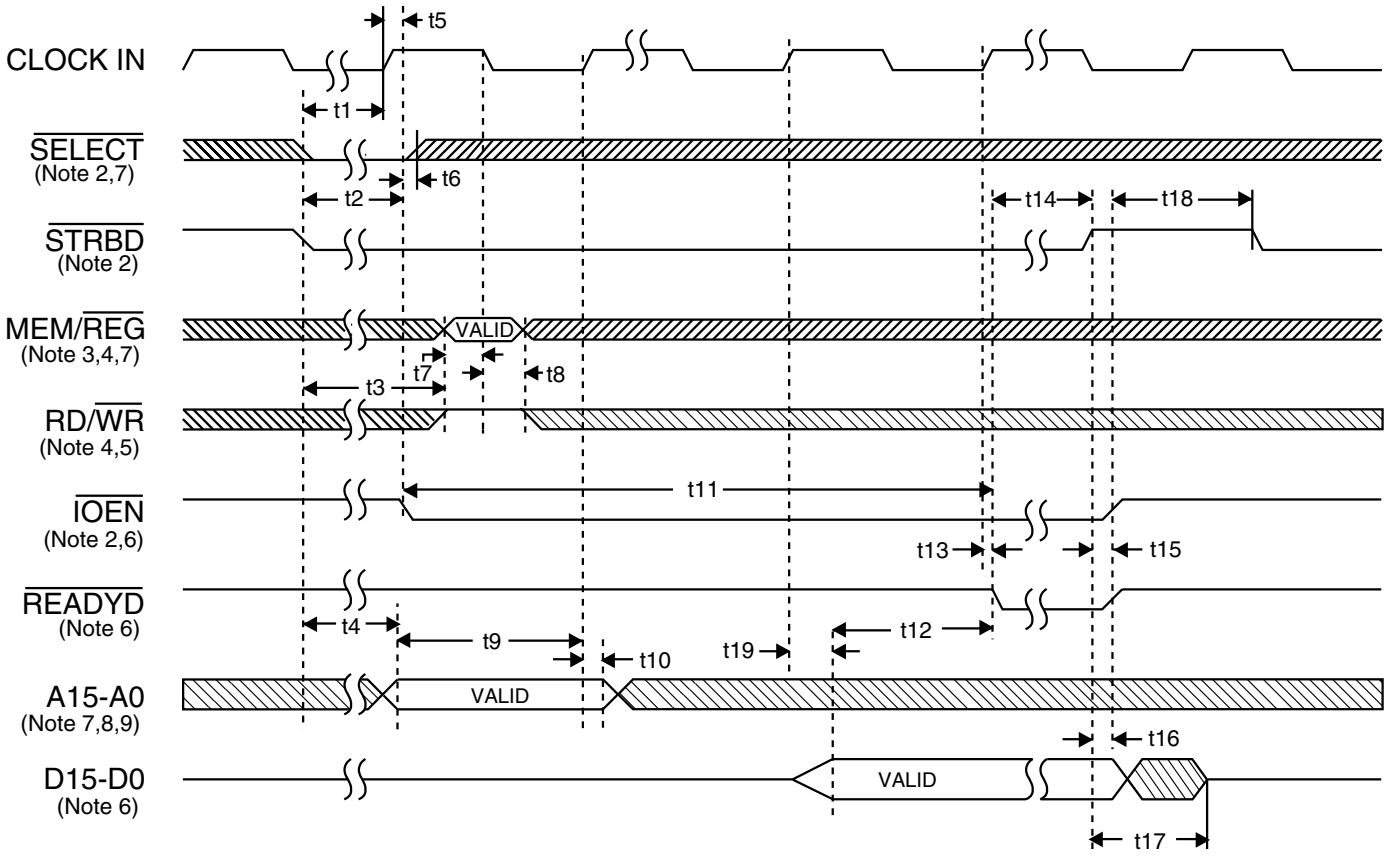
FIGURE 12 illustrates a generic connection diagram between a 16-bit (or 32-bit) microprocessor and an Mini-ACE Mark3 for the 16-bit buffered configuration, while FIGURES 13 and 14, and associated tables illustrate the processor read and write timing respectively.



NOTES:

1. CPU ADDRESS LATCH SIGNAL PROVIDED BY PROCESSORS WITH MULTIPLEXED ADDRESS/DATA BUSES. FOR PROCESSORS WITH NON-MULTIPLEXED ADDRESS AND DATA BUSSES, ADDR_LAT SHOULD BE CONNECTED TO +5V.
2. IF POLARITY_SEL = "1", RD/$\overline{WR}$ IS HIGH TO READ, LOW TO WRITE.
   IF POLARITY_SEL = "0", RD/$\overline{WR}$ IS LOW TO READ, HIGH TO WRITE.
3. $\overline{ZERO\_WAIT}$ SHOULD BE STRAPPED TO LOGIC "1" FOR NON-ZERO WAIT INTERFACE AND TO LOGIC "0" FOR ZERO WAIT INTERFACE.
4. $\overline{CPU\ ACKNOWLEDGE}$ PROCESSOR INPUT ONLY FOR NON-ZERO WAIT TYPE OF INTERFACE.
6. THE RISE TIME FOR MSTCLR MUST BE LESS THAN 10µS IN ORDER TO $\overline{ENSURE}$ CORRECT INITIALIZATION OF THE ENHANCED MINI-ACE'S TRANSCEIVERS.

FIGURE 12. HOST PROCESSOR INTERFACE - 16-BIT BUFFERED CONFIGURATION

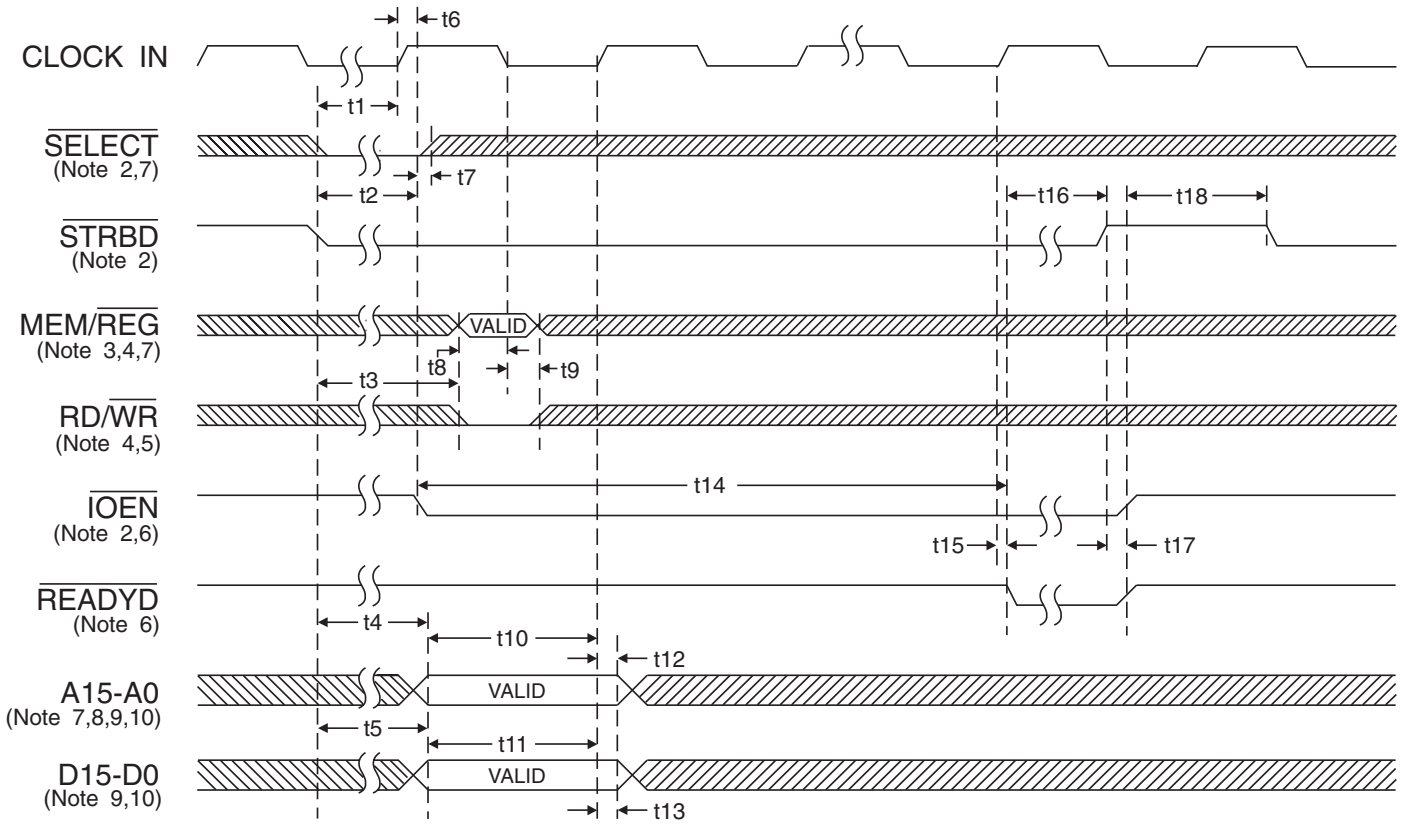


NOTES:

1. For the 16-bit buffered nonzero wait configuration, TRANSPARENT/$\overline{\text{BUFFERED}}$ must be connected to logic "0". $\overline{\text{ZERO\_WAIT}}$ and $\overline{\text{DTREQ}}$ / 16/$\overline{8}$ must be connected to logic "1". The inputs TRIGGER_SEL and MSB/LSB may be connected to either Vcc or ground.
2. $\overline{\text{SELECT}}$ and $\overline{\text{STRBD}}$ may be tied together. $\overline{\text{IOEN}}$ goes low on the first rising CLK edge when $\overline{\text{SELECT}}$ • $\overline{\text{STRBD}}$ is sampled low (satisfying t1) and the Mark3's protocol/memory management logic is not accessing the internal RAM. When this occurs, $\overline{\text{IOEN}}$ goes low, starting the transfer cycle. After $\overline{\text{IOEN}}$ goes low, $\overline{\text{SELECT}}$ may be released high.
3. MEM/$\overline{\text{REG}}$ must be presented high for memory access, low for register access.
4. MEM/$\overline{\text{REG}}$ and RD/$\overline{\text{WR}}$ are buffered transparently until the first falling edge of CLK after $\overline{\text{IOEN}}$ goes low. After this CLK edge, MEM/$\overline{\text{REG}}$ and RD/WR become latched internally.
5. The logic sense for RD/WR in the diagram assumes that POLARITY_SEL is connected to logic "1". If POLARITY_SEL is connected to logic "0", RD/$\overline{\text{WR}}$ must be asserted low to read.
6. The timing for $\overline{\text{IOEN}}$, $\overline{\text{READYD}}$ and D15-D0 assumes a 50 pf load. For loading above 50 pf, the validity of $\overline{\text{IOEN}}$, $\overline{\text{READYD}}$, and D15-D0 is delayed by an additional 0.14 ns/pf typ, 0.28 ns/pf max.
7. The timing for A15-A0, MEM/$\overline{\text{REG}}$ and $\overline{\text{SELECT}}$ assumes that ADDR-LAT is connected to logic "1". Refer to Address Latch timing for additional details.
8. The address bus A15-A0 is internally buffered transparently until the first rising edge of CLK after $\overline{\text{IOEN}}$ goes low. After this CLK edge, A15-A0 become latched internally.
9. Setup time given for use in worst case timing calculations. None of the Mark3's input signals are required to be synchronized to the system clock. When $\overline{\text{SELECT}}$ and $\overline{\text{STRBD}}$ do not meet the setup time of t1, but occur during the setup window of an internal flip-flop, an additional clock cycle will be inserted between the falling clock edge that latches MEM/$\overline{\text{REG}}$ and RD/$\overline{\text{WR}}$ and the rising clock edge that latches the Address (A15-A0). When this occurs, the delay from $\overline{\text{IOEN}}$ falling to $\overline{\text{READYD}}$ falling (t11) increases by one clock cycle and the address hold time (t10) must be increased by one clock cycle.

FIGURE 13. CPU READING RAM / REGISTER (16-BIT BUFFERED, NONZERO WAIT)

TABLE FOR FIGURE 13. CPU READING RAM OR REGISTERS (SHOWN FOR 16-BIT, BUFFERED, NONZERO WAIT MODE)										
REF	DESCRIPTION	NOTES	5V LOGIC			3.3V LOGIC			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
t1	$\overline{\text{SELECT}}$ and $\overline{\text{STRBD}}$ low setup time prior to clock rising edge	2, 9	10			15			ns
t2	$\overline{\text{SELECT}}$ and $\overline{\text{STRBD}}$ low to $\overline{\text{IOEN}}$ low (uncontended access @ 20 MHz)	2, 6			100			105	ns
	(contended access, with ENHANCED CPU ACCESS = "0" @ 20 MHz)	2, 6			3.6			3.6	µs
	(contended access, with ENHANCED CPU ACCESS = "1" @ 20 MHz)	2, 6			515			520	ns
	(uncontended access @ 16 MHz)	2, 6			112			117	ns
	(contended access, with ENHANCED CPU ACCESS = "0" @ 16 MHz)	2, 6			4.6			4.6	µs
	(contended access, with ENHANCED CPU ACCESS = "1" s @ 16 MHz)	2, 6			630			635	ns
	(uncontended access @ 12 MHz)	2, 6			133			138	ns
	(contended access, with ENHANCED CPU ACCESS = "0" @ 12 MHz)	2, 6			6.0			6.0	µs
	(contended access, with ENHANCED CPU ACCESS = "1" @ 12 MHz)	2, 6			815			820	ns
	(uncontended access @ 10 MHz)	2, 6			150			155	ns
	(contended access, with ENHANCED CPU ACCESS = "0" @ 10 MHz)	2, 6			7.2			7.2	µs
	(contended access, with ENHANCED CPU ACCESS = "1" @ 10 MHz)	2, 6			965			970	ns
t3	Time for MEM/$\overline{\text{REG}}$ and RD/$\overline{\text{WR}}$ to become valid following $\overline{\text{SELECT}}$ and $\overline{\text{STRBD}}$ low (@ 20 MHz)	3, 4, 5, 7			15			10	ns
	@ 16 MHz	3, 4, 5, 7			21			16	ns
	@ 12 MHz	3, 4, 5, 7			32			27	ns
	@ 10 MHz	3, 4, 5, 7			40			35	ns
t4	Time for Address to become valid following SELECT and STRBD low (@ 20MHz)				17			12	ns
	@ 16 MHz				30			25	ns
	@ 12 MHz				50			45	ns
	@ 10 MHz				67			62	ns
t5	CLOCK IN rising edge delay to $\overline{\text{IOEN}}$ falling edge	6			40			40	ns
t6	$\overline{\text{SELECT}}$ hold time following $\overline{\text{IOEN}}$ falling	2	0			0			ns
t7	MEM/$\overline{\text{REG}}$, RD/$\overline{\text{WR}}$ setup time prior to CLOCK IN falling edge	3, 4, 5, 7	10			15			ns
t8	MEM/$\overline{\text{REG}}$, RD/$\overline{\text{WR}}$ hold time following CLOCK IN falling edge	3, 4, 5, 7	30			30			ns
t9	Address valid setup time prior to CLOCK IN rising edge	7, 8	30			35			ns
t10	Address hold time following CLOCK IN rising edge	7, 8, 9	30			30			ns
t11	$\overline{\text{IOEN}}$ falling delay to $\overline{\text{READYD}}$ falling (@ 20 MHz)	6, 9	135	150	165	135	150	165	ns
	@ 16 MHz	6, 9	170	187.5	205	170	187.5	205	ns
	@ 12 MHz	6, 9	235	250	265	235	250	265	ns
	@ 10 MHz	6, 9	285	300	315	285	300	315	ns
t12	Output Data valid prior to $\overline{\text{READYD}}$ falling (@ 20 MHz)	6	21			11			ns
	@ 16 MHz	6	33			23			ns
	@ 12 MHz	6	54			44			ns
	@ 10 MHz	6	71			61			ns
t13	CLOCK IN rising edge delay to $\overline{\text{READYD}}$ falling	6			40			40	ns
t14	$\overline{\text{READYD}}$ falling to $\overline{\text{STRBD}}$ rising release time				∞			∞	ns
t15	$\overline{\text{STRBD}}$ rising edge delay to $\overline{\text{IOEN}}$ rising edge and $\overline{\text{READYD}}$ rising edge	6			30			40	ns
t16	Output Data hold time following $\overline{\text{STRBD}}$ rising edge		0			0			ns
t17	$\overline{\text{STRBD}}$ rising delay to output data tri-state				40			40	ns
t18	$\overline{\text{STRBD}}$ high hold time from $\overline{\text{READYD}}$ rising		0			0			ns
t19	CLOCK IN rising edge delay to output data valid				40			40	ns



NOTES:

1. For the 16-bit buffered nonzero wait configuration TRANSPARENT/$\overline{\text{BUFFERED}}$ must be connected to logic "0", $\overline{\text{ZERO\_WAIT}}$ and $\overline{\text{DTREG}}$ / 16/$\overline{8}$ must be connected to logic "1". The inputs TRIGGER_SEL and MSB/LSB may be connected to either Vcc or ground.
2. $\overline{\text{SELECT}}$ and $\overline{\text{STRBD}}$ may be tied together. IOEN goes low on the first rising CLK edge when $\overline{\text{SELECT}}$ • $\overline{\text{STRBD}}$ is sampled low (satisfying t1) and the Mark3's protocol/memory management logic is not accessing the internal RAM. When this occurs, $\overline{\text{IOEN}}$ goes low, starting the transfer cycle. After $\overline{\text{IOEN}}$ goes low, $\overline{\text{SELECT}}$ may be released high.
3. MEM/$\overline{\text{REG}}$ must be presented high for memory access, low for register access.
4. MEM/$\overline{\text{REG}}$ and RD/$\overline{\text{WR}}$ are buffered transparently until the first falling edge of CLK after $\overline{\text{IOEN}}$ goes low. After this CLK edge, MEM/$\overline{\text{REG}}$ and RD/$\overline{\text{WR}}$ become latched internally.
5. The logic sense for RD/WR in the diagram assumes that POLARITY_SEL is connected to logic "1". If POLARITY_SEL is connected to logic "0", RD/$\overline{\text{WR}}$ must be asserted high to write.
6. The timing for the $\overline{\text{IOEN}}$ and $\overline{\text{READYD}}$ outputs assume a 50 pf load. For loading above 50 pf, the validity of $\overline{\text{IOEN}}$ and $\overline{\text{READYD}}$ is delayed by an additional 0.14 ns/pf typ, 0.28 ns/pf max.
7. The timing for A15-A0, MEM/$\overline{\text{REG}}$, and $\overline{\text{SELECT}}$ assumes that ADDR-LAT is connected to logic "1". Refer to Address Latch timing for additional details.
8. The address bus A15-A0 and data bus D15-D0 are internally buffered transparently until the first rising edge of CLK after $\overline{\text{IOEN}}$ goes low. After this CLK edge, A15-A0 and D15-D0 become latched internally.
9. Setup time given for use in worst case timing calculations. None of the Mark3's input signals are required to be synchronized to the system clock. When $\overline{\text{SELECT}}$ and $\overline{\text{STRBD}}$ do not meet the setup time of t1, but occur during the setup time of an internal flip-flop, an additional clock cycle may be inserted between the falling clock edge that latches MEM/$\overline{\text{REG}}$ and RD/$\overline{\text{WR}}$ and the rising clock edge that latches the address (A15-A0) and data (D15-D0). When this occurs, the delay from $\overline{\text{IOEN}}$ falling to $\overline{\text{READYD}}$ falling (t14) increases by one clock cycle and the address and data hold time (t12 and t13) must be increased by one clock.

FIGURE 14. CPU WRITING RAM / REGISTER (16-BIT BUFFERED, NONZERO WAIT)

TABLE FOR FIGURE 14. CPU WRITING RAM OR REGISTERS (SHOWN FOR 16-BIT, BUFFERED, NONZERO WAIT MODE)										
REF	DESCRIPTION	NOTES	5V LOGIC			3.3V LOGIC			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
t1	$\overline{\text{SELECT}}$ and $\overline{\text{STRBD}}$ low setup time prior to clock rising edge	2, 10	10			15			ns
t2	$\overline{\text{SELECT}}$ and $\overline{\text{STRBD}}$ low to IOEN low (uncontended access @ 20 MHz)	2, 6			100			105	ns
	(contended access, with ENHANCED CPU ACCESS = "0" @ 20 MHz)	2, 6			3.6			3.6	µs
	(contended access, with ENHANCED CPU ACCESS = "1" @ 20 MHz)	2, 6			465			470	ns
	(uncontended access @ 16 MHz)	2, 6			112			117	ns
	(contended access, with ENHANCED CPU ACCESS = "0" @ 16 MHz)	2, 6			4.6			4.6	µs
	(contended access, with ENHANCED CPU ACCESS = "1" @ 16 MHz)	2, 6			565			570	ns
	(uncontended access @ 12 MHz)	2, 6			133			138	ns
	(contended access, with ENHANCED CPU ACCESS = "0" @ 12 MHz)	2, 6			6.0			6.0	µs
	(contended access, with ENHANCED CPU ACCESS = "1" @ 12 MHz)	2, 6			732			737	ns
	(uncontended access @ 10 MHz)	2, 6			150			155	ns
	(contended access, with ENHANCED CPU ACCESS = "0" @ 10 MHz)	2, 6			7.2			7.2	µs
	(contended access, with ENHANCED CPU ACCESS = "1" @ 10 MHz)	2, 6			865			870	ns
t3	Time for MEM/$\overline{\text{REG}}$ and RD/$\overline{\text{WR}}$ to become valid following $\overline{\text{SELECT}}$ and $\overline{\text{STRBD}}$ low (@ 20 MHz)	3, 4, 5, 7			15			10	ns
	@ 16 MHz	3, 4, 5, 7			21			16	ns
	@ 12 MHz	3, 4, 5, 7			32			27	ns
	@ 10 MHz	3, 4, 5, 7			40			35	ns
t4	Time for Address to become valid following $\overline{\text{SELECT}}$ and $\overline{\text{STRBD}}$ low (@ 20MHz)				17			12	ns
	@ 16 MHz				30			25	ns
	@ 12 MHz				50			45	ns
	@ 10 MHz				67			62	ns
t5	Time for data to become valid following $\overline{\text{SELECT}}$ and $\overline{\text{STRBD}}$ low (@ 20 MHz)				37			32	ns
	@ 16 MHz				50			45	ns
	@ 12 MHz				70			65	ns
	@ 10 MHz				87			82	ns
t6	CLOCK IN rising edge delay to $\overline{\text{IOEN}}$ falling edge	6			40			40	ns
t7	SELECT hold time following $\overline{\text{IOEN}}$ falling	2	0			0			ns
t8	MEM/$\overline{\text{REG}}$, RD/$\overline{\text{WR}}$ setup time prior to CLOCK IN falling edge	3, 4, 5, 7	10			15			ns
t9	MEM/$\overline{\text{REG}}$, RD/$\overline{\text{WR}}$ setup time following CLOCK IN falling edge	3, 4, 5, 7	30			35			ns
t10	Address valid setup time prior to CLOCK IN rising edge	7, 8	30			35			ns
t11	Data valid setup time prior to CLOCK IN rising edge		10			15			ns
t12	Address valid hold time following CLOCK IN rising edge	7, 8, 9	30			30			ns
t13	Data valid hold time following CLOCK IN rising edge	9	10			15			ns
t14	$\overline{\text{IOEN}}$ falling delay to $\overline{\text{READYD}}$ falling @ 20 MHz	6, 9	85	100	115	85	100	115	ns
	@ 16 MHz	6, 9	110	125	140	110	125	140	ns
	@ 12 MHz	6, 9	152	167	182	152	167	182	ns
	@ 10 MHz	6, 9	185	200	215	185	200	215	ns
t15	CLOCK IN rising edge delay to $\overline{\text{READYD}}$ falling	6			40			40	ns
t16	$\overline{\text{READYD}}$ falling to $\overline{\text{STRBD}}$ rising release time				∞			∞	ns
t17	$\overline{\text{STRBD}}$ rising delay to $\overline{\text{IOEN}}$ rising edge and $\overline{\text{READYD}}$ rising edge	6			30			40	ns
t18	$\overline{\text{STRBD}}$ high hold time from . rising		10			10			ns

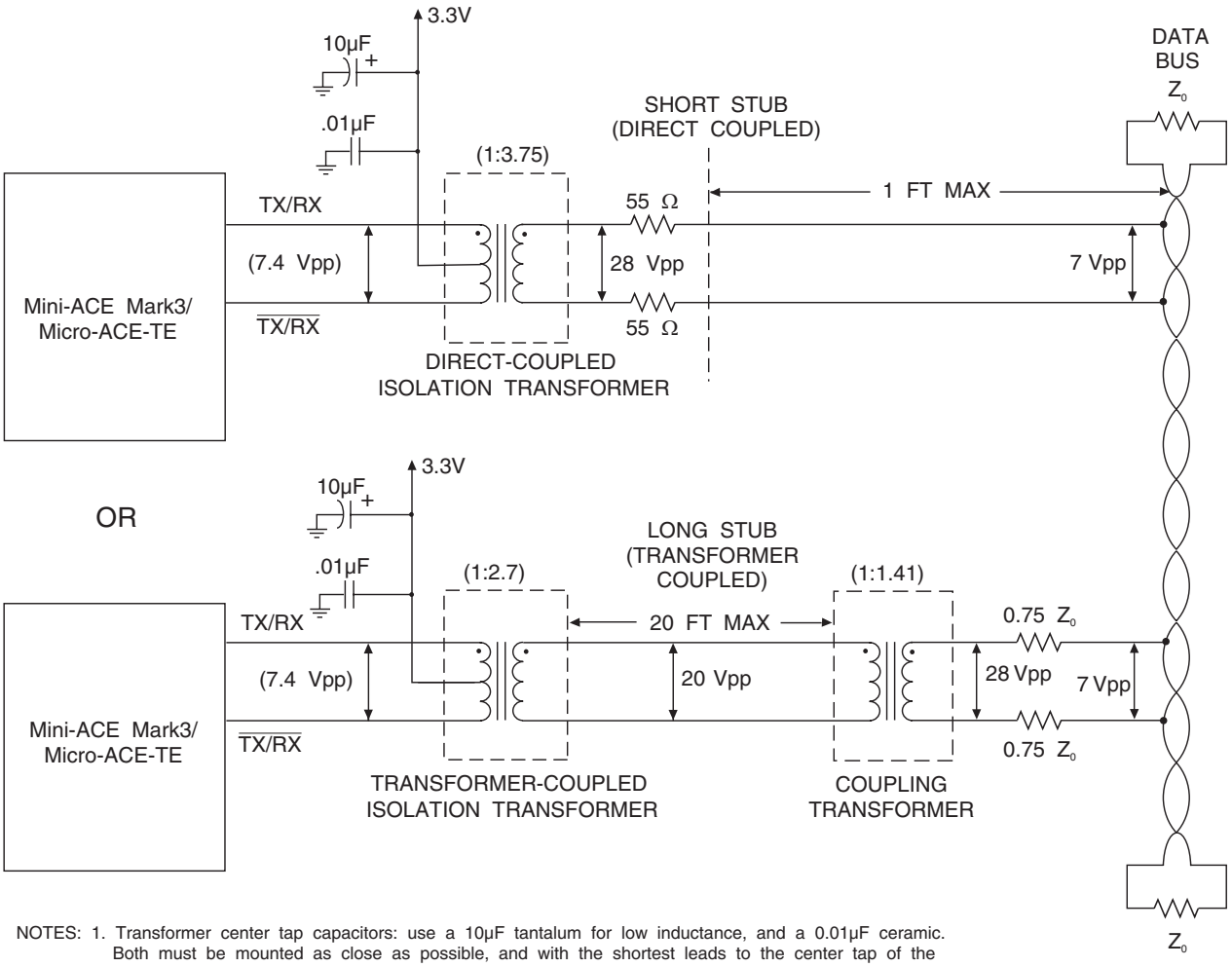
+3.3 VOLT INTERFACE TO MIL-STD-1553 BUS (BU-64XXXX8/9)

The Mini-ACE Mark3 is the world's first MIL-STD-1553 terminal powered entirely by 3.3 volts. Unique isolation transformer turns ratios, single output winding transformers and new interconnection methods are required in order to meet mandated MIL-STD-1553 differential voltage levels.

FIGURE 15 illustrates the two possible interface methods between the Mini-ACE Mark3 series and a MIL-STD-1553 bus. Connections for both direct (short stub, 1:3.75) and transformer (long stub, 1:2.7) coupling, as well as nominal peak-to-peak voltage levels at various points (when transmitting), are indicated in the diagram.

The center tap of the primary winding (the side of the transformer that connects to the Mark3) must be directly connected to the +3.3 volt plane. Additionally, a 10µf, low inductance tantalum capacitor and a 0.01µf ceramic capacitor must be mounted as close as possible and with the shortest leads to the center tap of the transformer(s) and ground plane.

Additionally, during transmission large currents flow from the transformer center tap, through the primaries and the TX/RX pins, and then out the transceiver grounds (pins 22 and 79) into the ground plane. The traces in this path should be sized accordingly and the connections to the ground plane should be as short as possible.



NOTES: 1. Transformer center tap capacitors: use a 10µF tantalum for low inductance, and a 0.01µF ceramic. Both must be mounted as close as possible, and with the shortest leads to the center tap of the transformer(s) and ground.
2. Connect the Mark3 hybrid grounds as directly as possible to the 3.3V ground plane.
3. Zo = 70 to 85 Ohms.

FIGURE 15. BU-64XXXX8/9 (+3.3 VOLT) INTERFACE TO MIL-STD-1553 BUS

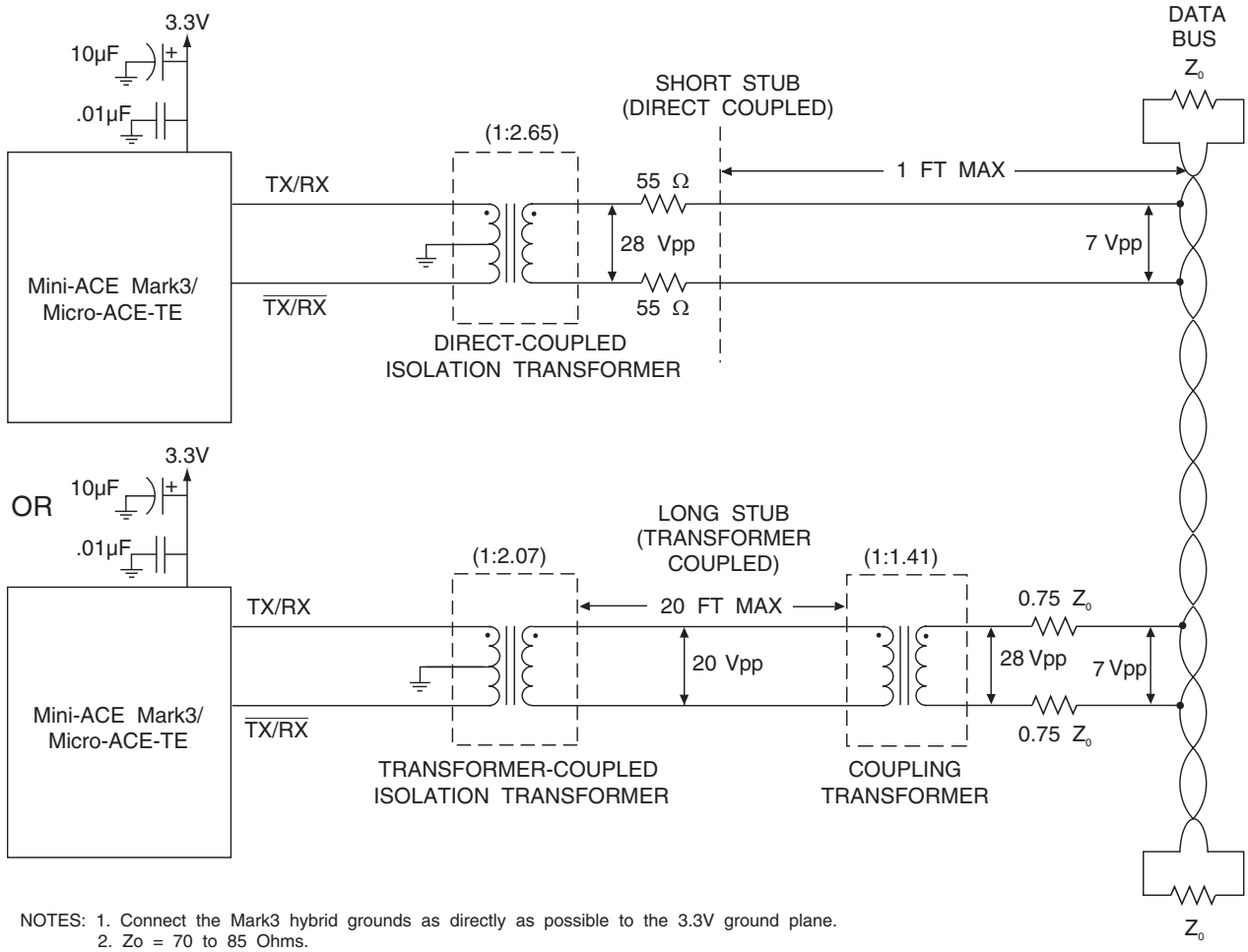
+3.3 VOLT INTERFACE TO MIL-STD-1553 BUS (BU-64XXXXC/D)

FIGURE 16 illustrates the two possible interface methods between the Mini-ACE Mark3 series and a MIL-STD-1553 bus. Connections for both direct (short stub, 1:2.65) and transformer (long stub, 1:2.07) coupling, as well as nominal peak-to-peak voltage levels at various points (when transmitting), are indicated in the diagram.

The center tap of the primary winding (the side of the transformer that connects to the Mark3) must be directly connected to ground.

Additionally, during transmission, large currents flow from the transceiver power supply through the TX/RX pins into the transformer primaries and then out the center tap into the ground plane. The traces in this path should be sized accordingly and the connections to the ground plane should be as short as possible.

A 10µf, low inductance tantalum capacitor and a 0.01µf ceramic capacitor must be mounted as close as possible and with the shortest leads to the transceiver power input of the Mini-ACE Mark 3.



NOTES: 1. Connect the Mark3 hybrid grounds as directly as possible to the 3.3V ground plane.
2. Zo = 70 to 85 Ohms.

FIGURE 16. BU-64XXXXC/D (+3.3 VOLT) INTERFACE TO MIL-STD-1553 BUS

+3.3 VOLT ISOLATION TRANSFORMERS

In selecting isolation transformers to be used with the Mini-ACE Mark3, there is a limitation on the maximum amount of leakage inductance. If this limit is exceeded, the transmitter rise and fall times may increase, possibly causing the bus amplitude to fall below the minimum level required by MIL-STD-1553.

In addition, an excessive leakage imbalance may result in a transformer dynamic offset that exceeds 1553 specifications. The maximum allowable leakage inductance is a function of the coupling method. For Transformer Coupled applications, it is a maximum of 5.0 µH . For Direct it is a maximum of 10.0 µH, and is measured as follows:

The side of the transformer that connects to the Mark3 is defined as the "primary" winding. If one side of the primary is shorted to the primary center-tap, the inductance should be measured across the "secondary" (stub side) winding. This inductance must be less than 5.0 µH (Transformer Coupled) and 10.0 µH (Direct Coupled). Similarly, if the other side of the primary is shorted to the primary center-tap, the inductance measured across the "secondary" (stub side) winding must also be less than 5.0 µH (Transformer Coupled) and 10.0 µH (Direct Coupled).

The difference between these two measurements is the "differential" leakage inductance. This value must be less than 1.0 µH (Transformer Coupled) and 2.0 µH (Direct Coupled).

Beta Transformer Technology Corporation (BTTC), a subsidiary of DDC, manufactures transformers in a variety of mechanical configurations with the required turns ratios of 1:3.75 direct coupled, and 1:2.7 transformer coupled for BU-6XXXXX8/9 Models and the required turns ratios of 1:2.65 direct coupled, and 1:2.07 transformer coupled for BU-6XXXXXC/D Models. TABLE 46 provides a listing of these transformers with the corresponding model numbers.

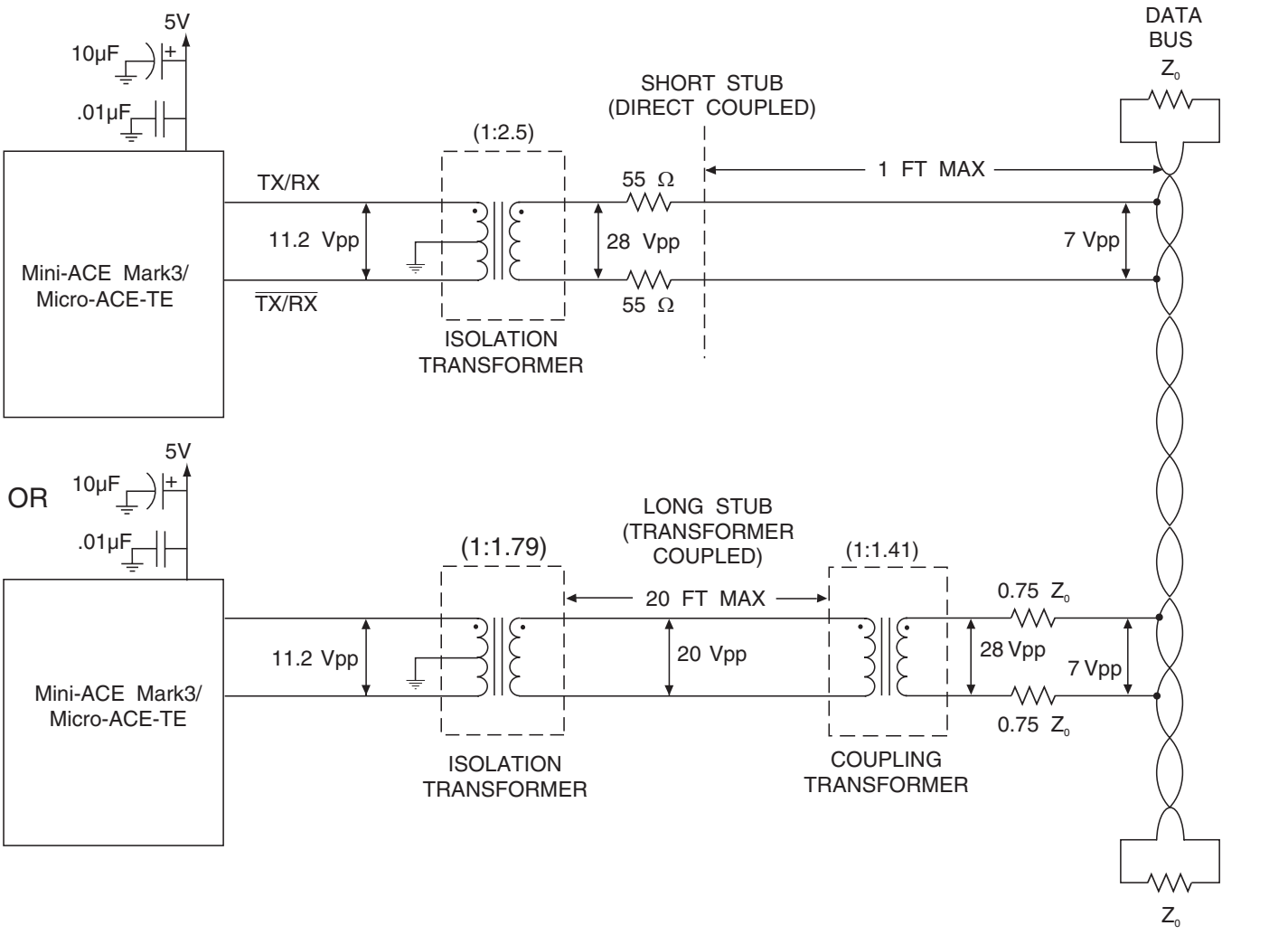
For further information, contact BTTC at 631-244-7393 or at www.bttc-beta.com.

TABLE 46. BTTC TRANSFORMERS FOR USE WITH +3.3 VOLT Mini-ACE Mark3

MODEL NUMBER	BTTC PART NUMBER	# OF CHANNELS, CONFIGURATION	COUPLING RATIO DESCRIPTION	COUPLING RATIO (1:X)	MOUNTING	MAX HEIGHT	WIDTH (INCLUDING LEADS)	LENGTH (INCLUDING LEADS)
BU-6XXXXX8/9	MLP-2033	Single	Direct	(1:3.75)	SMT	0.185"	0.4"	0.52"
BU-6XXXXXC/D	MLP-2030	Single	Direct	(1:2.65)	SMT	0.185"	0.4"	0.52"
BU-6XXXXX8/9	MLP-3033	Single	Direct	(1:3.75)	Through Hole	0.185"	0.4"	0.4"
BU-6XXXXX8/9	MLP-2233	Single	Transformer	(1:2.7)	SMT	0.185"	0.4"	0.52"
BU-6XXXXXC/D	MLP-2230	Single	Transformer	(1:2.07)	SMT	0.185"	0.4"	0.52"
BU-6XXXXX8/9	MLP-3233	Single	Transformer	(1:2.7)	Through Hole	0.185"	0.4"	0.4"
BU-6XXXXX8/9	MLP-3333	Single	Direct & Transformer	(1:3.75) & (1:2.7)	Through Hole	0.185"	0.4"	0.4"
BU-6XXXXXC/D	LVB-4230	Single	Transformer	(1:2.07)	Through Hole	0.165"	1.125"	0.625"
BU-6XXXXXC/D	DSS-3330	Dual (Side-by-Side)	Direct & Transformer	(1:2.65) & (1:2.07)	SMT	0.185"	0.52"	0.675"
BU-6XXXXX8/9	DSS-2033	Dual (Side-by-Side)	Direct	(1:3.75)	SMT	0.13"	0.72"	0.96"
BU-6XXXXX8/9	DSS-2233	Dual (Side-by-Side)	Transformer	(1:2.7)	SMT	0.13"	0.72"	0.96"
BU-6XXXXX8/9	DSS-1003	Dual (Side-by-Side)	Direct & Transformer	(1:3.75) & (1:2.7)	SMT	0.165"	0.72"	0.96"
BU-6XXXXXC/D	DSS-1630	Dual (Side-by-Side)	Direct & Transformer	(1:2.65) & (1:2.07)	SMT	0.165"	0.72"	0.96"
BU-6XXXXXC/D	DLVB-4230	Dual (Stacked)	Transformer	(1:2.07)	SMT	0.165"	0.72"	0.96"
BU-6XXXXX8/9	TSM-2033	Dual (Stacked)	Direct	(1:3.75)	SMT	0.32"	0.4"	0.52"
BU-6XXXXX8/9	TSM-2233	Dual (Stacked)	Transformer	(1:2.7)	SMT	0.32"	0.4"	0.52"
BU-6XXXXXC/D	TSM-2230	Dual (Stacked)	Transformer	(1:2.07)	SMT	0.32"	0.4"	0.52"
	LPB-5030	Single	Direct & Transformer	(1:1) & (1:0.707)	SMT	0.155"	1.11"	0.625"

+5.0 VOLT INTERFACE TO MIL-STD-1553 BUS

FIGURE 17 illustrates the interface between the +5.0 volt versions of the Mini-ACE Mark3 series and a MIL-STD-1553 bus. Connections for both direct (short stub) and transformer (long stub) coupling, as well as the nominal peak-to-peak voltage levels at various points (when transmitting), are indicated in the diagram.



NOTES: 1. Z_0 = 70 TO 85 OHMS
2. NOMINAL VOLTAGE LEVELS SHOWN

FIGURE 17. MINI-ACE MARK3 / MICRO-ACE-TE (+5.0 VOLT) INTERFACE TO MIL-STD-1553 BUS

+5.0 VOLT ISOLATION TRANSFORMERS

In selecting isolation transformers to be used with the Mini-ACE Mark3 / Micro-ACE-TE, there is a limitation on the maximum amount of leakage inductance. If this limit is exceeded, the transmitter rise and fall times may increase, possibly causing the bus amplitude to fall below the minimum level required by MIL-STD-1553. In addition, an excessive leakage imbalance may result in a transformer dynamic offset that exceeds 1553 specifications.

The maximum allowable leakage inductance is 6.0 µH, and is measured as follows:

The side of the transformer that connects to the Mini-ACE Mark3 / Micro-ACE-TE is defined as the "primary" winding. If one side of the primary is shorted to the primary center-tap, the inductance should be measured across the "secondary" (stub side) winding. This inductance must be less than 6.0 µH. Similarly, if the other side of the primary is shorted to the primary center-tap, the inductance measured across the "secondary" (stub side) winding must also be less than 6.0 µH.

The difference between these two measurements is the "differential" leakage inductance. This value must be less than 1.0 µH.

Beta Transformer Technology Corporation (BTTC), a subsidiary of DDC, manufactures transformers in a variety of mechanical configurations with the required turns ratios of 1:2.5 direct coupled, and 1:1.79 transformer coupled. TABLE 47 provides a listing of many of these transformers.

For further information, contact BTTC at 631-244-7393 or at www.bttc-beta.com.

TABLE 47. BTTC TRANSFORMERS FOR USE WITH 5.0 VOLT Mini-ACE Mark3 / MICRO-ACE-TE

BTTC PART NUMBER	# OF CHANNELS, CONFIGURATION	COUPLING RATIO DESCRIPTION	COUPLING RATIO (1:X)	MOUNTING	MAX HEIGHT	WIDTH (INCLUDING LEADS)	LENGTH (INCLUDING LEADS)
MLP-2005	Single	Direct	(1:2.5)	SMT	0.185"	0.4"	0.52"
MLP-3005	Single	Direct	(1:2.5)	Through Hole	0.185"	0.4"	0.4"
B-3230 (-30) #	Single	Direct	(1:2.5)	Through Hole	0.25"	0.35"	0.5"
MLP-2205	Single	Transformer	(1:1.79)	SMT	0.185"	0.4"	0.52"
MLP-3205	Single	Transformer	(1:1.79)	Through Hole	0.185"	0.4"	0.4"
B-3229 (-29) #	Single	Transformer	(1:1.79)	Through Hole	0.25"	0.35"	0.5"
HLP-6015 #	Single	Direct & Transformer	(1:2.5) & (1:1.79)	SMT	0.19"	0.63"	1.13"
B-3227 (-27) #	Single	Direct & Transformer	(1:2.5) & (1:1.79)	SMT	0.29"	0.63"	1.13"
MLP-3305	Single	Direct & Transformer	(1:2.5) & (1:1.79)	Through Hole	0.185"	0.4"	0.4"
B-3226 (-26) #	Single	Direct & Transformer	(1:2.5) & (1:1.79)	Through Hole	0.25"	0.625"	0.625"
HLP-6014 #	Single	Direct & Transformer	(1:2.5) & (1:1.79)	Flat Pack	0.19"	0.63"	1.13"
B-3231 (-31) #	Single	Direct & Transformer	(1:2.5) & (1:1.79)	Flat Pack	0.29"	0.63"	1.13"
DSS-2005	Dual (Side-by-Side)	Direct	(1:2.5)	SMT	0.13"	0.72"	0.96"
DSS-2205	Dual (Side-by-Side)	Transformer	(1:1.79)	SMT	0.13"	0.72"	0.96"
DSS-1005	Dual (Side-by-Side)	Direct & Transformer	(1:2.5) & (1:1.79)	SMT	0.165"	0.72"	0.96"
TSM-2005	Dual (Stacked)	Direct	(1:2.5)	SMT	0.32"	0.4"	0.52"
TSM-2205	Dual (Stacked)	Transformer	(1:1.79)	SMT	0.32"	0.4"	0.52"
TST-9117 #	Dual (Stacked)	Direct & Transformer	(1:2.5) & (1:1.79)	SMT	0.335"	1.125"	1.125"
TST-9107 #	Dual (Stacked)	Direct & Transformer	(1:2.5) & (1:1.79)	Through Hole	0.335"	0.625"	0.625"
TST-9127 #	Dual (Stacked)	Direct & Transformer	(1:2.5) & (1:1.79)	Flat Pack	0.335"	0.625"	0.625"

Notes:
1. All Transformers in the table above can be used with BU-6XXXXX3/6 (1553B transceivers).
2. Transformers identified with "#" in the table above are not recommended for use with the BU-6XXXXX4 (McAir-Compatable transceivers)

THERMAL MANAGEMENT FOR MICRO-ACE-TE (324-BALL BGA PACKAGE)

Ball Grid Array (BGA) components necessitate that thermal management issues be considered early in the design stage for MIL-STD-1553 terminals. This is especially true if high transmitter duty cycles are expected. The temperature range specified for DDC's Micro-ACE-TE device refers to the case temperature. Any duty cycle is acceptable as long as the case temperature is maintained within the extended industrial temperature range specified for the -Exx parts. See below for an explanation of the thermal management requirements for high transmitter duty cycles with the military temperature range components.

All Micro-ACE-TE devices incorporate multiple package connections which perform the dual function of transceiver circuit ground and thermal heat sink. Refer to the pinout tables for thermal ball connection locations. It is mandatory that these thermal balls be directly soldered to a circuit ground/thermal plane (a circuit trace is insufficient). Operation without an adequate ground/thermal plane is not recommended and extended exposure to these conditions may affect device reliability.

The purpose of this ground/thermal plane is to conduct the heat being generated by the transceivers within the package and conduct this heat away from the Micro-ACE-TE. In general, the circuit ground and thermal (chassis) ground are not the same ground plane. It is acceptable for these balls to be directly soldered to a ground plane but it must be located in close physical and thermal proximity ("0.003" pre-preg layer recommended) to the thermal plane.

The temperature of each chip within the Micor-Ace-TE must be maintained below its respective maximum operating junction temperature as specified in Table 1. The simplest method to ensure this is to attribute all internal power dissipation to the transceiver, use the θ_{JX} numbers also specified in Table 1 to calculate the temperature rise at the transceiver, and ensure that the temperature at the transceiver never exceeds the lowest maximum operating junction temperature allowed for any internal component (135°C for the protocol chip).

The general equation for the heat rise from ambient to the source of heat inside a component (typically the transistor junctions) is $\Delta T=P^*\theta$, where P is the power dissipation of the component and q is the thermal impedance from the junctions to ambient. Here there are two heat paths to the ambient, up through the top of the case, and down through the PCB, so we have a pair of equations:

$$\Delta T = P_C*(\theta_{JC}+\theta_{CA}) = P_B*(\theta_{JB}+\theta_{BA}) \text{ and } P = P_C+P_B.$$

Where P_C is the portion of the component power which flows through the top of the case to the ambient, θ_{JC} is the thermal impedance of the component from the junctions to the top of the case, and θ_{CA} is the thermal impedance of the system from the top of the case to ambient. Similarly, P_B is the portion of the component power which flows through the bottom of the case into the P_{CB}, θ_{JB} is the thermal impedance of the component from the transistor junctions to the board, and θ_{BA} is the thermal impedance of the system from the board under the component to ambient.

For the case of a BU-64843BC-102 used as a monitor terminal, P=0.19W and θ_{JB}=31.3°C/W. This can be simplified by assuming that no heat flows out through the top of the case and only measuring the rise above package temperature without considering the whole path to ambient (ignoring θ_{BA}). The equation thus simplifies to:

$$\Delta T = P*(\theta_{JB}) = 0.19*(31.3+0) = 5.9°C$$

With a package temperature of 125°, this leaves the junction temperature below the maximum of 135°C.

The transmit duty cycle of a remote terminal is typically under 25%, with a few exceptions for high bandwidth devices like data loaders. Substituting the 25% duty cycle power (P=0.33W) into the equation above leads to a temperature rise of 10.329°C, which is just beyond the acceptable limit for a board temp of 125°C, so board temp would have to be limited to 124°C, or duty cycle would need to be limited below 25%.

For a bus controller, higher duty cycles are common, so it may be necessary to add some form of heat sink to remove heat from the top of the component as well. For a BU-64863BC-102 with a duty cycle of 100%, P=0.67W. If the cooling paths from the top and bottom of the case to the ambient are assumed to be equally effective, ignoring θ_{CA} and θ_{BA} and setting the temperatures at both the top and bottom of the component to be the same, then the equations become:

$$\Delta T = P_C*(20.8) = P_B*(31.3)$$

And:

$$0.67 = P_C+P_B$$

Which turns into:

$$P_C = 0.67-P_B$$

Substituting for P_C and θ_{JX} in the equation for ΔT, we get:

$$\Delta T = (0.67-P_B)*(20.8) = P_B*(31.3)$$

$$13.936-20.8 *P_B = 31.3*P_B$$

$$13.936 = 52.1*P_B$$

$$P_B = 0.267$$

Substituting this result back into the ΔT equation, we get:

$$\Delta T = 0.2999*26.5 = 8.4°C$$

So as long as both the top and bottom of the case are maintained below 125°C, using heat sinks if necessary, the junction temperatures will remain within the acceptable limits.

For applications where high duty cycle operation is required at high ambient temperature, DDC also provides a thermal model that can be used with the FloTherm modeling tool from Mentor Graphics to assign power dissipation numbers to each internal component and determine the resulting operating junction temperature of each, allowing the assurance of proper operation without requiring excessively conservative estimates that can hurt performance and increase costs.

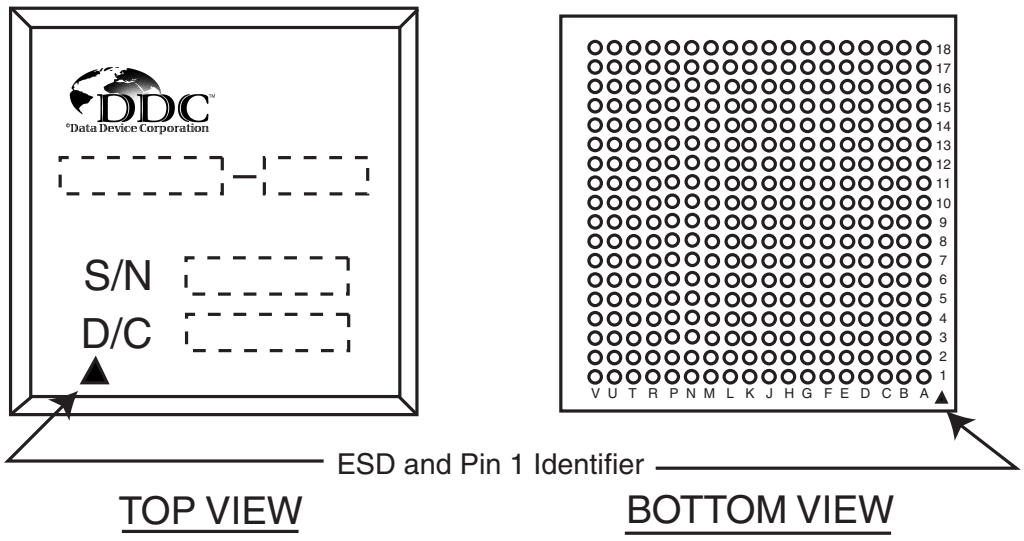


FIGURE 18. BALL LOCATIONS FOR MICRO-ACE-TE (324-BALL BGA PACKAGE)

FLAT PACK AND GULL WING PACKAGES - SIGNAL DESCRIPTIONS BY FUNCTIONAL GROUPS

TABLE 48. POWER AND GROUND

SIGNAL NAME	BU-64743F/G0 BU-64843F/G0 BU-64863F/G0	BU-64743F/G3/4 BU-64843F/G3/4 BU-64863F/G3/4	BU-64745F/G3/4 BU-64845F/G3/4	BU-64743F/G8/9/C/D BU-64843F/G8/9/C/D BU-64863F/G8/9/C/D	DESCRIPTION
	PIN	PIN	PIN	PIN	
+ 3.3V_Xcvr	-	-	-	10	+ 3.3 Volt Transceiver Power
+ 5.0V_Xcvr	-	10	10	-	+ 5.0 Volt Transceiver Power
+ 3.3V_Logic	10, 30, 51, 69	30, 51, 69	-	30, 51, 69	+3.3 Volt Logic Power
+ 5.0V_Logic	-	-	30, 51, 69	-	+5.0 Volt Logic Power
Gnd_Xcvr	-	22, 79	22, 79	22, 79	Transceiver Ground
Gnd_Logic	22, 79, 31, 50, 70	31, 50, 70	31, 50, 70	31, 50, 70	Logic Ground

NOTE: Logic ground and transceiver ground **are not** tied together inside the package.

TABLE 49. 1553 ISOLATION TRANSFORMER (BU-64XXXF/G3/4/8/9/C/D VERSIONS)

SIGNAL NAME	BU-6474XF/G3/4/8/9/C/D BU-6484XF/G3/4/8/9/C/D BU-64863F/G3/4/8/9/C/D	DESCRIPTION
	PIN	
TX/RX-A (I/O)	3	Analog Transmit/Receive Input/Outputs. Connect directly to 1553 isolation transformers.
$\overline{\text{TX/RX-A}}$ (I/O)	5	
TX/RX-B (I/O)	15	
$\overline{\text{TX/RX-B}}$ (I/O)	17	

TABLE 50. INTERFACE TO EXTERNAL TRANSCEIVER (BU-64XX3F/G0 TRANSCEIVERLESS VERSION)

SIGNAL NAME	BU-64743F/G0 BU-64843F/G0 BU-64863F/G0 PIN	DESCRIPTION
TXDATA_A (O)	3	Digital Manchester biphase transmit outputs, A bus
$\overline{\text{TXDATA\_A}}$ (O)	5	
RXDATA_A (I)	8	Digital Manchester biphase receive inputs, A bus
$\overline{\text{RXDATA\_A}}$ (I, not enabled)*	4	
TXINH_A_OUT (O)	11	Digital output to inhibit external transmitter, A bus
TXDATA_B (O)	15	Digital Manchester biphase transmit outputs, B bus
$\overline{\text{TXDATA\_B}}$ (O)	17	
RXDATA_B (I)	21	Digital Manchester biphase receive inputs, B bus
$\overline{\text{RXDATA\_B}}$ (I, not enabled)*	16	
TXINH_B_OUT (O)	9	Digital output to inhibit external transmitter, B bus
UPADDREN / NC	14	4K versions: UPADDREN / 64K versions: NC For 4K RAM versions, this signal is always configured as UPADDREN. This signal is used to control the function of the upper 4 address inputs (A15-A12). For these versions of Mark3 if UPADDREN is connected to logic "1", then these four signals operate as address lines A15-A12. If UPADDREN is connected to logic "0", then A15 and A14 function as CLK_SEL_1 and CLK_SEL_0 respectively; A13 MUST be connected to +3.3V-LOGIC; and A12 functions as $\overline{\text{RTBOOT}}$.

*NOTE: Standard transceiverless parts have their receiver inputs internally strapped for single-ended operation. The $\overline{\text{RXDATAx}}$ pins are connected to inputs that are not enabled. Contact the factory for a non-standard part that enables differential receive inputs.

TABLE 51. DATA BUS

SIGNAL NAME	BU-6474XF/GX BU-6484XF/GX BU-64863F/GX PIN	DESCRIPTION
D15 (MSB)	59	16-bit bi-directional data bus.This bus interfaces the host processor to the Mini-ACE Mark3's internal registers and internal RAM. In addition, in transparent mode, this bus allows data transfers to take place between the internal protocol/memory management logic and up to 64K x 16 of external RAM. Most of the time, the outputs for D15 through D0 are in the high impedance state. They drive outward in the buffered or transparent mode when the host CPU reads the internal RAM or registers. Also, in the transparent mode, D15-D0 will drive outward (towards the host) when the protocol/management logic is accessing (either reading or writing) internal RAM, or writing to external RAM. In the transparent mode, D15-D0 drives inward when the CPU writes internal registers or RAM, or when the protocol/memory management logic reads external RAM.
D14	56	
D13	54	
D12	55	
D11	58	
D10	60	
D9	57	
D8	52	
D7	53	
D6	41	
D5	49	
D4	43	
D3	48	
D2	47	
D1	42	
D0 (LSB)	46	

TABLE 52. PROCESSOR ADDRESS BUS

SIGNAL NAME		BU-6474XF/GX BU-6484XF/GX BU-64863F/GX	DESCRIPTION
64K RAM (BU-64863F/GX)	4K RAM (BU-6474XF/GX BU-6484XF/GX)	PIN	
A15 (MSB)	A15 / CLK_ SEL_1	73	16-bit bi-directional address bus. For 64K RAM versions, this signal is always configured as address line A15 (MSB). Refer to the description for A11-A0 below. For 4K RAM versions, if UPADDREN is connected to logic "1", this signal operates as address line A15. For 4K RAM versions, if UPADDREN is connected to logic "0", this signal operates as CLK_SEL_1. In this case, A15/CLK_SEL_1 and A14/CLK_SEL_0 are used to select the Mark3 clock frequency, as follows: CLK_SEL_1 — CLK_SEL_0 — Clock Frequency 0 — 0 — 10 MHz 0 — 1 — 20 MHz 1 — 0 — 12 MHz 1 — 1 — 16 MHz
A14	A14 / CLK_ SEL_0	80	For 64K RAM versions, this signal is always configured as address line A14. Refer to the description of A11-A0 below. For 4K RAM versions, if UPADDREN is connected to logic "1", this signal operates as A14. For 4K RAM versions, if UPADDREN is connected to logic "0", then this signal operates as CLK_SEL_0. In this case, CLK_SEL_1 and CLK_SEL_0 are used to select the Mark3 clock frequency, as defined in the description for A15/CLK_SEL1 above.
A13	A13 / +3.3V/+5.0V LOGIC	77	For 64K RAM versions, this signal is always configured as address line A13. Refer to the description for A11-A0 below. For 4K RAM versions, if UPADDREN is connected to logic "1", this signal operates as A13. For 4K RAM versions, if UPADDREN is connected to logic "0", then this signal MUST be connected to +3.3V-LOGIC (logic "1") for the BU-64XX3 or +5.0V (logic "1") for the BU-64XX5.
A12	A12 / $\overline{\text{RTBOOT}}$	76	For 64K RAM versions, this signal is always configured as address line A12. Refer to the description for A11-A0 below. For 4K RAM versions, if UPADDREN is connected to logic "1", this signal operates as A12. For 4K RAM versions, if UPADDREN is connected to logic "0", then this signal functions as $\overline{\text{RTBOOT}}$. If $\overline{\text{RTBOOT}}$ is connected to logic "0", the Mark3 will initialize in RT mode with the Busy status word bit set following power turn-on. If $\overline{\text{RTBOOT}}$ is hard-wired to logic "1", the Mark3 will initialize in either Idle mode (for an RT-only part), or in BC mode (for a BC/RT/MT part).

TABLE 52. PROCESSOR ADDRESS BUS (CONT.)

SIGNAL NAME	BU-6474XF/GX BU-6484XF/GX BU-64863F/GX PIN	DESCRIPTION
A11	1	Lower 12 bits of 16-bit bi-directional address bus. In both the buffered and transparent modes, the host CPU accesses Mark3 registers and internal RAM by means of A11 - A0 (4K versions). For 64K versions, A15-A12 are also used for this purpose. In buffered mode, A12-A0 (or A15-A0) are inputs only. In the transparent mode, A12-A0 (or A15-A0) are inputs during CPU accesses and become outputs, driving outward (towards the CPU) when the 1553 protocol/memory management logic accesses up to 64K words of external RAM. In transparent mode, the address bus is driven outward only when the signal $\overline{\text{DTACK}}$ is low (indicating that the Mark3 has control of the RAM interface bus) and $\overline{\text{IOEN}}$ is high, indicating a non-host access. Most of the time, including immediately after power turn-on, A12-A0 (or A15-A0) will be in high impedance (input) state.
A10	2	
A09	75	
A08	7	
A07	12	
A06	27	
A05	74	
A04	78	
A03	13	
A02	19	
A01	33	
A00 (LSB)	18	

TABLE 53. PROCESSOR INTERFACE CONTROL

SIGNAL NAME	BU-6474XF/GX BU-6484XF/GX BU-64863F/GX PIN	DESCRIPTION
$\overline{\text{SELECT}}$ (I)	66	Device Select. Generally connected to a CPU address decoder output to select the Mark3 for a transfer to/from either RAM or register.
$\overline{\text{STRBD}}$ (I)	68	Strobe Data. Used in conjunction with $\overline{\text{SELECT}}$ to initiate and control the data transfer cycle between the host processor and the Mark3. $\overline{\text{STRBD}}$ must be asserted low through the full duration of the transfer cycle.
RD / $\overline{\text{WR}}$ (I)	71	Read/Write. For host processor access, RD/$\overline{\text{WR}}$ selects between reading and writing. In the 16-bit buffered mode, if POL_SEL is logic "0", then RD/$\overline{\text{WR}}$ should be low (logic "0") for read accesses and high (logic "1") for write accesses. If POL_SEL is logic "1", or the interface is configured for a mode other than 16-bit buffered mode, then RD/$\overline{\text{WR}}$ is high (logic "1") for read accesses and low (logic "0") for write accesses.
ADDR_LAT(I) / $\overline{\text{MEMOE}}$ (O)	20	Memory Output Enable or Address Latch. In buffered mode, the ADDR_LAT input is used to configure the buffers for A15-A0, $\overline{\text{SELECT}}$, MEM/$\overline{\text{REG}}$, and MSB/LSB (for 8-bit mode only) in latched mode (when low) or transparent mode (when high). That is, the Mark3's internal transparent latches will track the values on A15-A0, $\overline{\text{SELECT}}$, MEM/$\overline{\text{REG}}$, and MSB/LSB when ADDR_LAT is high, and latch the values when ADDR_LAT goes low. In general, for interfacing to processors with a non-multiplexed address/data bus, ADDR_LAT should be hardwired to logic "1". For interfacing to processors with a multiplexed address/data bus, ADDR_LAT should be connected to a signal that indicates a valid address when ADDR_LAT is logic "1". In transparent mode, $\overline{\text{MEMOE}}$ output signal is used to enable data outputs for external RAM read cycles (normally connected to the $\overline{\text{OE}}$ input signal on external RAM chips).
$\overline{\text{ZEROWAIT}}$ (I) / $\overline{\text{MEMWR}}$ (O)	28	Memory Write or Zero Wait. In buffered mode, input signal ($\overline{\text{ZEROWAIT}}$) used to select between the zero wait mode ($\overline{\text{ZEROWAIT}}$ = "0") and the non-zero wait mode ($\overline{\text{ZEROWAIT}}$ = "1"). In transparent mode, active low output signal ($\overline{\text{MEMWR}}$) asserted low during memory write transfers to strobe data into external RAM (normally connected to the $\overline{\text{WR}}$ input signal on external RAM chips).
16 / $\overline{8}$ (I) / $\overline{\text{DTREQ}}$ (O)	29	Data Transfer Request or Data Bus Select. In buffered mode, input signal 16/$\overline{8}$ used to select between the 16 bit data transfer mode (16/$\overline{8}$= "1") and the 8-bit data transfer mode (16/$\overline{8}$ = "0"). In transparent mode (16-bit only), active low level output signal $\overline{\text{DTREQ}}$ used to request access to the processor/RAM interface bus (address and data buses).
MSB / LSB (I) / $\overline{\text{DTGRT}}$ (I)	72	Data Transfer Grant or Most Significant Byte/Least Significant Byte. In 8-bit buffered mode, input signal (MSB/LSB) used to indicate which byte is currently being transferred (MSB or LSB). The logic sense of MSB/LSB is controlled by the POL_SEL input. MSB/LSB is not used in the 16-bit buffered mode. In transparent mode, active low input signal ($\overline{\text{DTGRT}}$) asserted in response to the $\overline{\text{DTREQ}}$ output to indicate that control of the external processor/RAM bus has been transferred from the host processor to the Mark3.

TABLE 53. PROCESSOR INTERFACE CONTROL (CONT.)

SIGNAL NAME	BU-6474XF/GX BU-6484XF/GX BU-64863F/GX PIN	DESCRIPTION
POL_SEL (I) / $\overline{\text{DTACK}}$ (O)	35	Data Transfer Acknowledge or Polarity Select. In 16-bit buffered mode, if POL_SEL is connected to logic "1", RD/$\overline{\text{WR}}$ should be asserted high (logic "1") for a read operation and low (logic "0") for a write operation. In 16-bit buffered mode, if POL_SEL is connected to logic "0", RD/$\overline{\text{WR}}$ should be asserted low (logic "0") for a read operation and high (logic "1") for a write operation. In 8-bit buffered mode (TRANSPARENT/ BUFFERED = "0" and 16/8 = "0"), POL_SEL input signal used to control the logic sense of the MSB/$\overline{\text{LSB}}$ signal. If POL_SEL is connected to logic "0", MSB/$\overline{\text{LSB}}$ should be asserted low (logic "0") to indicate the transfer of the least significant byte and high (logic "1") to indicate the transfer of the most significant byte. If POL_SEL is connected to logic "1", MSB/$\overline{\text{LSB}}$ should be asserted high (logic "1") to indicate the transfer of the least significant byte and low (logic "0") to indicate the transfer of the most significant byte. In transparent mode, active low output signal ($\overline{\text{DTACK}}$) used to indicate acceptance of the processor/RAM interface bus in response to a data transfer grant ($\overline{\text{DTGRT}}$). Mark3 RAM transfers over A15-A0 and D15-D0 will be framed by the time that $\overline{\text{DTACK}}$ is asserted low.
TRIG_SEL (I) / $\overline{\text{MEMENA\_IN}}$ (I)	34	Memory Enable or Trigger Select input. In 8-bit buffered mode, input signal (TRIG-SEL) used to select the order in which byte pairs are transferred to or from the Mark3 by the host processor. In the 8-bit buffered mode, TRIG_SEL should be asserted high (logic 1) if the byte order for both read operations and write operations is MSB followed by LSB. TRIG_SEL should be asserted low (logic 0) if the byte order for both read operations and write operations is LSB followed by MSB. This signal has no operation in the 16-bit buffered mode (it does not need to be connected). In transparent mode, active low input $\overline{\text{MEMENA\_IN}}$, used as a Chip Select ($\overline{\text{CS}}$) input to the Mark3's internal shared RAM. If only internal RAM is used, should be connected directly to the output of a gate that is OR'ing the $\overline{\text{DTACK}}$ and $\overline{\text{IOEN}}$ output signals.
MEM / $\overline{\text{REG}}$(I)	6	Memory/Register. Generally connected to either a CPU address line or address decoder output. Selects between memory access (MEM/$\overline{\text{REG}}$ = "1") or register access (MEM/$\overline{\text{REG}}$ = "0").
$\overline{\text{SSFLAG}}$ (I) / EXT_TRIG(I)	37	Subsystem Flag (RT) or External Trigger (BC/Word Monitor) input. In RT mode, if this input is asserted low, the Subsystem Flag bit will be set in the Mark3's RT Status Word. If the $\overline{\text{SSFLAG}}$ input is logic "0" while bit 8 of Configuration Register #1 has been programmed to logic "1" (cleared), the Subsystem Flag RT Status Word bit will become logic "1," but bit 8 of Configuration Register #1, $\overline{\text{SUBSYSTEM FLAG}}$, will return logic "1" when read. That is, the sense on the $\overline{\text{SSFLAG}}$ input has no effect on the SUBSYSTEM FLAG register bit. In the non-enhanced BC mode, this signal operates as an External Trigger input. In BC mode, if the external BC Start option is enabled (bit 7 of Configuration Register #1), a low to high transition on this input will issue a BC Start command, starting execution of the current BC frame. In the enhanced BC mode, during the execution of a Wait for External Trigger (WTG) instruction, the Mark3 BC will wait for a low-to-high transition on EXT_TRIG before proceeding to the next instruction. In the Word Monitor mode, if the external trigger is enabled (bit 7 of Configuration Register #1), a low to high transition on this input will initiate a monitor start. This input has no effect in Message Monitor mode.
TRANSPARENT/ $\overline{\text{BUFFERED}}$ (I)	61	Used to select between the buffered mode (when strapped to logic "0") and transparent/DMA mode (when strapped to logic "1") for the host processor interface.

TABLE 53. PROCESSOR INTERFACE CONTROL (CONT.)

SIGNAL NAME	BU-6474XF/GX BU-6484XF/GX BU-64863F/GX PIN	DESCRIPTION
$\overline{\text{READYD}}$ (O)	62	Handshake output to host processor. For a nonzero wait state read access, $\overline{\text{READYD}}$ is asserted at the end of a host transfer cycle to indicate that data is available to be read on D15 through D0 when asserted (low). For a nonzero wait state write cycle, $\overline{\text{READYD}}$ is asserted at the end of the cycle to indicate that data has been transferred to a register or RAM location. For both nonzero wait reads and writes, the host must assert $\overline{\text{STRBD}}$ low until $\overline{\text{READYD}}$ is asserted low. In the (buffered) zero wait state mode, this output is normally logic "1", indicating that the Mark3 is in a state ready to accept a subsequent host transfer cycle. In zero wait mode, $\overline{\text{READYD}}$ will transition from high to low during (or just after) a host transfer cycle, when the Mark3 initiates its internal transfer to or from registers or internal RAM. When the Mark3 completes its internal transfer, $\overline{\text{READYD}}$ returns to logic "1", indicating it is ready for the host to initiate a subsequent transfer cycle.
$\overline{\text{IOEN}}$(O)	64	I/O Enable. Tri-state control for external address and data buffers. Generally not used in buffered mode. When low, indicates that the Mark3 is currently performing a host access to an internal register, or internal (for transparent mode) external RAM. In transparent mode, $\overline{\text{IOEN}}$ (low) should be used to enable external address and data bus tri-state buffers.

TABLE 54. RT ADDRESS

SIGNAL NAME	BU-6474XF/GX BU-6484XF/GX BU-64863F/GX PIN	DESCRIPTION
RTAD4 (MSB) (I)	40	RT Address input. If bit 5 of Configuration Register #6, RT ADDRESS SOURCE, is programmed to logic "0" (default), then the Mark3's RT address is provided by means of these 5 input signals. In addition, if RT ADDRESS SOURCE is logic "0", the source of RT address parity is RTADP. There are many methods for using these input signals for designating the Mark3's RT address. For details, refer to the description of RT_AD_LAT. If RT ADDRESS SOURCE is programmed to logic "1", then the Mark3's source for its RT address and parity is under software control, via data lines D5-D0. In this case, the RTAD4-RTAD0 and RTADP signals are not used.
RTAD3 (I)	39	
RTAD2 (I)	24	
RTAD1 (I)	45	
RTAD0 (LSB) (I)	38	
RTADP (I)	44	Remote Terminal Address Parity. This input signal must provide an odd parity sum with RTAD4-RTAD0 in order for the RT to respond to non-broadcast commands. That is, there must be an odd number of logic "1"s from among RTAD-4-RTAD0 and RTADP.
RT_AD_LAT (I)	36	RT Address Latch. Input signal used to control the Mark3's internal RT address latch. If RT_AD_LAT is connected to logic "0", then the Mark3 RT is configured to accept a hardwired (transparent) RT address from RTAD4-RTAD0 and RTADP. If RT_AD_LAT is initially logic "0", and then transitions to logic "1", the values presented on RTAD4-RTAD0 and RTADP will be latched internally on the rising edge of RT_AD_LAT. If RT_AD_LAT is connected to logic "1", then the Mark3's RT address is latchable under host processor control. In this case, there are two possibilities: (1) If bit 5 of Configuration Register #6, RT ADDRESS SOURCE, is programmed to logic "0" (default), then the source of the RT Address is the RTAD4-RTAD0 and RTADP input signals. (2) If RT ADDRESS SOURCE is programmed to logic "1", then the source of the RT Address is the lower 6 bits of the processor data bus, D5-D1 (for RTAD4-0) and D0 (for RTADP). In either of these two cases (with RT_AD_LAT = "1"), the processor will cause the RT address to be latched by: (1) Writing bit 15 of Configuration Register #3, ENHANCED MODE ENABLE, to logic "1". (2) Writing bit 3 of Configuration Register #4, LATCH RT ADDRESS WITH CONFIGURATION REGISTER #5, to logic "1". (3) Writing to Configuration Register #5. In the case of RT ADDRESS SOURCE = "1", then the values of RT address and RT address parity must be written to the lower 6 bits of Configuration Register #5, via D5-D0. In the case where RT ADDRESS SOURCE = "0", the bit values presented on D5-D0 become "don't care".

TABLE 55. MISCELLANEOUS

SIGNAL NAME			BU-6474XF/GX BU-6484XF/GX BU-64863F/GX	DESCRIPTION
64K RAM (BU-64863F/G 3/4/8/9/C/D)	4K RAM (BU-6474XF/GX BU-6484XF/GX)	64K RAM (BU-64863F/ G0)	PIN	
SLEEPIN (I)	UPADDREN (I)	NC	14	For 64K RAM versions with internal transceivers, this signal is always configured as SLEEPIN. This signal is used to control the transceiver sleep (power-down) circuitry in versions with 8/9 transceivers. For these versions of Mark3 if SLEEPIN is connected to logic "0", the transceivers are fully powered and operate normally. If SLEEPIN is connected to logic "1", the transceivers are in sleep mode (dormant, low-power mode) of operation and are NOT operational. For versions with 3/4/C/D transceivers, this signal has no effect. For 4K RAM versions, this signal is always configured as UPADDREN. This signal is used to control the function of the upper 4 address inputs (A15-A12). For these versions of Mark3 if UPADDREN is connected to logic "1", then these four signals operate as address lines A15-A12. If UPADDREN is connected to logic "0", then A15 and A14 function as CLK_SEL_1 and CLK_SEL_0 respectively; A13 MUST be connected to +3.3V-LOGIC; and A12 functions as $\overline{\text{RTBOOT}}$. For 64K RAM transceiverless versions, this signal is always a No Connect (NC).
$\overline{\text{INCMD}}$ (O) / $\overline{\text{MCRST}}$ (O)			32	In-command or Mode Code Reset. The function of this pin is controlled by bit 0 of Configuration Register #7, MODE CODE RESET/$\overline{\text{INCMD}}$ SELECT. If this register bit is logic "0" (default), $\overline{\text{INCMD}}$ will be active on this pin. For BC, RT, or Selective Message Monitor modes, $\overline{\text{INCMD}}$ is asserted low whenever a message is being processed by the Mark3. In Word Monitor mode, $\overline{\text{INCMD}}$ will be asserted low for as long as the monitor is online. For RT mode, if MODE CODE RESET/$\overline{\text{INCMD}}$ SELECT is programmed to logic "1", MCRST will be active. In this case, MCRST will be asserted low for two clock cycles following receipt of a Reset remote terminal mode command. In BC or Monitor modes, if MODE CODE RESET/$\overline{\text{INCMD}}$ SELECT is logic "1", this signal is inoperative; i.e., in this case, it will always output a value of logic "1".
$\overline{\text{INT}}$ (O)			63	Interrupt Request output. If the LEVEL/$\overline{\text{PULSE}}$ interrupt bit (bit 3) of Configuration Register #2 is logic "0", a negative pulse of approximately 500ns in width is output on $\overline{\text{INT}}$ to signal an interrupt request. If LEVEL/$\overline{\text{PULSE}}$ is high, a low level interrupt request output will be asserted on $\overline{\text{INT}}$. The level interrupt will be cleared (high) after either: (1) The processor writes a value of logic "1" to INTERRUPT RESET, bit 2 of the Start/Reset Register; or (2) If bit 4 of Configuration Register #2, INTERRUPT STATUS AUTO-CLEAR is logic "1" then it will only be necessary to read the Interrupt Status Register (#1 and/or #2) that is requesting an interrupt enabled by the corresponding Interrupt Mask Register. However, for the case where both Interrupt Status Register #1 and Interrupt Status Register #2 have bits set reflecting interrupt events, it will be necessary to read both interrupt status registers in order to clear $\overline{\text{INT}}$.
CLOCK_IN (I)			26	20 MHz, 16 MHz, 12 MHz, or 10 MHz clock input.
TX_INH_A (I)			65	Transmitter inhibit inputs for Channel A and Channel B, MIL-STD-1553 transmitters. For normal operation, these inputs should be connected to logic "0". To force a shutdown of Channel A and/or Channel B, a value of logic "1" should be applied to the respective TX_INH input.
TX_INH_B (I)			67	
$\overline{\text{MSTCLR}}$(I)			25	Master Clear. Negative true Reset input, normally asserted low following power turn-on.
TAG_CLK (I)			23	Time Tag Clock. External clock that may be used to increment the Time Tag Register. This option is selected by setting Bits 7, 8 and 9 of Configuration Register # 2 to Logic "1".

TABLE 56. NO USER CONNECTIONS

SIGNAL NAME	BU-6474XF/GX BU-6484XF/GX BU-64863F/GX PIN	DESCRIPTION
NC	4	No User Connections to these pins allowed.
	8	
	9	
	11	
	16	
	21	

TABLE 57. POWER AND GROUND

SIGNAL NAME	BU-64840B3/4 BU-64860B(R)3/4	BU-64743B8/C BU-64843B(R)8/C/D BU-64863B(R)8/C/D	DESCRIPTION
	BALL	BALL	
+ 3.3V_Xcvr	-	A4, A5, B4, B5, J1, J2, J3, J4, J5, K1, K2, K3, K4, K5, U4, U5, V4, V5	+ 3.3 Volt Transceiver Power
+ 5.0V_Xcvr	F1, F2, U13,V13	-	+ 5.0 Volt Transceiver Power
+ 3.3V_Logic	-	A8, A9, B8, B9, L16, L17, M16, M17, N12, N13, P12, P13, R6, R7, T6, T7, U6, U7, V6, V7	+3.3 V Logic Power
+ 5.0V/ + 3.3V_Logic	A7, L1, L2, L15, L16, M3, P7, P9, R9, V8	-	+5.0V/+3.3V Logic Power. These balls may connect to either +5.0V or +3.3V. Refer to input signal $\overline{\text{VDD\_Low}}$ (ball A13) to determine voltage selection options.
+ 5.0V_RAM	P4, R4, (BU-64860B(R)3 only)	-	For BU-64860B3 this ball must be connected to +5.0V
Gnd_Xcvr/ Thermal	D3, D4, D5, E2, E3, E4, E5, F3, F4, F5, G2, G3, G4, G5, H3, H4, H5, P11, P12, P13, P14, P15, R11, R12, R13, R14, R15, T11, T12, T13, T14, T15, U12, U14	D3, D4, D5, E3, E4, E5, F1, F2, F3, F4, F5, G3, G4, G5, L3, L4, L5, M3, M4, M5, N1, N2, N3, N4, N5, P3, P4, P5	Transceiver Ground/Thermal connections. See Thermal Management Section for important user information.
Gnd_Logic	E12, E13, E14, F12, F13, F14, G12, G13, G14, H12, H13, H14	E10, E11, E12, F10, F11, F12, G10, G11, G12, H10, H11, H12, R11, R12, R13, T11, T12, T13, U11, U12, U13	Logic Ground.
$\overline{\text{VDD\_Low}}$ (I)	A13	-	Input that selects logic threshold voltage. Set to logic "0" for 3.3V threshold and to +5V(logic "1") for 5V threshold. Must match "+5.0V/+3V Logic" input voltage.

NOTE: Logic ground and transceiver ground **are not** tied together inside the package.

TABLE 58. 1553 ISOLATION TRANSFORMER

SIGNAL NAME	BU-64840B3/4 BU-64860B(R)3/4	BU-64743B8/C BU-64843B(R)8/C/D BU-64863B(R)8/C/D	DESCRIPTION
	BALL	BALL	
TX/RX-A (I/O)	D1, D2, E1	D1, D2, E1, E2	Analog Transmit/Receive Input/Outputs. Connect directly to 1553 isolation transformers.
$\overline{\text{TX/RX-A}}$ (I/O)	G1, H1, H2	G1, G2, H1, H2	
TX/RX-B (I/O)	U11, V11, V12	L1, L2, M1, M2	
$\overline{\text{TX/RX-B}}$ (I/O)	U15, V14, V15	P1, P2, R1, R2	

TABLE 59. MANDATORY ADDITIONAL CONNECTIONS & INTERFACE TO EXTERNAL TRANSCEIVER

SIGNAL NAME	USING INTERNAL "BUILT-IN" TRANSCEIVERS	BU-64840B3/4 BU-64860B(R)3/4	BU-64743B8/C BU-64843B(R)8/C/D BU-64863B(R)8/C/D	FOR USE WITH EXTERNAL TRANSCEIVERS "TRANSCEIVERLESS"
		BALL	BALL	
$\overline{\text{SNGL\_END}}$ (I)	No Connect "NC" if utilizing "Built-In" Transceivers	A15	D14	If $\overline{\text{SNGL\_END}}$ is connected to logic "0" the Manchester decoder inputs will be configured to accept single-ended input signals (e.g.,MIL-STD-1773 fiber optic receiver outputs). If $\overline{\text{SNGL\_END}}$ is connected to logic "1," the decoder inputs will be configured to accept standard double-ended Manchester bi-phase input signals (i.e., MIL-STD-1553 receiver outputs).
TXINH_IN_A	These two signals MUST be directly connected for normal "Built-In" transceiver operation.	A4	E7	These two signals MUST be separated for "Transceiverless" operation. Transmitter inhibit inputs for Channel A of external MIL-STD-1553 transmitters. To enable transmitter this input should be connected to logic "0". To force a shutdown of Channel A, a value of logic "1" should be applied to the respective TXINH input.
TXINH_OUT_A		A5	E8	Digital transmit inhibit outputs. Connect to TX_INH_OUT inputs of external MIL-STD-1553 transceiver. Asserted high to inhibit when not transmitting on the respective bus.
TXDATA_IN_A	These two signals MUST be directly connected for normal "Built-In" transceiver operation.	C8	C7	These two signals MUST be separated for "Transceiverless" operation. Digital manchester biphase transmit data outputs. Connect directly to corresponding inputs of a MIL-STD-1553 or MIL-STD-1773 (fiber optic) transceiver.
TXDATA_OUT_A		B8	C8	
$\overline{\text{TXDATA\_IN\_A}}$	These two signals MUST be directly connected for normal "Built-In" transceiver operation.	C4	D7	These two signals MUST be separated for "Transceiverless" operation. Digital manchester biphase transmit data outputs. Connect directly to corresponding inputs of a MIL-STD-1553 or MIL-STD-1773 (fiber optic) transceiver.
$\overline{\text{TXDATA\_OUT\_A}}$		C5	D8	
$\overline{\text{RXDATA\_IN\_A}}$	These two signals MUST be directly connected for normal "Built-In" transceiver operation.	D10	G8	These two signals MUST be separated for "Transceiverless" operation. Digital manchester biphase receive data inputs. Connect directly to corresponding outputs of a MIL-STD-1553 or MIL-STD-1773 (fiber optic) transceiver.
$\overline{\text{RXDATA\_OUT\_A}}$		E10	G7	
RXDATA_IN_A	These two signals MUST be directly connected for normal "Built-In" transceiver operation.	E9	H8	These two signals MUST be separated for "Transceiverless" operation. Digital manchester biphase receive data inputs. Connect directly to corresponding outputs of a MIL-STD-1553 or MIL-STD-1773 (fiber optic) transceiver.
RXDATA_OUT_A		F9	H7	
TXINH_IN_B	These two signals MUST be directly connected for normal "Built-In" transceiver operation.	T8	N7	These two signals MUST be separated for "Transceiverless" operation. Transmitter inhibit inputs for Channel B of external MIL-STD-1553 transmitters. To enable transmitter this input should be connected to logic "0". To force a shutdown of Channel B, a value of logic "1" should be applied to the respective TXINH input.
TXINH_OUT_B		R8	N8	Digital transmit inhibit outputs. Connect to TX_INH_OUT inputs of external MIL-STD-1553 transceiver. Asserted high to inhibit when not transmitting on the respective bus.

TABLE 59. MANDATORY ADDITIONAL CONNECTIONS & INTERFACE TO EXTERNAL TRANSCEIVER (CONT.)

SIGNAL NAME	UTILIZING INTERNAL "BUILT-IN" TRANSCEIVERS	BU-64840B3/4 BU-64860B(R)3/4	BU-64743B8/C BU-64843B(R)8/C/D BU-64863B(R)8/C/D	FOR USE WITH EXTERNAL TRANSCEIVERS "TRANSCEIVERLESS"
		BALL	BALL	
TXDATA_IN_B	These two signals MUST be directly connected for normal "Built-In" transceiver operation.	R10	L7	These two signals MUST be separated for "Transceiverless" operation. Digital manchester biphase transmit data outputs. Connect directly to corresponding inputs of a MIL-STD-1553 or MIL-STD-1773 (fiber optic) transceiver.
TXDATA_OUT_B		P10	L8	
$\overline{\text{TXDATA\_IN\_B}}$	These two signals MUST be directly connected for normal "Built-In" transceiver operation.	N12	M7	These two signals MUST be separated for "Transceiverless" operation. Digital manchester biphase transmit data outputs. Connect directly to corresponding inputs of a MIL-STD-1553 or MIL-STD-1773 (fiber optic) transceiver.
$\overline{\text{TXDATA\_OUT\_B}}$		M12	M8	
$\overline{\text{RXDATA\_IN\_B}}$	These two signals MUST be directly connected for normal "Built-In" transceiver operation.	M13	P10	These two signals MUST be separated for "Transceiverless" operation. Digital manchester biphase receive data inputs. Connect directly to corresponding outputs of a MIL-STD-1553 or MIL-STD-1773 (fiber optic) transceiver.
$\overline{\text{RXDATA\_OUT\_B}}$		M14	P9	
RXDATA_IN_B	These two signals MUST be directly connected for normal "Built-In" transceiver operation.	N13	R10	These two signals MUST be separated for "Transceiverless" operation. Digital manchester biphase receive data inputs. Connect directly to corresponding outputs of a MIL-STD-1553 or MIL-STD-1773 (fiber optic) transceiver.
RXDATA_OUT_B		N14	R9	

TABLE 60. DATA BUS

SIGNAL NAME	BU-64840B3/4 BU-64860B(R)3/4	BU-64743B8/C BU-64843B(R)8/C/D BU-64863B(R)8/C/D	DESCRIPTION
	BALL	BALL	
D15 (MSB)	D15	D16	16-bit bi-directional data bus. This bus interfaces the host processor to the Mini-ACE Mark3's internal registers and internal RAM. In addition, in transparent mode, this bus allows data transfers to take place between the internal protocol/memory management logic and up to 64K x 16 of external RAM. Most of the time, the outputs for D15 through D0 are in the high impedance state. They drive outward in the buffered or transparent mode when the host CPU reads the internal RAM or registers. Also, in the transparent mode, D15-D0 will drive outward (towards the host) when the protocol/management logic is accessing (either reading or writing) internal RAM, or writing to external RAM. In the transparent mode, D15-D0 drives inward when the CPU writes internal registers or RAM, or when the protocol/memory management logic reads external RAM.
D14	E17	F15	
D13	E16	E16	
D12	E18	F18	
D11	E15	E17	
D10	F16	E18	
D09	F15	F16	
D08	F18	G18	
D07	F17	F17	
D06	G18	J18	
D05	G16	H17	
D04	G17	H18	
D03	G15	G17	
D02	H18	J17	
D01	J17	K16	
D00 (LSB)	H17	K17	

TABLE 61. PROCESSOR ADDRESS BUS

SIGNAL NAME		BU-64840B3/4 BU-64860B(R)3/4	BU-64743B8/C BU-64843B(R)8/C/D BU-64863B(R)8/C/D	DESCRIPTION
64K RAM (BU-6486XBX)	4K RAM (BU-64743B8 BU-6484XBX)	BALL	BALL	
A15 (MSB)	A15 / CLK_ SEL_1	C10	A11	16-bit bi-directional address bus. For 64K RAM versions, this signal is always configured as address line A15 (MSB). Refer to the description for A11-A0 below. For 4K RAM versions, if UPADDREN is connected to logic "1", this signal operates as address line A15. For 4K RAM versions, if UPADDREN is connected to logic "0", this signal operates as CLK_SEL_1. In this case, A15/CLK_SEL_1 and A14/CLK_ SEL_0 are used to select the Mark3 clock frequency, as follows: CLK_SEL_1 / CLK_SEL_0 / Clock Frequency 0 / 0 / 10 MHz 0 / 1 / 20 MHz 1 / 0 / 12 MHz 1 / 1 / 16 MHz
A14	A14 / CLK_ SEL_0	A10	A7	For 64K RAM versions, this signal is always configured as address line A14. Refer to the description of A11-A0 below. For 4K RAM versions, if UPADDREN is connected to logic "1", this signal operates as A14. For 4K RAM versions, if UPADDREN is connected to logic "0", then this signal operates as CLK_SEL_0. In this case, CLK_SEL_1 and CLK_SEL_0 are used to select the Mark3 clock frequency, as defined in the description for A15/CLK_SEL1 above.
A13	A13 / LOGIC “1”	B10	B10	For 64K RAM versions, this signal is always configured as address line A13. Refer to the description for A11-A0 below. For 4K RAM versions, if UPADDREN is connected to logic "1", this signal operates as A13. For 4K RAM versions, if UPADDREN is connected to logic "0", then this signal MUST be connected to +3.3V-LOGIC (logic "1").
A12	A12 / $\overline{\text{RTBOOT}}$	A9	A10	For 64K RAM versions, this signal is always configured as address line A12. Refer to the description for A11-A0 below. For 4K RAM versions, if UPADDREN is connected to logic "1", this signal operates as A12. For 4K RAM versions, if UPADDREN is connected to logic "0", then this signal functions as $\overline{\text{RTBOOT}}$. If $\overline{\text{RTBOOT}}$ is connected to logic "0", the Mark3 will initialize in RT mode with the Busy status word bit set following power turn-on. If $\overline{\text{RTBOOT}}$ is hardwired to logic "1", the Mark3 will initialize in either Idle mode (for an RT-only part), or in BC mode (for a BC/RT/MT part).

TABLE 61. PROCESSOR ADDRESS BUS (CONT.)

SIGNAL NAME		BU-64840B3/4 BU-64860B(R)3/4	BU-64743B8/C BU-64843B(R)8/C/D BU-64863B(R)8/C/D	DESCRIPTION
64K RAM (BU-6486XBX)	4K RAM (BU-64743B8 BU-6484XBX)	BALL	BALL	
A11	A11	B9	E6	Lower 12 bits of 16-bit bi-directional address bus. In both the buffered and transparent modes, the host CPU accesses Mark3 registers and internal RAM by means of A11 - A0 (4K versions). For 64K versions, A15-A12 are also used for this purpose. In buffered mode, A12-A0 (or A15-A0) are inputs only. In the transparent mode, A12-A0 (or A15-A0) are inputs during CPU accesses and become outputs, driving outward (towards the CPU) when the 1553 protocol/memory management logic accesses up to 64K words of external RAM. In transparent mode, the address bus is driven outward only when the signal $\overline{\text{DTACK}}$ is low (indicating that the Mark3 has control of the RAM interface bus) and $\overline{\text{IOEN}}$ is high, indicating a non-host access. Most of the time, including immediately after power turn-on, A12-A0 (or A15-A0) will be in high impedance (input) state.
A10	A10	A8	C15	
A09	A09	B7	C10	
A08	A08	C9	D10	
A07	A07	C7	D9	
A06	A06	D7	V9	
A05	A05	C6	C12	
A04	A04	D8	B7	
A03	A03	D6	E9	
A02	A02	E8	C9	
A01	A01	E7	U8	
A00	A00	F10	F8	

TABLE 62. PROCESSOR INTERFACE CONTROL

SIGNAL NAME	BU-64840B3/4 BU-64860B(R)3/4	BU-64743B8/C BU-64843B(R)8/C/D BU-64863B(R)8/C/D	DESCRIPTION
	BALL	BALL	
$\overline{\text{SELECT}}$ (I)	B12	B12	Device Select. Generally connected to a CPU address decoder output to select the Mark3 for a transfer to/from either RAM or register.
$\overline{\text{STRBD}}$ (I)	A12	A12	Strobe Data. Used in conjunction with $\overline{\text{SELECT}}$ to initiate and control the data transfer cycle between the host processor and the Mark3. $\overline{\text{STRBD}}$ must be asserted low through the full duration of the transfer cycle.
RD / $\overline{\text{WR}}$ (I)	A11	B11	Read/Write. For host processor access, RD/$\overline{\text{WR}}$ selects between reading and writing. In the 16-bit buffered mode, if POL_SEL is logic "0", then RD/$\overline{\text{WR}}$ should be low (logic "0") for read accesses and high (logic "1") for write accesses. If POL_SEL is logic "1", or the interface is configured for a mode other than 16-bit buffered mode, then RD/$\overline{\text{WR}}$ is high (logic "1") for read accesses and low (logic "0") for write accesses.
ADDR_LAT(I) / $\overline{\text{MEMOE}}$ (O)	L9	U10	Memory Output Enable or Address Latch. In buffered mode, the ADDR_LAT input is used to configure the buffers for A15-A0, $\overline{\text{SELECT}}$, MEM/$\overline{\text{REG}}$, and MSB/LSB (for 8-bit mode only) in latched mode (when low) or transparent mode (when high). That is, the Mark3's internal transparent latches will track the values on A15-A0, $\overline{\text{SELECT}}$, MEM/$\overline{\text{REG}}$, and MSB/LSB when ADDR_LAT is high, and latch the values when ADDR_LAT goes low. In general, for interfacing to processors with a non-multiplexed address/data bus, ADDR_LAT should be hardwired to logic "1". For interfacing to processors with a multiplexed address/data bus, ADDR_LAT should be connected to a signal that indicates a valid address when ADDR_LAT is logic "1". In transparent mode, $\overline{\text{MEMOE}}$ output signal is used to enable data outputs for external RAM read cycles (normally connected to the OE input signal on external RAM chips).
$\overline{\text{ZEROWAIT}}$ (I) / $\overline{\text{MEMWR}}$ (O)	M10	T8	Memory Write or Zero Wait. In buffered mode, input signal ($\overline{\text{ZEROWAIT}}$) used to select between the zero wait mode ($\overline{\text{ZEROWAIT}}$ = "0") and the non-zero wait mode ($\overline{\text{ZEROWAIT}}$ = "1"). In transparent mode, active low output signal ($\overline{\text{MEMWR}}$) asserted low during memory write transfers to strobe data into external RAM (normally connected to the $\overline{\text{WR}}$ input signal on external RAM chips).
16 / $\overline{8}$ (I) / $\overline{\text{DTREQ}}$ (O)	L10	R17	Data Transfer Request or Data Bus Select. In buffered mode, input signal 16/8 used to select between the 16 bit data transfer mode (16/$\overline{8}$ = "1") and the 8-bit data transfer mode (16/$\overline{8}$ = "0"). In transparent mode (16-bit only), active low level output signal $\overline{\text{DTREQ}}$ used to request access to the processor/RAM interface bus (address and data buses).
MSB / LSB (I) / $\overline{\text{DTGRT}}$ (I)	J7	B6	Data Transfer Grant or Most Significant Byte/Least Significant Byte. In 8-bit buffered mode, input signal (MSB/LSB) used to indicate which byte is currently being transferred (MSB or LSB). The logic sense of MSB/LSB is controlled by the POL_SEL input. MSB/LSB is not used in the 16-bit buffered mode. In transparent mode, active low input signal ($\overline{\text{DTGRT}}$) asserted in response to the $\overline{\text{DTREQ}}$ output to indicate that control of the external processor/RAM bus has been transferred from the host processor to the Mark3.

TABLE 62. PROCESSOR INTERFACE CONTROL (CONT.)

SIGNAL NAME	BU-64840B3/4 BU-64860B(R)3/4 BALL	BU-64743B8/C BU-64843B(R)8/C/D BU-64863B(R)8/C/D BALL	DESCRIPTION
POL_SEL (I) / $\overline{\text{DTACK}}$ (O)	N9	V8	Data Transfer Acknowledge or Polarity Select. In 16-bit buffered mode, if POL_SEL is connected to logic "1", RD/$\overline{\text{WR}}$ should be asserted high (logic "1") for a read operation and low (logic "0") for a write operation. In 16-bit buffered mode, if POL_SEL is connected to logic "0", RD/$\overline{\text{WR}}$ should be asserted low (logic "0") for a read operation and high (logic "1") for a write operation. In 8-bit buffered mode (TRANSPARENT/ BUFFERED = "0" and 16/8 = "0"), POL_SEL input signal used to control the logic sense of the MSB/$\overline{\text{LSB}}$ signal. If POL_SEL is connected to logic "0", MSB/$\overline{\text{LSB}}$ should be asserted low (logic "0") to indicate the transfer of the least significant byte and high (logic "1") to indicate the transfer of the most significant byte. If POL_SEL is connected to logic "1", MSB/$\overline{\text{LSB}}$ should be asserted high (logic "1") to indicate the transfer of the least significant byte and low (logic "0") to indicate the transfer of the most significant byte. In transparent mode, active low output signal ($\overline{\text{DTACK}}$) used to indicate acceptance of the processor/RAM interface bus in response to a data transfer grant ($\overline{\text{DTGRT}}$). Mark3 RAM transfers over A15-A0 and D15-D0 will be framed by the time that $\overline{\text{DTACK}}$ is asserted low.
TRIG_SEL (I) / $\overline{\text{MEMENA\_IN}}$ (I)	L11	N17	Memory Enable or Trigger Select input. In 8-bit buffered mode, input signal (TRIG-SEL) used to select the order in which byte pairs are transferred to or from the Mark3 by the host processor. In the 8-bit buffered mode, TRIG_SEL should be asserted high (logic 1) if the byte order for both read operations and write operations is MSB followed by LSB. TRIG_SEL should be asserted low (logic 0) if the byte order for both read operations and write operations is LSB followed by MSB. This signal has no operation in the 16-bit buffered mode (it does not need to be connected). In transparent mode, active low input $\overline{\text{MEMENA\_IN}}$, used as a Chip Select (CS) input to the Mark3's internal shared RAM. If only internal RAM is used, should be connected directly to the output of a gate that is OR'ing the $\overline{\text{DTACK}}$ and $\overline{\text{IOEN}}$ output signals.
MEM / $\overline{\text{REG}}$(I)	C11	A6	Memory/Register. Generally connected to either a CPU address line or address decoder output. Selects between memory access (MEM/$\overline{\text{REG}}$ = "1") or register access (MEM/$\overline{\text{REG}}$ = "0").

TABLE 62 . PROCESSOR INTERFACE CONTROL (CONT.)

SIGNAL NAME	BU-64840B3/4 BU-64860B(R)3/4 BALL	BU-64743B8/C BU-64843B(R)8/C/D BU-64863B(R)8/C/D BALL	DESCRIPTION
$\overline{\text{SSFLAG}}$ (I) / EXT_TRIG(I)	J8	R8	Subsystem Flag (RT) or External Trigger (BC/Word Monitor) input. In RT mode, if this input is asserted low, the Subsystem Flag bit will be set in the Mark3's RT Status Word. If the $\overline{\text{SSFLAG}}$ input is logic "0" while bit 8 of Configuration Register #1 has been programmed to logic "1" (cleared), the Subsystem Flag RT Status Word bit will become logic "1," but bit 8 of Configuration Register #1, $\overline{\text{SUBSYSTEM FLAG}}$, will return logic "1" when read. That is, the sense on the $\overline{\text{SSFLAG}}$ input has no effect on the SUBSYSTEM FLAG register bit. In the non-enhanced BC mode, this signal operates as an External Trigger input. In BC mode, if the external BC Start option is enabled (bit 7 of Configuration Register #1), a low to high transition on this input will issue a BC Start command, starting execution of the current BC frame. In the enhanced BC mode, during the execution of a Wait for External Trigger (WTG) instruction, the Mark3 BC will wait for a low-to-high transition on EXT_ TRIG before proceeding to the next instruction. In the Word Monitor mode, if the external trigger is enabled (bit 7 of Configuration Register #1), a low to high transition on this input will initiate a monitor start. This input has no effect in Message Monitor mode.
TRANSPARENT/ $\overline{\text{BUFFERED}}$ (I)	D16	D17	Used to select between the buffered mode (when strapped to logic "0") and transparent/DMA mode (when strapped to logic "1") for the host processor interface.
$\overline{\text{READYD}}$ (O)	C15	B15	Handshake output to host processor. For a nonzero wait state read access, $\overline{\text{READYD}}$ is asserted at the end of a host transfer cycle to indicate that data is available to be read on D15 through D0 when asserted (low). For a nonzero wait state write cycle, $\overline{\text{READYD}}$ is asserted at the end of the cycle to indicate that data has been transferred to a register or RAM location. For both nonzero wait reads and writes, the host must assert $\overline{\text{STRBD}}$ low until $\overline{\text{READYD}}$ is asserted low. In the (buffered) zero wait state mode, this output is normally logic "1", indicating that the Mark3 is in a state ready to accept a subsequent host transfer cycle. In zero wait mode, $\overline{\text{READYD}}$ will transition from high to low during (or just after) a host transfer cycle, when the Mark3 initiates its internal transfer to or from registers or internal RAM. When the Mark3 completes its internal transfer, $\overline{\text{READYD}}$ returns to logic "1", indicating it is ready for the host to initiate a subsequent transfer cycle.
$\overline{\text{IOEN}}$(O)	C14	A15	I/O Enable. Tri-state control for external address and data buffers. Generally not used in buffered mode. When low, indicates that the Mark3 is currently performing a host access to an internal register, or internal (for transparent mode) external RAM. In transparent mode, $\overline{\text{IOEN}}$ (low) should be used to enable external address and data bus tri-state buffers.

TABLE 63. RT ADDRESS

SIGNAL NAME	BU-64840B3/4 BU-64860B(R)3/4 BALL	BU-64743B8/C BU-64843B(R)8/C/D BU-64863B(R)8/C/D BALL	DESCRIPTION
RTAD4 (MSB) (I)	J16	J15	RT Address input. If bit 5 of Configuration Register #6, RT ADDRESS SOURCE, is programmed to logic "0" (default), then the Mark3's RT address is provided by means of these 5 input signals. In addition, if RT ADDRESS SOURCE is logic "0", the source of RT address parity is RTADP. There are many methods for using these input signals for designating the Mark3's RT address. For details, refer to the description of RT_AD_LAT. If RT ADDRESS SOURCE is programmed to logic "1", then the Mark3's source for its RT address and parity is under software control, via data lines D5-D0. In this case, the RTAD4-RTAD0 and RTADP signals are not used.
RTAD3 (I)	K17	M18	
RTAD2 (I)	L17	J16	
RTAD1 (I)	K18	L18	
RTAD0 (LSB) (I)	K16	N18	
RTADP (I)	J18	K18	Remote Terminal Address Parity. This input signal must provide an odd parity sum with RTAD4-RTAD0 in order for the RT to respond to non-broadcast commands. That is, there must be an odd number of logic "1"s from among RTAD-4-RTAD0 and RTADP.
RT_AD_LAT (I)	L18	P18	RT Address Latch. Input signal used to control the Mark3's internal RT address latch. If RT_AD_LAT is connected to logic "0", then the Mark3 RT is configured to accept a hardwired (transparent) RT address from RTAD4-RTAD0 and RTADP. If RT_AD_LAT is initially logic "0", and then transitions to logic "1", the values presented on RTAD4-RTAD0 and RTADP will be latched internally on the rising edge of RT_AD_LAT. If RT_AD_LAT is connected to logic "1", then the Mark3's RT address is latchable under host processor control. In this case, there are two possibilities: (1) If bit 5 of Configuration Register #6, RT ADDRESS SOURCE, is programmed to logic "0" (default), then the source of the RT Address is the RTAD4-RTAD0 and RTADP input signals. (2) If RT ADDRESS SOURCE is programmed to logic "1", then the source of the RT Address is the lower 6 bits of the processor data bus, D5-D1 (for RTAD4-0) and D0 (for RTADP). In either of these two cases (with RT_AD_LAT = "1"), the processor will cause the RT address to be latched by: (1) Writing bit 15 of Configuration Register #3, ENHANCED MODE ENABLE, to logic "1". (2) Writing bit 3 of Configuration Register #4, LATCH RT ADDRESS WITH CONFIGURATION REGISTER #5, to logic "1". (3) Writing to Configuration Register #5. In the case of RT ADDRESS SOURCE = "1", then the values of RT address and RT address parity must be written to the lower 6 bits of Configuration Register #5, via D5-D0. In the case where RT ADDRESS SOURCE = "0", the bit values presented on D5-D0 become "don't care".

TABLE 64. MISCELLANEOUS

SIGNAL NAME		BU-64840B3/4 BU-64860B(R)3/4	BU-64743B8/C BU-64843B(R)8/C/D BU-64863B(R)8/C/D	DESCRIPTION
64K RAM (BU-6486XB(R)X)	4K RAM (BU-64743B8/C BU-6484XB(R)X)	BALL	BALL	
Logic "1"	UPADDREN (I)	C12	F7	This signal is used to control the function of the upper 4 address inputs (A15-A12). If UPADDREN is connected to logic "1", then these four signals operate as address lines A15-A12. If UPADDREN is connected to logic "0", then A15 and A14 function as CLK_SEL_1 and CLK_SEL_0 respectively; A13 MUST be connected to LOGIC "1"; and A12 functions as $\overline{\text{RTBOOT}}$.
SLEEPIN (I)		-	R4	For versions with type 8 transceivers, this signal is used to control the transceiver sleep (power-down) circuitry. If SLEEPIN is connected to logic "0", the transceivers are fully powered and operate normally. If SLEEPIN is connected to logic "1", the transceivers are in sleep mode (dormant, low-power mode) of operation and are NOT operational. For versions with type C transceivers, this signal has no effect.
$\overline{\text{INCMD}}$ (O)		H16	P17	For BC, RT, or Selective Message Monitor modes, $\overline{\text{INCMD}}$ is asserted low whenever a message is being processed by the Micro-ACE-TE. In Word Monitor mode, $\overline{\text{INCMD}}$ will be asserted low for as long as the monitor is online.
$\overline{\text{MCRST}}$ (O)		B13	D11	For RT mode $\overline{\text{MCRST}}$ will be asserted low for two clock cycles following receipt of a Reset remote terminal mode command.
RSTBITEN (I)		M18	L14	If this input is set to logic "1", the Built-In-Self-Test (BIST) will be enabled after hardware reset (for example, following power-up). A logic "0" input disables both the power-up and user-initiated automatic BIST.
$\overline{\text{INT}}$ (O)		D17	D18	Interrupt Request output. If the LEVEL/$\overline{\text{PULSE}}$ interrupt bit (bit 3) of Configuration Register #2 is logic "0", a negative pulse of approximately 500 ns in width is output on $\overline{\text{INT}}$ to signal an interrupt request. If LEVEL/$\overline{\text{PULSE}}$ is high, a low level interrupt request output will be asserted on $\overline{\text{INT}}$. The level interrupt will be cleared (high) after either: (1) The processor writes a value of logic "1" to INTERRUPT RESET, bit 2 of the Start/Reset Register; or (2) If bit 4 of Configuration Register #2, INTERRUPT STATUS AUTO-CLEAR is logic "1" then it will only be necessary to read the Interrupt Status Register (#1 and/or #2) that is requesting an interrupt enabled by the corresponding Interrupt Mask Register. However, for the case where both Interrupt Status Register #1 and Interrupt Status Register #2 have bits set reflecting interrupt events, it will be necessary to read both interrupt status registers in order to clear $\overline{\text{INT}}$.
CLOCK_IN (I)		M9	T10	20 MHz, 16 MHz, 12 MHz, or 10 MHz clock input.
TX_INH_A (I)		A14	A14	Transmitter inhibit inputs for Channel A and Channel B, MIL-STD-1553 transmitters. For normal operation, these inputs should be connected to logic "0". To force a shutdown of Channel A and/or Channel B, a value of logic "1" should be applied to the respective TX_INH input.
TX_INH_B (I)		C13	B14	
$\overline{\text{MSTCLR}}$ (I)		B11	R18	Master Clear. Negative true Reset input, normally asserted low following power turn-on.
TAG_CLK (I)		D18	F14	Time Tag Clock. External clock that may be used to increment the Time Tag Register. This option is selected by setting Bits 7, 8 and 9 of Configuration Register # 2 to Logic "1".
NC/NSLOW_A/B		-	T5	For product types BU-64843B(R)D and BU-64863B(R)D, ball T5 is NSLOW_A_B, which must be connected to LOGIC '0'. T5 needs to be LOGIC '0' for McAir applications. For all other product types, ball T5 must be a no connect.

TABLE 65. NO USER CONNECTIONS

SIGNAL NAME	BU-64840B3/4 BU-64860B(R)3/4 BALL	BU-64743B8/C BU-64843B(R)8/C/D BU-64863B(R)8/C/D BALL	DESCRIPTION
NC	A1, A2, A3, A6, A16, A17, A18, B1, B2, B3, B4, B5, B6, B14, B15, B16, B17, B18, C1, C2, C3, C16, C17, C18, D9, D11, D12, D13, D14, E6, E11, F6, F7, F8, F11, G6, G7, G8, G9, G10, G11, H6, H7, H8, H9, H10, H11, H15, J1, J2, J3, J4, J5, J6, J9, J10, J11, J12, J13, J14, J15, K1, K2, K3, K4, K5, K6, K7, K8, K9, K10, K11, K12, K13, K14, K15, L3, L4, L5, L6, L7, L8, L12, L13, L14, M1, M2, M4, M5, M6, M7, M8, M11, M15, M16, M17, N1, N2, N3, N4, N5, N6, N7, N8, N10, N11, N15, N16, N17, N18, P1, P2, P3, P5, P6, P8, P16, P17, P18, R1, R2, R3, R5, R6, R7, R16, R17, R18, T1, T2, T3, T4, T5, T6, T7, T9, T10, T16, T17, T18, U1, U2, U3, U4, U5, U6, U7, U8, U9, U10, U16, U17, U18, V1, V2, V3, V4, V5, V6, V7, V9, V10, V16, V17, V18	A1, A2, A3, A13, A16, A17, A18, B1, B2, B3, B13, B16, B17, B18, C1, C2, C3, C4, C5, C6, C11, C13, C14, C16, C17, C18, D6, D12, D13, D15, E13, E14, E15, F6, F9, F13, G6, G9, G13, G14, G15, G16, H3, H4, H5, H6, H9, H13, H14, H15, H16, J6, J7, J8, J9, J10, J11, J12, J13, J14, K6, K7, K8, K9, K10, K11, K12, K13, K14, K15, L6, L9, L10, L11, L12, L13, L15, M6, M9, M10, M11, M12, M13, M14, M15, N6, N9, N10, N11, N14, N15, N16, P6, P7, P8, P11, P14, P15, P16, R3, R5, R14, R15, R16, T1, T2, T3, T4, T9, T14, T15, T16, T17, T18, U1, U2, U3, U9, U14, U15, U16, U17, U18, V1, V2, V3, V10, V11, V12, V13, V14, V15, V16, V17, V18	No User Connections to these balls allowed.

TABLE 66. MINI-ACE MARK3 BU-64XXXF/G3/4/8/9/C/D VERSIONS PINOUTS			
PIN	FUNCTION	PIN	FUNCTION
1	A11	41	DB06
2	A10	42	DB01
3	TX/RX_A	43	DB04
4	DO NOT CONNECT - FACTORY TEST POINT	44	RTADP
5	$\overline{\text{TX/RX\_A}}$	45	RTAD1
6	MEM/$\overline{\text{REG}}$	46	DB00
7	A08	47	DB02
8	DO NOT CONNECT - FACTORY TEST POINT	48	DB03
9	DO NOT CONNECT - FACTORY TEST POINT	49	DB05
10	+3.3V_XCVR for BU-64XXXF/G8/9/C/D or +5.0_XCVR for BU-64XXXF/G3/4	50	GND_LOGIC
		51	+3.3V_LOGIC for BU-64XX3 or +5.0V_LOGIC for BU-64XX5
11	DO NOT CONNECT - FACTORY TEST POINT	52	DB08
12	A07	53	DB07
13	A03	54	DB13
14	SLEEPIN* or UPADDREN**	55	DB12
15	TX/RX_B	56	DB14
16	DO NOT CONNECT - FACTORY TEST POINT	57	DB09
17	$\overline{\text{TX/RX\_B}}$	58	DB11
18	A00	59	DB15
19	A02	60	DB10
20	ADDR_LAT/$\overline{\text{MEMOE}}$	61	TRANS/$\overline{\text{BUFF}}$
21	DO NOT CONNECT - FACTORY TEST POINT	62	$\overline{\text{READYD}}$
22	GND_XCVR	63	$\overline{\text{INT}}$
23	TAG_CLK	64	$\overline{\text{IOEN}}$
24	RTAD2	65	TX_INH_A
25	$\overline{\text{MSTCLR}}$	66	$\overline{\text{SELECT}}$
26	CLOCK_IN	67	TX_INH_B
27	A06	68	$\overline{\text{STRBD}}$
28	$\overline{\text{ZEROWAIT}}$/$\overline{\text{MEMWR}}$	69	+3.3V_LOGIC for BU-64XX3 or +5.0V_LOGIC for BU-64XX5
29	16/$\overline{8}$/$\overline{\text{DTREQ}}$	70	GND_LOGIC
30	+3.3V_LOGIC for BU-64XX3 or +5.0V_LOGIC for BU-64XX5	71	RD/$\overline{\text{WR}}$
31	GND_LOGIC	72	MSB/LSB/$\overline{\text{DTGRT}}$
32	$\overline{\text{INCMD}}$/$\overline{\text{MCRST}}$	73	A15* or A15/CLK_SEL_1**
33	A01	74	A05
34	TRIG_SEL/$\overline{\text{MEMENA\_IN}}$	75	A09
35	POL_SEL/$\overline{\text{DTACK}}$	76	A12* or A12/$\overline{\text{RTBOOT}}$**
36	RT_AD_LAT	77	A13* or A13/+3.3V_LOGIC** for BU-64XX3 or +5.0V_LOGIC** for BU-64XX5
37	$\overline{\text{SSFLAG}}$/EXT_TRIG	78	A04
38	RTAD0	79	GND_XCVR
39	RTAD3	80	A14* or A14/CLK_SEL_0**
40	RTAD4		

* Applicable for 64K RAM option.
** Applicable for 4K RAM option.

TABLE 67. MINI-ACE MARK3 BU-64XX3F/G0 (TRANSCEIVERLESS) VERSION PINOUTS			
PIN	FUNCTION	PIN	FUNCTION
1	A11	41	DB06
2	A10	42	DB01
3	TXDATA_A	43	DB04
4	$\overline{\text{RXDATA\_A}}$ ***	44	RTADP
5	$\overline{\text{TXDATA\_A}}$	45	RTAD1
6	MEM/$\overline{\text{REG}}$	46	DB00
7	A08	47	DB02
8	RXDATA_A	48	DB03
9	TXINH_B_OUT	49	DB05
10	+3.3V_LOGIC	50	GND_LOGIC
11	TXINH_A_OUT	51	3.3V_LOGIC
12	A07	52	DB08
13	A03	53	DB07
14	UPADDREN** or NC*	54	DB13
15	TXDATA_B	55	DB12
16	$\overline{\text{RXDATA\_B}}$ ***	56	DB14
17	$\overline{\text{TXDATA\_B}}$	57	DB09
18	A00	58	DB11
19	A02	59	DB15
20	ADDR_LAT/$\overline{\text{MEMOE}}$	60	DB10
21	RXDATA_B	61	TRANS/$\overline{\text{BUFF}}$
22	GND_LOGIC	62	$\overline{\text{READYD}}$
23	TAG_CLK	63	$\overline{\text{INT}}$
24	RTAD2	64	$\overline{\text{IOEN}}$
25	MSTCLR	65	TX_INH_A
26	CLOCK_IN	66	$\overline{\text{SELECT}}$
27	A06	67	TX_INH_B
28	$\overline{\text{ZEROWAIT}}$/$\overline{\text{MEMWR}}$	68	$\overline{\text{STRBD}}$
29	16/$\overline{8}$/$\overline{\text{DTREQ}}$	69	3.3V_LOGIC
30	3.3V_LOGIC	70	GND_LOGIC
31	GND_LOGIC	71	RD/$\overline{\text{WR}}$
32	$\overline{\text{INCMD}}$/$\overline{\text{MCRST}}$	72	MSB/LSB/$\overline{\text{DTGRT}}$
33	A01	73	A15* or A15/CLK_SEL_1**
34	TRIG_SEL/$\overline{\text{MEMENA\_IN}}$	74	A05
35	POL_SEL/$\overline{\text{DTACK}}$	75	A09
36	RT_AD_LAT	76	A12* or A12/$\overline{\text{RTBOOT}}$**
37	$\overline{\text{SSFLAG}}$/EXT_TRIG	77	A13* or A13/+3.3V_LOGIC**
38	RTAD0	78	A04
39	RTAD3	79	GND_LOGIC
40	RTAD4	80	A14* or A14/CLK_SEL_0**

* Applicable for 64K RAM option.

** Applicable for 4K RAM option.

*** Standard transceiverless parts have their receiver inputs internally strapped for single-ended operation. The $\overline{\text{RXDATAx}}$ pins are connected to inputs that are not enabled.

TABLE 68. MICRO-ACE-TE BU-64743B8/C / BU-648X3B(R)8/C/D (+3.3V BGA PACKAGE) PINOUTS					
BALL	**SIGNAL**	**NOTES**	**BALL**	**SIGNAL**	**NOTES**
A1	NC		C1	NC	
A2	NC		C2	NC	
A3	NC		C3	NC	
A4	+3.3V_XCVR		C4	NC	
A5	+3.3V_XCVR		C5	NC	
A6	MEM/$\overline{\text{REG}}$		C6	NC	
A7	A14* or A14/CLK_SEL_0**		C7	TXDATA_IN_A	connect to ball C8
A8	+3.3V LOGIC		C8	TXDATA_OUT_A	connect to ball C7
A9	+3.3V LOGIC		C9	A2	
A10	A12* or A12/$\overline{\text{RTBOOT}}$**		C10	A9	
A11	A15* or A15/CLK_SEL_1**		C11	NC	
A12	$\overline{\text{STRBD}}$		C12	A5	
A13	NC		C13	NC	
A14	TX_INH_A		C14	NC	
A15	$\overline{\text{IOEN}}$		C15	A10	
A16	NC		C16	NC	
A17	NC		C17	NC	
A18	NC		C18	NC	
B1	NC		D1	TX/RX-A	
B2	NC		D2	TX/RX-A	
B3	NC		D3	GND_XCVR/THERMAL***	
B4	+3.3V_XCVR		D4	GND_XCVR/THERMAL***	
B5	+3.3V_XCVR		D5	GND_XCVR/THERMAL***	
B6	MSB/LSB / $\overline{\text{DTGRT}}$		D6	NC	
B7	A4		D7	$\overline{\text{TXDATA\_IN\_A}}$	connect to ball D8
B8	+3.3V LOGIC		D8	$\overline{\text{TXDATA\_OUT\_A}}$	connect to ball D7
B9	+3.3V LOGIC		D9	A7	
B10	A13* or LOGIC “1”***		D10	A8	
B11	RD/$\overline{\text{WR}}$		D11	$\overline{\text{MCRST}}$	
B12	$\overline{\text{SELECT}}$		D12	NC	
B13	NC		D13	NC	
B14	TX_INH_B		D14	$\overline{\text{SNGL\_END}}$ / NC	
B15	$\overline{\text{READY}}$		D15	NC	
B16	NC		D16	D15	
B17	NC		D17	TRANS/$\overline{\text{BUFF}}$	
B18	NC		D18	$\overline{\text{INT}}$	

* Applicable for 64K RAM option.
** Applicable for 4K RAM option.
*** See Thermal Management Section for important user information.

TABLE 68. MICRO-ACE-TE BU-64743B8/C / BU-648X3B(R)8/C/D (+3.3V BGA PACKAGE) PINOUTS (CONT.)					
BALL	**SIGNAL**	**NOTES**	**BALL**	**SIGNAL**	**NOTES**
E1	TX/RX-A		G1	$\overline{\text{TX/RX-A}}$	
E2	TX/RX-A		G2	$\overline{\text{TX/RX-A}}$	
E3	GND_XCVR/THERMAL***		G3	GND_XCVR/THERMAL***	
E4	GND_XCVR/THERMAL***		G4	GND_XCVR/THERMAL***	
E5	GND_XCVR/THERMAL***		G5	GND_XCVR/THERMAL***	
E6	A11		G6	NC	
E7	TXINH_IN_A	connect to ball E8	G7	$\overline{\text{RXDATA\_OUT\_A}}$	connect to ball G8
E8	TXINH_OUT_A	connect to ball E7	G8	$\overline{\text{RXDATA\_IN\_A}}$	connect to ball G7
E9	A3		G9	NC	
E10	GND_LOGIC		G10	GND_LOGIC	
E11	GND_LOGIC		G11	GND_LOGIC	
E12	GND_LOGIC		G12	GND_LOGIC	
E13	NC		G13	NC	
E14	NC		G14	NC	
E15	NC		G15	NC	
E16	D13		G16	NC	
E17	D11		G17	D3	
E18	D10		G18	D8	
F1	GND_XCVR/THERMAL***		H1	$\overline{\text{TX/RX-A}}$	
F2	GND_XCVR/THERMAL***		H2	$\overline{\text{TX/RX-A}}$	
F3	GND_XCVR/THERMAL***		H3	NC	
F4	GND_XCVR/THERMAL***		H4	NC	
F5	GND_XCVR/THERMAL***		H5	NC	
F6	NC		H6	NC	
F7	LOGIC 1* or UPADDREN**		H7	RXDATA_OUT_A	connect to ball H8
F8	A0		H8	RXDATA_IN_A	connect to ball H7
F9	NC		H9	NC	
F10	GND_LOGIC		H10	GND_LOGIC	
F11	GND_LOGIC		H11	GND_LOGIC	
F12	GND_LOGIC		H12	GND_LOGIC	
F13	NC		H13	NC	
F14	TAG_CLK		H14	NC	
F15	D14		H15	NC	
F16	D9		H16	NC	
F17	D7		H17	D5	
F18	D12		H18	D4	

* Applicable for 64K RAM option.
** Applicable for 4K RAM option.
*** See Thermal Management Section for important user information.

TABLE 68. MICRO-ACE-TE BU-64743B8/C / BU-648X3B(R)8/C/D (+3.3V BGA PACKAGE) PINOUTS (CONT.)					
BALL	**SIGNAL**	**NOTES**	**BALL**	**SIGNAL**	**NOTES**
J1	+3.3V_XCVR		L1	TX/RX-B	
J2	+3.3V_XCVR		L2	TX/RX-B	
J3	+3.3V_XCVR		L3	GND_XCVR/THERMAL***	
J4	+3.3V_XCVR		L4	GND_XCVR/THERMAL***	
J5	+3.3V_XCVR		L5	GND_XCVR/THERMAL***	
J6	NC		L6	NC	
J7	NC		L7	TXDATA_IN_B	connect to ball L8
J8	NC		L8	TXDATA_OUT_B	connect to ball L7
J9	NC		L9	NC	
J10	NC		L10	NC	
J11	NC		L11	NC	
J12	NC		L12	NC	
J13	NC		L13	NC	
J14	NC		L14	RSTBITEN	
J15	RTAD4		L15	NC	
J16	RTAD2		L16	+3.3V_LOGIC	
J17	D2		L17	+3.3V_LOGIC	
J18	D6		L18	RTAD1	
K1	+3.3V_XCVR		M1	TX/RX-B	
K2	+3.3V_XCVR		M2	TX/RX-B	
K3	+3.3V_XCVR		M3	GND_XCVR/THERMAL***	
K4	+3.3V_XCVR		M4	GND_XCVR/THERMAL***	
K5	+3.3V_XCVR		M5	GND_XCVR/THERMAL***	
K6	NC		M6	NC	
K7	NC		M7	$\overline{\text{TXDATA\_IN\_B}}$	connect to ball M8
K8	NC		M8	$\overline{\text{TXDATA\_OUT\_B}}$	connect to ball M7
K9	NC		M9	NC	
K10	NC		M10	NC	
K11	NC		M11	NC	
K12	NC		M12	NC	
K13	NC		M13	NC	
K14	NC		M14	NC	
K15	NC		M15	NC	
K16	D1		M16	+3.3V_LOGIC	
K17	D0		M17	+3.3V_LOGIC	
K18	RTADP		M18	RTAD3	

* Applicable for 64K RAM option.
** Applicable for 4K RAM option.
*** See Thermal Management Section for important user information.

TABLE 68. MICRO-ACE-TE BU-64743B8/C / BU-648X3B(R)8/C/D (+3.3V BGA PACKAGE) PINOUTS (CONT.)					
BALL	**SIGNAL**	**NOTES**	**BALL**	**SIGNAL**	**NOTES**
N1	GND_XCVR/THERMAL***		R1	$\overline{\text{TX/RX-B}}$	
N2	GND_XCVR/THERMAL***		R2	$\overline{\text{TX/RX-B}}$	
N3	GND_XCVR/THERMAL***		R3	NC	
N4	GND_XCVR/THERMAL***		R4	SLEEPIN	
N5	GND_XCVR/THERMAL***		R5	NC	
N6	NC		R6	+3.3V_LOGIC	
N7	TXINH_IN_B	connect to ball N8	R7	+3.3V_LOGIC	
N8	TXINH_OUT_B	connect to ball N7	R8	$\overline{\text{SSFLAG}}$/EXT_TRIG	
N9	NC		R9	RXDATA_OUT_B	connect to ball R10
N10	NC		R10	RXDATA_IN_B	connect to ball R9
N11	NC		R11	GND_LOGIC	
N12	+3.3V_LOGIC		R12	GND_LOGIC	
N13	+3.3V_LOGIC		R13	GND_LOGIC	
N14	NC		R14	NC	
N15	NC		R15	NC	
N16	NC		R16	NC	
N17	TRIG_SEL/$\overline{\text{MEMENA\_IN}}$		R17	16/$\overline{8}$ / $\overline{\text{DTREQ}}$	
N18	RTAD0		R18	$\overline{\text{MSTCLR}}$	
P1	$\overline{\text{TX/RX-B}}$		T1	NC	
P2	$\overline{\text{TX/RX-B}}$		T2	NC	
P3	GND_XCVR/THERMAL***		T3	NC	
P4	GND_XCVR/THERMAL***		T4	NC	
P5	GND_XCVR/THERMAL***		T5	NC/NSLOW_A/B ****	
P6	NC		T6	+3.3V_LOGIC	
P7	NC		T7	+3.3V_LOGIC	
P8	NC		T8	$\overline{\text{ZEROWAIT}}$/$\overline{\text{MEMWR}}$	
P9	$\overline{\text{RXDATA\_OUT\_B}}$	connect to ball P10	T9	NC	
P10	$\overline{\text{RXDATA\_IN\_B}}$	connect to ball P9	T10	CLOCK_IN	
P11	NC		T11	GND_LOGIC	
P12	+3.3V_LOGIC		T12	GND_LOGIC	
P13	+3.3V_LOGIC		T13	GND_LOGIC	
P14	NC		T14	NC	
P15	NC		T15	NC	
P16	NC		T16	NC	
P17	$\overline{\text{INCMD}}$		T17	NC	
P18	RT_AD_LAT		T18	NC	

* Applicable for 64K RAM option.
** Applicable for 4K RAM option.
*** See Thermal Management Section for important user information.
****NSLOW_A/B is applicable for McAir option, otherwise NC.

TABLE 68. MICRO-ACE-TE BU-64743B8/C / BU-648X3B(R)8/C/D (+3.3V BGA PACKAGE) PINOUTS (CONT.)					
BALL	**SIGNAL**	**NOTES**	**BALL**	**SIGNAL**	**NOTES**
U1	NC		V1	NC	
U2	NC		V2	NC	
U3	NC		V3	NC	
U4	+3.3V_XCVR		V4	+3.3V_XCVR	
U5	+3.3V_XCVR		V5	+3.3V_XCVR	
U6	+3.3V_LOGIC		V6	+3.3V_LOGIC	
U7	+3.3V_LOGIC		V7	+3.3V_LOGIC	
U8	A1		V8	POL_SEL/$\overline{\text{DTACK}}$	
U9	NC		V9	A6	
U10	ADDR_LAT/$\overline{\text{MEMOE}}$		V10	NC	
U11	GND_LOGIC		V11	NC	
U12	GND_LOGIC		V12	NC	
U13	GND_LOGIC		V13	NC	
U14	NC		V14	NC	
U15	NC		V15	NC	
U16	NC		V16	NC	
U17	NC		V17	NC	
U18	NC		V18	NC	

* Applicable for 64K RAM option.
** Applicable for 4K RAM option.
*** See Thermal Management Section for important user information.

TABLE 69. MICRO-ACE-TE BU-648X0B(R)3/4 (+5.0V BGA PACKAGE) PINOUTS					
BALL	**SIGNAL**	**NOTES**	**BALL**	**SIGNAL**	**NOTES**
A1	NC		C1	NC	
A2	NC		C2	NC	
A3	NC		C3	NC	
A4	TXINH_IN_A	connect to ball A5	C4	$\overline{\text{TXDATA\_IN\_A}}$	connect to ball C5
A5	TXINH_OUT_A	connect to ball A4	C5	$\overline{\text{TXDATA\_OUT\_A}}$	connect to ball C4
A6	NC		C6	A05	
A7	+5.0V/+3.3V_LOGIC		C7	A07	
A8	A10		C8	TXDATA_IN_A	connect to ball B8
A9	A12* or A12/$\overline{\text{RTBOOT}}$**		C9	A08	
A10	A14* or A14/CLK_SEL_0**		C10	A15* or A15/CLK_SEL_1**	
A11	RD/$\overline{\text{WR}}$		C11	MEM/$\overline{\text{REG}}$	
A12	$\overline{\text{STRBD}}$		C12	LOGIC “1”* or UPADDREN**	
A13	$\overline{\text{VDD\_LOW}}$		C13	TX_INH_B	
A14	TX_INH_A		C14	$\overline{\text{IOEN}}$	
A15	$\overline{\text{SNGL\_END}}$		C15	$\overline{\text{READYD}}$	
A16	NC		C16	NC	
A17	NC		C17	NC	
A18	NC		C18	NC	
B1	NC		D1	TX/RX-A	
B2	NC		D2	TX/RX-A	
B3	NC		D3	GND_XCVR/THERMAL***	
B4	NC		D4	GND_XCVR/THERMAL***	
B5	NC		D5	GND_XCVR/THERMAL***	
B6	NC		D6	A03	
B7	A09		D7	A06	
B8	TXDATA_OUT_A	connect to ball C8	D8	A04	
B9	A11		D9	NC	
B10	A13* or A13 / LOGIC “1”**		D10	$\overline{\text{RXDATA\_IN\_A}}$	connect to ball E10
B11	$\overline{\text{MSTCLR}}$		D11	NC	
B12	$\overline{\text{SELECT}}$		D12	NC	
B13	$\overline{\text{MCRST}}$		D13	NC	
B14	NC		D14	NC	
B15	NC		D15	D15	
B16	NC		D16	TRANS/$\overline{\text{BUFF}}$	
B17	NC		D17	$\overline{\text{INT}}$	
B18	NC		D18	TAG_CLK	

* Applicable for 64K RAM option.
** Applicable for 4K RAM option.
*** See Thermal Management Section for important user information.

TABLE 69. MICRO-ACE-TE BU-648X0B(R)3/4 (+5.0V BGA PACKAGE) PINOUTS (CONT.)					
BALL	**SIGNAL**	**NOTES**	**BALL**	**SIGNAL**	**NOTES**
E1	TX/RX-A		G1	$\overline{\text{TX/RX-A}}$	
E2	GND_XCVR/THERMAL***		G2	GND_XCVR/THERMAL***	
E3	GND_XCVR/THERMAL***		G3	GND_XCVR/THERMAL***	
E4	GND_XCVR/THERMAL***		G4	GND_XCVR/THERMAL***	
E5	GND_XCVR/THERMAL***		G5	GND_XCVR/THERMAL***	
E6	NC		G6	NC	
E7	A01		G7	NC	
E8	A02		G8	NC	
E9	RXDATA_IN_A	connect to ball F9	G9	NC	
E10	$\overline{\text{RXDATA\_OUT\_A}}$	connect to ball D10	G10	NC	
E11	NC		G11	NC	
E12	GND_LOGIC		G12	GND_LOGIC	
E13	GND_LOGIC		G13	GND_LOGIC	
E14	GND_LOGIC		G14	GND_LOGIC	
E15	D11		G15	D03	
E16	D13		G16	D05	
E17	D14		G17	D04	
E18	D12		G18	D06	
F1	+5.0V_XCVR		H1	$\overline{\text{TX/RX-A}}$	
F2	+5.0V_XCVR		H2	$\overline{\text{TX/RX-A}}$	
F3	GND_XCVR/THERMAL***		H3	GND_XCVR/THERMAL***	
F4	GND_XCVR/THERMAL***		H4	GND_XCVR/THERMAL***	
F5	GND_XCVR/THERMAL***		H5	GND_XCVR/THERMAL***	
F6	NC		H6	NC	
F7	NC		H7	NC	
F8	NC		H8	NC	
F9	RXDATA_OUT_A	connect to ball E9	H9	NC	
F10	A00		H10	NC	
F11	NC		H11	NC	
F12	GND_LOGIC		H12	GND_LOGIC	
F13	GND_LOGIC		H13	GND_LOGIC	
F14	GND_LOGIC		H14	GND_LOGIC	
F15	D09		H15	NC	
F16	D10		H16	$\overline{\text{INCMD}}$	
F17	D07		H17	D00	
F18	D08		H18	D02	

* Applicable for 64K RAM option.
** Applicable for 4K RAM option.
*** See Thermal Management Section for important user information.

TABLE 69. MICRO-ACE-TE BU-648X0B(R)3/4 (+5.0V BGA PACKAGE) PINOUTS (CONT.)					
BALL	**SIGNAL**	**NOTES**	**BALL**	**SIGNAL**	**NOTES**
J1	NC		L1	+5.0V/+3.3V_LOGIC	
J2	NC		L2	+5.0V/+3.3V_LOGIC	
J3	NC		L3	NC	
J4	NC		L4	NC	
J5	NC		L5	NC	
J6	NC		L6	NC	
J7	MSB/LSB / $\overline{\text{DTGRT}}$		L7	NC	
J8	$\overline{\text{SSFLAG}}$/EXT_TRIG		L8	NC	
J9	NC		L9	ADDR_LAT/$\overline{\text{MEMOE}}$	
J10	NC		L10	16/$\overline{8}$ / $\overline{\text{DTREQ}}$	
J11	NC		L11	TRIG_SEL/$\overline{\text{MEMENA\_IN}}$	
J12	NC		L12	NC	
J13	NC		L13	NC	
J14	NC		L14	NC	
J15	NC		L15	+5.0V/+3.3V_LOGIC	
J16	RTAD4		L16	+5.0V/+3.3V_LOGIC	
J17	D01		L17	RTAD2	
J18	RTADP		L18	RT_AD_LAT	
K1	NC		M1	NC	
K2	NC		M2	NC	
K3	NC		M3	+5.0V/+3.3V_LOGIC	
K4	NC		M4	NC	
K5	NC		M5	NC	
K6	NC		M6	NC	
K7	NC		M7	NC	
K8	NC		M8	NC	
K9	NC		M9	CLOCK_IN	
K10	NC		M10	$\overline{\text{ZEROWAIT}}$/$\overline{\text{MEMWR}}$	
K11	NC		M11	NC	
K12	NC		M12	$\overline{\text{TXDATA\_OUT\_B}}$	connect to ball N12
K13	NC		M13	$\overline{\text{RXDATA\_IN\_B}}$	connect to ball M14
K14	NC		M14	$\overline{\text{RXDATA\_OUT\_B}}$	connect to ball M13
K15	NC		M15	NC	
K16	RTAD0		M16	NC	
K17	RTAD3		M17	NC	
K18	RTAD1		M18	RSTBITEN	

* Applicable for 64K RAM option.
** Applicable for 4K RAM option.
*** See Thermal Management Section for important user information.

TABLE 69. MICRO-ACE-TE BU-648X0B(R)3/4 (+5.0V BGA PACKAGE) PINOUTS (CONT.)					
BALL	**SIGNAL**	**NOTES**	**BALL**	**SIGNAL**	**NOTES**
N1	NC		R1	NC	
N2	NC		R2	NC	
N3	NC		R3	NC	
N4	NC		R4	+5.0V_RAM* or NC**	
N5	NC		R5	NC	
N6	NC		R6	NC	
N7	NC		R7	NC	
N8	NC		R8	TXINH_OUT_B	connect to ball T8
N9	POL_SEL/$\overline{\text{DTACK}}$		R9	+5.0V/+3.3V_LOGIC	
N10	NC		R10	TXDATA_IN_B	connect to ball P10
N11	NC		R11	GND_XCVR/THERMAL***	
N12	$\overline{\text{TXDATA\_IN\_B}}$	connect to ball M12	R12	GND_XCVR/THERMAL***	
N13	RXDATA_IN_B	connect to ball N14	R13	GND_XCVR/THERMAL***	
N14	RXDATA_OUT_B	connect to ball N13	R14	GND_XCVR/THERMAL***	
N15	NC		R15	GND_XCVR/THERMAL***	
N16	NC		R16	NC	
N17	NC		R17	NC	
N18	NC		R18	NC	
P1	NC		T1	NC	
P2	NC		T2	NC	
P3	NC		T3	NC	
P4	+5.0V_RAM* or NC**		T4	NC	
P5	NC		T5	NC	
P6	NC		T6	NC	
P7	+5.0V/+3.3V_LOGIC		T7	NC	
P8	NC		T8	TXINH_IN_B	connect to ball R8
P9	+5.0V/+3.3V_LOGIC		T9	NC	
P10	TXDATA_OUT_B	connect to ball R10	T10	NC	
P11	GND_XCVR/THERMAL***		T11	GND_XCVR/THERMAL***	
P12	GND_XCVR/THERMAL***		T12	GND_XCVR/THERMAL***	
P13	GND_XCVR/THERMAL***		T13	GND_XCVR/THERMAL***	
P14	GND_XCVR/THERMAL***		T14	GND_XCVR/THERMAL***	
P15	GND_XCVR/THERMAL***		T15	GND_XCVR/THERMAL***	
P16	NC		T16	NC	
P17	NC		T17	NC	
P18	NC		T18	NC	

* Applicable for 64K RAM option.
** Applicable for 4K RAM option.
*** See Thermal Management Section for important user information.

TABLE 69. MICRO-ACE-TE BU-648X0B(R)3/4 (+5.0V BGA PACKAGE) PINOUTS (CONT.)		
BALL	**SIGNAL**	**NOTES**
U1	NC	
U2	NC	
U3	NC	
U4	NC	
U5	NC	
U6	NC	
U7	NC	
U8	NC	
U9	NC	
U10	NC	
U11	TX/RX-B	
U12	GND_XCVR/THERMAL***	
U13	+5.0V_XCVR	
U14	GND_XCVR/THERMAL***	
U15	$\overline{\text{TX/RX-B}}$	
U16	NC	
U17	NC	
U18	NC	
V1	NC	
V2	NC	
V3	NC	
V4	NC	
V5	NC	
V6	NC	
V7	NC	
V8	+5.0V/+3.3V_LOGIC	
V9	NC	
V10	NC	
V11	TX/RX-B	
V12	TX/RX-B	
V13	+5.0V_XCVR	
V14	$\overline{\text{TX/RX-B}}$	
V15	$\overline{\text{TX/RX-B}}$	
V16	NC	
V17	NC	
V18	NC	

* Applicable for 64K RAM option.
** Applicable for 4K RAM option.
*** See Thermal Management Section for important user information.

(R)TABLE 70. MICRO-ACE-TE BU-64863B8-600 (BGA PACKAGE) "DAISY CHAIN" MECHANICAL SAMPLE CONNECTIONS				
BALL PAIRS WIRED TOGETHER	**BALL PAIRS WIRED TOGETHER**	**BALL PAIRS WIRED TOGETHER**	**BALL PAIRS WIRED TOGETHER**	**BALL PAIRS WIRED TOGETHER**
A1-A2	E1-E2	J1-J2	N1-N2	U1-U2
A3-A4	E3-E4	J3-J4	N3-N4	U3-U4
A5-A6	E5-E6	J5-J6	N5-N6	U5-U6
A7-A8	E7-E8	J7-J8	N7-N8	U7-U8
A9-A10	E9-E10	J9-J10	N9-N10	U9-U10
A11-A12	E11-E12	J11-J12	N11-N12	U11-U12
A13-A14	E13-E14	J13-J14	N13-N14	U13-U14
A15-A16	E15-E16	J15-J16	N15-N16	U15-U16
A17-A18	E17-E18	J17-J18	N17-N18	U17-U18
B1-B2	F1-F2	K1-K2	P1-P2	V1-V2
B3-B4	F3-F4	K3-K4	P3-P4	V3-V4
B5-B6	F5-F6	K5-K6	P5-P6	V5-V6
B7-B8	F7-F8	K7-K8	P7-P8	V7-V8
B9-B10	F9-F10	K9-K10	P9-P10	V9-V10
B11-B12	F11-F12	K11-K12	P11-P12	V11-V12
B13-B14	F13-F14	K13-K14	P13-P14	V13-V14
B15-B16	F15-F16	K15-K16	P15-P16	V15-V16
B17-B18	F17-F18	K17-K18	P17-P18	V17-V18
C1-C2	G1-G2	L1-L2	R1-R2	
C3-C4	G3-G4	L3-L4	R3-R4	
C5-C6	G5-G6	L5-L6	R5-R6	
C7-C8	G7-G8	L7-L8	R7-R8	
C9-C10	G9-G10	L9-L10	R9-R10	
C11-C12	G11-G12	L11-L12	R11-R12	
C13-C14	G13-G14	L13-L14	R13-R14	
C15-C16	G15-G16	L15-L16	R15-R16	
C17-C18	G17-G18	L17-L18	R17-R18	
D1-D2	H1-H2	M1-M2	T1-T2	
D3-D4	H3-H4	M3-M4	T3-T4	
D5-D6	H5-H6	M5-M6	T5-T6	
D7-D8	H7-H8	M7-M8	T7-T8	
D9-D10	H9-H10	M9-M10	T9-T10	
D11-D12	H11-H12	M11-M12	T11-T12	
D13-D14	H13-H14	M13-M14	T13-T14	
D15-D16	H15-H16	M15-M16	T15-T16	
D17-D18	H17-H18	M17-M18	T17-T18	

TABLE 71. BU-64863E8 EVALUATION BOARD PINOUTS MADE FROM 80-PIN MINI-ACE MARK3 BU-64863G8 BC/RT/MT 64K RAM					
P1 PIN #	**DEVICE PIN #**	**FUNCTION**	**P2 PIN #**	**DEVICE PIN #**	**FUNCTION**
1	2	A10	1	-	NC
2	1	A11	2	-	NC
3	6	MEM/$\overline{\text{REG}}$	3	-	$\overline{\text{STUB\_TX/RX\_B}}$
4	7	A08	4	-	$\overline{\text{STUB\_TX/RX\_B}}$
5	18	A00	5	22, 31, 50, 70, 79	GND
6	13	A03	6	22, 31, 50, 70, 79	GND
7	19	A02	7	-	STUB_TX/RX_B
8	12	A07	8	-	STUB_TX/RX_B
9	80	A14	9	-	NC
10	22, 31, 50, 70, 79	GND	10	-	NC
11	22, 31, 50, 70, 79	GND	11	-	+3.3V_XFMR_CT
12	22, 31, 50, 70, 79	GND	12	-	+3.3V_XFMR_CT
13	77	A13	13	10	+3.3V_XCVR
14	78	A04	14	10	+3.3V_XCVR
15	75	A09	15	-	NC
16	76	A12	16	-	NC
17	73	A15	17	-	$\overline{\text{STUB\_TX/RX\_A}}$
18	74	A05	18	-	$\overline{\text{STUB\_TX/RX\_A}}$
19	71	RD/$\overline{\text{WR}}$	19	22, 31, 50, 70, 79	GND
20	72	MSB/LSB / $\overline{\text{DTGRT}}$	20	22, 31, 50, 70, 79	GND
21	30, 51, 69	+3.3V_LOGIC	21	-	STUB_TX/RX_A
22	30, 51, 69	+3.3V_LOGIC	22	-	STUB_TX/RX_A
23	68	$\overline{\text{STRBD}}$	23	-	NC
24	-	NC	24	-	NC
25	66	$\overline{\text{SELECT}}$			
26	67	TX_INH_B			
27	64	$\overline{\text{IOEN}}$			
28	65	TX_INH_A			
29	62	$\overline{\text{READYD}}$			
30	63	$\overline{\text{INT}}$			
31	-	NC			
32	61	TRANS/$\overline{\text{BUFF}}$			

TABLE 71. BU-64863E8 EVALUATION BOARD PINOUTS (CONT.) MADE FROM 80-PIN MINI-ACE MARK3 BU-64863G8 BC/RT/MT 64K RAM					
P3 PIN #	DEVICE PIN #	FUNCTION	P4 PIN #	DEVICE PIN #	FUNCTION
1	14	SLEEPIN	1	41	D06
2	20	ADDR_LAT/$\overline{\text{MEMOE}}$	2	-	NC
3	22, 31, 50, 70, 79	GND	3	43	D04
4	-	NC	4	42	D01
5	30, 51, 69	+3.3V_LOGIC	5	45	RTAD1
6	30, 51, 69	+3.3V_LOGIC	6	44	RTADP
7	22, 31, 50, 70, 79	GND	7	47	D02
8	22, 31, 50, 70, 79	GND	8	46	D00
9	22, 31, 50, 70, 79	GND	9	49	D05
10	23	TAG_CLK	10	48	D03
11	24	RTAD2	11	22, 31, 50, 70, 79	GND
12	22, 31, 50, 70, 79	GND	12	22, 31, 50, 70, 79	GND
13	25	$\overline{\text{MSTCLR}}$	13	30, 51, 69	+3.3V_LOGIC
14	26	CLOCK_IN	14	30, 51, 69	+3.3V_LOGIC
15	22, 31, 50, 70, 79	GND	15	52	D08
16	27	A06	16	53	D07
17	28	ZEROWAIT/$\overline{\text{MEMWR}}$	17	54	D13
18	29	16/$\overline{8}$ / $\overline{\text{DTREQ}}$	18	55	D12
19	30, 51, 69	+3.3V_LOGIC	19	56	D14
20	30, 51, 69	+3.3V_LOGIC	20	57	D09
21	-	NC	21	58	D11
22	-	NC	22	59	D15
23	32	$\overline{\text{INCMD}}$/$\overline{\text{MCRST}}$	23	60	D10
24	33	A01	24	-	NC
25	34	TRIG_SEL/$\overline{\text{MEMENA\_IN}}$			
26	35	POL_SEL/$\overline{\text{DTACK}}$			
27	36	RT_AD_LAT			
28	37	$\overline{\text{SSFLAG}}$/EXT_TRIG			
29	38	RTAD0			
30	39	RTAD3			
31	-	NC			
32	40	RTAD4			

TABLE 72. BU-61860E3 EVALUATION BOARD PINOUTS MADE FROM 128-BALL µ-ACE (MICRO-ACE) BU-61860B3 BC/RT/MT 64K RAM					
P1 PIN #	**DEVICE PIN #**	**FUNCTION**	**P2 PIN #**	**DEVICE PIN #**	**FUNCTION**
1	A6	A10	1	-	$\overline{\text{DIR\_TX/RX\_B}}$
2	B7	A11	2	-	$\overline{\text{DIR\_TX/RX\_B}}$
3	B13	MEM/REG	3	-	$\overline{\text{STUB\_TX/RX\_B}}$
4	B5	A08	4	-	$\overline{\text{STUB\_TX/RX\_B}}$
5	A1	A00	5	A9,B9,C17,C18,E2,F2,G2,K17, K18,U4,U9,U13,U14,U15,V1,V4	GND
6	B3	A03			
7	A2	A02	6	A9,B9,C17,C18,E2,F2,G2,K17, K18,U4,U9,U13,U14,U15,V1,V4	GND
8	A5	A07			
9	B10	A14	7	-	STUB_TX/RX_B
10	A9,B9,C17,C18,E2,F2,G2,K17, K18,U4,U9,U13,U14,U15,V1,V4	GND	8	-	STUB_TX/RX_B
			9	-	DIR_TX/RX_B
11	A9,B9,C17,C18,E2,F2,G2,K17, K18,U4,U9,U13,U14,U15,V1,V4	GND	10	-	DIR_TX/RX_B
			11	-	NC
12	A9,B9,C17,C18,E2,F2,G2,K17, K18,U4,U9,U13,U14,U15,V1,V4	GND	12	-	NC
			13	E1,F1,G1	+5.0V Vcc CH A
13	A10	A13	14	E1,F1,G1	+5.0V Vcc CH A
14	A3	A04	15	-	$\overline{\text{DIR\_TX/RX\_A}}$
15	B6	A09	16	-	$\overline{\text{DIR\_TX/RX\_A}}$
16	A7	A12	17	-	$\overline{\text{STUB\_TX/RX\_A}}$
17	A11	A15	18		$\overline{\text{STUB\_TX/RX\_A}}$
18	B4	A05	19	A9,B9,C17,C18,E2,F2,G2,K17, K18,U4,U9,U13,U14,U15,V1,V4	GND
19	A12	RD/$\overline{\text{WR}}$			
20	U6	MSB/LSB / $\overline{\text{DTGRT}}$	20	A9,B9,C17,C18,E2,F2,G2,K17, K18,U4,U9,U13,U14,U15,V1,V4	GND
21	A8,A16,B8,B16,L1,L2,L17,L18, U3,V3	+5.0V_LOGIC			
			21	-	STUB_TX/RX_A
22	A8,A16,B8,B16,L1,L2,L17,L18, U3,V3	+5.0V_LOGIC	22	-	STUB_TX/RX_A
			23	-	DIR_TX/RX_A
23	B14	$\overline{\text{STRBD}}$	24	-	DIR_TX/RX_A
24	-	NC			
25	B12	$\overline{\text{SELECT}}$			
26	A15	TX_INH_B			
27	A17	$\overline{\text{IOEN}}$			
28	A14	TX_INH_A			
29	B15	$\overline{\text{READYD}}$			
30	A18	$\overline{\text{INT}}$			
31	B18	TAG_CLK			
32	B17	TRANS/$\overline{\text{BUFF}}$			

TABLE 72. BU-61860E3 EVALUATION BOARD PINOUTS (CONT.) MADE FROM 128-BALL µ-ACE (MICRO-ACE) BU-61860B3 BC/RT/MT 64K RAM					
P3 PIN #	**DEVICE PIN #**	**FUNCTION**	**P4 PIN #**	**DEVICE PIN #**	**FUNCTION**
1	N2	UPADDREN	1	J18	D06
2	V8	ADDR_LAT/$\overline{\text{MEMOE}}$	2	P17	RSTBITEN
3	A9,B9,C17,C18,E2,F2,G2,K17, K18,U4,U9,U13,U14,U15,V1,V4	GND	3	M18	D04
			4	M17	D01
4	V2	$\overline{\text{VDD\_LOW}}$	5	V18	RTAD1
5	A8,A16,B8,B16,L1,L2,L17,L18, U3,V3	+5.0V_LOGIC	6	T18	RTADP
			7	G18	D02
6	A8,A16,B8,B16,L1,L2,L17,L18, U3,V3	+5.0V_LOGIC	8	H18	D00
			9	H17	D05
7	A9,B9,C17,C18,E2,F2,G2,K17, K18,U4,U9,U13,U14,U15,V1,V4	GND	10	G17	D03
			11	A9,B9,C17,C18,E2,F2,G2,K17, K18,U4,U9,U13,U14,U15,V1,V4	GND
8	A9,B9,C17,C18,E2,F2,G2,K17, K18,U4,U9,U13,U14,U15,V1,V4	GND			
			12	A9,B9,C17,C18,E2,F2,G2,K17, K18,U4,U9,U13,U14,U15,V1,V4	GND
9	A9,B9,C17,C18,E2,F2,G2,K17, K18,U4,U9,U13,U14,U15,V1,V4	GND			
			13	A8,A16,B8,B16,L1,L2,L17,L18, U3,V3	+5.0V_LOGIC
10	-	NC			
11	U17	RTAD2	14	A8,A16,B8,B16,L1,L2,L17,L18, U3,V3	+5.0V_LOGIC
12	A9,B9,C17,C18,E2,F2,G2,K17, K18,U4,U9,U13,U14,U15,V1,V4	GND			
			15	F18	D08
13	B11	$\overline{\text{MSTCLR}}$	16	F17	D07
14	V9	CLOCK_IN	17	J17	D13
15	A9,B9,C17,C18,E2,F2,G2,K17, K18,U4,U9,U13,U14,U15,V1,V4	GND	18	E18	D12
			19	D18	D14
16	A4	A06	20	N18	D09
17	U8	$\overline{\text{ZEROWAIT}}$/$\overline{\text{MEMWR}}$	21	E17	D11
18	V7	16/$\overline{8}$ / $\overline{\text{DTREQ}}$	22	D17	D15
19	A8,A16,B8,B16,L1,L2,L17,L18, U3,V3	+5.0V_LOGIC	23	N17	D10
			24	A13	$\overline{\text{MCRST}}$
20	A8,A16,B8,B16,L1,L2,L17,L18, U3,V3	+5.0V_LOGIC			
21	V13,V14,V15	+5.0V Vcc CH B			
22	V13,V14,V15	+5.0V Vcc CH B			
23	M1	$\overline{\text{INCMD}}$			
24	B1	A01			
25	V6	TRIG_SEL/$\overline{\text{MEMENA\_IN}}$			
26	U7	POL_SEL/$\overline{\text{DTACK}}$			
27	P18	RT_AD_LAT			
28	T2	$\overline{\text{SSFLAG}}$/EXT_TRIG			
29	V17	RTAD0			
30	U18	RTAD3			
31	-	NC			
32	T17	RTAD4			

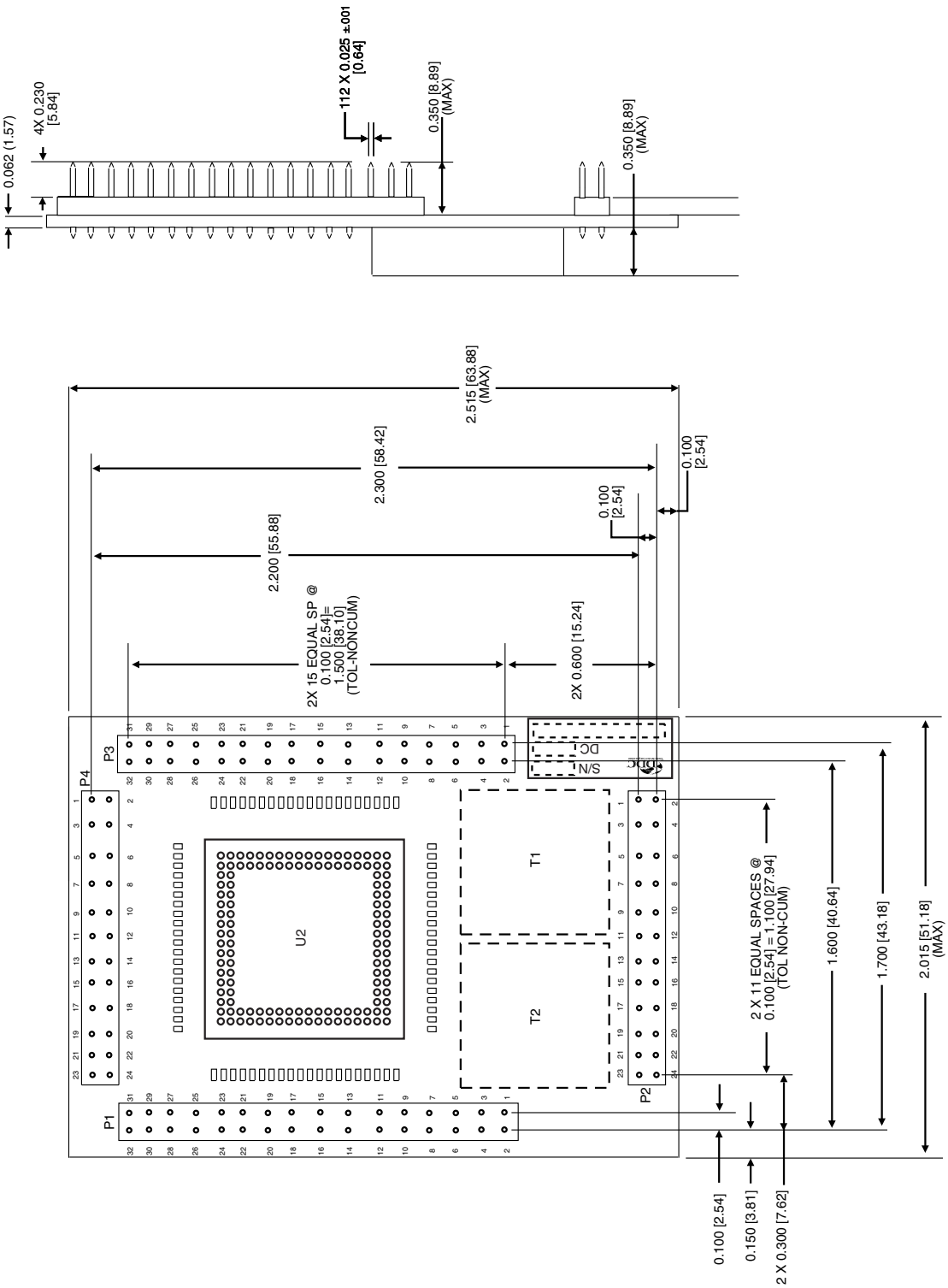


FIGURE 19. BU-61860E3 +5.0V µ-ACE (MICRO-ACE) & TRANSFORMER EVALUATION BOARD

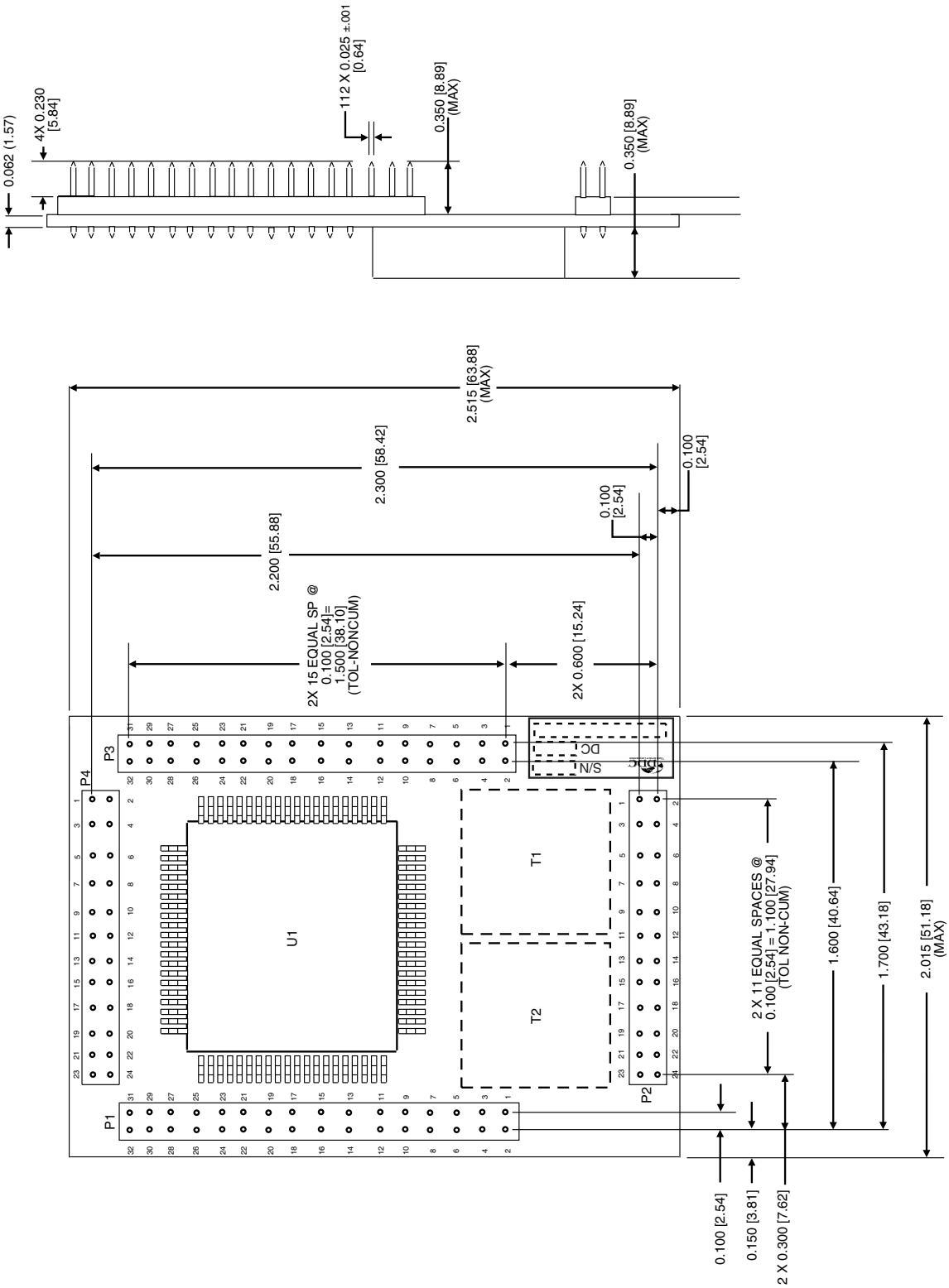
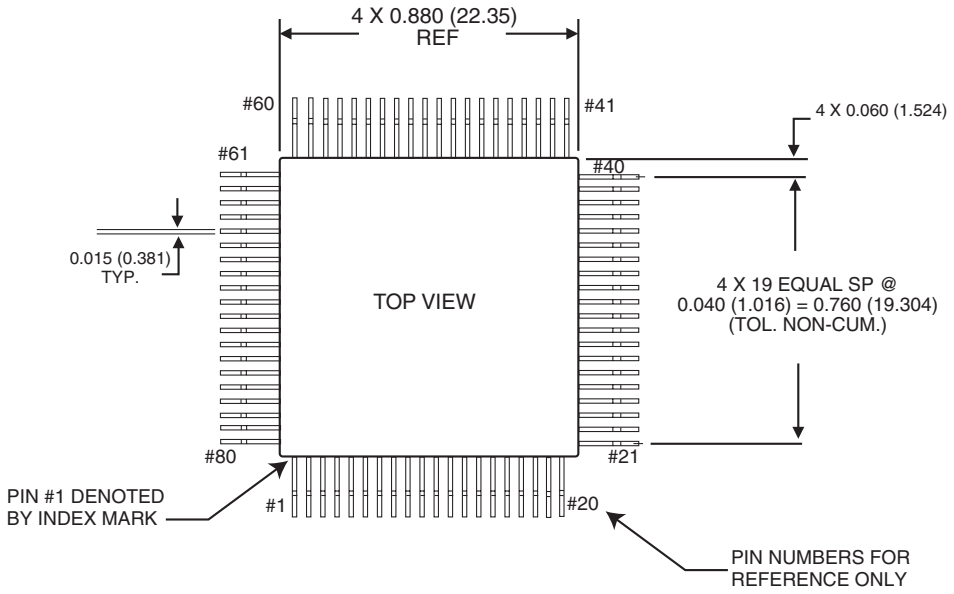
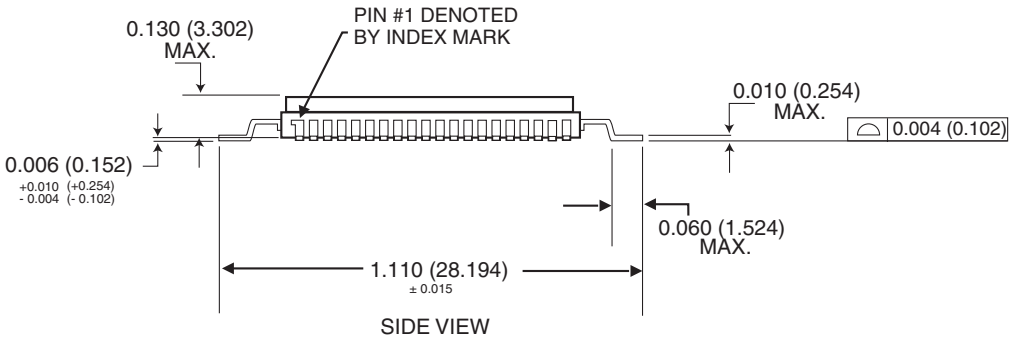


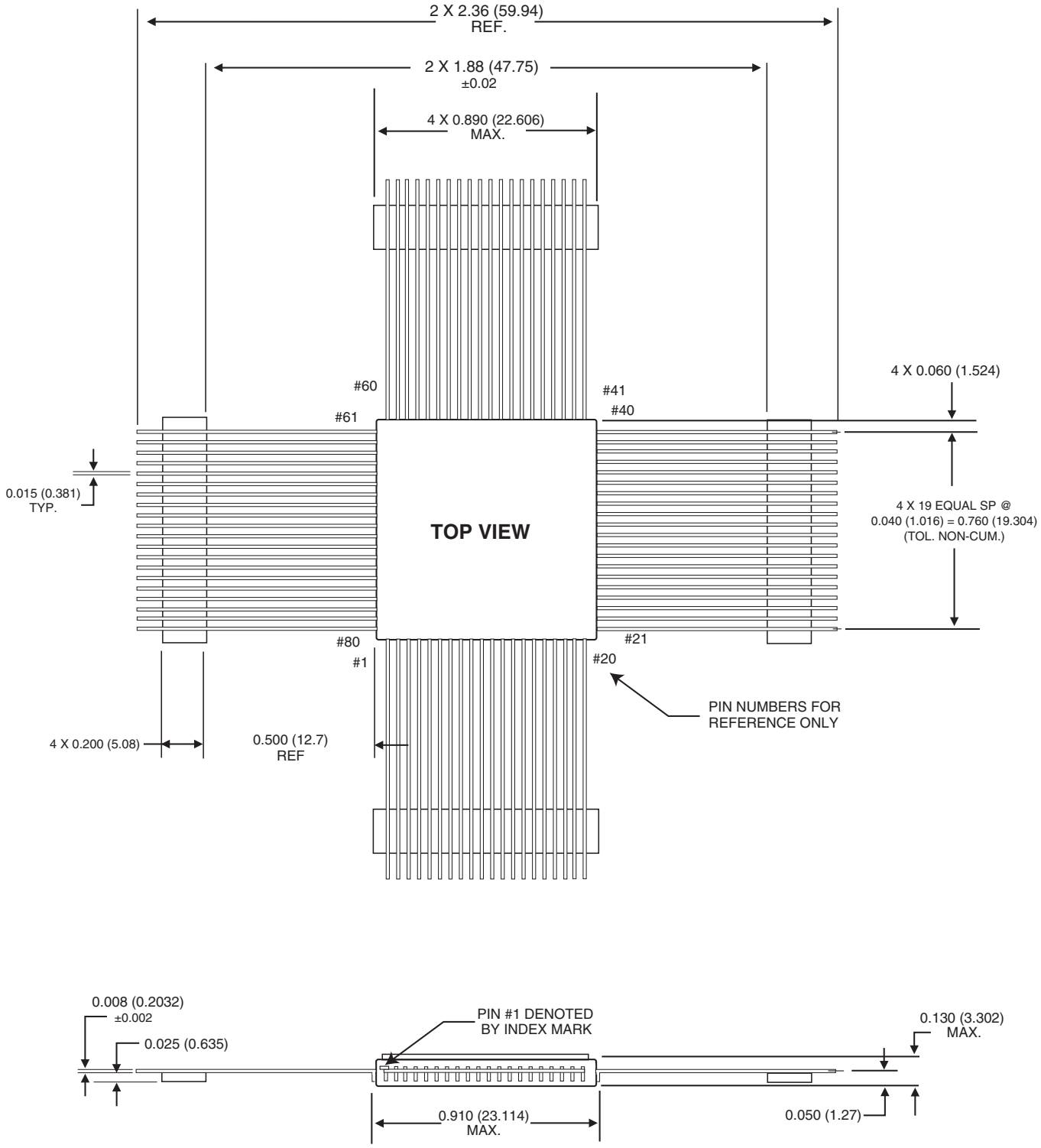
FIGURE 20. BU-64863E8 MINI-ACE MARK3 (+3.3 VOLT) & TRANSFORMER EVALUATION BOARD





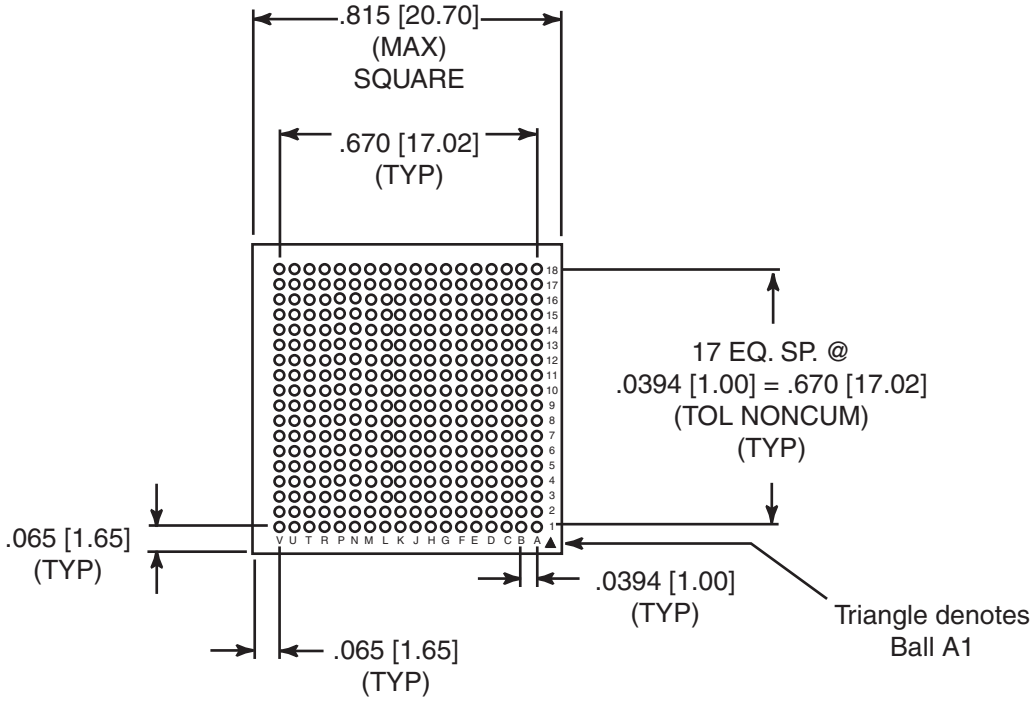
Notes:
1) Dimensions are in inches (mm).
2) Tolerances = ±0.005 inches unless otherwise specified.
3) Package Material: Alumina (AL203)
4) Lead Material: Kovar, Plated by 50µ in. minimum nickel under 60µ in. minimum gold.

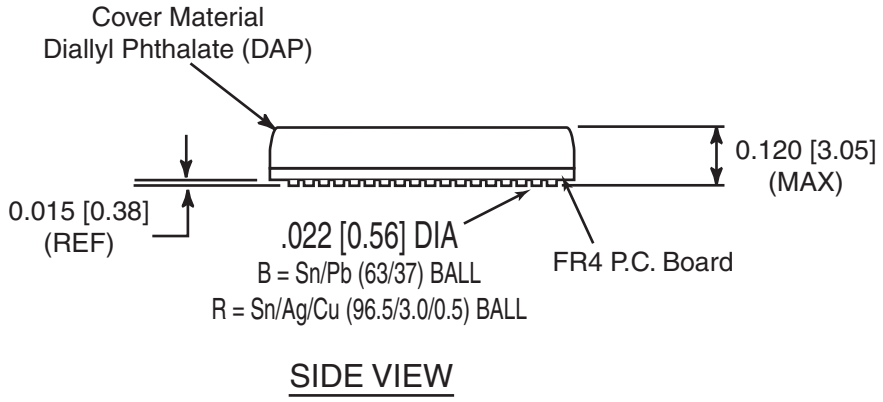
FIGURE 21. MECHANICAL OUTLINE DRAWING FOR MINI-ACE MARK3 80-PIN GULL WING PACKAGE



Notes:
1) Dimensions are in inches (mm).
2) Tolerances = ±0.005 inches unless otherwise specified.
3) Package Material: Alumina (AL203)
4) Lead Material: Kovar, Plated by 50µ in. minimum nickle under 60µ in. minimum gold.

FIGURE 22. MECHANICAL OUTLINE DRAWING FOR MINI-ACE MARK3 80-PIN FLAT PACKAGE





Notes:
1) Dimensions are in inches (mm).
2) Cover material: Diallyl Phthalate (DAP).
3) Base material: FR4 PC board.
4) Solder Ball Cluster to be centralized within ±.010 of outline dimensions.
5) The copper pads (324 places) on the bottom of the BGA package are .025” (0.635 mm) in diameter prior to processing. Final ball size is .022” (0.56 mm) after processing (typical).

FIGURE 23. MECHANICAL OUTLINE DRAWING FOR MICRO-ACE-TE BGA PACKAGE

ORDERING INFORMATION FOR MINI-ACE MARK3

BU-64XXXXX-XXXX

Supplemental Process Requirements:
- S = Pre-Cap Source Inspection
- L = 100% Pull Test
- Q = 100% Pull Test and Pre-Cap Source Inspection
- K = One Lot Date Code
- W = One Lot Date Code and Pre-Cap Source Inspection
- Y = One Lot Date Code and 100% Pull Test
- Z = One Lot Date Code, Pre-Cap Source Inspection and 100% Pull Test
- Blank = None of the Above

Test Criteria:
- 0 = Standard Testing
- 1 = X-Ray
- 2 = MIL-STD-1760 Amplitude Compliant (not available with Voltage/Transceiver Options 0 "Transceiverless" or 4/9/D "McAir compatible")
- 3 = MIL-STD-1760 and X-Ray

Process Requirements:
- 0 = Standard DDC practices, no Burn-In
- 1 = MIL-PRF-38534 Compliant (note 3)
- 2 = B (note 1)
- 3 = MIL-PRF-38534 Compliant (note 3) with PIND Testing
- 4 = MIL-PRF-38534 Compliant (note 3) with Solder Dip
- 5 = MIL-PRF-38534 Compliant (note 3) with PIND Testing and Solder Dip
- 6 = B (note 1) with PIND Testing
- 7 = B (note 1) with Solder Dip
- 8 = B (note 1) with PIND Testing and Solder Dip
- 9 = Standard DDC Processing with Solder Dip, no Burn-In (see table on next page)

Temperature Range (note 2)/Data Requirements:
- 1 = -55°C to +125°C
- 2 = -40°C to +85°C
- 3 = 0°C to +70°C
- 4 = -55°C to +125°C with Variables Test Data
- 5 = -40°C to +85°C with Variables Test Data
- 6 = Custom Part (Reserved)
- 7 = Custom Part (Reserved)
- 8 = 0°C to +70°C with Variables Test Data

Voltage/Transceiver Option:
- 0 = Transceiverless (contact factory for availability)
- 3 = +5.0 Volts rise/fall times = 100 to 300 ns (-1553B)
- 4 = +5.0 Volts rise/fall times = 200 to 300 ns (-1553B and McAir compatible. Not available with Test Criteria option 2 "MIL-STD-1760 Amplitude Compliant")
- 8 = +3.3 Volts rise/fall times = 100 to 300 ns (-1553B) (note 5) (Not available with Logic/RAM Voltage option 5 "+5.0 Volt".)
- 9 = +3.3 Volts rise/fall times = 200 to 300 ns (-1553B and McAir compatible. Not available with Test Criteria option 2 "MIL-STD-1760 Amplitude Compliant" or with Logic/RAM Voltage option 5 "+5.0 Volt".) (note 5)
- C = +3.3 Volts rise/fall times = 100 to 300 ns (-1553B) (note 6) (Not available with Logic/RAM Voltage option 5 "+5.0 Volt".)
- D = +3.3 Volts rise/fall times = 200 to 300 ns (-1553B and McAir compatible. Not available with Test Criteria option 2 "MIL-STD-1760 Amplitude Compliant" or with Logic/RAM Voltage option 5 "+5.0 Volt".) (note 6)

Package Type:
- F = 80-Lead Flat Pack
- G = 80-Lead "Gull Wing" (Formed Lead)

Logic / RAM Voltage:
- 3 = 3.3 Volt
- 5 = 5.0 Volt (applicable only for BU-64745 and BU-64845)

Product Type (see next page for Product Matrix):
- BU-6474 = RT only with 4K RAM
- BU-6484 = BC /RT / MT with 4K x 16 RAM
- BU-6486 = BC /RT / MT with 64K x 17 RAM

Notes:

1. Standard DDC processing with burn-in and full temp test. See table on next page.
2. Temperature Range applies to case temperature.
3. MIL-PRF-38534 product grading is designated with the following dash numbers:
   Class H is a -11X, 13X, 14X, 15X, 41X, 43X, 44X, 45X
   Class G is a -21X, 23X, 24X, 25X, 51X, 53X, 54X, 55X
   Class D is a -31X, 33X, 34X, 35X, 81X, 83X, 84X, 85X
4. The above products contain tin-lead solder finish as applicable to solder dip requirements.
5. Transformer center-tap connected to +3.3V_XCVR, see FIGURE 15 (Obsolete)
6. Transformer center-tap connected to GND, see FIGURE 16

STANDARD DDC PROCESSING FOR HYBRID AND MONOLITHIC HERMETIC PRODUCTS		
TEST	MIL-STD-883	
	METHOD(S)	CONDITION(S)
INSPECTION	2009, 2010, 2017, and 2032	—
SEAL	1014	A and C
TEMPERATURE CYCLE	1010	C
CONSTANT ACCELERATION	2001	3000g
BURN-IN	1015 (note 1), 1030 (note 2)	TABLE 1

Notes:
1. For Process Requirement "B" (refer to ordering information), devices may be non-compliant with MIL-STD-883, Test Method 1015, Paragraph 3.2. Contact factory for details.
2. When applicable.

MINI-ACE MARK3 PRODUCT MATRIX				
PART NUMBER	LOGIC VOLTAGE	MEMORY	RAM VOLTAGE	TRANSCEIVER VOLTAGE
BU-64743X3	3.3 V	4K x 16	3.3 V	5.0 V
BU-64743X4	3.3 V	4K x 16	3.3 V	5.0 V
BU-64743XC	3.3 V	4K x 16	3.3 V	3.3 V
BU-64743XD	3.3 V	4K x 16	3.3 V	3.3 V
BU-64745X3	5.0 V	4K x 16	5.0 V	5.0 V
BU-64745X4	5.0 V	4K x 16	5.0 V	5.0 V
BU-64843X3	3.3 V	4K x 16	3.3 V	5.0 V
BU-64843X4	3.3 V	4K x 16	3.3 V	5.0 V
BU-64843XC	3.3 V	4K x 16	3.3 V	3.3 V
BU-64843XD	3.3 V	4K x 16	3.3 V	3.3 V
BU-64845X3	5.0 V	4K x 16	5.0 V	5.0 V
BU-64845X4	5.0 V	4K x 16	5.0 V	5.0 V
BU-64863X3	3.3 V	64K x 17	3.3 V	5.0 V
BU-64863X4	3.3 V	64K x 17	3.3 V	5.0 V
BU-64863XC	3.3 V	64K x 17	3.3 V	3.3 V
BU-64863XD	3.3 V	64K x 17	3.3 V	3.3 V

ORDERING INFORMATION FOR MICRO-ACE-TE (NOTE 3)

BU-6XXXXBX-E0X

Test Criteria:
0 = 18V Amplitude, only available with “Voltage transceiver option = 4”
2 = MIL-STD-1760 Amplitude Compliant, Standard

Process Requirements:
0 = Standard DDC practices, no Burn-In

Temperature Range (note 2) /Data Requirements:
E = -40°C to +100°C
1 = -55°C to +125°C (only available with transceiver option C)

Voltage/Transceiver Option:
3 = +5.0 Volts rise/fall times = 100 to 300 ns (1553B)
4 = +5.0 Volts 200 to 300 ns rise/fall times, 1553 and McAir compatible
(not available with “Test Criteria option = 2”)
8 = +3.3 Volts rise/fall times = 100 to 300 ns (1553B) (note 5)
C = +3.3 Volts rise/fall times = 100 to 300 ns (1553B) (note 6)
D = +3.3 Volts rise/fall times = 200 to 300 ns (1553B and McAir compatible. Not Available with Test Critera option 2 "MIL-STD-1760 Amplitude Compliant") (note 6)

Package Type:
B = 324-ball BGA Package
R = RoHS Compliant 324-ball BGA Package

Logic / RAM Voltage:
0 = 3.3 Volt or +5.0 Volt logic
(For BU-64860, 64K x 17 RAM voltage is always +5.0V)
3 = 3.3 Volt

Product Type (see Product Matrix):
BU-6474 = RT only with 4K x 16 RAM
BU-6484 = BC /RT / MT with 4K x 16 RAM
BU-6486 = BC /RT / MT with 64K x 17 RAM

STANDARD DDC PROCESSING FOR BGA PRODUCTS		
TEST	MIL-STD-883	
	METHOD(S)	CONDITION(S)
INSPECTION	2010, 2017, and 2032	—
TEMPERATURE CYCLE	1010	B

MICRO-ACE TE PRODUCT MATRIX					
PART NUMBER	SPECIAL ORDER MIN QTY MAY APPLY	LOGIC VOLTAGE	MEMORY	RAM VOLTAGE	TRANSCEIVER VOLTAGE
BU-64840B(R)3-E02	X	3.3V or 5.0V	4K x 16	Same as Logic	5.0V
BU-64843B(R)C-X02		3.3V	4K x 16	3.3V	3.3V
BU-64843B(R)D-X00		3.3V	4K x 16	3.3V	3.3V
BU-64860B(R)3-E02		3.3V or 5.0V	64K x 17	5.0V	5.0V
BU-64863B(R)C-X02		3.3V	64K x 17	3.3V	3.3V
BU-64863B(R)D-X00		3.3V	64K x 17	3.3V	3.3V
BU-64860B(R)4-E00		3.3V or 5.0V	64K x 17	5.0V	5.0V

ORDERING INFORMATION FOR MICRO-ACE-TE MECHANICAL SAMPLE

BU-64863B8-600

MICRO-ACE-TE (324 Ball BGA) Mechanical Sample, with "daisy chain" connections of alternating balls, for use in environmental (mechanical / thermal) integrity testing.

ORDERING INFORMATION FOR +5.0V TRANSCEIVER EVALUATION BOARD

BU-61860E3-300

Evaluation board intended to support customers who are interested in electrically connecting and evaluating the performance of +5.0V Enhanced Mini-ACE and/or +5.0V µ-ACE (MICRO-ACE) series of products.

ORDERING INFORMATION FOR +3.3V TRANSCEIVER EVALUATION BOARD

BU-64863E8-300

Evaluation board intended to support customers who are interested in electrically connecting and evaluating the performance of the +3.3V Mini-ACE Mark3 and/or +3.3V MICRO-ACE-TE series of products.

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