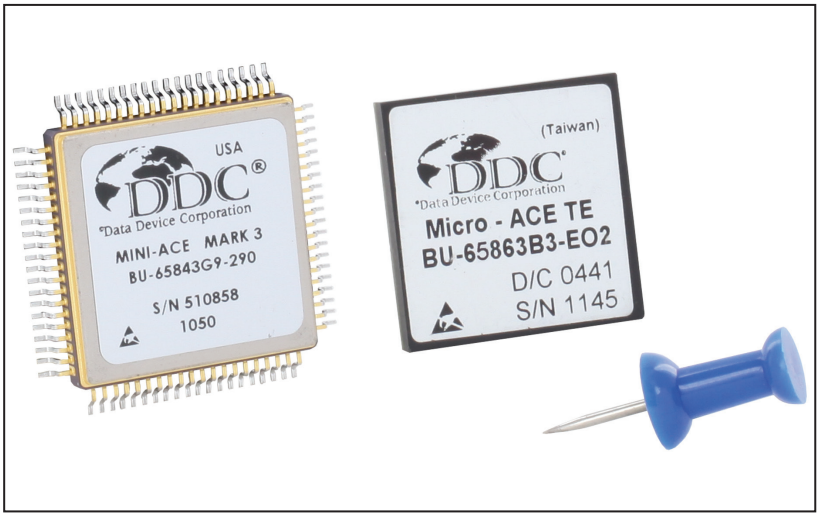
BU-65743/65843/65863/65864

PCI MINI-ACE® MARK3 AND PCI MICRO-ACE®*-TE



DESCRIPTION

The PCI Mini-ACE Mark3/Micro-ACE TE family of MIL-STD-1553 terminals provides a complete interface between a 32-Bit/33Mhz 3.3V signaling PCI Bus and a MIL-STD-1553 bus. These terminals integrate dual transceiver, protocol logic, and 4K or 64K words of RAM, all of which can be powered from 3.3V.

With a 0.88-inch square package, the PCI Mini-ACE Mark3 is the smallest ceramic CQFP PCI 1553 solution available. The 0.80-inch square 324 ball BGA PCI Micro-ACE TE has an even smaller footprint, but has a more restricted operating temperature range. Both are 100% software compatible with the larger PCI Enhanced Mini-ACE and add TAG_CLK inputs. The TAG_CLK input allows a software selectable external time tag clock input. Both parts are available with a choice of either 3.3V transceivers or 5V transceivers.

The PCI Micro-ACE TE has a more restricted set of options compared to the PCI Mini-ACE Mark3. Please consult the ordering information at the rear of the data sheet to see which options are available. In addition, the PCI Micro-ACE TE adds RTBOOT and 1553 clock select inputs for applications which must boot into RT mode with Busy bit set.

The PCI Mini-ACE Mark3/Micro-ACE TE is nearly 100% software compatible with the Enhanced Mini-ACE and previous generation Mini-ACE terminals. The PCI interface to this terminal is not 5V tolerant.

Multiprotocol support of MIL-STD-1553A/B and STANAG 3838, including Mark3 versions incorporating McAir compatible transmitters, is provided. There is a choice of 10, 12, 16, or 20 MHz 1553 clocks. The BC/RT/MT versions with 64K words of RAM include built-in RAM parity checking.

BC features include a built-in message sequence control engine, with a set of 20 instructions. This provides an autonomous means of implementing multi-frame message scheduling, message retry schemes, data double buffering, asynchronous message insertion, and reporting to the host CPU.

The PCI Mini-ACE Mark3 and Micro-ACE TE RT offer single and circular sub-address buffering schemes, along with a global circular buffering option, 50% rollover interrupt for circular buffers, and an interrupt status queue.

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FEATURES

- 32-Bit/33MHz, 3.3Volt, PCI Target Interface
- Fully Integrated 1553A/B Notice 2, 1760, McAir, STANAG 3838 Interface Terminal
- All +3.3V Operation or +3.3V Logic and +5V Transceivers
- 0.88 inch square, 80-Pin CQFP (PCI Mini-ACE Mark3) or 0.80 inch square 324 ball BGA (PCI Micro-ACE TE)
- Compatible with PCI Enhanced Mini-ACE, Enhanced Mini-ACE, Mini-ACE and ACE Generations
- Choice of :
  - RT only with 4K RAM (BU-65743)
  - BC/RT/MT with 4K RAM (BU-65843)
  - BC/RT/MT with 64K RAM, and RAM Parity (BU-65863, BU-65864)
- Sleep Mode Option
- Choice of 10, 12, 16, or 20 MHz 1553 Clock
- Highly Autonomous BC with Built-In Message Sequence Control:
  - Frame Scheduling
  - Branching
  - Asynchronous Message Insertion
  - General Purpose Queue
  - User-defined Interrupts
- Advanced RT Functions
  - Global Circular Buffering
  - Interrupt Status Queue
  - 50% Circular Buffer Rollover Interrupts
- Selective Message Monitor or RT/Monitor

FOR MORE INFORMATION CONTACT:

Technical Support:
1-800-DDC-5757 ext. 7771

* The technology used in DDC's Micro-ACE series of products may be subject to one or more patents pending.
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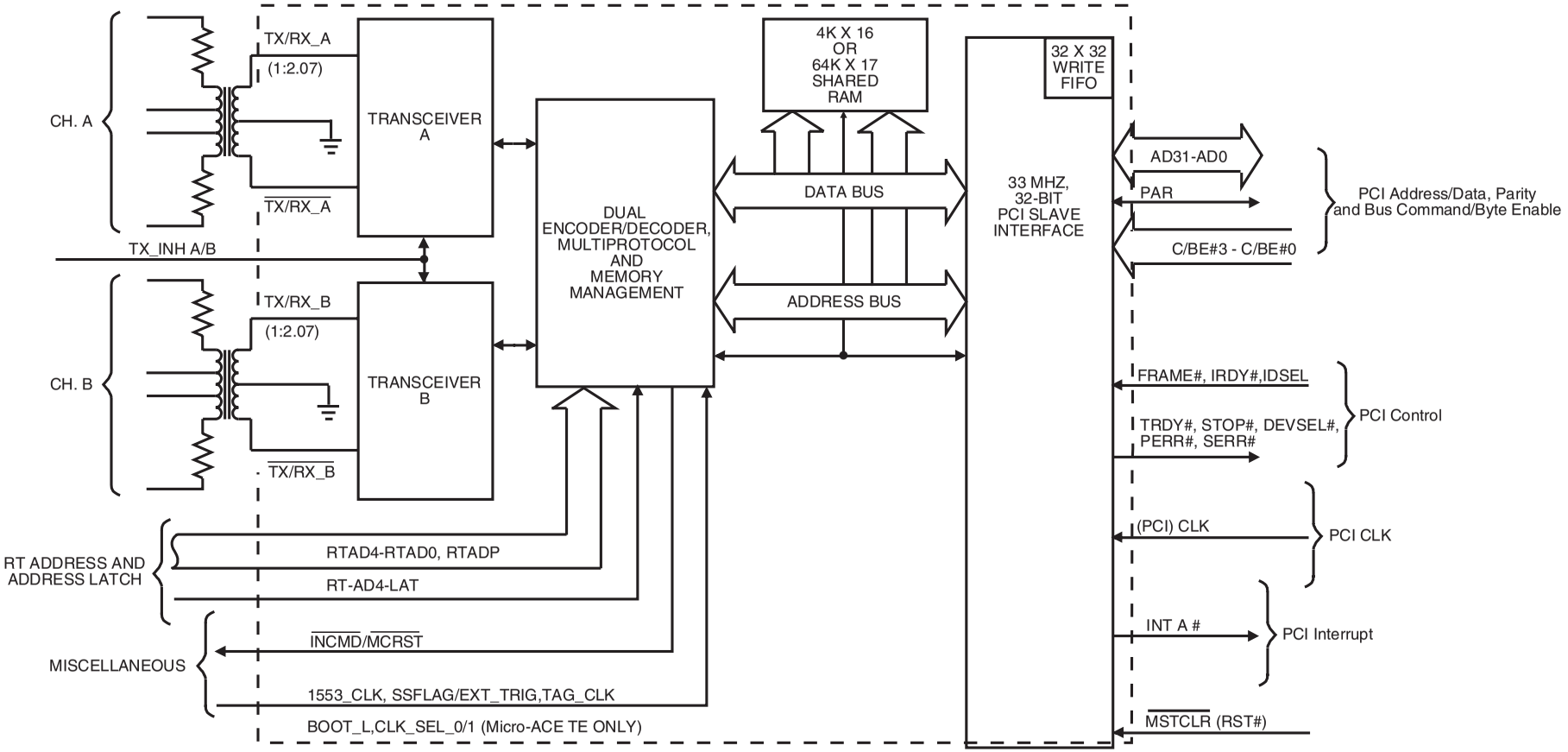


NOTE 1: Shown with 3.3V transceivers. 5V transceivers are available.

FIGURE 1. PCI MINI-ACE MARK3/MICRO-ACE TE (3.3V TRANSCEIVERS) BLOCK DIAGRAM

TABLE 1. PCI MINI-ACE MARK3/MICRO-ACE TE SPECIFICATIONS

PARAMETER	MIN	TYP	MAX	UNITS
ABSOLUTE MAXIMUM RATING				
Supply Voltage				
• Logic +3.3V	-0.3		4.0	V
• Transceiver +3.3V (BU65XX3X8/9/C/D)	-0.3		4.5	V
• Transceiver +5V(BU-65XX3F3/4, BU-65XX3G3/4, BU-658XXB3)	-0.3		7.0	V
Logic				
• Voltage Input Range	-0.3		Vdd+0.3	V
• Voltage Input Range, +5V Tolerant Pins (Note 16)	-0.3		6.0	V
RECEIVER				
Differential Input Resistance (Notes 1-6)	2.5			kΩ
Differential Input Capacitance (Notes 1-6, 19)			50	pF
Threshold Voltage, Transformer Coupled	0.200		0.860	Vp-p
Common Mode Voltage (Note 7)			10	Vpeak
TRANSMITTER				
Differential Output Voltage				
• Direct Coupled Across 35 Ω, Measured on Bus	6	7	9	Vp-p
• Transformer Coupled Across 70 Ω, Measured on Bus				
(BU-65XXXXX-XX0,	18	20	27	Vp-p
BU-65XXXXX-XX2) (Note 13)	20	21.5	27	Vp-p
Output Noise, Diff (Direct Coupled)			10	mVp-p
Output Offset Voltage, Transformer Coupled Across 70 ohms	-250	150	250	mVp
Rise/Fall Time				
(BU-65XXXX3/8/C,	100	150	300	ns
BU-65XXXX4/9/D)	200	250	300	ns
LOGIC				
V_{IH}				
All signals except PCI, SLEEP_IN	2.1			V
V_{IL}				
All signals except PCI, SLEEP_IN			0.7	V
Schmidt Hysteresis				
All signals except PCI	0.4			V
I_{IH}, I_{IL}				
All signals except PCI, SLEEP_IN				
I_{IH} (Vcc=3.6V, V_{IN}=Vcc)	-10		10	µA
I_{IH} (Vcc=3.6V, V_{IN}=2.7V)	-100		-33	µA
I_{IL} (Vcc=3.6V, V_{IN}=0.4V)	-100		-33	µA
V_{IH} SLEEP_IN (Vcc=3.6V)	2.5			V
V_{IL} SLEEP_IN (Vcc=3.0V)			0.9	V
I_{IH}, I_{IL} SLEEP_IN				
I_{IH} (Vcc=3.6V, V_{IN}=2.7V)	10		70	µA
I_{IL} (Vcc=3.6V, V_{IN}=0.0V)	-20		+20	µA
V_{OH} (Vcc=3.0V, $I_{OH=max}$)	2.4			V
V_{OL} (Vcc=3.0V, $I_{OL=max}$)			0.4	V
I_{OL}	3.4			mA
I_{OH}			-3.4	mA
C_I (Input Capacitance)			20	pF
PCI LOGIC see PCI spec 3.3V signaling environment				
C_I (Input Capacitance) all PCI except PCI_CLK & IDSEL			10	pF
C_I (Input Capacitance) PCI_CLK			4	pF
C_I (Input Capacitance) IDSEL			6	pF

TABLE 1. PCI MINI-ACE MARK3/MICRO-ACE TE SPECIFICATIONS (CONT.)

PARAMETER	MIN	TYP	MAX	UNITS
POWER SUPPLY REQUIREMENTS (3.3V TRANSCEIVER)				
Voltages/Tolerances				
• +3.3V	3.15	3.3	3.45	V
Current Drain (Total Hybrid) (Note 17)				
• BU-65863F(G)8(9)-XX0				
• Idle w/ transceiver SLEEPIN asserted		31	67	mA
• Idle w/ transceiver SLEEPIN negated		77	110	mA
• 25% Transmitter Duty Cycle		267	315	mA
• 50% Transmitter Duty Cycle		457	515	mA
• 100% Transmitter Duty Cycle		837	915	mA
• BU-65863F(G)8-XX2, BU-65863B(R)8-E02				
• Idle w/ transceiver SLEEPIN asserted		27	67	mA
• Idle w/ transceiver SLEEPIN negated		76	110	mA
• 25% Transmitter Duty Cycle		242	335	mA
• 50% Transmitter Duty Cycle		383	535	mA
• 100% Transmitter Duty Cycle		725	995	mA
• BU-65843F(G)8(9)-XX0, BU-65743F(G)8(9)-XX0				
• Idle w/ transceiver SLEEPIN asserted		16	52	mA
• Idle w/ transceiver SLEEPIN negated		56	95	mA
• 25% Transmitter Duty Cycle		246	300	mA
• 50% Transmitter Duty Cycle		436	500	mA
• 100% Transmitter Duty Cycle		816	900	mA
• BU-65743F(G)8-XX2, BU-65843X8(R)-XX2				
• Idle w/ transceiver SLEEPIN asserted		12	52	mA
• Idle w/ transceiver SLEEPIN negated		55	95	mA
• 25% Transmitter Duty Cycle		221	320	mA
• 50% Transmitter Duty Cycle		362	520	mA
• 100% Transmitter Duty Cycle		704	980	mA
• BU-65X43XC/D-XXX				
• Idle		25	51	mA
• 25% Transmitter Duty Cycle		163	230	mA
• 50% Transmitter Duty Cycle		301	384	mA
• 100% Transmitter Duty Cycle		613	752	mA
• BU-65863XC/D-XXX				
• Idle		46	66	mA
• 25% Transmitter Duty Cycle		184	245	mA
• 50% Transmitter Duty Cycle		322	399	mA
• 100% Transmitter Duty Cycle		634	767	mA

TABLE 1. PCI MINI-ACE MARK3/MICRO-ACE TE SPECIFICATIONS (CONT.)

PARAMETER	MIN	TYP	MAX	UNITS
POWER DISSIPATION (NOTES 17-18)				
Total Hybrid (3.3V Transceiver)				
• BU-65863X8(9)-XX0				
• Idle w/ transceiver SLEEPIN asserted		0.10	0.22	W
• Idle w/ transceiver SLEEPIN negated		0.25	0.36	W
• 25% Transmitter Duty Cycle		0.62	0.74	W
• 50% Transmitter Duty Cycle		0.97	1.09	W
• 100% Transmitter Duty Cycle		1.64	1.79	W
• BU-65863F(G)8-XX2, BU-65863B8-E02				
• Idle w/ transceiver SLEEPIN asserted		0.10	0.22	W
• Idle w/ transceiver SLEEPIN negated		0.25	0.36	W
• 25% Transmitter Duty Cycle		0.64	0.76	W
• 50% Transmitter Duty Cycle		1.00	1.13	W
• 100% Transmitter Duty Cycle		1.73	1.88	W
• BU-65743F(G)8(9)-XX0, BU-65843F(G)8(9)-XX0				
• Idle w/ transceiver SLEEPIN asserted		0.10	0.17	W
• Idle w/ transceiver SLEEPIN negated		0.18	0.31	W
• 25% Transmitter Duty Cycle		0.47	0.69	W
• 50% Transmitter Duty Cycle		0.72	1.04	W
• 100% Transmitter Duty Cycle		1.22	1.74	W
• BU-65743F(G)8-XX2, BU-65843F(G)8-XX2, BU-65843B8-E02				
• Idle w/ transceiver SLEEPIN asserted		0.10	0.17	W
• Idle w/ transceiver SLEEPIN negated		0.18	0.31	W
• 25% Transmitter Duty Cycle		0.49	0.71	W
• 50% Transmitter Duty Cycle		0.76	1.08	W
• 100% Transmitter Duty Cycle		1.31	1.83	W
• BU-65X43XC/D-XXX				
• Idle		0.08	0.19	W
• 25% Transmitter Duty Cycle		0.23	0.35	W
• 50% Transmitter Duty Cycle		0.27	0.42	W
• 100% Transmitter Duty Cycle		0.46	0.64	W
• BU-65863XC/D-XXX				
• Idle		0.15	0.24	W
• 25% Transmitter Duty Cycle		0.30	0.40	W
• 50% Transmitter Duty Cycle		0.34	0.47	W
• 100% Transmitter Duty Cycle		0.53	0.69	W
HOTTEST DIE (3.3V TRANSCEIVER)				
• BU-65XXXX8(9)-XX0				
• Idle		0.07	0.11	W
• 25% Transmitter Duty Cycle		0.37	0.45	W
• 50% Transmitter Duty Cycle		0.70	0.80	W
• 100% Transmitter Duty Cycle		1.37	1.51	W
• BU-65XXXX8-XX2				
• Idle		0.07	0.11	W
• 25% Transmitter Duty Cycle		0.37	0.47	W
• 50% Transmitter Duty Cycle		0.59	0.84	W
• 100% Transmitter Duty Cycle		1.13	1.59	W
• BU-65XX3XC/D-XXX				
• Idle		0.07	0.11	W
• 25% Transmitter Duty Cycle		0.20	0.25	W
• 50% Transmitter Duty Cycle		0.30	0.39	W
• 100% Transmitter Duty Cycle		0.42	0.54	W

TABLE 1. PCI MINI-ACE MARK3/MICRO-ACE TE SPECIFICATIONS (CONT.)

PARAMETER	MIN	TYP	MAX	UNITS
POWER SUPPLY REQUIREMENTS (5V TRANSCEIVER)				
Voltages/Tolerances				
+3.3V (Logic) V_{CC}	3.0	3.3	3.6	V
+5V (XCVR or 5V V_{CC} CHA/B)	4.75	5.0	5.5	V
+5V (RAM for BU-65864B(R)3)	4.5	5.0	5.5	V
Current Drain (Total Hybrid)				
• BU-65863F(G)3(4)-XX0				
+5V (XCVR)				
• Idle		65	100	mA
• 25% Transmitter Duty Cycle		169	205	mA
• 50% Transmitter Duty Cycle		273	310	mA
• 100% Transmitter Duty Cycle		481	520	mA
+3.3V (Logic)		45	60	mA
• BU-65863F(G)3-XX2				
+5V (XCVR)				
• Idle		65	100	mA
• 25% Transmitter Duty Cycle		180	216	mA
• 50% Transmitter Duty Cycle		295	332	mA
• 100% Transmitter Duty Cycle		525	565	mA
+3.3V (Logic)		45	60	mA
• BU-65864B(R)3-E02				
+5V (RAM, CHA, CHB)				
• Idle		66	120	mA
• 25% Transmitter Duty Cycle		174	236	mA
• 50% Transmitter Duty Cycle		282	352	mA
• 100% Transmitter Duty Cycle		498	585	mA
+3.3V (Logic)		25	40	mA
• BU-65743F(G)3(4)-XX0, BU-65843F(G)3(4)-XX0				
+5V (XCVR)				
• Idle		65	100	mA
• 25% Transmitter Duty Cycle		169	205	mA
• 50% Transmitter Duty Cycle		273	310	mA
• 100% Transmitter Duty Cycle		481	520	mA
+3.3V (Logic)		25	40	mA
• BU-65743F(G)3-XX2, BU-65843F(G)3-XX2, BU-65843B3-E02				
+5V (XCVR or 5V ChA, 5V Ch B)				
• Idle		65	100	mA
• 25% Transmitter Duty Cycle		180	216	mA
• 50% Transmitter Duty Cycle		295	332	mA
• 100% Transmitter Duty Cycle		525	565	mA
+3.3V (Logic)		25	40	mA

TABLE 1. PCI MINI-ACE MARK3/MICRO-ACE TE SPECIFICATIONS (CONT.)

PARAMETER	MIN	TYP	MAX	UNITS
POWER DISSIPATION (NOTE 15)				
TOTAL HYBRID (5V TRANSCEIVER)				
• BU-65863F(G)3(4)-XX0				
• Idle		0.41	0.75	W
• 25% Transmitter Duty Cycle		0.73	1.00	W
• 50% Transmitter Duty Cycle		1.02	1.23	W
• 100% Transmitter Duty Cycle		1.63	1.68	W
• BU-65863F(G)3-XX2				
• Idle		0.41	0.75	W
• 25% Transmitter Duty Cycle		0.76	1.04	W
• 50% Transmitter Duty Cycle		1.13	1.34	W
• 100% Transmitter Duty Cycle		1.86	1.94	W
• BU-65864B(R)3-E02				
• Idle		0.44	0.80	W
• 25% Transmitter Duty Cycle		0.80	1.09	W
• 50% Transmitter Duty Cycle		1.17	1.39	W
• 100% Transmitter Duty Cycle		1.89	1.97	W
• BU-65743F(G)3(4)-XX0 BU-65843F(G)3(4)-XX0				
• Idle		0.41	0.63	W
• 25% Transmitter Duty Cycle		0.70	0.85	W
• 50% Transmitter Duty Cycle		0.94	1.07	W
• 100% Transmitter Duty Cycle		1.40	1.51	W
• BU-65743F(G)3-XX2 BU-65843F(G)3-XX2, BU-65843B3-E02				
• Idle		0.41	0.63	W
• 25% Transmitter Duty Cycle		0.72	0.86	W
• 50% Transmitter Duty Cycle		0.97	1.09	W
• 100% Transmitter Duty Cycle		1.45	1.56	W
HOTTEST DIE (5V TRANSCEIVER)				
• BU-65XXXX3(4)-xx0				
• Idle		0.18	0.28	W
• 25% Transmitter Duty Cycle		0.42	0.51	W
• 50% Transmitter Duty Cycle		0.66	0.75	W
• 100% Transmitter Duty Cycle		1.14	1.22	W
• BU-65XXXX3-xx2				
• Idle		0.18	0.28	W
• 25% Transmitter Duty Cycle		0.48	0.58	W
• 50% Transmitter Duty Cycle		0.78	0.88	W
• 100% Transmitter Duty Cycle		1.39	1.48	W
CLOCK INPUT				
PCI CLOCK INPUT FREQUENCY			33.3	MHz
1553 Clock Frequency				
• Default Mode		16.0		MHz
• Option		12.0		MHz
• Option		10.0		MHz
• Option		20.0		MHz
• Long Term Tolerance				
• 1553A Compliance	-0.01		0.01	%
• 1553B Compliance	-0.10		0.10	%
• Short Term Tolerance, 1 second				
• 1553A Compliance	-0.001		0.001	%
• 1553B Compliance	-0.01		0.01	%
1553 MESSAGE TIMING				
Completion of CPU Write (BC Start)-to-Start of First Message (for Non-enhanced BC Mode)		2.5		µs
BC Intermessage Gap (Note 8)				
Non-enhanced (Mini-ACE compatible) BC mode		9.5		µs
Enhanced BC mode (Note 9)		10.0 to 10.5		µs

TABLE 1. PCI MINI-ACE MARK3/MICRO-ACE TE SPECIFICATIONS (CONT.)

PARAMETER	MIN	TYP	MAX	UNITS
1553 MESSAGE TIMING (CONT.)				
BC/RT/MT Response Timeout (Note 10)				
• 18.5 nominal	17.5	18.5	19.5	µs
• 22.5 nominal	21.5	22.5	23.5	µs
• 50.5 nominal	49.5	50.5	51.5	µs
• 128.0 nominal	127	129.5	131	µs
RT Response Time (mid-parity to mid-sync) (Note 11)	4		7	µs
Transmitter Watchdog Timeout		660.5		µs
THERMAL				
80-Pin, Ceramic Flatpack/Gull Lead Thermal Resistance, Junction-to-Case, Hottest Die (θ_{JC}) (Note 12)		9	11	°C/W
324-Ball Plastic BGA (See Thermal Management section)				
• Junction-to-Ambient (θ_{JA} via simulation)				
- Per JESD 51-2 standard at 25°C θ_{JA} in Still Air		55.0		°C/W
- Per JESD 51-6 standard at 25°C θ_{JA} @1M/S		44.5		°C/W
θ_{JA} @2M/S		41.8		°C/W
• Junction-to-Case (θ_{JC} via simulation)				
- Per JESD 51-12 standard at 25°C θJC		20.8		°C/W
• Junction-to-Board (θ_{JB} via simulation)				
- Per JESD 51-2 standard at 25°C θJB		31.3		°C/W
ALL PACKAGES				
Operating Case/Ball Temperature				
-1XX, -4XX	-55		+125	°C
-2XX, -5XX	-40		+85	°C
-3XX, -8XX	0		+70	°C
-EXX	-40		+100	°C
Operating Junction Temperature				
-Transceiver	-55		+150	°C
-Protocol	-55		+135	°C
-Memory	-55		+140	°C
Storage Temperature	-65		+150	°C
Soldering				
Flat Pack/Gull Wing Lead Temperature (soldering, 10 sec.)			+300	°C
324-ball BGA Package The reflow profile detailed in IPC/ JEDEC J-STD-020 is applicable for both leaded and lead-free products			+250	°C
PHYSICAL CHARACTERISTICS				
80-Pin, Ceramic Flatpack/Gull Lead Size, MAXIMUM	0.89 X 0.89 X 0.130 (22.6 x 22.6 x 3.3)			in. (mm)
Micro-ACE-TE				
Moisture Sensitivity Level	MSL-3			
Electrostatic Discharge Sensitivity	ESD Class 0			
Lead Toe-to-Toe Distance	1.13			in.
80-Pin Gull Lead, MAXIMUM	(28.7)			(mm)
Weight	0.4 (10)			Oz. (g)
324-ball Plastic BGA Size, Maximum	0.815 X 0.815 X 0.120 (20.7 x 20.7 x 3.05)			in. (mm)
Weight	0.088 (2.5)			Oz. (g)

TABLE 1 NOTES:

Notes 1 through 6 are applicable to the Receiver Differential Resistance and Differential Capacitance specifications:

1. Specifications include both transmitter and receiver (tied together internally).
2. Impedance parameters are specified directly between pins TX/RX_A(B) and $\overline{\text{TX/RX\_A(B)}}$ of the PCI Mini-ACE Mark3/PCI Micro-ACE TE hybrid.
3. It is assumed that all power and ground inputs to the hybrid are connected.
4. The specifications are applicable for both unpowered and powered conditions.
5. The specifications assume a 2 volt rms balanced, differential, sinusoidal input. The applicable frequency range is 75 kHz to 1 MHz.
6. Minimum resistance and maximum capacitance parameters are guaranteed over the operating range, but are not tested.

TABLE 1 NOTES (Cont.):

7. Assumes a common mode voltage within the frequency range of dc to 2 MHz, applied to pins of the isolation transformer on the stub side (either direct or transformer coupled), and referenced to hybrid ground. Transformer must be a DDC recommended transformer or other transformer that provides an equivalent minimum CMRR.
8. Typical value for minimum intermessage gap time. Under software control, this may be lengthened to 65,535 ms - message time, in increments of 1 µs. If ENHANCED CPU ACCESS, bit 14 of Configuration Register #6, is set to logic "1", then host accesses during BC Start-of-Message (SOM) and End-of-Message (EOM) transfer sequences could have the effect of lengthening the intermessage gap time. For each host access during an SOM or EOM sequence, the intermessage gap time will be lengthened by 6 clock cycles. Since there are 7 internal transfers during SOM, and 5 during EOM, this could theoretically lengthen the intermessage gap by up to 72 clock cycles; i.e., up to 7.2 µs with a 10 MHz clock, 6.0 µs with a 12 MHz clock, 4.5 µs with a 16 MHz clock, or 3.6 µs with a 20 MHz clock.
9. For Enhanced BC mode, the typical value for intermessage gap time is approximately 10 clock cycles longer than for the non-enhanced BC mode. That is, an addition of 1.0 µs at 10 MHz, 833 ns at 12 MHz, 625 ns at 16 MHz, or 500 ns at 20 MHz.
10. Software programmable (4 options). Includes RT-to-RT Timeout (measured mid-parity of transmit Command Word to mid-sync of transmitting RT Status Word).
11. Measured from mid-parity crossing of Command Word to mid-sync crossing of RT's Status Word.
12. θJC is measured to the bottom of the case, and the numbers indicated are preliminary
13. External 10 µF Tantalum and 0.1 µF capacitors should be located as close as possible to Pin 10, and a 0.1 µF at pins 30, 51 & 69.
14. MIL-STD-1760 requires that the PCI Mini-ACE Mark3 produce a 20 Vp-p minimum output on the stub connection.
15. Power dissipation specifications assume a transformer coupled configuration with external dissipation (while transmitting) of 0.14 watts for the active isolation transformer, 0.08 watts for the active bus coupling transformer, 0.45 watts for each of the two bus isolation resistors and 0.15 watts for

INTRODUCTION

The BU-65743 RT, and BU-65843/65864 BC/RT/MT PCI Mini-ACE Mark3/Micro-ACE TE family of MIL-STD-1553 terminals comprise a complete integrated interface between a PCI host processor and a MIL-STD-1553 bus.

All members of the PCI Mini-ACE Mark3 family are packaged in the same 0.88" square, 80-lead CQFP package. All members of the PCI Micro-ACE TE family are packaged in the same 0.8" square, 324 ball, plastic BGA package.

The PCI Mini-ACE Mark3/Micro-ACE TE hybrid's provide software compatibility with the Enhanced Mini-ACE, Mini-ACE (Plus) terminals, as well as software compatibility with the older ACE series.

The PCI Mini-ACE Mark3/Micro-ACE TE provides complete multiprotocol support of MIL-STD-1553A/B/McAir and STANAG 3838. All versions integrate dual transceivers; along with protocol, host interface, memory management logic; and a minimum of 4K words of RAM. In addition, the BU-6586X BC/RT/MT terminals include 64K words of internal RAM, with built-in parity checking.

The PCI Mini-ACE Mark3s include a 3.3V or 5V voltage source transceiver for improved line driving capability, with options for MIL-STD-1760 and McAir compatibility. The PCI Micro-ACE TEs are available with 3.3V or 5V voltage source transceivers but do not offer a McAir option. Please consult the ordering information section at the end of this document for all available options.

To provide further flexibility, the PCI Mini-ACE Mark3/Micro-ACE TE has internal 1553 master clock dividers that allow operation with either 10, 12, 16, or 20 MHz clock inputs. The 1553 master clock divider is software programmable or, in the case of the Micro ACE TE, can be controlled via pins when the RTBoot mode is strapped.

The PCI Mini-ACE Mark3/Micro-ACE TEs are fully compliant targets, as defined by the PCI Local Bus Specification Revision 2.2, using a 32 bit interface that operates at clock speeds of up to 33 Mhz, from a 3.3V bus. The interface supports PCI interrupts and contains a FIFO that handles PCI burst write transfer cycles. The FIFO is deep enough to accept an entire 1553 message. The PCI interface is NOT 5V tolerant and can not be used in a 5V PCI signaling environment.

One of the salient features of the PCI Mini-ACE Mark3 is its Enhanced Bus Controller architecture. The Enhanced BC's highly autonomous message sequence control engine provides a means for offloading the host processor for implementing multi-frame message scheduling, message retry schemes, data double buffering, and asynchronous message insertion. For the purpose of performing messaging to the host processor, the Enhanced BC mode includes a General Purpose Queue, along with user-defined interrupts.

The PCI Mini-ACE Mark3/Micro-ACE TE RT offers the same choices of single and circular buffering for individual subaddresses as ACE, Mini-ACE(Plus), and Enhanced Mini-ACE. New enhancements to the RT architecture include a global circular buffering option for multiple (or all) receive subaddresses, a 50% rollover interrupt for circular buffers, an interrupt status queue for logging up to 32 interrupt events, and an option to automatically initialize to RT mode with the Busy bit set. The interrupt status queue and 50% rollover interrupt features are also included as improvements to the PCI Mini-ACE Mark3/Micro-ACE TE's Monitor architecture.

The PCI Mini-ACE Mark3 series terminals operate over the full military temperature range of -55°C to +125°C. Available screened to MIL-PRF-38534C, the terminals are ideal for military and industrial processor to 1553 applications.

The PCI Micro-ACE TE terminals operate over an extended temperature range of -40°C to +100°C.

TRANSCEIVERS

The transceivers in the PCI Mini-ACE Mark3 series terminals are fully monolithic, requiring only a +3.3V power input or a +5V power input. The transmitters are voltage sources, which provide improved line driving capability over current sources. This serves to improve performance on long buses with many taps. The transmitters also offer an option which satisfies the MIL-STD-1760 requirement for a minimum of 20 volts peak-to-peak, transformer coupled output. The transceivers in the PCI Micro-ACE TE are only available with the MIL-STD-1760 option.

Besides eliminating the demand for an additional power supply, the use of a +3.3V only or +5V only transceiver requires the use of a step-up, rather than a step-down, isolation transformer. This provides the advantage of higher terminal input impedance than is possible for a 15 volt or 12 volt transmitter. As a result, there is a greater margin for the input impedance test, mandated for the

1553 validation test. This characteristic allows for longer cable lengths between a system connector and the isolation transformers of an embedded 1553 terminal.

To provide compatibility to McAir specs, the PCI Mini-ACE Mark3 is available with an option for transmitters with increased rise and fall times.

All PCI Micro-ACE TE parts can be operated with external transceivers. This is achieved by bonding out the required protocol and transceiver I/O pads to BGA balls. Most applications will use the internal transceivers, which requires PCB traces to interconnect protocol output balls to transceiver input balls and transceiver output balls to protocol input balls. These interconnections are listed in TABLE 71.

The 3.3V transceiver parts also have a SLEEP_IN input. Asserting SLEEP_IN puts the transceivers into a power saving mode during which the receiver and transmitter of the transceivers are disabled.

The receiver sections of the PCI Mini-ACE Mark3/Micro-ACE TE are fully compliant with MIL-STD-1553B Notice 2 in terms of front-end overvoltage protection, threshold, common mode rejection, and word error rate.

PCI REGISTER AND MEMORY ADDRESS

The PCI Interface contains a set of "Type 00h" PCI configuration registers that are used to map the device into the host system. There are two Base Address Registers that are used to implement ACE memory space (BAR0) and register space (BAR1). The PCI configuration register space is mapped in accordance with PCI revision 2.2 specifications.

The PCI Mini-ACE Mark3 acts as a target and responds to the following PCI commands:

TABLE 2. PCI TARGET COMMAND CODES

COMMAND TYPE	CODE (C/BE[3:0]#)
MEMORY READ	0110 (6h)
MEMORY WRITE	0111 (7h)
CONFIGURATION READ	1010 (Ah)
CONFIGURATION WRITE	1011 (Bh)
MEMORY READ MULTIPLE	1100 (Ch)
MEMORY READ LINE	1110 (Eh)
MEMORY WRITE & INVALIDATE	1111 (Fh)

The PCI Mini-ACE Mark3 does **not** implement the Memory Read Multiple, Memory Read Line or Memory Write and Invalidate commands. However, in accordance with PCI rules, the PCI Mini-ACE Mark3 will accept these requests and alias them to the basic memory commands. For example, Memory Read Multiple and Memory Read Line commands will be accepted and treated as Memory Read commands. Similarly, the PCI Mini-ACE Mark3 will accept a memory Write and Invalidate command and treat it as a Memory Write command.

ACE memory is accessed internally in 16-bit words, but memory is accessed sequentially allowing for 32-bits of data to be read from the PCI bus. In other words, if a 32-bit PCI read is requested the first 16 bits of data would be read from the requested internal address, the next 16 bits of data would be read from the initial internal address + 1, and then the resulting 32-bit double word would be transferred to the PCI bus. The PCI Mini-ACE Mark3 supports 32-bit and 16-bit read and write operations, 8 bit reads will return 16 bit data, and 8 bit writes are illegal and will cause target-aborts.

TABLE 3. CONFIGURATION REGISTER SPACE FOR THE PCI MINI-ACE MARK3/MICRO-ACE TE				
ADDRESS	**31 24**	**23 16**	**15 8**	**7 0**
00h	Device ID		Vendor ID	
	04h	0Xh (X varies with part #, see text)	DDC Manufacturer Device ID value (4DDCH)	
04h	Status Register		Command Register	
08h	Class Code = 078000h			Rev ID = 02h
0Ch	BIST 00h	Header Type 00h	Latency Timer 00h	Cache Line Size 00h
10h	Base Address Register 0 (for ACE memory)			
	R/W	R/W and 0's (see text)	00h	00h
14h	Base Address Register 1 (for ACE registers)			
	R/W	R/W	R/W and 0's (see text)	00h
18h - 24h	Base Address Registers 2 through 5 (not used) 00000000h			
28h	Card Bus CIS pointer (not used) 00000000h			
2Ch	Subsystem Device and Subsystem Vendor ID Same as Configuration Register 0, Alias Reads to Configuration Register 00			
30h	Expansion ROM Base Address (Not Used, bit = 0)			
34h-38h	Reserved			
3Ch	Max Lat 00h	Min Gnt 00h	Interrupt Pin 01h	Interrupt Line R/W

The ACE register mapping is located in PCI memory space. Although the PCI Mini-ACE Mark3 can be accessed in 32-bit words, all ACE registers are accessed in 16 bit word reads / writes. If a 32-bit read is performed from the PCI bus in ACE register space only the first 16 bits of data are valid.

This data sheet will only describe the PCI registers that are specific to configuring the integrated terminal and shared RAM. For specifics or definitions on other PCI bus configuration registers, please see the PCI Local Bus specification revision 2.2.

Vendor ID field contains the vendor's ID configuration register. Data Device Corporation's ID code is 4DDCh.

Device ID field is used to indicate the device being used. This field is configured by DDC to reflect the part value of the device. The following TABLE 4 represents all possible combinations for the Device ID field:

TABLE 4. DEVICE ID FIELD MAPPING	
DEVICE ID	**DESCRIPTION**
0400h	BC/RT/MT WITH 4K OF RAM (BU-65843)
0402h	BC/RT/MT WITH 64K OF RAM (BU-65864)
0404h	RT ONLY WITH 4K OF RAM (BU-65743)

TABLE 5. PCI COMMAND REGISTER	
BIT	**DESCRIPTION**
15:10	RESERVED, 0'S
9	0
8	SERR# ENABLE
7	0
6	PARITY ERROR CONTROL
5:2	0
1	MEMORY SPACE
0 (LSB)	0

PCI COMMAND REGISTER

Reserved: These bits are read-only and return zeroes when read.

SERR# Enable: This is an enable bit for the SERR# driver. A value of 0b disables the driver. A value of 1b enables the driver. The value after RST# is 0b.

Parity Error Control: This bit controls the device's response to parity errors. When the bit is 1b, the device will take its normal action when a parity error is detected. When this bit is 0b, the device will ignore any parity errors that it detects and continue normal operation. The value after RST# is 0b.

Memory Space: This bit controls the device's response to memory space accesses. A value of 0b disables the device response. A value of 1b allows the device to respond to memory space accesses. The value after RST# is 0b.

PCI STATUS REGISTER

This register records status information for PCI bus related events. Reads to this register behave normally, but writes can only reset bits. A bit is reset whenever the register is written and the data in the corresponding bit location is a 1.

Detected Parity Error: This bit will be set by the device whenever it detects a parity error, even if the Parity Error Control bit in the PCI Control register is 0b.

Signaled System Error: This bit indicates when the device has asserted SERR#. The value after RST# is 0b.

Signaled Target Abort: This bit is set whenever the device terminates a transaction with a Target-Abort. The value after RST# is 0b.

DEVSEL# Timing: The PCI Mini-ACE Mark3 is 01b, medium.

Fast Back-to-Back Capable: This bit is set to 1b and indicates that the device is capable of accepting fast back-to-back transactions.

Reserved: These bits are read-only and return zeroes when read.

Subsystem Vendor ID/Subsystem Device ID: Field is an alias of the Vendor ID/Device ID fields in Configuration Register 00h.

Base Address Registers: Used to implement ACE memory space (BAR0) and ACE register space (BAR1). Base Address Registers 2 through 5 are not used.

BAR0: Used to access ACE memory space. The ACE is allotted a maximum of 64K words, 128K bytes, for its memory space. BAR0 will read back as FFFE0000 after all Fs are written to it.

TABLE 6. PCI STATUS REGISTER

BIT	DESCRIPTION
31	DETECTED PARITY ERROR
30	SIGNALED SYSTEM ERROR
29:28	0
27	SIGNALED TARGET ABORT
26:25	DEVSEL# TIMING = 01 (MEDIUM)
24	0
23	FAST BACK-TO-BACK CAPABLE = 1
22:21	0
20:16	RESERVED, 0'S

TABLE 7. (BAR0) ACE MEMORY

ADDRESS OFF-SET	DEFINITION
00000-1FFFC	PCI MINI-ACE MARK3/MICRO-ACE TE MEMORY SPACE

BAR0 will read back the same for both the 4K word ACE parts (BU-65743/843) and the 64K word ACE (BU-65864).

PCI Mini-ACE MARK3/Micro-ACE TE Memory Space: The least significant bit (LSB) of the PCI address is dropped to form the ACE memory address.

BAR1: Used to access ACE register locations. The ACE is allotted a maximum of 4K bytes for its register space. BAR1 will read back as FFFFF000h after all Fs are written to it. All ACE register locations are accessible through the PCI host via the BAR1 offsets 000h to 0FCh. The PCI-to-ACE interface control/status registers are at 800h to 81Ch. PCI accesses outside of these specific regions (e.g., to offset 100h or 820h, etc.) will produce Target Aborts.

PCI Mini-ACE MARK3/Micro-ACE TE Register Space: Register accesses are on a 32-bit boundary: the last 2 bits of the PCI address are dropped to form the internal ACE address. (e.g. 000 = ACE Reg 0, 004 = ACE Reg1, 008 = ACE Reg2, etc.). Refer to TABLE 18 for a listing of these registers. These registers are nearly 100% compatible with the Enhanced Mini-ACE registers. For an exhaustive discussion of these registers and 1553 BC/RT/MT operation, please refer to the "Enhanced Mini-ACE User Guide".

TABLE 8. (BAR1)ACE/CONTROL REGISTERS - 4K BYTE TOTAL SPACE		
ADDRESS OFFSET	**NAME**	**DEFINITION/ACCESSIBILITY**
000-0FC	ACE	PCI MINI-ACE MARK3/MICRO-ACE TE/REGISTER SPACE
100-7FC	--	RESERVED (TARGET ABORT IF ACCESSED)
800	REG0	GLOBAL ACTIVITY (RD)
804	REG1	FAIL-SAFE OPERATION/INTERRUPT (RW/WR)
808	REG2	FAIL-SAFE TIMER (RD)
80C	REG3	FAIL-SAFE TIMER PRELOAD (RD/WR)
810	REG4	DISCARD TIMER (RD)
814	REG5	DISCARD TIMER PRELOAD (RD/WR)
818	REG6	GENERAL PURPOSE, CUSTOMER USE (RD/WR)
81C	REG7	CLEAR FAIL-SAFE INT/RESET ACE (WR)
820-FFC	--	RESERVED (TARGET ABORT IF ACCESSED)

TABLE 9. REG0 GLOBAL ACTIVITY REGISTER (READ 800H)	
BIT	**DESCRIPTION**
31 (MSB)	PCI INTERRUPT ACTIVE
30	FIFO NOT EMPTY
29	0
28	0
27	0
26	0
25	0
24	1
23	BAR1 DRR_DATA_DISCARD
22	FAIL_SAFE ERROR
21	0
20	0
19	0
18	0
17	0
16	PCI MINI-ACE MARK3/MICRO-ACE TE INTERRUPT ACTIVE
15	0
•	•
•	•
•	•
0 (LSB)	0

This register will be all 0s after RST#, except for bit 24.

PCI_INTERRUPT ACTIVE: When set to '1', indicates that PCI Mini-ACE Mark3/Micro-ACE TE has asserted it's interrupt pin. The three possible sources (if enabled and active) are the ACE core, FailSafe timer and BAR1 DRR_DATA_DISCARD.

FIFO NOT EMPTY: When set to '1', indicates that the write FIFO is not empty.

BAR1_DRR_DATA_DISCARD: If the data discard timer times out while waiting for a retry on a BAR1 access, this bit will be set. If BAR1 read is discarded, it may have caused an action (for example clearing an ACE interrupt) that has not been recognized by the PCI MASTER.

FAIL_SAFE_ERROR: If not in FAIL_SAFE OFF mode and fail safe error occurs (ACE does not respond), this bit will be set. Failsafe errors are extremely unlikely.

DRR_HOLD: When '0', a delayed read request is discarded if the PCI Mini-ACE Mark3/Micro-ACE TE has obtained requested data and a different transaction is requested. When '1', delayed read request is held until master repeats original request or timeout occurs.

BITS 30 - 22: Reserved, write as 0s

PCI MINI-ACE MARK3/MICRO-ACE TE INTERRUPT ENABLE: Must be set to "1".

BAR1_DRR_DATA_DISCARD INTERRUPT ENABLE: Enables interrupt to occur on a BAR1 delayed read timeout.

FAILSAFE INTERRUPT ENABLE: When set to a "1", an interrupt is generated if not in FAILSAFE OFF mode and a FAILSAFE error is detected.

FAILSAFE INTERRUPT AUTOCLEAR ENABLE: If set, causes interrupt and the FAIL_SAFE ERROR bit (REG0-bit 22) to be cleared whenever upper word of REG0 is read by the PCI MASTER. If not set, bit 1 in Reg 7 must be used to clear Failsafe interrupts.

FAILSAFE MODE: Fail Safe Errors occur when the internal ACE fails to assert it's hand-shake signal within 1 millisecond (programmable) of when the internal Strobe or Request signal is asserted. Four possible FAILSAFE Modes determine how this situation is handled.

TABLE 10. REG1 FAIL-SAFE OPERATION/INTERRUPT REGISTER (READ/WRITE 804H)

BIT	DESCRIPTION
31 (MSB)	DRR_HOLD
30	RESERVED, WRITE AS 0
•	•
•	•
•	•
22	RESERVED, WRITE AS 0
21	PCI MINI-ACE MARK3/MICRO-ACE TE INTERRUPT ENABLE
20	BAR1 DRR_DATA_DISCARD INTERRUPT ENABLE
19	FAILSAFE INTERRUPT ENABLE
18	FAILSAFE INTERRUPT AUTOCLEAR ENABLE
17	FAILSAFE MODE - BIT 1 (MSB)
16	FAILSAFE MODE - BIT 0 (LSB)
15	RESERVED , WRITE AS 0
•	•
•	•
•	•
0(LSB)	RESERVED, WRITE AS 0

This register will be all 0s after RST#, except for bit 17 will be 1 (Fail-safe mode = fail-safe halt). Note that Failsafe errors are extremely unlikely.

TABLE 11. FAILSAFE MODE		
BIT 17	BIT 16	FAILSAFE MODE
0	0	FAILSAFE OFF
0	1	FAILSAFE RETRY
1	0	FAILSAFE HALT
1	1	FAILSAFE SKIP

NOTE: FAILSAFE errors are extremely unlikely.

MODE 1 - FAILSAFE OFF. PCI Mini-ACE Mark3/Micro-ACE TE will wait indefinitely for the transaction to complete. The local bus could hang as a result. The FAILSAFE ERROR bit and interrupt will not be generated even if the enable bit is set.

MODE 2 - FAILSAFE RETRY. PCI Mini-ACE Mark3/Micro-ACE TE will retry the transfer on the local bus when the FAILSAFE timer times out.

MODE 3 - FAILSAFE HALT. Once the FAILSAFE timer times out, all future transfers will be terminated with a target abort until the PCI master clears the interrupt.

MODE 4 - FAILSAFE SKIP. Once the FAILSAFE timer times out, the current transaction is discarded or skipped and the next transaction, whether a stored write in the FIFO or a new transaction, will be attempted.

BITS 15-0 ARE RESERVED: Write these bits as 0s.

TABLE 12. REG2 FAIL-SAFE TIMER REGISTER (READ 808H)	
BIT	DESCRIPTION
31(MSB)	0
•	•
•	•
•	•
16	0
15	FAIL-SAFE TIMER COUNT - BIT 15 (MSB)
•	•
•	•
•	•
0 (LSB)	FAIL-SAFE TIMER COUNT - BIT 0 (LSB)

FAIL-SAFE TIMER COUNT: Read this register to obtain the current value of the fail-safe timer. Default is 8400h.

TABLE 13. REG3 FAIL-SAFE TIMER PRELOAD REGISTER (READ/WRITE 80CH)	
BIT	DESCRIPTION
31(MSB)	0
•	•
•	•
•	•
16	0
15	FAIL-SAFE TIMER VALUE - BIT 15 (MSB)
•	•
•	•
•	•
0 (LSB)	FAIL-SAFE TIMER VALUE - BIT 0 (LSB)

FAIL-SAFE TIMER VALUE: Write to this register to set the value for the fail-safe timer. The default value is 8400h and no access to this register is needed for normal applications.

TABLE 14. REG4 DISCARD TIMER REGISTER (READ 810H)	
BIT	DESCRIPTION
31(MSB)	0
•	•
•	•
•	•
16	0
15	DISCARD TIMER CURRENT - BIT 15 (MSB)
•	•
•	•
•	•
0 (LSB)	DISCARD TIMER CURRENT - BIT 0 (LSB)

DISCARD TIMER CURRENT: Read this register to obtain the current value of the DISCARD TIMER. Default is 0000h.

TABLE 15. REG5 DISCARD TIMER PRELOAD REGISTER (READ/WRITE 814H)	
BIT	**DESCRIPTION**
31(MSB)	0
•	•
•	•
•	•
16	0
15	DISCARD TIMER VALUE - BIT 15 (MSB)
•	•
•	•
•	•
0 (LSB)	DISCARD TIMER VALUE - BIT 0 (LSB)

DISCARD TIMER VALUE: Write this register to set the value to be used for the discard timer. The default value is "0". The default value meets the PCI spec and no access to this register is needed for normal applications.

TABLE 16. REG6 GENERAL PURPOSE REGISTER (READ/WRITE 818H)	
BIT	**DESCRIPTION**
31(MSB)	RESERVED - BIT 31 (MSB)
•	•
•	•
•	•
0 (LSB)	RESERVED - BIT 0 (LSB)

This register will be all 0s after RST#. This read/write register is available for customer use, perhaps as a flag register for signaling between bus masters.

TABLE 17. REG7 RESERVED REGISTER (WRITE 81CH)	
BIT	**DESCRIPTION**
31(MSB)	RESERVED, WRITE AS 0 - BIT 31 (MSB)
•	•
•	•
•	•
1	CLEAR FAILSAFE INTERRUPT
0 (LSB)	RESERVED - BIT 0 (LSB)

This register will be all 0s after RST#. No access to this register is needed for normal applications.

BITS 31-2 ARE RESERVED AND MUST BE WRITTEN AS 0s

CLEAR FAILSAFE INTERRUPT: Clears the Failsafe Interrupt when set to "1". Failsafe interrupts can also be cleared via the Failsafe Interrupt Autoclear mechanism, enabled by bit 18 in Reg 1.

ACE RESET: Resets the ACE when set to "1".

PCI MINI-ACE MARK3/MICRO-ACE TE REGISTER AND MEMORY ADDRESSING

The software interface of the enhanced Mini-ACE portion of the PCI Mini-ACE Mark3/Micro ACE TE to the host processor consists of 24 internal operational registers for normal operation, an additional 24 test registers, plus 64K words of shared memory address space. The PCI Mini-ACE Mark3/Micro-ACE TE's 4K X 16 or 64K X 17 internal RAM resides in this address space.

For normal operation, the host processor only needs to access the lower 32 register address locations (internal address 00-1F). The next 32 locations (internal address 20-3F) should be reserved, since many of these are used for factory test.

INTERNAL REGISTERS

The internal address mapping, with the corresponding PCI BAR1 address offset, for the PCI Mini-ACE Mark3/Micro-ACE TE registers is illustrated in TABLE 18. Note that the address lines shown are the PCI Mini-ACE Mark3/Micro-ACE TE's internal ACE register bus and are left shifted 2 bits with respect to the PCI address: A0 = PCI A2, A1 = PCI A3, etc. For example, Interrupt mask register #1 is located at PCI address BAR1 offset + 0h, Configuration Register #1 is at BAR1 offset + 4h, etc. Note that the table below does not show the internal A5 register address line, which is normally 0 and is set only for access to the reserved factory test registers.

Also note that the ACE registers are internally 16 bits wide, appear in the lower 16 bits of a 32-bit PCI DWord and that the upper 16 bits will read as zeroes during a 32-bit PCI read.

The configuration registers will be cleared to 0000h after hardware or software reset, with the exception of the Enhanced CPU Access bit (bit 14 in Configuration register #6).

TABLE 18. ACE REGISTER ADDRESS MAPPING						
ADDRESS LINES					BAR1 ADDR OFFSET	REGISTER DESCRIPTION/ACCESSIBILITY
A4	A3	A2	A1	A0		
0	0	0	0	0	**00h**	Interrupt Mask Register #1 (RD/WR)
0	0	0	0	1	**04h**	Configuration Register #1 (RD/WR)
0	0	0	1	0	**08h**	Configuration Register #2 (RD/WR)
0	0	0	1	1	**0Ch**	Start/Reset Register (WR)
0	0	0	1	1	**0Ch**	Non-Enhanced BC/RT Command Stack Pointer / Enhanced BC Instruction List Pointer Register (RD)
0	0	1	0	0	10h	BC Control Word / RT Subaddress Control Word Register (RD/WR)
0	0	1	0	1	14h	Time Tag Register (RD/WR)
0	0	1	1	0	18h	Interrupt Status Register #1 (RD)
0	0	1	1	1	1Ch	Configuration Register #3 (RD/WR)
0	1	0	0	0	20h	Configuration Register #4 (RD/WR)
0	1	0	0	1	24h	Configuration Register #5 (RD/WR)
0	1	0	1	0	28h	RT / Monitor Data Stack Address Register (RD/WR)
0	1	0	1	1	2Ch	BC Frame Time Remaining Register (RD)
0	1	1	0	0	30h	BC Time Remaining to Next Message Register (RD)
0	1	1	0	1	34h	Non-Enhanced BC Frame Time / Enhanced BC Initial Instruction Pointer / RT Last Command / MT Trigger Word Register(RD/WR)
0	1	1	1	0	38h	RT Status Word Register (RD)
0	1	1	1	1	3Ch	RT BIT Word Register (RD)
1	0	0	0	0	40h	Test Mode Register 0
1	0	0	0	1	44h	Test Mode Register 1
1	0	0	1	0	48h	Test Mode Register 2
1	0	0	1	1	4Ch	Test Mode Register 3
1	0	1	0	0	50h	Test Mode Register 4
1	0	1	0	1	54h	Test Mode Register 5
1	0	1	1	0	58h	Test Mode Register 6
1	0	1	1	1	5Ch	Test Mode Register 7
1	1	0	0	0	60h	Configuration Register #6 (RD/WR)
1	1	0	0	1	64h	Configuration Register #7 (RD/WR)
1	1	0	1	0	68h	RESERVED
1	1	0	1	1	6Ch	BC Condition Code Register (RD)
1	1	0	1	1	6Ch	BC General Purpose Flag Register (WR)
1	1	1	0	0	70h	BIT Test Status Register (RD)
1	1	1	0	1	74h	Interrupt Mask Register #2 (RD/WR)
1	1	1	1	0	78h	Interrupt Status Register #2 (RD)
1	1	1	1	1	7Ch	BC General Purpose Queue Pointer / RT-MT Interrupt Status Queue Pointer Register (RD/WR)

TABLE 19. INTERRUPT MASK REGISTER #1 (READ/WRITE 00H,PCI 00H)	
BIT	**DESCRIPTION**
15(MSB)	RESERVED
14	RAM PARITY ERROR
13	BC/RT TRANSMITTER TIMEOUT
12	BC/RT COMMAND STACK ROLLOVER
11	MT COMMAND STACK ROLLOVER
10	MT DATA STACK ROLLOVER
9	HANDSHAKE FAIL
8	BC RETRY
7	RT ADDRESS PARITY ERROR
6	TIME TAG ROLLOVER
5	RT CIRCULAR BUFFER ROLLOVER
4	RT SUBADDRESS CONTROL WORD EOM
3	BC END OF FRAME
2	FORMAT ERROR
1	BC STATUS SET/RT MODE CODE/MT PATTERN TRIGGER
0(LSB)	END OF MESSAGE

TABLE 20. CONFIGURATION REGISTER #1 (READ/WRITE 01H, PCI 04H)				
BIT	**BC FUNCTION (Bits 11-0 Enhanced Mode Only)**	**RT WITHOUT ALTERNATE STATUS**	**RT WITH ALTERNATE STATUS (Enhanced Only)**	**MONITOR FUNCTION (Enhanced mode only bits 12-0)**
15 (MSB)	RT/$\overline{\text{BC-MT}}$ (logic 0)	(logic 1)	(logic 1)	(logic 0)
14	MT/$\overline{\text{BC-RT}}$ (logic 0)	(logic 0)	(logic 0)	(logic 1)
13	CURRENT AREA B/$\overline{\text{A}}$	CURRENT AREA B/$\overline{\text{A}}$	CURRENT AREA B/$\overline{\text{A}}$	CURRENT AREA B/$\overline{\text{A}}$
12	MESSAGE STOP-ON-ERROR	MESSAGE MONITOR ENABLED (MMT)	MESSAGE MONITOR ENABLED	MESSAGE MONITOR ENABLED
11	FRAME STOP-ON-ERROR	$\overline{\text{DYNAMIC BUS CONTROL ACCEPTANCE}}$	S10	TRIGGER WORD ENABLED
10	STATUS SET STOP-ON-MESSAGE	$\overline{\text{BUSY}}$	S09	START-ON-TRIGGER
9	STATUS SET STOP-ON-FRAME	$\overline{\text{SERVICE REQUEST}}$	S08	STOP-ON-TRIGGER
8	FRAME AUTO-REPEAT	$\overline{\text{SSFLAG}}$	S07	NOT USED
7	EXTERNAL TRIGGER ENABLED	$\overline{\text{RTFLAG}}$ (Enhanced Mode Only)	S06	EXTERNAL TRIGGER ENABLED
6	INTERNAL TRIGGER ENABLED	NOT USED	S05	NOT USED
5	INTERMESSAGE GAP TIMER ENABLED	NOT USED	S04	NOT USED
4	RETRY ENABLED	NOT USED	S03	NOT USED
3	DOUBLED/$\overline{\text{SINGLE}}$ RETRY	NOT USED	S02	NOT USED
2	BC ENABLED (Read Only)	NOT USED	S01	MONITOR ENABLED(Read Only)
1	BC FRAME IN PROGRESS (Read Only)	NOT USED	S00	MONITOR TRIGGERED (Read Only)
0 (LSB)	BC MESSAGE IN PROGRESS (Read Only)	RT MESSAGE IN PROGRESS (Enhanced mode only,Read Only)	RT MESSAGE IN PROGRESS (Read Only)	MONITOR ACTIVE (Read Only)

TABLE 21. CONFIGURATION REGISTER #2 (READ/WRITE 02H, PCI 08H)	
BIT	**DESCRIPTION**
15(MSB)	ENHANCED INTERRUPTS
14	RAM PARITY ENABLE
13	BUSY LOOKUP TABLE ENABLE
12	RESERVED FOR FUTURE USE, MUST BE 0
11	OVERWRITE INVALID DATA
10	256-WORD BOUNDARY DISABLE
9	TIME TAG RESOLUTION 2
8	TIME TAG RESOLUTION 1
7	TIME TAG RESOLUTION 0
6	CLEAR TIME TAG ON SYNCHRONIZE
5	LOAD TIME TAG ON SYNCHRONIZE
4	INTERRUPT STATUS AUTO CLEAR
3	LEVEL/$\overline{\text{PULSE}}$ INTERRUPT REQUEST
2	CLEAR SERVICE REQUEST
1	ENHANCED RT MEMORY MANAGEMENT
0(LSB)	SEPARATE BROADCAST DATA

TABLE 22. START/RESET REGISTER (WRITE 03H, PCI 0CH)	
BIT	**DESCRIPTION**
15(MSB)	RESERVED
14	RESERVED
13	RESERVED
12	RESERVED
11	CLEAR RT HALT
10	CLEAR SELF-TEST REGISTER
9	INITIATE RAM SELF-TEST
8	RESERVED
7	RESERVED
6	BC/MT STOP-ON-MESSAGE
5	BC STOP-ON-FRAME
4	TIME TAG TEST CLOCK
3	TIME TAG RESET
2	INTERRUPT RESET
1	BC/MT START
0(LSB)	RESET

TABLE 23. BC/RT COMMAND STACK POINTER REGISTER (READ 03H, PCI 0CH)	
BIT	**DESCRIPTION**
15(MSB)	COMMAND STACK POINTER 15
•	•
•	•
•	•
0(LSB)	COMMAND STACK POINTER 0

TABLE 24. BC CONTROL WORD REGISTER (READ/WRITE 04H, PCI 10H)	
BIT	**DESCRIPTION**
15(MSB)	RESERVED
14	MESSAGE ERROR MASK
13	SERVICE REQUEST BIT MASK
12	BUSY BIT MASK
11	SUBSYSTEM FLAG BIT MASK
10	TERMINAL FLAG BIT MASK
9	RESERVED BITS MASK
8	RETRY ENABLED
7	BUS CHANNEL A/$\overline{\text{B}}$
6	OFF-LINE SELF-TEST
5	MASK BROADCAST BIT
4	EOM INTERRUPT ENABLE
3	1553A/B SELECT
2	MODE CODE FORMAT
1	BROADCAST FORMAT
0(LSB)	RT-to-RT FORMAT

TABLE 25. RT SUBADDRESS CONTROL WORD (READ/WRITE 04H, PCI 10H)	
BIT	**DESCRIPTION**
15(MSB)	RX: GLOBAL CIRCULAR BUFFER ENABLE
14	TX: EOM INT
13	TX: CIRC BUF INT
12	TX: MEMORY MANAGEMENT 2 (MM2)
11	TX: MEMORY MANAGEMENT 1 (MM1)
10	TX: MEMORY MANAGEMENT 0 (MM0)
9	RX: EOM INT
8	RX: CIRC BUF INT
7	RX: MEMORY MANAGEMENT 2 (MM2)
6	RX: MEMORY MANAGEMENT 1 (MM1)
5	RX: MEMORY MANAGEMENT 0 (MM0)
4	BCST: EOM INT
3	BCST: CIRC BUF INT
2	BCST: MEMORY MANAGEMENT 2 (MM2)
1	BCST: MEMORY MANAGEMENT 1 (MM1)
0(LSB)	BCST: MEMORY MANAGEMENT 0 (MM0)

TABLE 26. TIME TAG REGISTER (READ/WRITE 05H, PCI 14H)	
BIT	**DESCRIPTION**
15(MSB)	TIME TAG 15
•	•
•	•
•	•
0(LSB)	TIME TAG 0

TABLE 27. INTERRUPT STATUS REGISTER #1 (READ 06H, PCI 18H)	
BIT	**DESCRIPTION**
15(MSB)	MASTER INTERRUPT
14	RAM PARITY ERROR
13	TRANSMITTER TIMEOUT
12	BC/RT COMMAND STACK ROLLOVER
11	MT COMMAND STACK ROLLOVER
10	MT DATA STACK ROLLOVER
9	HANDSHAKE FAIL
8	BC RETRY
7	RT ADDRESS PARITY ERROR
6	TIME TAG ROLLOVER
5	RT CIRCULAR BUFFER ROLLOVER
4	RT SUBADDRESS CONTROL WORD EOM
3	BC END OF FRAME
2	FORMAT ERROR
1	BC STATUS SET / RT MODE CODE / MT PATTERN TRIGGER
0(LSB)	END OF MESSAGE

TABLE 28. CONFIGURATION REGISTER #3 (READ/WRITE 07H, PCI 1CH)	
BIT	**DESCRIPTION**
15(MSB)	ENHANCED MODE ENABLE
14	BC/RT COMMAND STACK SIZE 1
13	BC/RT COMMAND STACK SIZE 0
12	MT COMMAND STACK SIZE 1
11	MT COMMAND STACK SIZE 0
10	MT DATA STACK SIZE 2
9	MT DATA STACK SIZE 1
8	MT DATA STACK SIZE 0
7	ILLEGALIZATION DISABLED
6	OVERRIDE MODE T/$\overline{R}$ ERROR
5	ALTERNATE STATUS WORD ENABLE
4	ILLEGAL RX TRANSFER DISABLE
3	RESERVED, SET TO 0
2	$\overline{RTFAIL}$ / $\overline{RTFLAG}$ WRAP ENABLE
1	1553A MODE CODES ENABLE
0(LSB)	ENHANCED MODE CODE HANDLING

TABLE 29. CONFIGURATION REGISTER #4 (READ/WRITE 08H, PCI 20H)	
BIT	**DESCRIPTION**
15(MSB)	External Bit Word Enable
14	Inhibit Bit Word if Busy
13	Mode Command Override Busy
12	Expanded Control Word
11	BROADCAST MASK ENA/XOR
10	RETRY IF -A AND M.E.
9	RETRY IF STATUS SET
8	1ST RETRY ALT/$\overline{SAME}$ BUS
7	2ND RETRY ALT/$\overline{SAME}$ BUS
6	VALID M.E./NO DATA
5	VALID BUSY/NO DATA
4	MT TAG GAP OPTION
3	LATCH RT ADDRESS WITH CONFIG #5
2	TEST MODE 2
1	TEST MODE 1
0(LSB)	TEST MODE 0

TABLE 30. CONFIGURATION REGISTER #5 (READ/WRITE 09H, PCI 24H)	
BIT	**DESCRIPTION**
15(MSB)	12 / $\overline{16}$ MHZ CLOCK SELECT
14	SINGLE-ENDED SELECT
13	EXTERNAL TX INHIBIT A
12	EXTERNAL TX INHIBIT B
11	EXPANDED CROSSING ENABLED
10	RESPONSE TIMEOUT SELECT 1
9	RESPONSE TIMEOUT SELECT 0
8	GAP CHECK ENABLED
7	BROADCAST DISABLED
6	RT ADDRESS LATCH/$\overline{TRANSPARENT}$
5	RT ADDRESS 4
4	RT ADDRESS 3
3	RT ADDRESS 2
2	RT ADDRESS 1
1	RT ADDRESS 0
0(LSB)	RT ADDRESS PARITY

TABLE 31. RT / MONITOR DATA STACK ADDRESS REGISTER (READ/WRITE 0AH, PCI 28H)	
BIT	**DESCRIPTION**
15(MSB)	RT / MONITOR DATA STACK ADDRESS 15
•	•
•	•
•	•
0(LSB)	RT / MONITOR DATA STACK ADDRESS 0

TABLE 32. BC FRAME TIME REMAINING REGISTER (READ/WRITE 0BH, PCI 2CH)	
BIT	**DESCRIPTION**
15(MSB)	BC FRAME TIME REMAINING 15
•	•
•	•
•	•
0(LSB)	BC FRAME TIME REMAINING 0

Note: resolution = 100 μs per LSB

TABLE 33. BC MESSAGE TIME REMAINING REGISTER (READ/WRITE 0CH, PCI 30H)	
BIT	**DESCRIPTION**
15(MSB)	BC MESSAGE TIME REMAINING 15
•	•
•	•
•	•
0(LSB)	BC MESSAGE TIME REMAINING 0

Note: resolution = 1 μs per LSB

TABLE 34. BC FRAME TIME / RT LAST COMMAND / MT TRIGGER REGISTER (READ/WRITE 0DH, PCI 34H)	
BIT	**DESCRIPTION**
15(MSB)	BIT 15
•	•
•	•
•	•
0(LSB)	BIT 0

TABLE 35. RT STATUS WORD REGISTER (READ/WRITE 0EH, PCI 38H)	
BIT	**DESCRIPTION**
15(MSB)	LOGIC “0”
14	LOGIC “0”
13	LOGIC “0”
12	LOGIC “0”
11	LOGIC “0”
10	MESSAGE ERROR
9	INSTRUMENTATION
8	SERVICE REQUEST
7	RESERVED
6	RESERVED
5	RESERVED
4	BROADCAST COMMAND RECEIVED
3	BUSY
2	SSFLAG
1	DYNAMIC BUS CONTROL ACCEPT
0(LSB)	TERMINAL FLAG

TABLE 36. RT BIT WORD REGISTER (READ 0FH, PCI 3CH)	
BIT	**DESCRIPTION**
15(MSB)	TRANSMITTER TIMEOUT
14	LOOP TEST FAILURE B
13	LOOP TEST FAILURE A
12	HANDSHAKE FAILURE
11	TRANSMITTER SHUTDOWN B
10	TRANSMITTER SHUTDOWN A
9	TERMINAL FLAG INHIBITED
8	BIT TEST FAIL
7	HIGH WORD COUNT
6	LOW WORD COUNT
5	INCORRECT SYNC RECEIVED
4	PARITY / MANCHESTER ERROR RECEIVED
3	RT-to-RT GAP / SYNCH / ADDRESS ERROR
2	RT-to-RT NO RESPONSE ERROR
1	RT-to-RT 2ND COMMAND WORD ERROR
0(LSB)	COMMAND WORD CONTENTS ERROR

TABLE 37. CONFIGURATION REGISTER #6 (READ/WRITE 18H, PCI 60H)	
BIT	**DESCRIPTION**
15(MSB)	ENHANCED BUS CONTROLLER
14	ENHANCED CPU ACCESS
13	COMMAND STACK POINTER INCREMENT ON EOM (RT, MT)
12	GLOBAL CIRCULAR BUFFER ENABLE
11	GLOBAL CIRCULAR BUFFER SIZE 2
10	GLOBAL CIRCULAR BUFFER SIZE 1
9	GLOBAL CIRCULAR BUFFER SIZE 0
8	DISABLE INVALID MESSAGES TO INTERRUPT STATUS QUEUE
7	DISABLE VALID MESSAGES TO INTERRUPT STATUS QUEUE
6	INTERRUPT STATUS QUEUE ENABLE
5	RT ADDRESS SOURCE
4	ENHANCED MESSAGE MONITOR
3	RESERVED
2	64-WORD REGISTER SPACE
1	CLOCK SELECT 1
0(LSB)	CLOCK SELECT 0

TABLE 38. CONFIGURATION REGISTER #7 (READ/WRITE 19H, PCI 64H)	
BIT	**DESCRIPTION**
15(MSB)	MEMORY MANAGEMENT BASE ADDRESS 15
14	MEMORY MANAGEMENT BASE ADDRESS 14
13	MEMORY MANAGEMENT BASE ADDRESS 13
12	MEMORY MANAGEMENT BASE ADDRESS 12
11	MEMORY MANAGEMENT BASE ADDRESS 11
10	MEMORY MANAGEMENT BASE ADDRESS 10
9	RESERVED
8	RESERVED
7	RESERVED
6	RESERVED
5	RESERVED
4	RT HALT ENABLE
3	1553B RESPONSE TIME
2	ENHANCED TIMETAG SYNCHRONIZE
1	ENHANCED BC WATCHDOG TIMER ENABLED
0(LSB)	MODE CODE RESET / INCMD SELECT

TABLE 39. BC CONDITION REGISTER (READ 1BH, PCI 6CH)	
BIT	**DESCRIPTION**
15(MSB)	ALWAYS
14	RETRY 1
13	RETRY 0
12	BAD MESSAGE
11	MESSAGE STATUS SET
10	GOOD BLOCK TRANSFER
9	FORMAT ERROR
8	NO RESPONSE
7	GENERAL PURPOSE FLAG 7
6	GENERAL PURPOSE FLAG 6
5	GENERAL PURPOSE FLAG 5
4	GENERAL PURPOSE FLAG 4
3	GENERAL PURPOSE FLAG 3
2	GENERAL PURPOSE FLAG 2
1	LESS THAN FLAG / GENERAL PURPOSE FLAG 1
0(LSB)	EQUAL FLAG / GENERAL PURPOSE FLAG 1

Note: If the Enhanced Mini-ACE is not online in enhanced BC mode (i.e., processing instructions), the BC condition code register will always return a value of 0000.

TABLE 40. BC GENERAL PURPOSE FLAG REGISTER (WRITE 1BH, PCI 6CH)	
BIT	**DESCRIPTION**
15(MSB)	CLEAR GENERAL PURPOSE FLAG 7
14	CLEAR GENERAL PURPOSE FLAG 6
13	CLEAR GENERAL PURPOSE FLAG 5
12	CLEAR GENERAL PURPOSE FLAG 4
11	CLEAR GENERAL PURPOSE FLAG 3
10	CLEAR GENERAL PURPOSE FLAG 2
9	CLEAR GENERAL PURPOSE FLAG 1
8	CLEAR GENERAL PURPOSE FLAG 0
7	SET GENERAL PURPOSE FLAG 7
6	SET GENERAL PURPOSE FLAG 6
5	SET GENERAL PURPOSE FLAG 5
4	SET GENERAL PURPOSE FLAG 4
3	SET GENERAL PURPOSE FLAG 3
2	SET GENERAL PURPOSE FLAG 2
1	SET GENERAL PURPOSE FLAG 1
0(LSB)	SET GENERAL PURPOSE FLAG 0

TABLE 41. BIT TEST STATUS REGISTER (READ 1CH, PCI 70H)	
BIT	**DESCRIPTION**
15(MSB)	LOGIC “0”
14	LOGIC “0”
13	LOGIC “0”
12	LOGIC “0”
11	LOGIC “0”
10	LOGIC “0”
9	LOGIC “0”
8	LOGIC “0”
7	RAM BUILT-IN TEST COMPLETE
6	RAM BUILT-IN TEST IN-PROGRESS
5	RAM BUILT-IN TEST IN-PASSED
4	LOGIC “0”
3	LOGIC “0”
2	LOGIC “0”
1	LOGIC “0”
0(LSB)	LOGIC “0”

TABLE 42. INTERRUPT MASK REGISTER #2 (READ/WRITE 1DH, PCI 74H)	
BIT	**DESCRIPTION**
15(MSB)	NOT USED
14	BC OP CODE PARITY ERROR
13	ILLEGAL COMMAND
12	GENERAL PURPOSE QUEUE / INTERRUPT STATUS QUEUE ROLLOVER
11	CALL STACK POINTER REGISTER ERROR
10	BC TRAP OP CODE
9	RT COMMAND STACK 50% ROLLOVER
8	RT CIRCULAR BUFFER 50% ROLLOVER
7	MONITOR COMMAND STACK 50% ROLLOVER
6	MONITOR DATA STACK 50% ROLLOVER
5	ENHANCED BC IRQ3
4	ENHANCED BC IRQ2
3	ENHANCED BC IRQ1
2	ENHANCED BC IRQ0
1	BIT TEST COMPLETE
0(LSB)	NOT USED

TABLE 43. INTERRUPT STATUS REGISTER #2 (READ 1EH, PCI 78H)	
BIT	**DESCRIPTION**
15(MSB)	MASTER INTERRUPT
14	BC OP CODE PARITY ERROR
13	ILLEGAL COMMAND
12	GENERAL PURPOSE QUEUE / INTERRUPT STATUS QUEUE ROLLOVER
11	CALL STACK POINTER REGISTER ERROR
10	BC TRAP OP CODE
9	RT COMMAND STACK 50% ROLLOVER
8	RT CIRCULAR BUFFER 50% ROLLOVER
7	MONITOR COMMAND STACK 50% ROLLOVER
6	MONITOR DATA STACK 50% ROLLOVER
5	ENHANCED BC IRQ3
4	ENHANCED BC IRQ2
3	ENHANCED BC IRQ1
2	ENHANCED BC IRQ0
1	BIT TEST COMPLETE
0(LSB)	INTERRUPT CHAIN BIT

TABLE 44. BC GENERAL PURPOSE QUEUE POINTER REGISTER RT, MT INTERRUPT STATUS QUEUE POINTER REGISTER (READ/WRITE 1FH, PCI 7CH)	
BIT	**DESCRIPTION**
15(MSB)	QUEUE POINTER BASE ADDRESS 15
14	QUEUE POINTER BASE ADDRESS 14
13	QUEUE POINTER BASE ADDRESS 13
12	QUEUE POINTER BASE ADDRESS 12
11	QUEUE POINTER BASE ADDRESS 11
10	QUEUE POINTER BASE ADDRESS 10
9	QUEUE POINTER BASE ADDRESS 9
8	QUEUE POINTER BASE ADDRESS 8
7	QUEUE POINTER BASE ADDRESS 7
6	QUEUE POINTER BASE ADDRESS 6
5	QUEUE POINTER BASE ADDRESS 5
4	QUEUE POINTER BASE ADDRESS 4
3	QUEUE POINTER BASE ADDRESS 3
2	QUEUE POINTER BASE ADDRESS 2
1	QUEUE POINTER BASE ADDRESS 1
0(LSB)	QUEUE POINTER BASE ADDRESS 0

NOTE: TABLES 45 TO 51 ARE NOT REGISTERS, BUT THEY ARE WORDS STORED IN RAM.

TABLE 45. BC MODE BLOCK STATUS WORD

BIT	DESCRIPTION
15(MSB)	EOM
14	SOM
13	CHANNEL B/$\overline{A}$
12	ERROR FLAG
11	STATUS SET
10	FORMAT ERROR
9	NO RESPONSE TIMEOUT
8	LOOP TEST FAIL
7	MASKED STATUS SET
6	RETRY COUNT 1
5	RETRY COUNT 0
4	GOOD DATA BLOCK TRANSFER
3	WRONG STATUS ADDRESS / NO GAP
2	WORD COUNT ERROR
1	INCORRECT SYNC TYPE
0(LSB)	INVALID WORD

TABLE 46. RT MODE BLOCK STATUS WORD

BIT	DESCRIPTION
15(MSB)	EOM
14	SOM
13	CHANNEL B/$\overline{A}$
12	ERROR FLAG
11	RT-to-RT FORMAT
10	FORMAT ERROR
9	NO RESPONSE TIMEOUT
8	LOOP TEST FAIL
7	DATA STACK ROLLOVER
6	ILLEGAL COMMAND WORD
5	WORD COUNT ERROR
4	INCORRECT DATA SYNC
3	INVALID WORD
2	RT-to-RT GAP / SYNC / ADDRESS ERROR
1	RT-to-RT 2ND COMMAND ERROR
0(LSB)	COMMAND WORD CONTENTS ERROR

TABLE 47. 1553 COMMAND WORD

BIT	DESCRIPTION
15(MSB)	REMOTE TERMINAL ADDRESS BIT 4
14	REMOTE TERMINAL ADDRESS BIT 3
13	REMOTE TERMINAL ADDRESS BIT 2
12	REMOTE TERMINAL ADDRESS BIT 1
11	REMOTE TERMINAL ADDRESS BIT 0
10	TRANSMIT / $\overline{\text{RECEIVE}}$
9	SUBADDRESS / MODE CODE BIT 4
8	SUBADDRESS / MODE CODE BIT 3
7	SUBADDRESS / MODE CODE BIT 2
6	SUBADDRESS / MODE CODE BIT 1
5	SUBADDRESS / MODE CODE BIT 0
4	DATA WORD COUNT / MODE CODE BIT 4
3	DATA WORD COUNT / MODE CODE BIT 3
2	DATA WORD COUNT / MODE CODE BIT 2
1	DATA WORD COUNT / MODE CODE BIT 1
0(LSB)	DATA WORD COUNT / MODE CODE BIT 0

TABLE 48. WORD MONITOR IDENTIFICATION WORD

BIT	DESCRIPTION
15(MSB)	GAP TIME
•	•
•	•
•	•
8	GAP TIME
7	WORD FLAG
6	$\overline{\text{THIS RT}}$
5	$\overline{\text{BROADCAST}}$
4	ERROR
3	COMMAND / $\overline{\text{DATA}}$
2	CHANNEL B/$\overline{A}$
1	CONTIGUOUS DATA / $\overline{\text{GAP}}$
0(LSB)	$\overline{\text{MODE\_CODE}}$

TABLE 49. MESSAGE MONITOR MODE BLOCK STATUS WORD	
BIT	**DESCRIPTION**
15(MSB)	EOM
14	SOM
13	CHANNEL B/$\overline{A}$
12	ERROR FLAG
11	RT-to-RT TRANSFER
10	FORMAT ERROR
9	NO RESPONSE TIMEOUT
8	GOOD DATA BLOCK TRANSFER
7	DATA STACK ROLLOVER
6	RESERVED
5	WORD COUNT ERROR
4	INCORRECT SYNC
3	INVALID WORD
2	RT-to-RT GAP / SYNC / ADDRESS ERROR
1	RT-to-RT 2ND COMMAND ERROR
0(LSB)	COMMAND WORD CONTENTS ERROR

TABLE 51. RT/MONITOR INTERRUPT STATUS WORD (FOR INTERRUPT STATUS QUEUE)		
BIT	**DEFINITION FOR MESSAGE INTERRUPT EVENT**	**DEFINITION FOR NON-MESSAGE INTERRUPT EVENT**
15	TRANSMITTER TIMEOUT	NOT USED
14	ILLEGAL COMMAND	NOT USED
13	MONITOR DATA STACK 50% ROLLOVER	NOT USED
12	MONITOR DATA STACK ROLLOVER	NOT USED
11	RT CIRCULAR BUFFER 50% ROLLOVER	NOT USED
10	RT CIRCULAR BUFFER ROLLOVER	NOT USED
9	MONITOR COMMAND (DESCRIPTOR) STACK 50% ROLLOVER	NOT USED
8	MONITOR COMMAND (DESCRIPTOR) STACK ROLLOVER	NOT USED
7	RT COMMAND (DESCRIPTOR) STACK 50% ROLLOVER	NOT USED
6	RT COMMAND (DESCRIPTOR) STACK ROLLOVER	NOT USED
5	HANDSHAKE FAIL	NOT USED
4	FORMAT ERROR	TIME TAG ROLLOVER
3	MODE CODE INTERRUPT	RT ADDRESS PARITY ERROR
2	SUBADDRESS CONTROL WORD EOM	NOT USED
1	END-OF-MESSAGE (EOM)	RAM PARITY ERROR
0	“1” FOR MESSAGE INTERRUPT EVENT “0” FOR NON-MESSAGE INTERRUPT EVENT	

TABLE 50. 1553B STATUS WORD	
BIT	**DESCRIPTION**
15(MSB)	REMOTE TERMINAL ADDRESS BIT 4
14	REMOTE TERMINAL ADDRESS BIT 3
13	REMOTE TERMINAL ADDRESS BIT 2
12	REMOTE TERMINAL ADDRESS BIT 1
11	REMOTE TERMINAL ADDRESS BIT 0
10	MESSAGE ERROR
9	INSTRUMENTATION
8	SERVICE REQUEST
7	RESERVED
6	RESERVED
5	RESERVED
4	BROADCAST COMMAND RECEIVED
3	BUSY
2	SSFLAG
1	DYNAMIC BUS CONTROL ACCEPTANCE
0(LSB)	TERMINAL FLAG

NON-TEST REGISTER FUNCTION SUMMARY

A summary of the PCI Mini-ACE Mark3/Micro-ACE TE’s 24 non-test registers follows.

INTERRUPT MASK REGISTERS #1 AND #2

Interrupt Mask Registers #1 and #2 are used to enable and disable interrupt requests for various events and conditions.

NOTE: Please see Appendix “F” of the Enhanced Mini-ACE User’s Guide for important information applicable only to RT MODE operation, enabling of the interrupt status queue and use of specific non-message interrupts.

CONFIGURATION REGISTERS #1 AND #2

Configuration Registers #1 and #2 are used to select the PCI Mini-ACE Mark3/Micro-ACE TE’s mode of operation, and for software control of RT Status Word bits, Active Memory Area, BC Stop-On-Error, RT Memory Management mode selection, and control of the Time Tag operation. Note that the LEVEL/$\overline{\text{PULSE}}$ INTERRUPT REQUEST bit in Configuration Register #2 MUST be set to 1 for correct PCI operation.

START/RESET REGISTER

The Start/Reset Register is used for "command" type functions such as software reset, BC/MT Start, Interrupt reset, Time Tag Reset, Time Tag Register Test, Initiate RAM self-test, Clear self-test register, and Clear RT Halt. The Start/Reset Register also includes provisions for stopping the BC in its auto-repeat mode, either at the end of the current message or at the end of the current BC frame.

BC/RT COMMAND STACK REGISTER

The BC/RT Command Stack Register allows the host CPU to determine the pointer location for the current or most recent message.

BC INSTRUCTION LIST POINTER REGISTER

The BC Instruction List Pointer Register may be read to determine the current location of the Instruction List Pointer for the Enhanced BC mode.

BC CONTROL WORD/RT SUBADDRESS CONTROL WORD REGISTER

In BC mode, the BC Control Word/RT Subaddress Control Word Register allows host access to the current word or most recent BC Control Word. The BC Control Word contains bits that select the active bus and message format, enable off-line self-test, masking of Status Word bits, enable retries and interrupts, and specify MIL-STD-1553A or -1553B error handling. In RT mode, this register allows host access to the current or most recent Subaddress Control Word. The Subaddress Control Word is used to select the memory management scheme and enable interrupts for the current message.

TIME TAG REGISTER

The Time Tag Register maintains the value of a real-time clock. The resolution of this register is programmable from among 2, 4, 8, 16, 32, and 64 µs/LSB. The Start-of-Message (SOM) and End-of-Message (EOM) sequences in BC, RT, and Message Monitor modes cause a write of the current value of the Time Tag Register to the stack area of the RAM.

INTERRUPT STATUS REGISTERS #1 AND #2

Interrupt Status Registers #1 and #2 allow the host processor to determine the cause of an interrupt request by means of one or two read accesses. The interrupt events of the two Interrupt Status Registers are mapped to correspond to the respective bit positions in the two Interrupt Mask Registers. Interrupt Status Register #2 contains an INTERRUPT CHAIN bit, used to indicate an interrupt event from Interrupt Status Register #1.

CONFIGURATION REGISTERS #3, #4, AND #5

Configuration Registers #3, #4, and #5 are used to enable many of the Mini-ACE Mark3/Micro-ACE TE's advanced features that were implemented by the prior generation products, the ACE and Mini-ACE (Plus). For BC, RT, and MT modes, use of the Enhanced Mode enables the various read-only bits in Configuration Register #1. For BC mode, Enhanced Mode features include the expanded BC Control Word and BC Block Status Word, additional Stop-On-Error and Stop-On-Status Set functions, frame auto-repeat, programmable intermessage gap times, automatic retries, expanded Status Word Masking, and the capability to generate interrupts following the completion of any selected message. For RT mode, the Enhanced Mode features include the expanded RT Block Status Word, combined RT/Selective Message Monitor mode, internal wrapping of the $\overline{\text{RTFAIL}}$ output signal to the $\overline{\text{RTFLAG}}$ RT Status Word bit, and the alternate (fully software programmable) RT Status Word. For MT mode, use of the Enhanced Mode enables the Selective Message Monitor, the combined RT/Selective Monitor modes, and the monitor triggering capability.

RT/MONITOR DATA STACK ADDRESS REGISTER

The RT/Monitor Data Stack Address Register provides a read/writable indication of the last data word stored for RT or Monitor modes.

BC FRAME TIME REMAINING REGISTER

The BC Frame Time Remaining Register provides a read-only indication of the time remaining in the current BC frame. In the enhanced BC mode, this timer may be used for minor or major frame control, or as a watchdog timer for the BC message sequence control processor. The resolution of this register is 100 µs/LSB.

BC TIME REMAINING TO NEXT MESSAGE REGISTER

The BC Time Remaining to Next Message Register provides a read-only indication of the time remaining before the start of the next message in a BC frame. In the enhanced BC mode, this timer may also be used for the BC message sequence control processor's Delay (DLY) instruction, or for minor or major frame control. The resolution of this register is 1 µs/LSB.

BC FRAME TIME/ RT LAST COMMAND /MT TRIGGER WORD REGISTER

In BC mode, this register is used to program the BC frame time, for use in the frame auto-repeat mode. The resolution of this register is 100 µs/LS, with a range up to 6.55 seconds. In RT mode, this register stores the current (or most previous) 1553 Command Word processed by the PCI Mini-ACE Mark3/Micro-ACE TE RT. In the Word Monitor mode, this register is used to specify a 16-bit Trigger (Command) Word. The Trigger Word may be used to start or stop the monitor, or to generate interrupts.

BC INITIAL INSTRUCTION LIST POINTER REGISTER

The BC Initial Instruction List Pointer Register enables the host to assign the starting address for the enhanced BC Instruction List.

RT STATUS WORD REGISTER AND BIT WORD REGISTERS

The RT Status Word Register and BIT Word Registers provide read-only indications of the RT Status and BIT Words.

CONFIGURATION REGISTERS #6 AND #7

Configuration Registers #6 and #7 are used to enable the PCI Mini-ACE Mark3/Micro-ACE TE features that extend beyond the architecture of the ACE/Mini-ACE (Plus). These include the Enhanced BC mode; Enhanced CPU Access (note that this bit is the only configuration bit that is SET after reset), RT Global Circular Buffer (including buffer size); the RT/MT Interrupt Status Queue, including valid/invalid message filtering; enabling a software-assigned RT address; clock frequency selection; a base

address for the "non-data" portion of Mini-ACE Mark3/Micro-ACE TE memory; LSB filtering for the Synchronize (with data) time tag operations; and enabling a watchdog timer for the Enhanced BC message sequence control engine.

NOTE: Please see Appendix "F" of the Enhanced Mini-ACE User's Guide for important information applicable only to RT MODE operation, enabling of the interrupt status queue **and** use of specific non-message interrupts.

BC CONDITION CODE REGISTER

The BC Condition Code Register is used to enable the host processor to read the current value of the Enhanced BC Message Sequence Control Engine's condition flags.

BC GENERAL PURPOSE FLAG REGISTER

The BC General Purpose Flag Register allows the host processor to be able to set, clear, or toggle any of the Enhanced BC Message Sequence Control Engine's General Purpose condition flags.

BIT TEST STATUS REGISTER

The BIT Test Status Register is used to provide read-only access to the status of the RAM built-in self-tests (BIT).

BC GENERAL PURPOSE QUEUE POINTER

The BC General Purpose Queue Pointer provides a means for initializing the pointer for the General Purpose Queue, for the Enhanced BC mode. In addition, this register enables the host to determine the current location of the General Purpose Queue pointer, which is incremented internally by the Enhanced BC message sequence control engine.

RT/MT INTERRUPT STATUS QUEUE POINTER

The RT/MT Interrupt Status Queue Pointer provides a means for initializing the pointer for the Interrupt Status Queue, for RT, MT, and RT/MT modes. In addition, this register enables the host to determine the current location of the Interrupt Status Queue pointer, which is incremented by the RT/MT message processor.

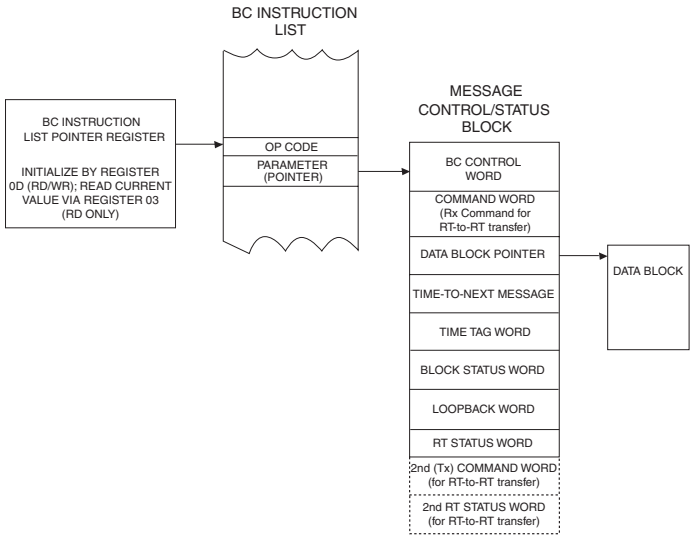


FIGURE 2. BC MESSAGE SEQUENCE CONTROL

BUS CONTROLLER (BC) ARCHITECTURE

The BC functionality for the PCI Mini-ACE Mark3/Micro-ACE TE includes two separate architectures: (1) the older, non-Enhanced Mode, which provides complete compatibility with the previous ACE and Mini-ACE (Plus) generation products; and (2) the newer, Enhanced BC mode. The Enhanced BC mode offers several new powerful architectural features. These include the incorporation of a highly autonomous BC message sequence control engine, which greatly serves to offload the operation of the host CPU.

The Enhanced BC's message sequence control engine provides a high degree of flexibility for implementing major and minor frame scheduling; capabilities for inserting asynchronous messages in the middle of a frame; to separate 1553 message data from control/status data for the purpose of implementing double buffering and performing bulk data transfers; for implementing message retry schemes, including the capability for automatic bus channel switchover for failed messages; and for reporting various conditions to the host processor by means of 4 user-defined interrupts and a general purpose queue.

In both the non-Enhanced and Enhanced BC modes, the PCI Mini-ACE Mark3/Micro-ACE TE BC implements all MIL-STD-1553B message formats. Message format is programmable on a message-by-message basis by means of the BC Control Word and the T/R bit of the Command Word for the respective message. The BC Control Word allows 1553 message format, 1553A/B type RT, bus channel, self-test, and Status Word masking to be specified on an individual message basis. In addition, automatic retries and/or interrupt requests may be enabled or disabled for individual messages. The BC performs all error checking required by MIL-STD-1553B. This includes validation of response time, sync type and sync encoding, Manchester II encoding, parity, bit count, word count, Status Word RT Address field, and various RT-to-RT transfer errors. The PCI Mini-ACE Mark3/Micro-ACE TE BC response timeout value is programmable with choices of 18, 22, 50, and 130 µs. The longer response timeout values allow for operation over long buses and/or the use of repeaters.

In its non-Enhanced Mode, the PCI Mini-ACE Mark3/Micro-ACE TE may be programmed to process BC frames of up to 512 messages with no processor intervention. In the Enhanced BC mode, there is no explicit limit to the number of messages that may be processed in a frame. In both modes, it is possible to program for either single frame or frame auto-repeat operation. In the auto-repeat mode, the frame repetition rate may be controlled either internally, using a programmable BC frame timer, or from an external trigger input.

ENHANCED BC MODE: MESSAGE SEQUENCE CONTROL

One of the major new architectural features of the PCI Mini-ACE Mark3/Micro-ACE TE series is its advanced capability for BC message sequence control. The PCI Mini-ACE Mark3/Micro-ACE TE supports highly autonomous BC operation, which greatly offloads the operation of the host processor.

The operation of the PCI Mini-ACE Mark3/Micro-ACE TE's message sequence control engine is illustrated in FIGURE 2. The BC message sequence control involves an instruction list pointer register; an instruction list which contains multiple 2-word entries; a message control/status stack, which contains multiple 8-word or 10-word descriptors; and data blocks for individual messages.

The initial value of the instruction list pointer register is initialized by the host processor (via Register 0D), and is incremented by the BC message sequence processor (host readable via Register 03). During operation, the message sequence control processor fetches the operation referenced by the instruction list pointer register from the instruction list.

Note that the pointer parameter referencing the first word of a message's control/status block (the BC Control Word) must contain an address value that is **modulo 8**. Also, note that if the message is an RT-to-RT transfer, the pointer parameter must contain an address value that is **modulo 16**.

OP CODES

The instruction list pointer register references a pair of words in the BC instruction list: an op code word, followed by a parameter word. The format of the op code word, which is illustrated in FIGURE 3, includes a 5-bit op code field and a 5-bit condition code field. The op code identifies the instruction to be executed by the BC message sequence controller.

Most of the operations are conditional, with execution dependent on the contents of the condition code field. Bits 3-0 of the condition code field identifies a particular condition. Bit 4 of the condition code field identifies the logic sense ("1" or "0") of the selected condition code on which the conditional execution is dependent. TABLE 52 lists all the op codes, along with their respective mnemonic, code value, parameter, and description. TABLE 53 defines all the condition codes.

Eight of the condition codes (8 through F) are set or cleared as the result of the most recent message. The other eight are defined as "General Purpose" condition codes GP0 through GP7. There are three mechanisms for programming the values of the General Purpose Condition Code bits: (1) They may be set, cleared, or toggled by the host processor, by means of the BC GENERAL PURPOSE FLAG REGISTER; (2) they may be set, cleared, or toggled by the BC message sequence control processor, by means of the GP Flag Bits (FLG) instruction; and (3) GP0 and GP1 only (but none of the others) may be set or cleared by means of the BC message sequence control processor's Compare Frame Timer (CFT) or Compare Message Timer (CMT) instructions.

The host processor also has read-only access to the BC condition codes by means of the BC CONDITION CODE REGISTER.

Note that four (4) instructions are **unconditional**. These are Compare to Frame Timer (CFT), Compare to Message Timer (CMT), GP Flag Bits (FLG), and Execute and Flip (XQF). For these instructions, the Condition Code Field is "don't care". That is, these instructions are **always** executed, regardless of the result of the condition code test.

All of the other instructions are conditional. That is, they will only be executed if the condition code specified by the condition code field in the op code word tests true. If the condition code field tests false, the instruction list pointer will skip down to the next instruction.

As shown in TABLE 52, many of the operations include a single-word parameter. For an XEQ (execute message) operation, the parameter is a pointer to the start of the message's Control / Status block. For other operations, the parameter may be an address, a time value, an interrupt pattern, a mechanism to set or clear general purpose flag bits, or an immediate value. For several op codes, the parameter is "don't care" (not used).

As described above, some of the op codes will cause the message sequence control processor to execute messages. In this case, the parameter references the first word of a message Control/Status block. With the exception of RT-to-RT transfer messages, all message status/control blocks are eight words long: a block control word, time-to-next-message parameter, data block pointer, command word, status word, loopback word, block status word, and time tag word.

In the case of an RT-to-RT transfer message, the size of the message control/status block increases to 16 words. However, in this case, the last six words are not used; the ninth and tenth words are for the second command word and second status word.

The third word in the message control/status block is a pointer that references the first word of the message's data word block. Note that the data word block stores only data words, which are to be either transmitted or received by the BC. By segregating data words from command words, status words, and other control and "housekeeping" functions, this architecture enables the

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Odd Parity	OpCode Field					0	1	0	1	0	Condition Code Field				

FIGURE 3. BC OP CODE FORMAT

TABLE 52. BC OPERATIONS FOR MESSAGE SEQUENCE CONTROL

INSTRUCTION	MNEMONIC	OP CODE (HEX)	PARAMETER	CONDITIONAL OR UNCONDITIONAL	DESCRIPTION
Execute Message	XEQ	0001	Message Control / Status Block Address	Conditional **(See Note)**	Executes the message at the specified Message Control/Status Block Address if the condition flag tests TRUE, otherwise continue execution at the next OpCode in the instruction list.
Jump	JMP	0002	Instruction List Address	Conditional	Jump to the OpCode specified in the Instruction List if the condition flag tests TRUE, otherwise continue execution at the next OpCode in the instruction list.
Subroutine Call	CAL	0003	Instruction List Address	Conditional	Jump to the OpCode specified by the Instruction List Address and push the Address of the Next OpCode on the Call Stack if the condition flag tests TRUE, otherwise continue execution at the next OpCode in the instruction list. Note that the maximum depth of the subroutine call stack is **four**.
Subroutine Return	RTN	0004	Not Used (Don't Care)	Conditional	Return to the OpCode popped off the Call Stack if the condition flag tests TRUE, otherwise continue execution at the next OpCode in the instruction list.
Interrupt Request	IRQ	0006	Interrupt Bit Pattern in 4 LS bits	Conditional	Generate an interrupt if the condition flag tests TRUE, otherwise continue execution at the next OpCode in the instruction list. The passed parameter (Interrupt Bit Pattern) specifies which of the ENHANCED BC IRQ bit(s) (bits 5-2) will be set in Interrupt Status Register #2. Only the four LSBs of the passed parameter are used. A parameter where the four LSBs are logic "0" will **not** generate an interrupt.
Halt	HLT	0007	Not Used (Don't Care)	Conditional	Stop execution of the Message Sequence Control Program until a new BC Start is issued by the host if the condition flag tests TRUE, otherwise continue execution at the next OpCode in the instruction list.
Delay	DLY	0008	Delay Time Value (Resolution = 1µS / LSB)	Conditional	Delay the time specified by the Time parameter before executing the next OpCode if the condition flag tests TRUE, otherwise continue execution at the next OpCode without delay. The delay generated will use the Time to Next Message Timer.
Wait Until Frame Timer = 0	WFT	0009	Not Used (Don't Care)	Conditional	Wait until Frame Time counter is equal to Zero before continuing execution of the Message Sequence Control Program if the condition flag tests TRUE, otherwise continue execution at the next OpCode without delay.
Compare to Frame Timer	CFT	000A	Delay Time Value (Resolution = 100µS / LSB)	Unconditional	Compare Time Value to Frame Time Counter, and set or clear the LT and EQ flag based on the results of the compare.
Compare to Message Timer	CMT	000B	Delay Time Value (Resolution = 1µS / LSB)	Unconditional	Compare Time Value to Frame Time Counter, and set or clear the LT and EQ flag based on the results of the compare.
GP Flag Bits	FLG	000C	Used to set, clear, or toggle GP(General Purpose) Flag bits (See description)	Unconditional	Used to set, toggle, or clear any or all of the eight general purpose flags. The table below illustrates the use of the GP Flag Bits instruction for the case of GP0 (General Purpose Flag 0). Bits 1 and 9 of the parameter byte affect flag GP1, bits 2 and 10 effect GP2, etc., according to the following rules:

Bit 8	Bit 0	Effect on GP0
0	0	No Change
0	1	Set Flag
1	0	Clear Flag
1	1	Toggle Flag

TABLE 52. BC OPERATIONS FOR MESSAGE SEQUENCE CONTROL (CONT.)					
INSTRUCTION	**MNEMONIC**	**OP CODE (HEX)**	**PARAMETER**	**CONDITIONAL OR UNCONDITIONAL**	**DESCRIPTION**
Load Time Tag Counter	LTT	000D	Time Value. Resolution (µs/LSB) is defined by bits 9, 8, and 7 of Configuration Register #2.	Conditional	Load Time Tag Counter with Time Value if the condition flag tests TRUE, otherwise continue execution at the next OpCode in the instruction list.
Load Frame Timer	LFT	000E	Time Value (resolution = 100 µs/LSB)	Conditional	Load Frame Timer Register with the Time Value parameter if the condition flag tests TRUE, otherwise continue execution at the next OpCode in the instruction list.
Start Frame Timer	SFT	000F	Not Used (Don't Care)	Conditional	Start Frame Time Counter with Time Value in Time Frame register if the condition flag tests TRUE, otherwise continue execution at the next OpCode in the instruction list.
Push Time Tag Register	PTT	0010	Not Used (Don't Care)	Conditional	Push the value of the Time Tag Register on the General Purpose Queue if the condition flag tests TRUE, otherwise continue execution at the next OpCode in the instruction list.
Push Block Status Word	PBS	0011	Not Used (Don't Care)	Conditional	Push the Block Status Word for the most recent message on the General Purpose Queue if the condition flag tests TRUE, otherwise continue execution at the next OpCode in the instruction list.
Push Immediate Value	PSI	0012	Immediate Value	Conditional	Push Immediate data on the General Purpose Queue if the condition flag tests TRUE, otherwise continue execution at the next OpCode in the instruction list.
Push Indirect	PSM	0013	Memory Address	Conditional	Push the data stored at the specified memory location on the General Purpose Queue if the condition flag tests TRUE, otherwise continue execution at the next OpCode in the instruction list.
Wait for External Trigger	WTG	0014	Not Used (Don't Care)	Conditional	Wait for a logic "0"-to-logic "1" transition on the EXT_TRIG input signal before proceeding to the next OpCode in the instruction list if the condition flag tests TRUE, otherwise continue execution at the next OpCode without delay.
Execute and Flip	XQF	0015	Message Control / Status Block Address	Unconditional	Execute (unconditionally) the message referenced by the Message Control/Status Block Address. Following the processing of this message, if the condition flag tests TRUE, then flip bit 4 in the Message Control/Status Block Address, and store the new Message Block Address as the updated value of the parameter following the XQF instruction code. As a result, the **next** time that this line in the instruction list is executed, the Message Control/Status Block at the **updated** address (**old address XOR 0010h**), rather than the old address, will be processed. If the condition flag tests FALSE, the value of the Message Control/Status Block Address parameter will not change.

NOTE: While the XEQ (Execute Message) instruction is conditional, not all condition codes may be used to enable its use. The ALWAYS and NEVER condition codes may be used. The eight general purpose flag bits, GP0 through GP7, may also be used. However, if GP0 through GP7 are used, it is imperative that the host processor **not** modify the value of the specific general purpose flag bit that enabled a particular message while that message is being processed. Similarly, the LT, GT-EQ, EQ, and NE flags, which the BC only updates by means of the CFT and CMT instructions, may also be used. However, these two flags are dual use. Therefore, if these are used, it is imperative that the host processor not modify the value of the specific flag (GP0 or GP1) that enabled a particular message while that message is being processed. The NORESP, FMT ERR, GD BLK XFER, MASKED STATUS SET, BAD MESSAGE, RETRY0, and RETRY1 condition codes are **not** available for use with the XEQ instruction and should not be used to enable its execution.

TABLE 53. CONDITION CODES

BIT CODE	NAME (BIT 4 = 0)	INVERSE (BIT 4 = 1)	FUNCTIONAL DESCRIPTION
0	LT/GP0	GT/ $\overline{\text{GP0}}$	Less Than Flag set or cleared after CFT or CMT operation. Also, General Purpose Flag 0 may be set or cleared by a FLG operation.
1	EQ/GP1	NE/$\overline{\text{GP1}}$	Equal Flag set or cleared after CFT or CMT operation. Also, General Purpose Flag 1 may also be set or cleared by a FLG operation.
2 3 4 5 6 7	GP2 GP3 GP4 GP5 GP6 GP7	$\overline{\text{GP2}}$ $\overline{\text{GP3}}$ $\overline{\text{GP4}}$ $\overline{\text{GP5}}$ $\overline{\text{GP6}}$ $\overline{\text{GP7}}$	General Purpose Flags may be set, cleared, or toggled by a FLG operation. The host processor can set, clear, or toggle these flags in the same way as the FLG instruction by means of the BC GENERAL PURPOSE FLAG REGISTER.
8	NORESP	$\overline{\text{RESP}}$	NORESP indicates that an RT has either not responded or has responded later than the BC No Response Timeout time. The PCI Mini-ACE Mark3/Micro-ACE TE's No Response Timeout Time is defined per MIL-STD-1553B as the time from the mid-bit crossing of the parity bit to the mid-sync crossing of the RT Status Word. The value of the No Response Timeout value is programmable from among the nominal values 18.5, 22.5, 50.5, and 130 µs (±1 µs) by means of bits 10 and 9 of Configuration Register #5.
9	FMT ERR	$\overline{\text{FMT ERR}}$	FMT ERR indicates that the received portion of the most recent message contained one or more violations of the 1553 message validation criteria (sync, encoding, parity, bit count, word count, etc.), or the RT's status word received from a responding RT contained an incorrect RT address field.
A	GD BLK XFER	$\overline{\text{GD BLK XFER}}$	For the most recent message, GD BLK XFER will be set to logic "1" following completion of a valid (error-free) RT-to-BC transfer, RT-to-RT transfer, or transmit mode code with data message. This bit is set to logic "0" following an invalid message. GOOD DATA BLOCK TRANSFER is **always** logic "0" following a BC-to-RT transfer, a mode code with data, or a mode code without data. The Loop Test has **no effect** on GOOD DATA BLOCK TRANSFER. GOOD DATA BLOCK TRANSFER may be used to determine if the transmitting portion of an RT-to-RT transfer was error free.
B	MASKED STATUS BIT	$\overline{\text{MASKED STATUS BIT}}$	Indicates that one or both of the following conditions have occurred for the most recent message: (1) If one (or more) of the Status Mask bits (14 through 9) in the BC Control Word is logic "0" **and** the corresponding bit(s) is (are) set (logic "1") in the received RT Status Word. In the case of the RESERVED BITS MASK (bit 9) set to logic "0", any or all of the 3 Reserved Status Word bits being set will result in a MASKED STATUS SET condition; and/or (2) If BROADCAST MASK ENABLED/$\overline{\text{XOR}}$ (bit 11 of Configuration Register #4) is logic "1" **and** the MASK BROADCAST bit of the message's BC Control Word is logic "0" and the BROADCAST COMMAND RECEIVED bit in the received RT Status Word is logic "1".
C	BAD MESSAGE	GOOD MESSAGE	BAD MESSAGE indicates either a format error, loop test fail, or no response error for the most recent message. Note that a "Status Set" condition has **no effect** on the "BAD MESSAGE/GOOD MESSAGE" condition code.
D E	RETRY0 RETRY1	$\overline{\text{RETRY0}}$ $\overline{\text{RETRY1}}$	These two bits reflect the retry status of the most recent message. The number of times that the message was retried is delineated by these two bits as shown below: RETRY COUNT 1 (bit 14) / RETRY COUNT 0 (bit 13) / Number of Message Retries 0 / 0 / 0 0 / 1 / 1 1 / 0 / N/A 1 / 1 / 2
F	ALWAYS	NEVER	The ALWAYS bit should be set (bit 4 = 0) to designate an instruction as unconditional. The NEVER bit (bit 4 =1) can be used to implement an NOP instruction.

use of convenient, usable data structures, such as circular buffers and double buffers.

Other operations support program flow control; i.e., jump and call capability. The call capability includes maintenance of a call stack which supports a maximum of four (4) entries; there is also a return instruction. In the case of a call stack overrun or underrun, the BC will issue a CALL STACK POINTER REGISTER ERROR interrupt, if enabled.

Other op codes may be used to delay for a specified time; start a new BC frame; wait for an external trigger to start a new frame; perform comparisons based on frame time and time-to-next message; load the time tag or frame time registers; halt; and issue host interrupts. In the case of host interrupts, the message control processor passes a 4-bit user-defined interrupt vector to the host, by means of the PCI Mini-ACE Mark3/Micro-ACE TE's Interrupt Status Register.

The purpose of the FLG instruction is to enable the message sequence controller to set, clear, or toggle the value(s) of any or all of the eight general purpose condition flags.

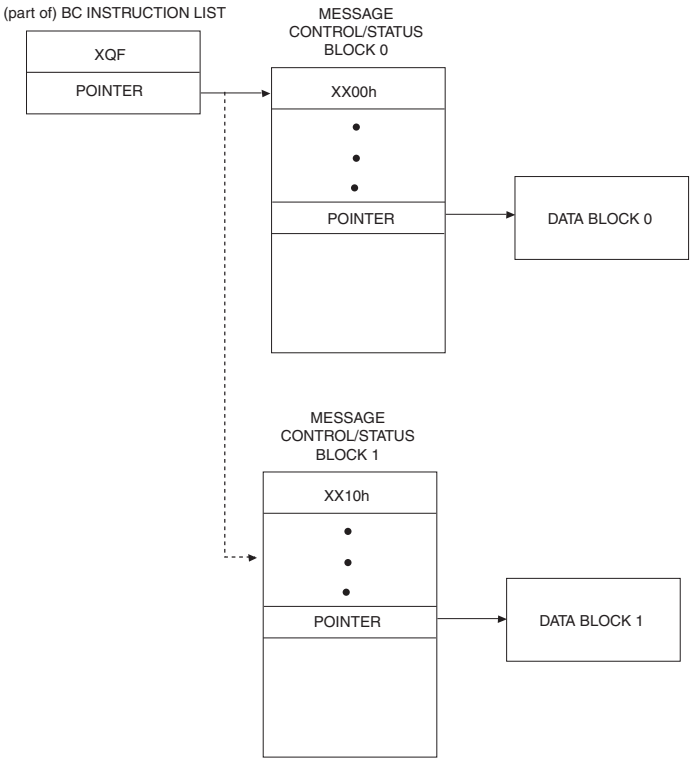


FIGURE 4. EXECUTE and FLIP (XQF) OPERATION

The op code parity bit encompasses all sixteen bits of the op code word. This bit must be programmed for odd parity. If the message sequence control processor fetches an undefined op code word, an op code word with even parity, or bits 9-5 of an op code word do not have a binary pattern of 01010, the message sequence control processor will immediately halt the BC's operation. In addition, if enabled, a BC TRAP OP CODE interrupt will be issued. Also, if enabled, a parity error will result in an OP CODE PARITY ERROR interrupt. TABLE 53 describes the Condition Codes.

BC MESSAGE SEQUENCE CONTROL

The PCI Mini-ACE Mark3/Micro-ACE TE BC message sequence control capability enables a high degree of offloading of the host processor. This includes using the various timing functions to enable autonomous structuring of major and minor frames. In addition, by implementing conditional jumps and subroutine calls, the message sequence control processor greatly simplifies the insertion of asynchronous, or "out-of-band" messages.

Execute and Flip Operation. The PCI Mini-ACE Mark3/Micro-ACE TE BC's XQF, or "Execute and Flip" operation, provides some unique capabilities. Following execution of this unconditional instruction, if the condition code tests TRUE, the BC will modify the value of the current XQF instruction's pointer parameter by toggling bit 4 of the pointer. That is, if the selected condition flag tests true, the value of the parameter will be **updated** to the value = **old address XOR 0010h**. As a result, the next time that this line in the instruction list is executed, the Message Control/Status Block at the updated address (old address XOR 0010h) will be processed, rather than the one at the old address. The operation of the XQF instruction is illustrated in FIGURE 4.

There are multiple ways of utilizing the "execute and flip" instruction. One is to facilitate the implementation of a double buffering data scheme for individual messages. This allows the message sequence control processor to "ping-pong" between a pair of data buffers for a particular message. By doing so, the host processor can access one of the two Data Word blocks, while the BC reads or writes the alternate Data Word block.

A second application of the "execute and flip" capability is in conjunction with message retries. This allows the BC to not only switch buses when retrying a failed message, but to automatically switch buses **permanently** for all future times that the same message is to be processed. This not only provides a high degree of autonomy from the host CPU, but saves BC bandwidth, by eliminating the need for future attempts to process messages on an RT's failed channel.

General Purpose Queue. The PCI Mini-ACE Mark3/Micro-ACE TE BC allows for the creation of a general purpose queue. This data structure provides a means for the message sequence processor to convey information to the BC host. The BC op code repertoire provides mechanisms to push various items on this queue. These include the contents of the Time Tag Register, the Block Status Word for the most recent message, an immediate data value, or the contents of a specified memory address.

FIGURE 5 illustrates the operation of the BC General Purpose Queue. Note that the BC General Purpose Queue Pointer Register will always point to the **next** address location (modulo 64); that is, the location **following** the last location written by the BC message sequence control engine.

If enabled, a BC GENERAL PURPOSE QUEUE ROLLOVER interrupt will be issued when the value of the queue pointer address rolls over at a 64-word boundary. The rollover will always occur at a modulo 64 address.

REMOTE TERMINAL (RT) ARCHITECTURE

The PCI Mini-ACE Mark3/Micro-ACE TE's RT architecture builds upon that of the ACE and Mini-ACE. The PCI Mini-ACE Mark3/Micro-ACE TE provides multiprotocol support, with full compliance to all of the commonly used data bus standards, including MIL-STD-1553A, MIL-STD-1553B Notice 2, STANAG 3838, General Dynamics 16PP303, and McAirA3818, A5232, and A5690. For the PCI Mini-ACE Mark3/Micro-ACE TE RT mode, there is programmable flexibility enabling the RT to be configured to fulfill any set of system requirements. This includes the capability to meet the MIL-STD-1553A response time requirement of 2 to 5 µs, and multiple options for mode code subaddresses, mode codes, RT status word, and RT BIT word.

The PCI Mini-ACE Mark3/Micro-ACE TE RT protocol design implements all of the MIL-STD-1553B message formats and dual redundant mode codes. The design has passed validation testing for MIL-STD-1553B compliance. The PCI Mini-ACE Mark3/Micro-ACE TE RT performs comprehensive error checking including word and format validation, and checks for various RT-to-RT transfer errors. One of the main features of the PCI Mini-ACE Mark3/Micro-ACE TE RT is its choice of memory management options. These include single buffering by subaddress, circular buffering by individual subaddresses, and global circular buffering for multiple (or all) subaddresses.

Other features of the PCI Mini-ACE Mark3/Micro-ACE TE RT include a set of interrupt conditions, an interrupt status queue with filtering based on valid and/or invalid messages, internal command illegalization, programmable busy by subaddress, multiple options on time tagging.

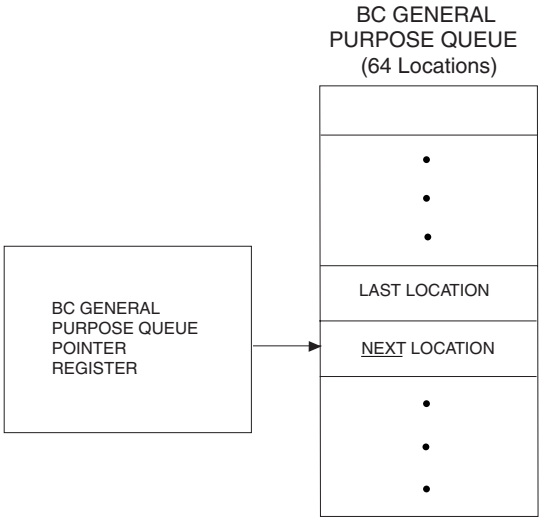


FIGURE 5. BC GENERAL PURPOSE QUEUE

RT MEMORY ORGANIZATION

TABLE 54 illustrates a typical memory map for a PCI Mini-ACE Mark3/Micro-ACE TE RT with 4K RAM. Note that this table and subsequent references to it are using word addressing: PCI BAR0 address offsets (byte addresses) are TWO times the word addresses indicated. The two Stack Pointers reside in fixed locations in the shared RAM address space: address 0100h (PCI BAR0 offset 0200h) for the Area A Stack Pointer and address 0104h (PCI BAR0 offset 208h) for the Area B Stack Pointer. In addition to the Stack Pointer, there are several other areas of the shared RAM address space that are designated as fixed locations (all shown in bold). These are for the Area A and Area B lookup tables, the illegalization lookup table, the busy lookup table, and the mode code data tables.

The RT lookup tables provide a mechanism for allocating data blocks for individual transmit, receive, or broadcast subaddresses. The RT lookup tables include subaddress control words as well as the individual data block pointers. If command illegalization is used, address range 0300-03FF is used for command illegalizing. The descriptor stack RAM area, as well as the individual data blocks, may be located in any of the non-fixed areas in the shared RAM address space.

Note that in TABLE 54, there is no area allocated for "Stack B". This is shown for purpose of illustration. Also, note that in TABLE 54, the allocated area for the RT command stacks is 256 words. However, larger stack sizes are possible. That is, the RT command stack size may be programmed for 256 words (64 messages), 512, 1024, or 2048 words (512 messages) by means of bits 14 and 13 of Configuration Register 3.

TABLE 54. TYPICAL RT MEMORY MAP (SHOWN AS 4K RAM)

WORD ADDRESS (HEX)	PCI BAR0 OFFSET(HEX)	DESCRIPTION
0000-00FF	0000-01FE	STACK A
0100	0200	**STACK POINTER A**
0101	0202	**GLOBAL CIRCULAR BUFFER A POINTER**
0102-0103	0204-0206	RESERVED
0104	0208	**STACK POINTER B**
0105	020A	**GLOBAL CIRCULAR BUFFER B POINTER**
0106-0107	020C-020E	RESERVED
0108-010F	0210-021E	**MODE CODE SELECTIVE INTERRUPT TABLE**
0110-013F	0220-027E	**MODE CODE DATA**
0140-01BF	0280-037E	**LOOKUP TABLE A**
01C0-023F	0380-047E	**LOOKUP TABLE B**
0240-0247	0480-048E	**BUSY BIT LOOKUP TABLE**
0248-025F	0490-04BE	(NOT USED)
0260-027F	04C0-04FE	DATA BLOCK 0
0280-02FF	0500-05FE	DATA BLOCK 1-4
0300-03FF	0600-07FE	**COMMAND ILLEGALIZING TABLE**
0400-041F	0800-083E	DATA BLOCK 5
0420-043F	0840-087E	DATA BLOCK 6
• • •	• • •	• • •
0FE0-0FFF	1FC0-1FFE	DATA BLOCK 100

RT MEMORY MANAGEMENT

The PCI Mini-ACE Mark3/Micro-ACE TE provides a variety of RT memory management capabilities. As with the ACE and Mini-ACE (Plus), and Enhanced Mini-ACE the choice of memory management scheme is fully programmable on a transmit/receive/broadcast subaddress basis.

In compliance with MIL-STD-1553B Notice 2, received data from broadcast messages may be optionally separated from non-broadcast received data. For each transmit, receive or broadcast subaddress, either a single-message data block, or a variable-sized (128 to 8192 words) subaddress circular buffer may be allocated for data storage. The memory management scheme for individual subaddresses is designated by means of the subaddress control word (reference TABLE 56).

For received data, there is also a global circular buffer mode. In this configuration, the data words received from multiple (or all) subaddresses are stored in a common circular buffer structure. Like the subaddress circular buffer, the size of the global circular buffer is programmable, with a range of 128 to 8192 data words.

In addition to helping ensure data sample consistency, the circular buffer options provide a means for greatly reducing host processor overhead for multi-message bulk data transfer applications.

End-of-message interrupts may be enabled either globally (following all messages), following error messages, on a transmit/receive/broadcast subaddress or mode code basis, or when a circular buffer reaches its midpoint (50% boundary) or lower (100%) boundary. A pair of interrupt status registers allow the host processor to determine the cause of all interrupts by means of a single read operation.

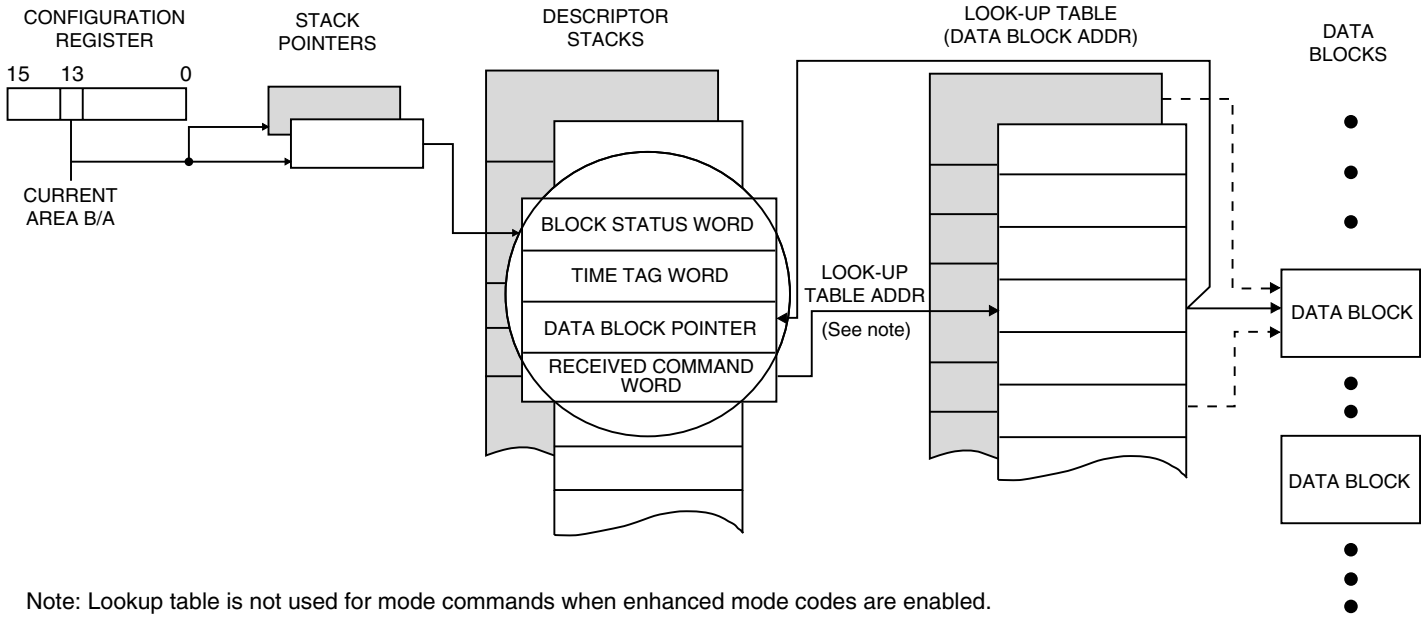
SINGLE BUFFERED MODE

The operation of the single buffered RT mode is illustrated in FIGURE 6. In the single buffered mode, the respective lookup table entry must be written by the host processor. Received data words are written to, or transmitted data words are read from the data word block with starting address referenced by the lookup table pointer. In the single buffered mode, the current lookup table pointer is **not** updated by the PCI Mini-ACE Mark3/Micro-ACE TE memory management logic. Therefore, if a subsequent message is received for the same subaddress, the **same** Data Word block will be overwritten or overread.

CIRCULAR BUFFER MODE

The operation of the PCI Mini-ACE Mark3/Micro-ACE TE circular buffer RT memory management mode is illustrated in FIGURE 7. As in the single buffered mode, the individual lookup table entries are initially loaded by the host processor. At the start of each message, the lookup table entry is stored in the third position of the respective message block descriptor in the descriptor stack area of RAM. Receive or transmit data words are transferred to (from) the circular buffer, starting at the location referenced by the lookup table pointer.

In general, the location after the last data word written or read (modulo the circular buffer size) during the message is written to the respective lookup table location during the end-of-message sequence. By so doing, data for the next message for the respective transmit, receive(/broadcast), or broadcast subaddress will be accessed from the next lower contiguous block of locations in the circular buffer.



Note: Lookup table is not used for mode commands when enhanced mode codes are enabled.

FIGURE 6. RT SINGLE BUFFERED MODE

For the case of a receive (or broadcast receive) message with a data word error, there is an option such that the lookup table pointer will only be updated following receipt of a **valid** message. That is, the pointer will **not** be updated following receipt of a message with an error in a data word. This allows failed messages in a bulk data transfer to be retried without disrupting the circular buffer data structure, and without intervention by the RT's host processor.

GLOBAL CIRCULAR BUFFER

Beyond the programmable choice of single buffer mode or circular buffer mode, programmable on an individual subaddress basis, the PCI Mini-ACE Mark3/Micro-ACE TE architecture provides an additional option, a variable sized **global** circular buffer.

TABLE 55. RT LOOK-UP TABLES (ALL ADDRESSES IN HEX)

AREA A (INTERNAL MEMORY OFFSET	AREA A (PCI BAR0 OFFSET)	AREA B (INTERNAL MEMORY OFFSET)	AREA B (PCI BAR0 OFFSET)	DESCRIPTION	COMMENT
0140 • • • 015F	0280 • • • 02BE	01C0 • • • 01DF	0380 • • • 03BE	Rx(/Bcst) SA0 • • • Rx(/Bcst) SA31	Receive (/Broadcast) Lookup Pointer Table
0160 • • • 017F	02C0 • • • 02FE	01E0 • • • 01FF	03C0 • • • 03FE	Tx SA0 • • • Tx SA31	Transmit Lookup Pointer Table
0180 • • • 019F	0300 • • • 033E	0200 • • • 021F	0400 • • • 043F	Bcst SA0 • • • Bcst SA31	Broadcast Lookup Pointer Table (Optional)
01A0 • • • 01BF	0340 • • • 037E	0220 • • • 023F	0440 • • • 047E	SACW SA0 • • • SACW SA31	Subaddress Control Word Lookup Table (Optional)

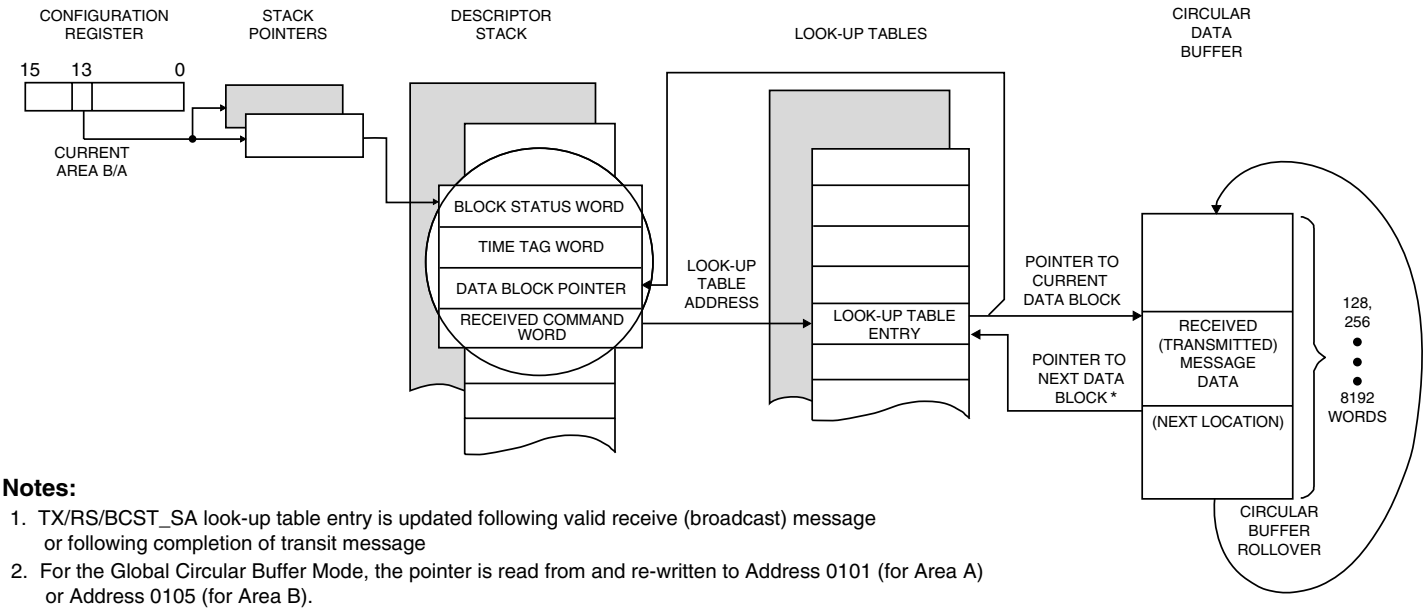
TABLE 56. RT SUBADDRESS CONTROL WORD - MEMORY MANAGEMENT OPTIONS

GLOBAL CIRCULAR BUFFER (bit 15)	SUBADDRESS CONTROL WORD BITS			MEMORY MANAGEMENT SUBADDRESS BUFFER SCHEME DESCRIPTION	
	MM2	MM1	MM0		
0	0	0	0	Single Message	
1	0	0	0	Reserved for future use	
0	0	0	1	128-Word	Subaddress - specific circular buffer of specified size.
0	0	1	0	256-Word	
0	0	1	1	512-Word	
0	1	0	0	1024-Word	
0	1	0	1	2048-Word	
0	1	1	0	4096-Word	
0	1	1	1	8192-Word	
1	1	1	1	(for receive and / or broadcast subaddresses only) Global Circular Buffer: The buffer size is specified by Configuration Register #6, bits 11-9. The pointer to the global circular buffer is stored at address 0101h (for Area A, PCI BAR0 offset 0202h) or address 0105h (for Area B, PCI BAR0 offset 020Ah)	

In the global circular buffer mode, the data for **multiple** receive subaddresses is stored in the same circular buffer data structure. The size of the global circular buffer may be programmed for 128, 256, 512, 1024, 2048, 4096, or 8192 words, by means of bits 11, 10, and 9 of Configuration Register #6. As shown in TABLE 56, individual subaddresses may be mapped to the global circular buffer by means of their respective subaddress control words.

The pointer to the Global Circular Buffer will be stored in location 0101 (for Area A, PCI BAR0 offset 0202h), or location 0105h (for Area B, PCI BAR0 offset 020Ah).

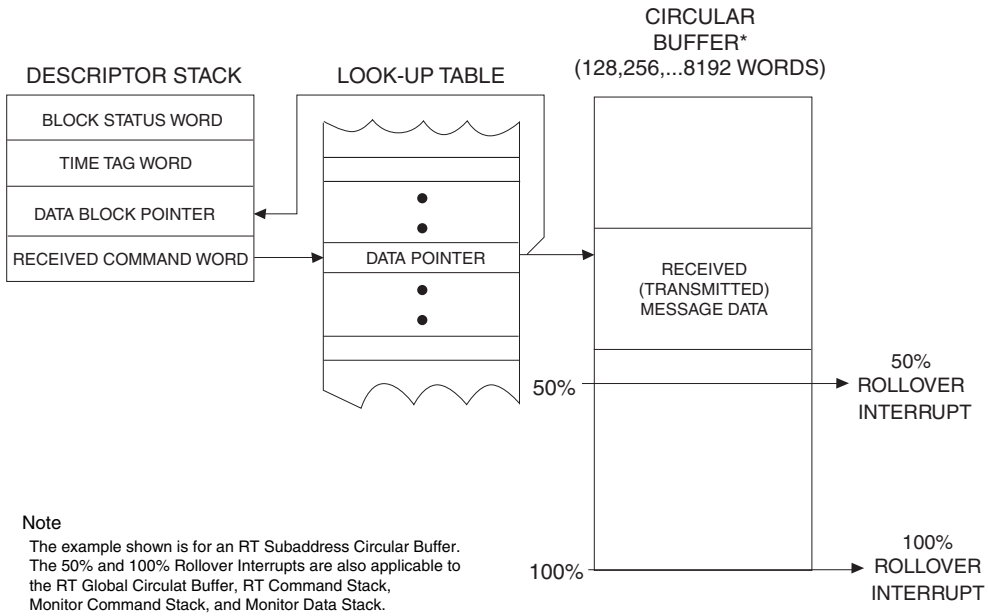
The global circular buffer option provides a highly efficient method for storing received message data. It allows for frequently used subaddresses to be mapped to individual data blocks, while also providing a method for asynchronously received messages to infrequently used subaddresses to be logged to a common area. Alternatively, the global circular buffer provides an efficient means for storing the received data words for all subaddresses. Under this method, all received data words are stored chronologically, regardless of subaddress.



Notes:

1. TX/RS/BCST_SA look-up table entry is updated following valid receive (broadcast) message or following completion of transit message
2. For the Global Circular Buffer Mode, the pointer is read from and re-written to Address 0101 (for Area A) or Address 0105 (for Area B).

FIGURE 7. RT CIRCULAR BUFFERED MODE



Note
The example shown is for an RT Subaddress Circular Buffer. The 50% and 100% Rollover Interrupts are also applicable to the RT Global Circulat Buffer, RT Command Stack, Monitor Command Stack, and Monitor Data Stack.

FIGURE 8. 50% and 100% ROLLOVER INTERRUPTS

RT DESCRIPTOR STACK

The descriptor stack provides a chronology of all messages processed by the PCI Mini-ACE Mark3/Micro-ACE TE RT. Reference FIGURES 6 and 7. Similar to BC mode, there is a four-word block descriptor in the Stack for each message processed. The four entries to each block descriptor are the Block Status Word, Time Tag Word, the pointer to the start of the message's data block, and the 16-bit received Command Word.

The RT Block Status Word includes indications of whether a particular message is ongoing or has been completed, what bus channel it was received on, indications of illegal commands, and flags denoting various message error conditions. For the subaddress circular buffering, and global circular buffering modes, the data block pointer may be used for locating the data blocks for specific messages. Note that for mode code commands, there is an option to store the transmitted or received data word as the third word of the descriptor, in place of the data block pointer.

The Time Tag Word provides a 16-bit indication of relative time for individual messages. The resolution of the PCI Mini-ACE Mark3/Micro-ACE TE's time tag is programmable from among 2, 4, 8, 16, 32, or 64 µs/LSB using the internal clock, or it can be programmed to increment directly from the TAG_CLK input by writing all ones to the time tag resolution bits. If enabled, there is a time tag rollover interrupt, which is issued when the value of the time tag rolls over from FFFF(hex) to 0. Other time tag options include the capabilities to clear the time tag register following receipt of a Synchronize (without data) mode command and/or to set the time tag following receipt of a Synchronize (with data) mode command. For that latter, there is an added option to filter the "set" capability based on the LSB of the received data word being equal to logic "0".

RT INTERRUPTS

The PCI Mini-ACE Mark3/Micro-ACE TE offers a great deal of flexibility in terms of RT interrupt processing. By means of the Enhanced Mini-ACE/Micro-ACE's two Interrupt Mask Registers, the PCI Mini-ACE Mark3/Micro-ACE TE's RT may be programmed to issue interrupt requests for the following events/conditions: End-of-(every)Message, Message Error, Selected (transmit or receive) Subaddress, 100% Circular Buffer Rollover, 50% Circular Buffer Rollover, 100% Descriptor Stack Rollover, 50% Descriptor Stack Rollover, Selected Mode Code, Transmitter Timeout, Illegal Command, and Interrupt Status Queue Rollover.

Interrupts for 50% Rollovers of Stacks and Circular Buffers. The PCI Mini-ACE Mark3/Micro-ACE TE RT and Monitor are capable of issuing host interrupts when a subaddress circular buffer pointer or stack pointer crosses its mid-point boundary. For RT circular buffers, this is applicable for both transmit and receive subaddresses. Reference FIGURE 8. There are four interrupt mask and interrupt status register bits associated with the 50% rollover function:

(1) RT circular buffer;
(2) RT command (descriptor) stack;
(3) Monitor command (descriptor) stack; and
(4) Monitor data stack.

The 50% rollover interrupt is beneficial for performing bulk data transfers. For example, when using circular buffering for a particular receive subaddress, the 50% rollover interrupt will inform the host processor when the circular buffer is half full. At that time, the host may proceed to read the received data words in the upper half of the buffer, while the PCI Mini-ACE Mark3/Micro-ACE TE RT writes received data words to the lower half of the circular buffer. Later, when the RT issues a 100% circular buffer rollover interrupt, the host can proceed to read the received data from the lower half of the buffer, while the PCI Mini-ACE Mark3/

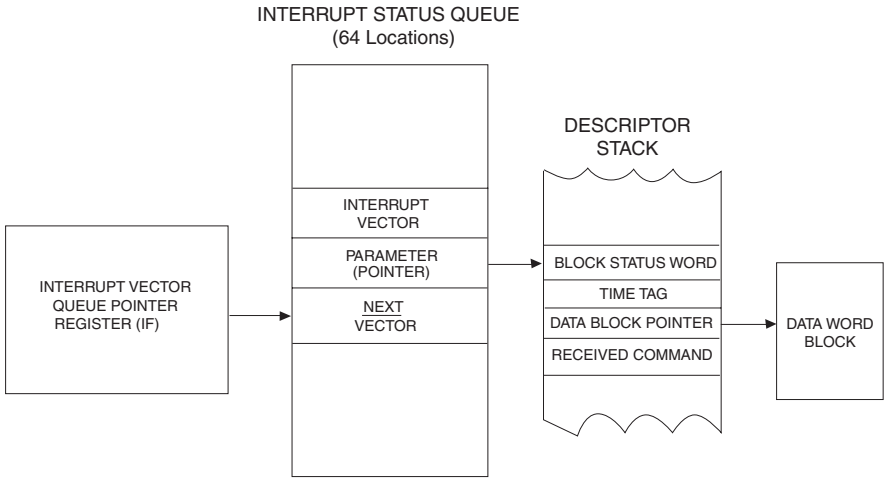


FIGURE 9. RT (and MONITOR) INTERRUPT STATUS QUEUE (shown for message Interrupt event)

Micro-ACE TE RT continues to write received data words to the upper half of the buffer.

Interrupt status queue. The PCI Mini-ACE Mark3/Micro-ACE TE RT, Monitor, and combined RT/Monitor modes include the capability for generating an interrupt status queue. As illustrated in FIGURE 9, this provides a chronological history of interrupt generating events and conditions. In addition to the Interrupt Mask Register, the Interrupt Status Queue provides additional filtering capability, such that only valid messages and/or only invalid messages may result in the creation of an entry to the Interrupt Status Queue. Queue entries for invalid and/or valid messages may be disabled by means of bits 8 and 7 of configuration register #6.

The pointer to the Interrupt Status Queue is stored in the INTERRUPT VECTOR QUEUE POINTER REGISTER (register address 1F). This register must be initialized by the host, and is subsequently incremented by the RT message processor. The interrupt status queue is 64 words deep, providing the capability to store entries for up to 32 messages.

The queue rolls over at addresses of modulo 64. The events that result in queue entries include both message-related and non-message-related events. Note that the Interrupt Vector Queue Pointer Register will always point to the next location (modulo 64) **following** the last vector/pointer pair written by the PCI Mini-ACE Mark3/Micro-ACE TE RT, Monitor, or RT/Monitor.

Each event that causes an interrupt results in a two-word entry to be written to the queue. The first word of the entry is the interrupt vector. The vector indicates which interrupt event(s)/condition(s) caused the interrupt.

The interrupt events are classified into two categories: message interrupt events and non-message interrupt events. Message-based interrupt events include End-of-Message, Selected mode code, Format error, Subaddress control word interrupt, RT Circular buffer Rollover, Handshake failure, RT Command stack rollover, transmitter timeout, MT Data Stack rollover, MT Command Stack rollover, RT Command Stack 50% rollover, MT Data Stack 50% rollover, MT Command Stack 50% rollover, and RT Circular buffer 50% rollover. Non-message interrupt events/conditions include time tag rollover, RT address parity error, RAM parity error, and BIT completed.

Bit 0 of the interrupt vector (interrupt status) word indicates whether the entry is for a message interrupt event (if bit 0 is logic "1") or a non-message interrupt event (if bit 0 is logic "0"). It is **not** possible for one entry on the queue to indicate both a message interrupt and a non-message interrupt.

As illustrated in FIGURE 9, for a message interrupt event, the parameter word is a pointer. The pointer will reference the first word of the RT or MT command stack descriptor (i.e., the Block Status Word).

For a RAM Parity Error non-message interrupt, the parameter will be the RAM address where the parity check failed. For the RT address Parity Error, and Time Tag rollover non-message interrupts, the parameter is not used; it will have a value of 0000.

If enabled, an INTERRUPT STATUS QUEUE ROLLOVER interrupt will be issued when the value of the queue pointer address rolls over at a 64-word address boundary.

RT COMMAND ILLEGALIZATION

The PCI Mini-ACE Mark3/Micro-ACE TE provides an internal mechanism for RT Command Word illegalizing. By means of a 256-word area in shared RAM, the host processor may designate that any message be illegalized, based on the command word T/R bit, subaddress, and word count/mode code fields. The PCI Mini-ACE Mark3/Micro-ACE TE illegalization scheme provides the maximum in flexibility, allowing any subset of the 4096 possible combinations of broadcast/own address, T/R bit, subaddress, and word count/mode code to be illegalized.

The address map of the PCI Mini-ACE Mark3/Micro-ACE TE's illegalizing table is illustrated in TABLE 57.

BUSY BIT

The PCI Mini-ACE Mark3/Micro-ACE TE RT provides two different methods for setting the Busy status word bit: (1) globally, by means of Configuration Register #1; or (2) on a T/R-bit/subaddress basis, by means of a RAM lookup table. If the host CPU asserts the BUSY bit low in Configuration Register #1, the PCI Mini-ACE Mark3/Micro-ACE TE RT will respond to **all** non-broadcast commands with the Busy bit set in its RT Status Word.

Alternatively, there is a Busy lookup table in the PCI Mini-ACE Mark3/Micro-ACE TE shared RAM. By means of this table, it is possible for the host processor to set the busy bit for any selectable subset of the 128 combinations of broadcast/own address, T/R bit, and subaddress.

If the busy bit is set for a transmit command, the PCI Mini-ACE Mark3/Micro-ACE TE RT will respond with the busy bit set in the status word, but will not transmit any data words. If the busy bit is set for a receive command, the RT will also respond with the busy status bit set. There are two programmable options regarding the reception of data words for a non-mode code receive command for which the RT is busy: (1) to transfer the received data words to shared RAM; or (2) to **not** transfer the data words to shared RAM.

RT ADDRESS

The PCI Mini-ACE Mark3/Micro-ACE TE offers several different options for designating the Remote Terminal address. These include the following: (1) hardwired, by means of the 5 RT ADDRESS inputs, and the RT ADDRESS PARITY input; (2) by means of the RT ADDRESS (and PARITY) inputs, but latched via

TABLE 57. ILLEGALIZATION TABLE MEMORY MAP		
ADDRESS	PCI BAR0 OFFSET	DESCRIPTION
300	600	Brdcst / Rx, SA 0, MC15-0
301	602	Brdcst / SA 0, MC31-16
302	604	Brdcst / Rx, SA 1, WC15-0
303	606	Brdcst / Rx, SA 1, WC31-16
• • •	• • •	• • •
33F	67E	Brdcst / Rx, SA 0, MC15-0
340	680	Brdcst / Tx, SA 0, MC31-16
341	682	Brdcst / Tx, SA 1,WC15-0
342	684	Brdcst / Tx, SA 1, WC31-16
• • •	• • •	• • •
37D	6FA	Brdcst / Tx, SA 30, WC31-16
37E	6FC	Brdcst / Tx, SA 31, MC15-0
37F	6FE	Brdcst / Tx, SA 31, MC31-16
380	700	Own Addr / Rx, SA 0, MC15-0
381	702	Own Addr / Rx, SA 0, MC31-16
382	704	Own Addr / Rx, SA 1, WC15-0
383	706	Own Addr / Rx, SA 1, WC31-15
• • •	• • •	• • •
3BE	77C	Own Addr / Rx, SA 31, MC15-0
3BF	77E	Own Addr / Rx, SA 31, MC31-16
3C0	780	Own Addr / Tx, SA 0, MC15-0
3C1	782	Own Addr / Tx, SA 0, MC31-16
3C2	784	Own Addr / Tx, SA 1, WC15-0
3C3	786	Own Addr / Tx, SA 1, WC31-16
• • •	• • •	• • •
3FC	7F8	Own Addr / Tx, SA 30, WC15-0
3FD	7FA	Own Addr / Tx, SA 30, WC31-16
3FE	7FC	Own Addr / Tx, SA 31, MC15-0
3FF	7FE	Own Addr / Tx, SA 31, MC31-16

hardware, on the rising edge of the RT_AD_LAT input signal; (3) input by means of the RT ADDRESS (and PARITY) inputs, but latched via host software; and (4) software programmable, by means of an internal register. In all four configurations, the RT address is readable by the host processor.

RT BUILT-IN-TEST (BIT) WORD

The bit map for the PCI Mini-ACE Mark3/Micro-ACE TE's internal RT Built-in-Test (BIT) Word is indicated in TABLE 58.

OTHER RT FEATURES

The PCI Mini-ACE Mark3/Micro-ACE TE includes options for the Terminal flag status word bit to be set either under software control and/or automatically following a failure of the loopback self-test. Other software programmable RT options include software programmable RT status and RT BIT words, automatic clearing of the Service Request bit following receipt of a Transmit vector word mode command, options regarding Data Word transfers for the Busy and Message error (illegal) Status word bits, and options for the handling of 1553A and reserved mode codes.

MONITOR ARCHITECTURE

The PCI Mini-ACE Mark3/Micro-ACE TE includes three monitor modes:

(1) A Word Monitor mode
(2) A selective message monitor mode
(3) A combined RT/message monitor mode

For new applications, it is recommended that the selective message monitor mode be used, rather than the word monitor mode. Besides providing monitor filtering based on RT address, T/$\overline{R}$ bit, and subaddress, the message monitor eliminates the need to determine the start and end of messages by software.

WORD MONITOR MODE

In the Word Monitor Terminal mode, the PCI Mini-ACE Mark3/Micro-ACE TE monitors both 1553 buses. After the software initialization and Monitor Start sequences, the PCI Mini-ACE Mark3/Micro-ACE TE stores all Command, Status, and Data Words received from both buses. For each word received from either bus, a pair of words is stored to the PCI Mini-ACE Mark3/Micro-ACE TE's shared RAM. The first word is the word received from the 1553 bus. The second word is the Monitor Identification (ID), or "Tag" word. The ID word contains information relating to bus channel, word validity, and inter-word time gaps. The data and ID words are stored in a circular buffer in the shared RAM address space.

WORD MONITOR MEMORY MAP

A typical word monitor memory map is illustrated in **TABLE 59**. TABLE 59 assumes a 64K address space for the PCI Mini-ACE Mark3/Micro-ACE TE's monitor. The Active Area Stack pointer provides the address where the first monitored word is stored. In the example, it is assumed that the Active Area Stack Pointer for Area A (location 0100) is initialized to 0000. The first received data word is stored in location 0000, the ID word for the first word is stored in location 0001, etc.

The current Monitor address is maintained by means of a counter register. This value may be read by the CPU by means of the Data Stack Address Register. It is important to note that when the counter reaches the Stack Pointer address of 0100 or 0104, the initial pointer value stored in this shared RAM location **will be overwritten** by the monitored data and ID Words. When the internal counter reaches an address of FFFF (or 0FFF, for an PCI Mini-ACE Mark3/Micro-ACE TE with 4K RAM), the counter rolls over to 0000.

WORD MONITOR TRIGGER

In the Word Monitor mode, there is a pattern recognition trigger and a pattern recognition interrupt. The 16-bit compare word for both the trigger and the interrupt is stored in the Monitor Trigger Word Register. The pattern recognition interrupt is enabled by setting the MT Pattern Trigger bit in Interrupt Mask Register. The pattern recognition trigger is enabled by setting the Trigger Enable bit in Configuration Register #1 and selecting either the Start-on-trigger or the Stop-on-trigger bit in Configuration Register #1. The Word Monitor may also be started by means of a low-to-high transition on the EXT_TRIG input signal.

SELECTIVE MESSAGE MONITOR MODE

The PCI Mini-ACE Mark3/Micro-ACE TE Selective Message Monitor provides monitoring of 1553 messages with filtering based on RT address, T/R bit, and subaddress with no host processor intervention. By autonomously distinguishing between 1553 command and status words, the Message Monitor determines when messages begin and end, and stores the messages into RAM, based on a programmable filter of RT address, T/R bit, and subaddress.

The selective monitor may be configured as just a monitor, or as a **combined RT/Monitor.** In the combined RT/Monitor mode, the PCI Mini-ACE Mark3/Micro-ACE TE functions as an RT for one RT address (including broadcast messages), and as a selective message monitor for the other 30 RT addresses. The PCI Mini-ACE Mark3/Micro-ACE TE Message Monitor contains two stacks, a command stack and a data stack, that are independent from the

TABLE 58. RT BIT WORD

BIT	DESCRIPTION
15(MSB)	TRANSMITTER TIMEOUT
14	LOOP TEST FAILURE B
13	LOOP TEST FAILURE A
12	HANDSHAKE FAILURE
11	TRANSMITTER SHUTDOWN B
10	TRANSMITTER SHUTDOWN A
9	TERMINAL FLAG INHIBITED
8	BIT TEST FAILURE
7	HIGH WORD COUNT
6	LOW WORD COUNT
5	INCORRECT SYNC RECEIVED
4	PARITY / MANCHESTER ERROR RECEIVED
3	RT-to-RT GAP / SYNC ADDRESS ERROR
2	RT-to-RT NO RESPONSE ERROR
1	RT-to-RT 2ND COMMAND WORD ERROR
0(LSB)	COMMAND WORD CONTENTS ERROR

TABLE 59. TYPICAL WORD MONITOR MEMORY MAP

HEX ADDRESS	FUNCTION
0000	First Received 1553 Word
0001	First Identification Word
0002	Second Received 1553 Word
0003	Second Identification Word
0004	Third Received 1553 Word
005	Third Identification Word
• • •	• • •
0100	Stack Pointer (Fixed Location - gets overwritten)
• • • FFFF	• • • Received 1553 Words and Identification Word

RT command stack. The pointers for these stacks are located at fixed locations in RAM.

MONITOR SELECTION FUNCTION

Following receipt of a valid command word in Selective Monitor mode, the PCI Mini-ACE Mark3/Micro-ACE TE will reference the selective monitor lookup table to determine if the particular command is enabled. The address for this location in the table is determined by means of an offset based on the RT Address, T/$\overline{R}$ bit, and Subaddress bit 4 of the current command word, and concatenating it to the monitor lookup table base address of 0280 (hex). The bit location within this word is determined by subaddress bits 3-0 of the current command word.

If the specified bit in the lookup table is logic "0", the command is not enabled, and the PCI Mini-ACE Mark3/Micro-ACE TE will ignore this command. If this bit is logic "1", the command is enabled and the PCI Mini-ACE Mark3/Micro-ACE TE will create an entry in the monitor command descriptor stack (based on the monitor command stack pointer), and store the data and status words associated with the command into sequential locations in the monitor data stack. In addition, for an RT-to-RT transfer in which the receive command is selected, the second command word (the transmit command) is stored in the monitor data stack.

NOTE: After a command is discarded the monitor will immediately look for another "Command." Where only a subset of Subaddresses are enabled, it is possible that a succeeding Status words may be captured as a "Command". This will always be flagged as an error because the Word Count or timing will fail.

The address definition for the Selective Monitor Lookup TABLE is illustrated in TABLE 60.

SELECTIVE MESSAGE MONITOR MEMORY ORGANIZATION

A typical memory map for the PCI Mini-ACE Mark3/Micro-ACE TE in the Selective Message Monitor mode, assuming a 4K RAM space, is illustrated in TABLE 61. This mode of operation defines several fixed locations in the RAM. These locations are allocated in a way in which none of them overlap with the fixed RT locations. This allows for the combined RT/Selective Message Monitor mode.

The fixed memory map consists of two Monitor Command Stack Pointers (locations 102 and 106 hex), two Monitor Data Stack Pointers (locations 103 and 107 hex), and a Selective Message Monitor Lookup Table (locations 0280 through 02FF hex). For this example, the Monitor Command Stack size is assumed to be 1K words, and the Monitor Data Stack size is assumed to be 2K words.

FIGURE 10 illustrates the Selective Message Monitor operation. Upon receipt of a valid Command Word, the PCI Mini-ACE Mark3/Micro-ACE TE will reference the Selective Monitor Lookup Table to determine if the current command is enabled. If the current command is disabled, the PCI Mini-ACE Mark3/Micro-ACE TE monitor will ignore (and not store) the current message. If the command is enabled, the monitor will create an entry in the Monitor Command Stack at the address location referenced by the Monitor Command Stack Pointer, and an entry in the monitor data stack starting at the location referenced by the Monitor Data Stack Pointer.

The format of the information in the data stack depends on the format of the message that was processed. For example, for a BC-to-RT transfer (receive command), the monitor will store the command word in the monitor command descriptor stack, with the data words and the receiving RT's status word stored in the monitor data stack.

The size of the monitor command stack is programmable, with choices of 256, 1K, 4K, or 16K words. The monitor data stack size is programmable with choices of 512, 1K, 2K, 4K, 8K, 16K, 32K or 64K words.

MONITOR INTERRUPTS

Selective monitor interrupts may be issued for End-of-message and for conditions relating to the monitor command stack pointer and monitor data stack pointer. The latter, which are shown in FIGURE 8, include Command Stack 50% Rollover, Command Stack 100% Rollover, Data Stack 50% Rollover, and Data Stack 100% Rollover.

The 50% rollover interrupts may be used to inform the host processor when the command stack or data stack is half full. At that time,

TABLE 60. MONITOR SELECTION TABLE LOOKUP ADDRESS

BIT	DESCRIPTION
15(MSB)	Logic “0”
14	Logic “0”
13	Logic “0”
12	Logic “0”
11	Logic “0”
10	Logic “0”
9	Logic “1”
8	Logic “0”
7	Logic “1”
6	RTAD_4
5	RTAD_3
4	RTAD_2
3	RTAD_1
2	RTAD_0
1	TRANSMIT / $\overline{\text{RECEIVE}}$
0(LSB)	SUBADDRESS 4

the host may proceed to read the received messages in the upper half of the respective stack, while the PCI Mini-ACE Mark3/Micro-ACE TE monitor writes messages to the lower half of the stack. Later, when the monitor issues a 100% stack rollover interrupt, the host can proceed to read the received data from the lower half of the stack, while the PCI Mini-ACE Mark3/Micro-ACE TE monitor continues to write received data words to the upper half of the stack.

INTERRUPT STATUS QUEUE

Like the PCI Mini-ACE Mark3/Micro-ACE TE RT, the Selective Monitor mode includes the capability for generating an interrupt status queue. As illustrated in FIGURE 9, this provides a chronological history of interrupt generating events. Besides the two Interrupt Mask Registers, the Interrupt Status Queue provides additional filtering capability, such that only valid messages and/or only invalid messages may result in entries to the Interrupt Status Queue. The interrupt status queue is 64 words deep, providing the capability to store entries for up to 32 monitored messages.

MISCELLANEOUS

1553 CLOCK INPUT

The PCI Mini-ACE Mark3/Micro-ACE TE decoder is capable of operating from a 10, 12, 16, or 20 MHz clock input. The clock frequency may be specified by means of the host processor writing to Configuration Register #6. In addition when PCI Micro-ACE TE parts have their RTBOOT_L ball asserted, the 1553 input clock divider is controlled by the CLK_SEL 0 and CLK_SEL_1 balls.

ENCODER/DECODERS

For the selected clock frequency, there is internal logic to derive the necessary clocks for the Manchester encoder and decoders. For all clock frequencies, the decoders sample the receiver outputs on both edges of the input clock. By in effect doubling the decoders' sampling frequency, this serves to widen the tolerance to zero-crossing distortion, and reduce the bit error rate.

TIME TAG

The PCI Mini-ACE Mark3/Micro-ACE TE includes an internal read/writable Time Tag Register. This register is a CPU read/writable 16-bit counter with a programmable resolution of either 2, 4, 8, 16, 32, or 64 ms per LSB. In addition, this register can be incremented directly by the TAG_CLK input pin by writing all ones to the time tag resolution bits. Another option allows software controlled incrementing of the Time Tag Register. This supports self-test for the Time Tag Register. For each message processed, the value of the Time Tag Register is loaded into the second location of the respective descriptor stack entry ("TIME TAG WORD") for BC/RT/MT modes.

The functionality of the Time Tag Register is compatible with ACE/Mini-ACE (Plus) includes: the capability to issue an interrupt request and set a bit in the Interrupt Status Register when the Time Tag Register rolls over FFFF to 0000; for RT mode, the capability to automatically clear the Time Tag Register following reception of a Synchronize (without data) mode command, or to load the Time Tag Register following a Synchronize (with data) mode command.

Additional time tag features supported by the PCI Mini-ACE Mark3/Micro-ACE TE include the capability for the BC to transmit the contents of the Time Tag Register as the data word for a Synchronize (with data) mode command; the capability for the RT to "filter" the data word for the Synchronize with data mode command, by only loading the Time Tag Register if the LSB of the received data word is "0"; an instruction enabling the BC Message Sequence Control engine to autonomously load the Time Tag Register with a specified value; and an instruction enabling the BC Message Sequence Control engine to write the value of the Time Tag Register to the General Purpose Queue.

INTERRUPTS

The PCI Mini-ACE Mark3/Micro-ACE TE series terminals provide many programmable options for interrupt generation and handling. The interrupt output pin ($\overline{INT}$) has two software programmable modes of operation: a level output cleared under software control, or a level output automatically cleared following a read of the Interrupt Status Register (#1 or #2).

Individual interrupts are enabled by the two Interrupt Mask Registers. The host processor may determine the cause of the interrupt by reading the two Interrupt Status Registers, which provide the current state of interrupt events and conditions. The Interrupt Status Registers may be updated in two ways. In one interrupt handling mode, a particular bit in Interrupt Status Register #1 or #2 will be updated only if the event occurs and the corresponding bit in Interrupt Mask Register #1 or #2 is enabled. In the enhanced interrupt handling mode, a particular bit in one of the Interrupt Status Registers will be updated if the event/condition occurs regardless of the value of the corresponding

TABLE 61. TYPICAL SELECTIVE MESSAGE MONITOR MEMORY MAP (shown for 4K RAM for "Monitor only" mode)

ADDRESS (HEX)	DESCRIPTION
0100-0101	**Not Used**
0102	Monitor Command Stack Pointer A (fixed location)
0103	Monitor Data Stack Pointer A (fixed location)
0104-0105	**Not Used**
0106	Monitor Command Stack Pointer B (fixed location)
0107	Monitor Data Stack Pointer B (fixed location)
0108-027F	**Not Used**
0280-02FF	Selective Monitor Lookup Table
0300-03FF	**Not Used**
0400-07FF	Monitor Command Stack A
0800-0FFF	Monitor Data Stack A

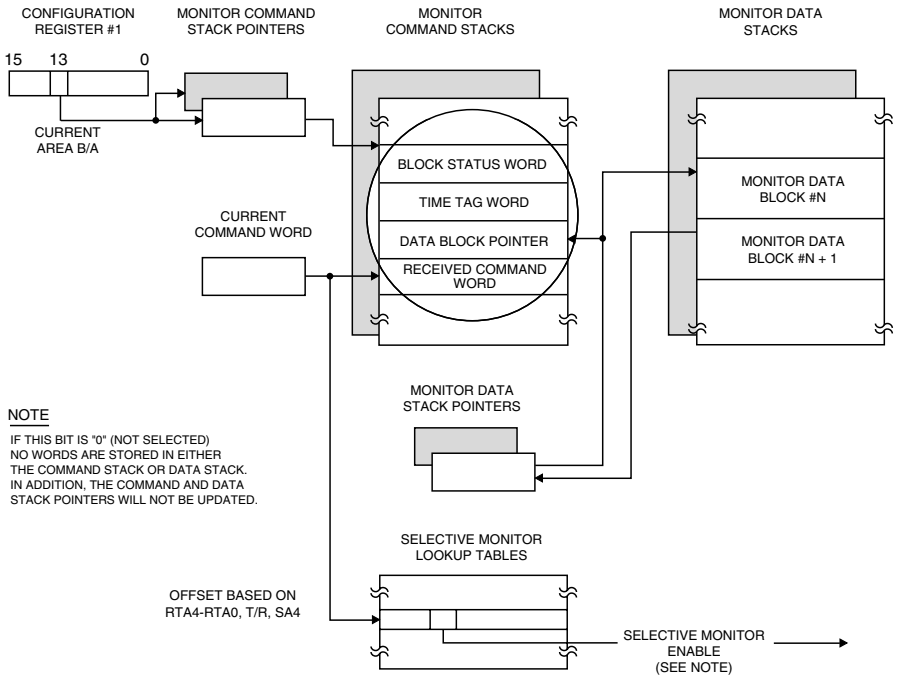


FIGURE 10. SELECTIVE MESSAGE MONITOR MEMORY MANAGEMENT

Interrupt Mask Register bit. In either case, the respective Interrupt Mask Register (#1 or #2) bit is used to enable an interrupt for a particular event/condition.

The PCI Mini-ACE Mark3/Micro-ACE TE supports all the interrupt events from ACE/Mini-ACE (Plus) and Enhanced Mini-ACE including RAM Parity Error, Transmitter Timeout, BC/RT Command Stack Rollover, MT Command Stack and Data Stack Rollover, Handshake Error, BC Retry, RT Address Parity Error, Time Tag Rollover, RT Circular Buffer Rollover, BC Message, RT Subaddress, BC End-of-Frame, Format Error, BC Status Set, RT Mode Code, MT Trigger, and End-of-Message.

For the PCI Mini-ACE Mark3/Micro-ACE TE's Enhanced BC mode, there are four user-defined interrupt bits. The BC Message Sequence Control Engine includes an instruction enabling it to issue these interrupts at any time.

For RT and Monitor modes, the PCI Mini-ACE Mark3/Micro-ACE TE architecture includes an Interrupt Status Queue. This provides a mechanism for logging messages that result in interrupt requests. Entries to the Interrupt Status Queue may be filtered such that only valid and/or invalid messages will result in entries on the queue.

The PCI Mini-ACE Mark3/Micro-ACE TE incorporates additional interrupt conditions beyond ACE/Mini-ACE (Plus), based on the addition of Interrupt Mask Register #2 and Interrupt Status Register #2. This is accomplished by chaining the two Interrupt Status Registers using the INTERRUPT CHAIN BIT (bit 0) in Interrupt Status Register #2 to indicate that an interrupt has occurred in Interrupt Status Register #1. Additional interrupts include "Self-Test Completed", masking bits for the Enhanced BC Control Interrupts, 50% Rollover interrupts for RT Command Stack, RT Circular Buffers, MT Command Stack, and MT Data Stack; BC Op Code Parity Error, (RT) Illegal Command, (BC) General Purpose Queue or (RT/MT) Interrupt Status Queue Rollover, Call Stack Pointer Register Error, BC Trap Op Code, and four User-Defined interrupts for the Enhanced BC mode.

RAM PARITY

The BC/RT/MT version of the PCI Mini-ACE Mark3/Micro-ACE TE is available with options of 4K or 64K words of internal RAM. For the 64K option, the RAM is 17 bits wide. The 64K X 17 internal RAM allows for parity generation for RAM write accesses, and parity checking for RAM read accesses. When the PCI Mini-ACE Mark3/Micro-ACE TE detects a RAM parity error, it reports it to the host processor by means of an interrupt and a register bit. Also, for the RT and Selective Message Monitor modes, the RAM address(es) where a parity error(s) was detected will be stored on the Interrupt Status Queue (if enabled).

FIGURE 11 illustrates a generic connection diagram between a PCI "Initiator" and a PCI Mini-ACE Mark3/Micro-ACE TE "Target."

The following timing diagrams illustrate the PCI commands that the PCI Mini-ACE Mark3/Micro-ACE TE responds to. Note that these diagrams are meant to show the basic PCI bus operation of the PCI Mini-ACE Mark3/Micro-ACE TE itself and do not show masters inserting wait states, masters burst reading or writing past address boundaries, masters writing into a full FIFO, etc.

To help understand the following timing diagrams an explanation of the basic architecture of the PCI Mini-ACE Mark3/Micro-ACE TE is helpful. The PCI Mini-ACE Mark3/Micro-ACE TE can be

thought of as the very successful Mini-ACE terminal family integrated with a 3.3V 33MHz PCI target interface. To simplify descriptions of the PCI Mini-ACE Mark3/Micro-ACE TE architecture, the term ACE will be used as a substitute for "enhanced Mini-ACE" even though the 1553 terminal function is really an enhanced Mini-ACE. When reference is made to ACE memory (BAR0) or ACE registers (BAR1 00-FCh) these functions are part of the ACE portion of the die. These ACE functions are accessed via the write FIFO (for writes) and delayed read request logic (for reads). The "PCI interface registers" (BAR1 800-81Ch) are part of the PCI interface portion of the die and are written and read directly from the PCI bus, without use of the write FIFO or delayed read request logic.

The PCI Mini-ACE Mark3/Micro-ACE TE's basic PCI transaction takes 3 PCI clocks, on top of the command phase. For example, a single write to any location within the PCI Mini-ACE Mark3/ Micro-ACE TE's memory space takes 4 PCI clocks, as shown in FIGURE 12. Note that this is a single write, not an attempted burst write: FRAME# is not held asserted by the master. Also note that a write to the ACE registers or ACE memory is actually a write into the write FIFO whereas a write to the PCI interface

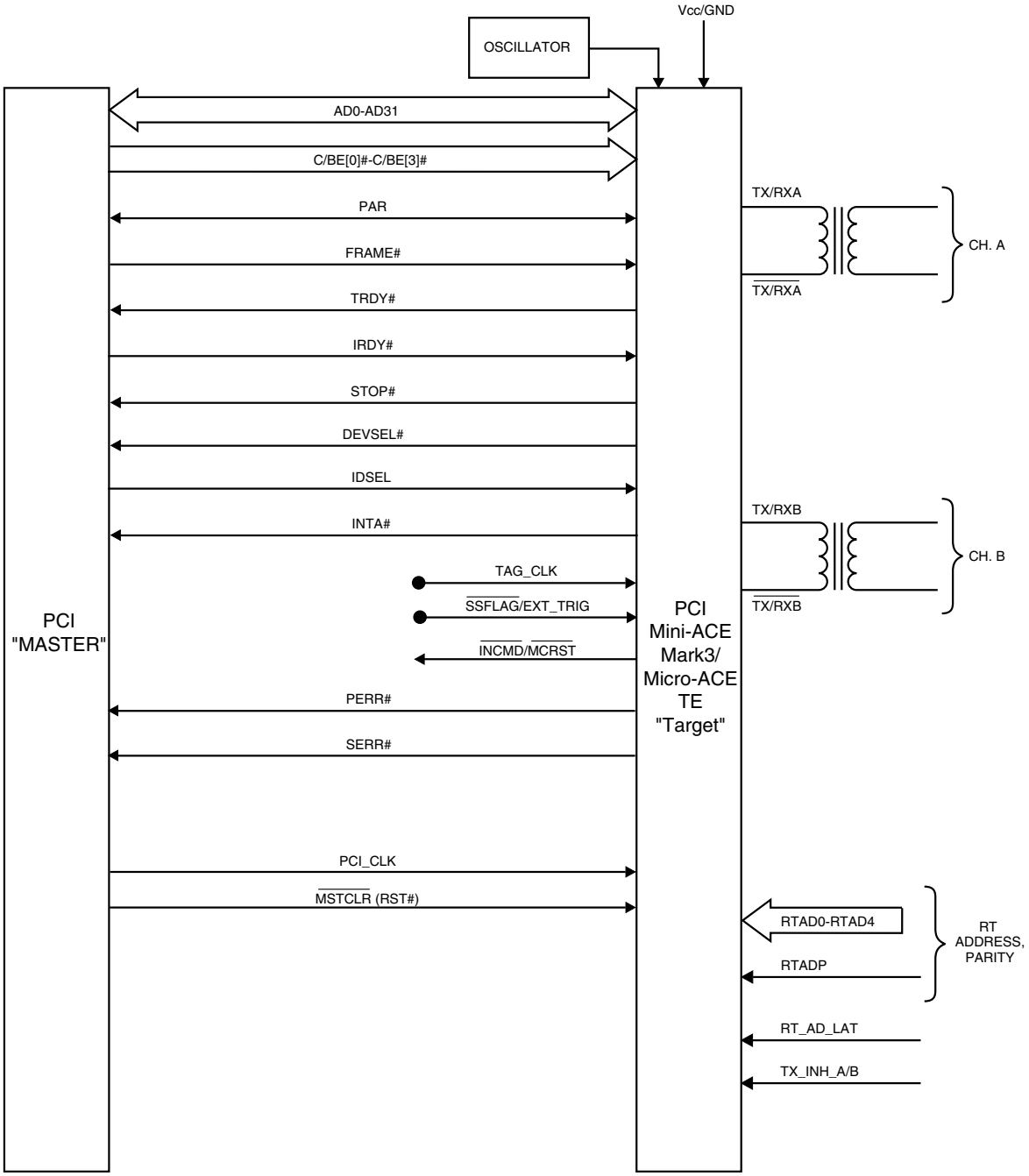


FIGURE 11. PCI INITIATOR TO PCI MINI-ACE MARK3/MICRO-ACE TE TARGET INTERFACE

registers (BAR1 800-81Ch) is a write to the registers themselves.

Table 62 provides the timing parameters for 3.3V PCI signaling environments applicable to the PCI Mini-ACE Mark3/Micro-ACE TE, and FIGURE 13 shows the timing reference points. The timing parameters apply to the other timing diagrams, but are not illustrated. The PCI Mini-ACE Mark3/Micro-ACE TE conforms to revision 2.2 of the PCI Local Bus specification. The timing parameters are provided here for ease of reference only.

FIGURE 13 illustrates a PCI read from the PCI Mini-ACE Mark3/Micro-ACE TE's configuration space. The PCI Mini-ACE Mark3/Micro-ACE TE only responds to Type Zero configuration access: AD[1:0] must be 00 during the command phase. The PCI Mini-ACE Mark3/Micro-ACE TE will drive a full Dword on the AD lines independent of which byte enables are asserted during the configuration read.

FIGURE 14 illustrates a PCI single write to PCI Mini-ACE Mark3/Micro-ACE TE configuration space. The PCI Mini-ACE Mark3/Micro-ACE TE only responds to Type Zero configuration access: AD[1:0] must be 00 during the command phase. Note that all combinations of byte enables for configuration writes are supported. If no byte enables are asserted during a burst write to configuration space no internal write will occur, but the internal address will be incremented.

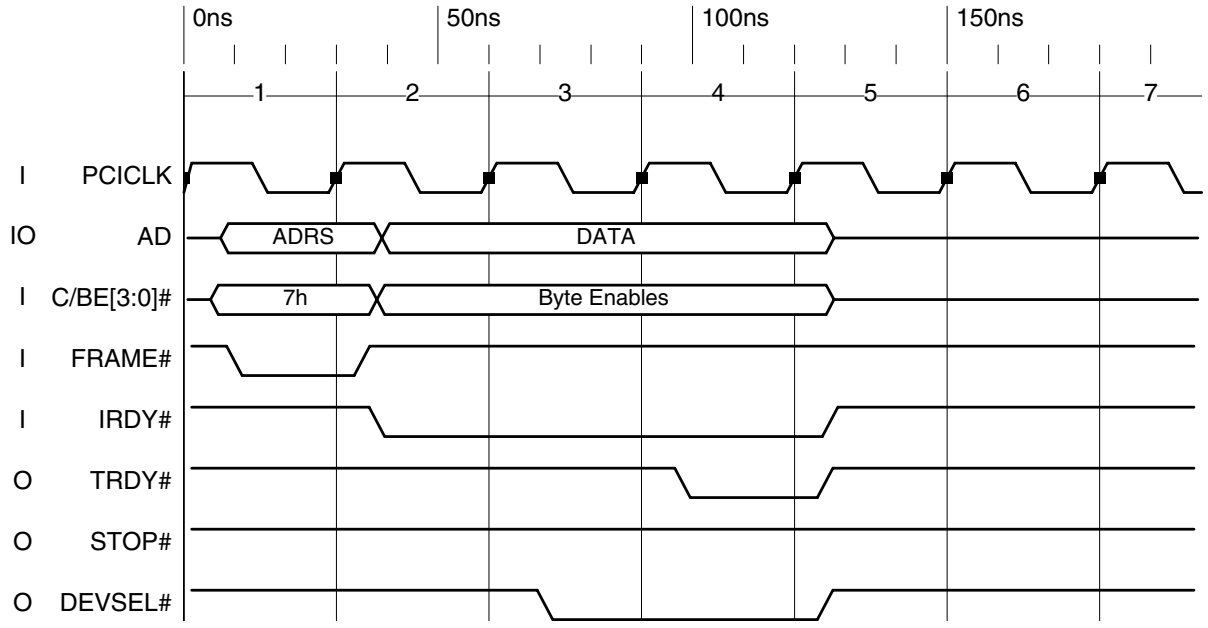
FIGURE 15 shows the specific case of memory reads from the PCI-ACE interface registers at BAR1 800h-81Ch. Note that these registers are accessed quickly and without the Delayed Read Request mechanism required by reads from the other memory locations (see next section).

TABLE 62. PCI INTERFACE TIMINGS

SYMBOL	PARAMETER	MIN	MAX	UNITS
tv	CLK TO SIGNAL VALID DELAY	2	11	ns
tsu	INPUT SETUP TIME TO CLK	7		ns
th	INPUT HOLD TIME FROM CLK	0		ns

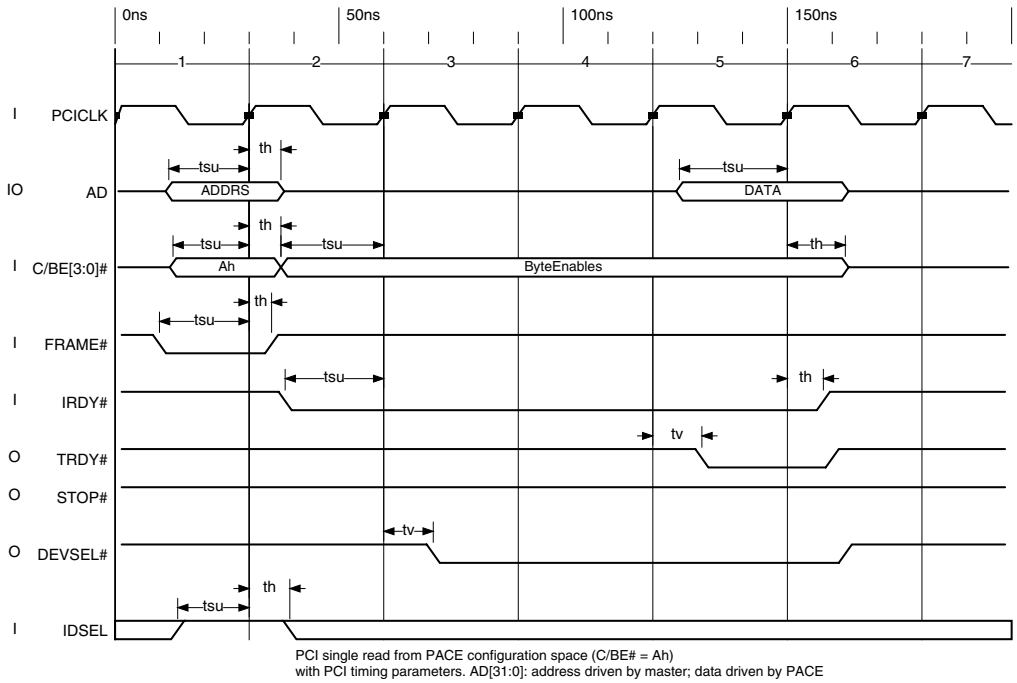
FIGURE 16 illustrates the process of reading an ACE memory (BAR0) or ACE register (BAR1 00-FCh) location. The actual read shown is that of a single word read, due to the ~600 nS response time shown, see following text and timing formula tables. If the write FIFO is empty and there isn't a previous Delayed Read Request (DRR) pending, a read from these locations enques a DRR, which is then processed by the PCI Mini-ACE Mark3/Micro-ACE TE. If either of these conditions is true, the PCI Mini-ACE Mark3/Micro-ACE TE will respond with a Retry, but will not enque any new DRR.

The PCI Mini-ACE Mark3/Micro-ACE TE responds to the first read with a Retry. By PCI rules the master must repeat the same exact request until it completes. This is shown by the master's second read attempt, which also produces a Retry. Each repeated read request from the master will be target terminated with a Retry until the data from the enqued DRR is present in the PCI Mini-ACE Mark3/Micro-ACE TE's PCI interface. The successful completion is



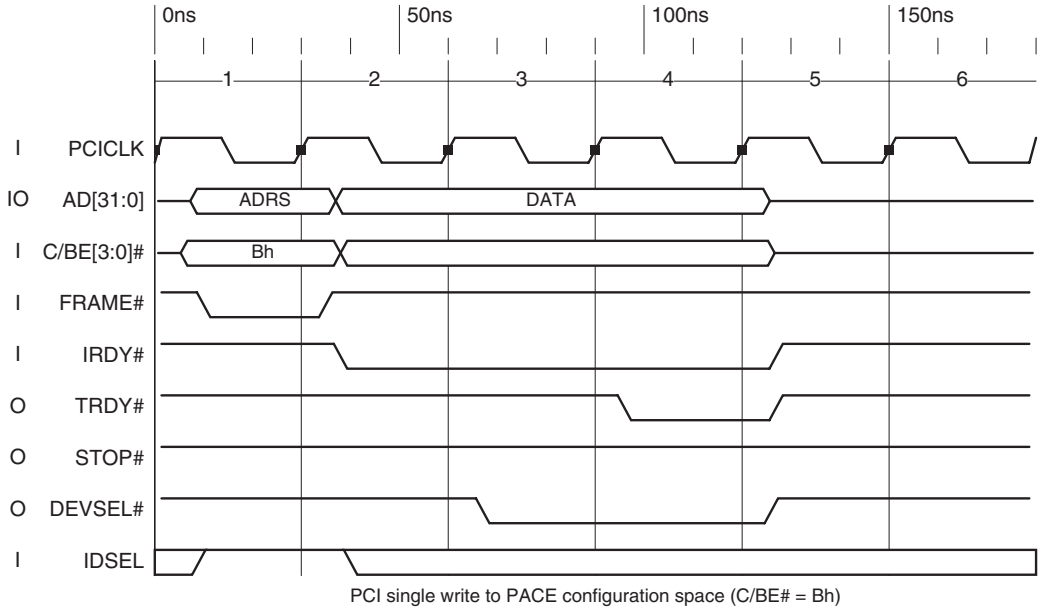
PCI single write to any legal memory location (C/BE# = 7h)

FIGURE 12. PCI SINGLE MEMORY WRITE TO PCI MINI-ACE MARK3/MICRO-ACE TE



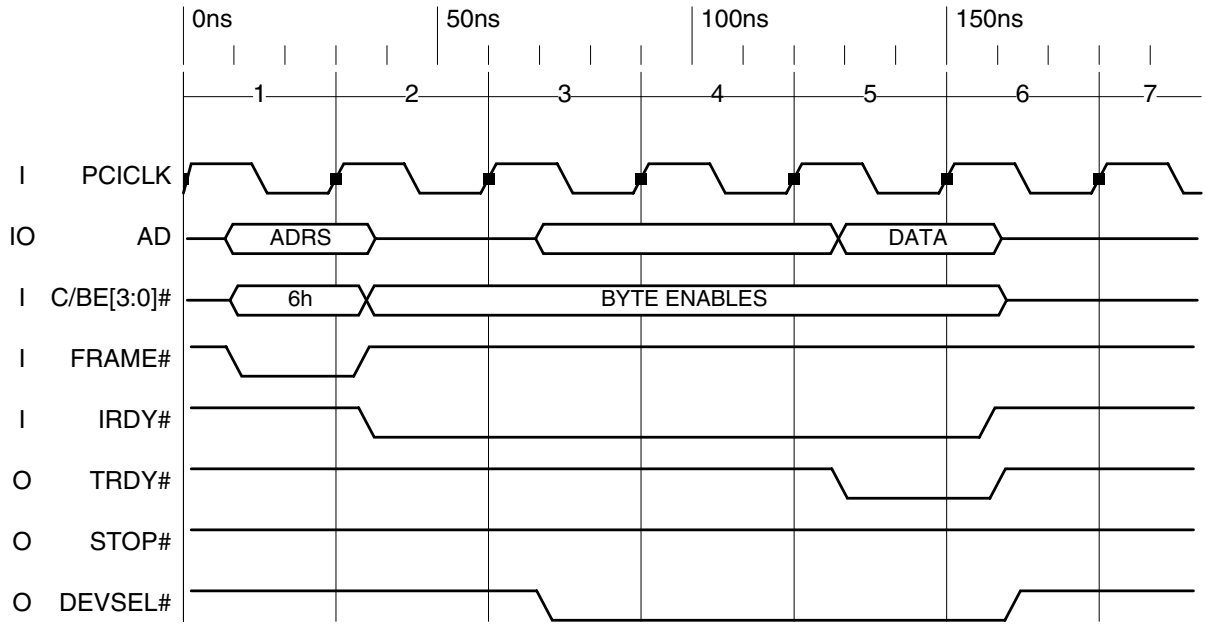
PCI single read from PACE configuration space (C/BE# = Ah)
with PCI timing parameters. AD[31:0]: address driven by master; data driven by PACE

FIGURE 13. PCI SINGLE READ OF CONFIGURATION SPACE WITH TIMING



PCI single write to PACE configuration space (C/BE# = Bh)

FIGURE 14. PCI SINGLE WRITE TO CONFIGURATION SPACE



PCI memory read from PCI-ACE interface register space (BAR1 800-81Ch)

FIGURE 15. PCI READ OF PCI-ACE IF REGISTERS (BAR1 800-81CH)

shown at the third read request, which produces a Disconnect with Data.

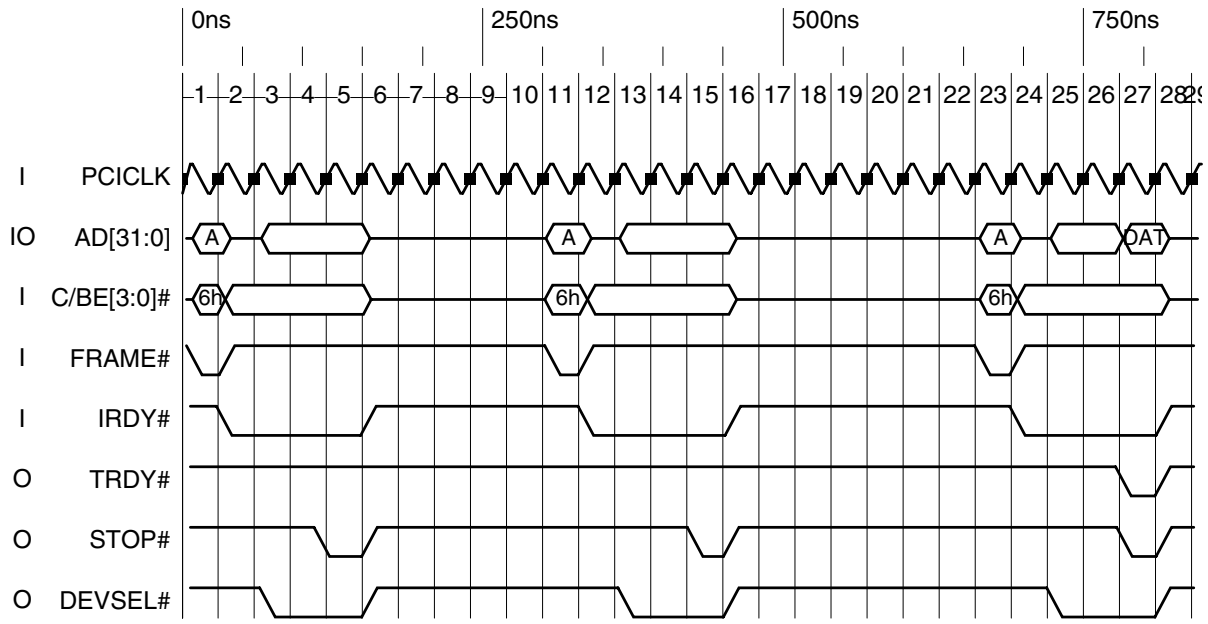
This process applies to any memory read from legal address space **other** than the PCI-ACE interface registers at BAR1 offset 800-81Ch.

Note that one of the conditions for enquing a DRR is that the write FIFO must be empty. For efficient use of PCI bus bandwidth, the driver software should be written such that it checks the FIFO condition (BAR1 800-81CH registers are directly readable, bypassing the DRR mechanism) before reading from the other PCI Mini-ACE Mark3/Micro-ACE TE locations. If the FIFO is not empty (BAR1 800h bit 30 is the FIFO not empty flag) and a read is attempted, the bus master will be using PCI bandwidth repeating the read request while the FIFO empties, BEFORE the read request is actually enqued as a DRR.

When reading ACE memory (BAR0), any combination of byte enables is supported, but the PCI Mini-ACE Mark3/Micro-ACE TE will drive the entire word onto the AD lines when only a single byte enable in the word is asserted.

When reading ACE registers (BAR 00-FCh), byte enable combinations where only a single byte within a word is requested will cause the PCI Mini-ACE Mark3/Micro-ACE TE to terminate the transaction with a target abort. The PCI Mini-ACE Mark3/Micro-ACE TE will drive all zeros onto the AD lines if only the upper word byte enables or no byte enables are asserted.

With relation to actual timing, PCI double word reads of ACE memory (BAR0) will take longer to complete than single word ACE memory reads because the internal ACE memory data path is 16 bits wide. In addition, read cycles will take longer to complete with slower ACE clocks. See Table 63 for min/max formulas for calculating completion time for the various types of reads.



PCI memory read from ACE registers/memory with no DRR pending & FIFO empty produces Retry & enques DRR. Master should attempt read as soon as possible (preferably within 33 clocks). 3rd read produces disconnect with data, DRR complete

FIGURE 16. PCI READ OF ACE MEMORY/REGISTER

TABLE 63. MIN/MAX DELAYED READ FORMULAS

TYPE OF READ	MIN TIME FORMULA	MAX TIME FORMULA
ACE MEMORY (BAR0), DOUBLE WORD	13 x PCI_CLK PERIOD + 11 x ACE_CLK PERIOD	16 x PCI_CLK PERIOD + 14 x ACE_CLK PERIOD
ACE MEMORY (BAR0), SINGLE WORD OR ACE REGISTER (BAR1, DOUBLE WORD OR LOWER WORD	8 x PCI_CLK PERIOD + 5 x ACE_CLK PERIOD	10 x PCI_CLK PERIOD + 6 x ACE_CLK PERIOD
No CBEN# ASSERTED OR ACE REGISTER (BAR1) UPPER WORD	3 x PCI_CLK PERIOD	3 x PCI_CLK PERIOD

The third case returns all zeroes and is shown only for completeness.

The following examples have the same conditions: PCI clock = 33MHz, ACE clock = 16MHz, no ACE contention.

Single word read

Min time = 8 x 30 nS + 5 x 62.5 nS = 552.5 nS

Max time = 10 x 30nS + 6 x 62.5 nS = 675 nS

Double word read

Min time = 13 x 30 nS + 11 x 62.5 nS = 1077.5 nS

Max time = 16 x 30nS + 14 x 62.5 nS = 1167.5 nS

In addition, the following amount of ACE clocks should be added for maximum time if the ACE is active.

TABLE 64. ADDITIONAL DRR DELAY FOR CONTESTED ACE RAM ACCESS

ACE OPERATING MODE	MAXIMUM ADDITIONAL ACE CLOCKS
ENHANCED CPU ACCESS ENABLED, SINGLE WORD XFER	3
ENHANCED CPU ACCESS ENABLED, DOUBLE WORD XFER	6
ENHANCED CPU ACCESS DISABLED, SINGLE WORD XFER	67
ENHANCED CPU ACCESS DISABLED, DOUBLE WORD XFER	74
THE ENHANCED CPU ACCESS IC CONTROLLED BY BIT 14 OF CONFIGURATION REGISTER #6	

FIGURE 17 illustrates a 16 Dword (32 word) PCI memory write burst, with the write FIFO empty (or with enough free space to absorb the 16 Dwords in the FIFO). The write FIFO accepts PCI memory writes to the ACE memory (BAR0) and ACE registers (BAR1 offset 00h - FCh). It does not accept writes to the PCI interface registers at BAR1 offset 800-81Ch. Writes to the BAR1 800-81Ch space go directly into the PCI interface registers. The 32 byte write shown could be an entire 1553 message being written to ACE memory.

Writes into the BAR 0 space must be word or Dword. If only one byte enable is asserted in a word, the PCI Mini-ACE Mark3/ Micro-ACE TE terminates the transaction with a Target-Abort.

Writes into the BAR 1 00-FCh space must be word or Dword. If only one byte enable is asserted in a word, the PCI Mini-ACE Mark3/Micro-ACE TE terminates the transaction with a Target-Abort. Since the ACE registers in this space are really 16 bit registers packed into the lower word of a 32-bit structure, only lower word or Dword writes transfer bits into these ACE registers.

In addition, as per PCI spec, a Memory Write and Invalidate (C/BE[3:0]# = Fh) command will be aliased to the basic Memory Write command and the timing diagram would look the same as FIGURE 17.

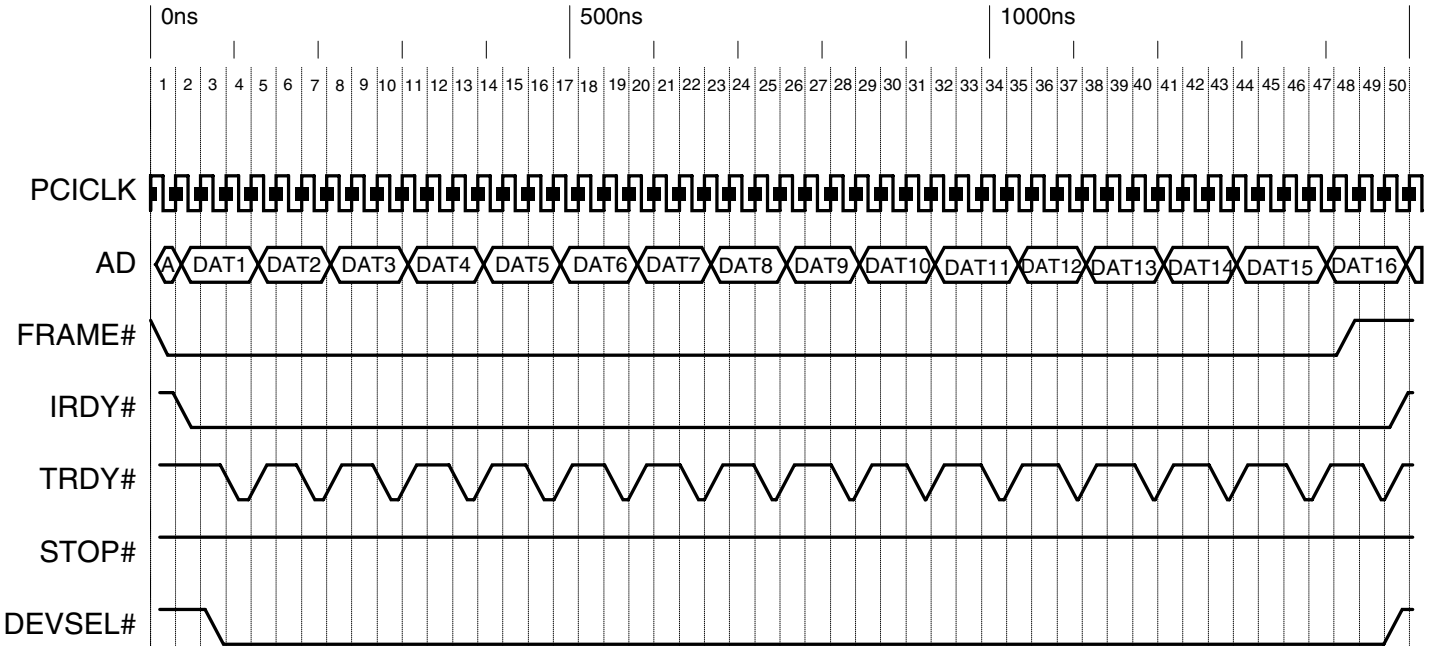


FIGURE 17. PCI WRITE BURST TO ACE MEMORY WITH FIFO EMPTY

INTERFACE TO MIL-STD-1553 BUS WITH 3.3V TRANSCEIVERS (BU-65XXXX8/9)

FIGURE 18 illustrates the interface between the BU-65XXXX8/9 (3.3V transceivers) and a MIL-STD-1553 bus. Connections for both direct (short stub) and transformer (long stub) coupling, as well as the peak to peak voltage levels at various points (when transmitting), are indicated in the diagram.

The center tap of the primary winding (the side of the transformer that connects to the device) must be directly connected to the 3.3V plane. Additionally, a 10µF low inductance tantalum capacitor and 0.01µF ceramic capacitor must be mounted as close as possible and with the shortest leads to the center tap of the transformer(s) and the ground plane.

Furthermore, when the transmitter is transmitting, large currents will flow from the 3.3V plane, into the transformer center tap, thru the primaries, into the TX/RX pins and then out thru the transceiver ground pins into the ground plane. The traces in this path should be sized accordingly and the connections to the ground plane should be as short as possible.

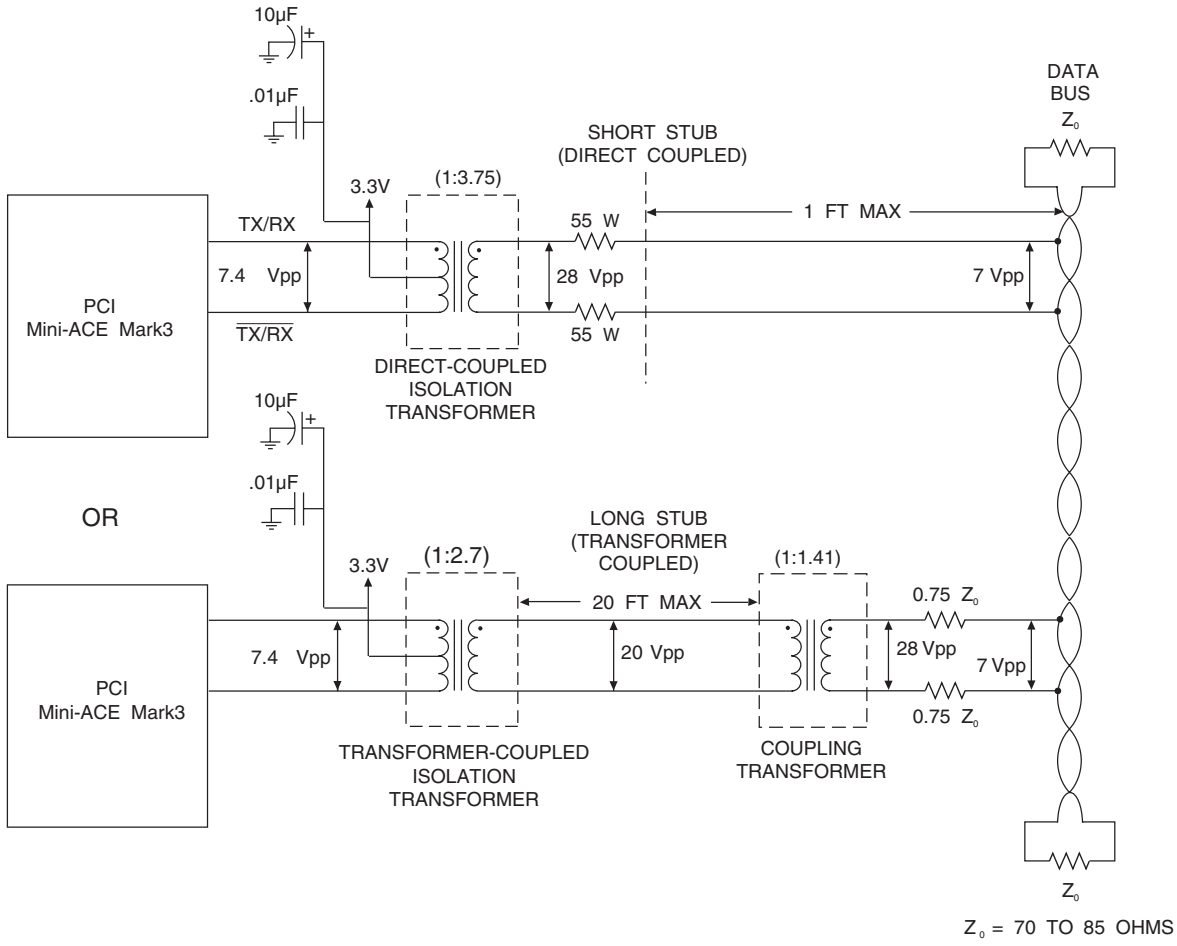


FIGURE 18. BU-65XXXX8/9 (3.3V TRANSCEIVER) INTERFACE TO MIL-STD-1553 BUS

INTERFACE TO MIL-STD-1553 BUS WITH 3.3V TRANSCEIVERS (BU-65XXXXC/D)

FIGURE 19 illustrates the two possible interface methods between the BU-65XXXXC/D and a MIL-STD-1553 bus. Connections for both direct (short stub, 1:2.65) and transformer (long stub, 1:2.07) coupling, as well as nominal peak-to-peak voltage levels at various points (when transmitting), are indicated in the diagram.

The center tap of the primary winding (the side of the transformer that connects to the Mark3) must be directly connected to ground.

Additionally, during transmission, large currents flow from the transceiver power supply through the TX/RX pins into the transformer primaries and then out the center tap into the ground plane. The traces in this path should be sized accordingly and the connections to the ground plane should be as short as possible.

A 10µf, low inductance tantalum capacitor and a 0.01µf ceramic capacitor must be mounted as close as possible and with the shortest leads to the transceiver power input of the Mini-ACE Mark 3.

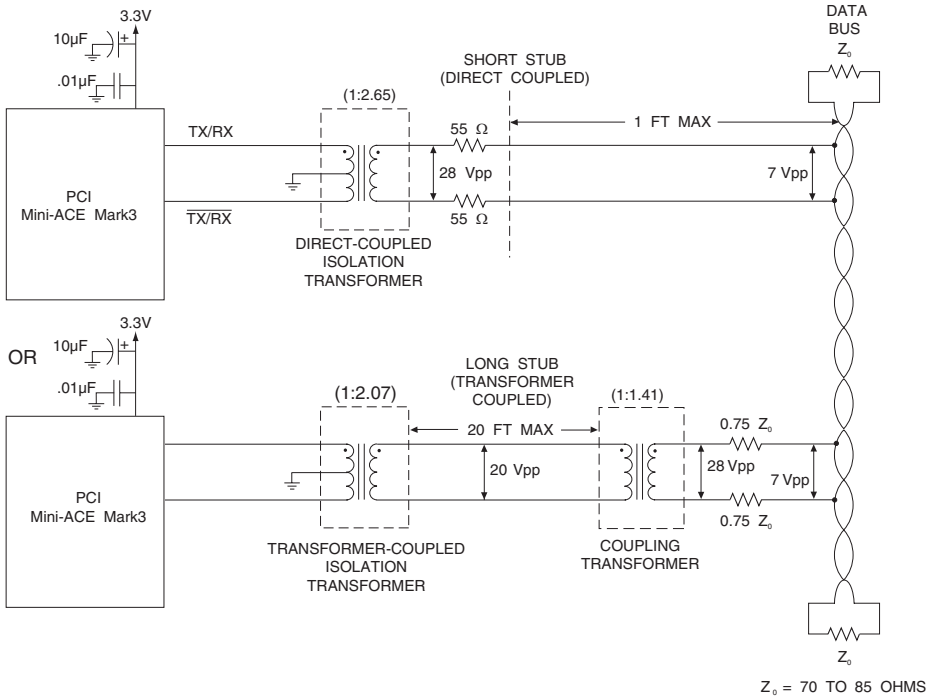


FIGURE 19. BU-65XXXXC/D (3.3V TRANSCEIVER) INTERFACE TO MIL-STD-1553 BUS

3.3V TRANSFORMERS (PCI MINI-ACE MARK3/PCI MICRO-ACE TE WITH 3.3V TRANSCEIVER OPTION)

In selecting 3.3V isolation transformers to be used with the PCI Mini-ACE Mark3/Micro-ACE TE, there is a limitation on the maximum amount of leakage inductance. If this limit is exceeded, the transmitter rise and fall times may increase, possibly causing the bus amplitude to fall below the minimum level required by MIL-STD-1553. In addition, an excessive leakage imbalance may result in a transformer dynamic offset that exceeds 1553 specifications.

The maximum allowable leakage inductance is a function of the coupling method. For Transformer Coupled applications, it is a maximum of 5.0 µH. For Direct it is a maximum of 10.0 µH, and is measured as follows:

The side of the transformer that connects to the device is defined as the "primary" winding. If one side of the primary is shorted to the primary center-tap, the inductance should be measured across the "secondary" (stub side) winding.

This inductance must be less than 5.0 µH (Transformer Coupled) and 10.0 µH (Direct Coupled). Similarly, if the other side of the primary is shorted to the primary center-tap, the inductance measured across the "secondary" (stub side) winding must also be less than 5.0 µH (Transformer Coupled) and 10.0 µH (Direct Coupled).

The difference between these two measurements is the "differential" leakage inductance. This value must be less than 1.0 µH (Transformer Coupled) and 2.0 µH (Direct Coupled).

Beta Transformer Technology Corporation (BTTC), a subsidiary of DDC, manufactures 3.3V transformers in a variety of mechanical configurations with the required turns ratios of 1:3.75 direct coupled, and 1:2.7 transformer coupled for the BU-6XXXX8/9 or 1:2.65 direct coupled and 1:2.07 transformer coupled for the BU-6XXXXC/D. Table 65 provides a listing of these transformers.

For further information, contact BTTC at 631-244-7393 or at www.bttc-beta.com.

TABLE 65. BTTC TRANSFORMERS FOR USE WITH +3.3 VOLT PCI Mini-ACE Mark3 AND PCI MICRO-ACE-TE								
MODEL NUMBER	BTTC PART NUMBER	# OF CHANNELS, CONFIGURATION	COUPLING RATIO DESCRIPTION	COUPLING RATIO (1:X)	MOUNTING	MAX HEIGHT	WIDTH (INCLUDING LEADS)	LENGTH (INCLUDING LEADS)
BU-6XXXXX8/9	MLP-2033	Single	Direct	(1:3.75)	SMT	0.185"	0.4"	0.52"
BU-6XXXXXC/D	MLP-2030	Single	Direct	(1:2.65)	SMT	0.185"	0.4"	0.52"
BU-6XXXXX8/9	MLP-3033	Single	Direct	(1:3.75)	Through Hole	0.185"	0.4"	0.4"
BU-6XXXXX8/9	MLP-2233	Single	Transformer	(1:2.7)	SMT	0.185"	0.4"	0.52"
BU-6XXXXXC/D	MLP-2230	Single	Transformer	(1:2.07)	SMT	0.185"	0.4"	0.52"
BU-6XXXXX8/9	MLP-3233	Single	Transformer	(1:2.7)	Through Hole	0.185"	0.4"	0.4"
BU-6XXXXX8/9	MLP-3333	Single	Direct & Transformer	(1:3.75) & (1:2.7)	Through Hole	0.185"	0.4"	0.4"
BU-6XXXXXC/D	LVB-4230	Single	Transformer	(1:2.07)	SMT	0.165"	1.125"	0.625"
BU-6XXXXXC/D	DSS-3330	Dual (Side-by-Side)	Direct & Transformer	(1:2.65) & (1:2.07)	SMT	0.185"	0.52"	0.675"
BU-6XXXXX8/9	DSS-2033	Dual (Side-by-Side)	Direct	(1:3.75)	SMT	0.13"	0.72"	0.96"
BU-6XXXXX8/9	DSS-2233	Dual (Side-by-Side)	Transformer	(1:2.7)	SMT	0.13"	0.72"	0.96"
BU-6XXXXX8/9	DSS-1003	Dual (Side-by-Side)	Direct & Transformer	(1:3.75) & (1:2.7)	SMT	0.165"	0.72"	0.96"
BU-6XXXXXC/D	DSS-1630	Dual (Side-by-Side)	Direct & Transformer	(1:2.65) & (1:2.07)	SMT	0.165"	0.72"	0.96"
BU-6XXXXXC/D	DLVB-4230	Dual (Stacked)	Transformer	(1:2.07)	SMT	0.165"	0.72"	0.96"
BU-6XXXXX8/9	TSM-2033	Dual (Stacked)	Direct	(1:3.75)	SMT	0.32"	0.4"	0.52"
BU-6XXXXX8/9	TSM-2233	Dual (Stacked)	Transformer	(1:2.7)	SMT	0.32"	0.4"	0.52"
BU-6XXXXXC/D	TSM-2230	Dual (Stacked)	Transformer	(1:2.07)	SMT	0.32"	0.4"	0.52"

INTERFACE TO MIL-STD-1553 BUS (PCI MINI-ACE MARK3/PCI MICRO-ACE TE WITH 5V TRANSCEIVER OPTION)

FIGURE 20 illustrates the interface between the PCI Mini-ACE Mark3/PCI Micro-ACE TE with 5V transceiver option, and a MIL-STD-1553 bus. Connections for both direct (short stub) and transformer (long stub) coupling, as well as the peak to peak voltage levels at various points (when transmitting), are indicated in the diagram.

5V TRANSFORMERS

In selecting 5V isolation transformers to be used with the PCI Mini-ACE Mark3/Micro-ACE TE, there is a limitation on the maximum amount of leakage inductance. If this limit is exceeded, the transmitter rise and fall times may increase, possibly causing the bus amplitude to fall below the minimum level required by MIL-STD-1553. In addition, an excessive leakage inductance imbalance may result in a transmitter dynamic offset that exceeds 1553 specifications.

The maximum allowable leakage inductance is 6.0µH. It is measured as follows:

Defining the side of the transformer that connects to the device as the "primary" winding, if one side of the primary is shorted to the primary center-tap, the inductance should be measured across the "secondary" (stud side) winding. This inductance must be less than 6.0µH. Similarly, if the other side of the primary is shorted to the primary center-tap, the inductance measured across the "secondary" (stub side) winding must also be less than 6.0µH.

The difference between those two measurement is the "differential" leakage inductance. This value must be less than 1.0µH.

Beta Transformer Technology Corporation (BTTC), a subsidiary of DDC, manufactures 5V transformers in a variety of mechanical configurations with the required turns ratios of 1:2.5 direct coupled, and 1:1.79 transformer coupled. Table 66 provides a listing of these transformers.

For further information, contact BTTC at 631-244-7393 or at www.bttc-beta.com.

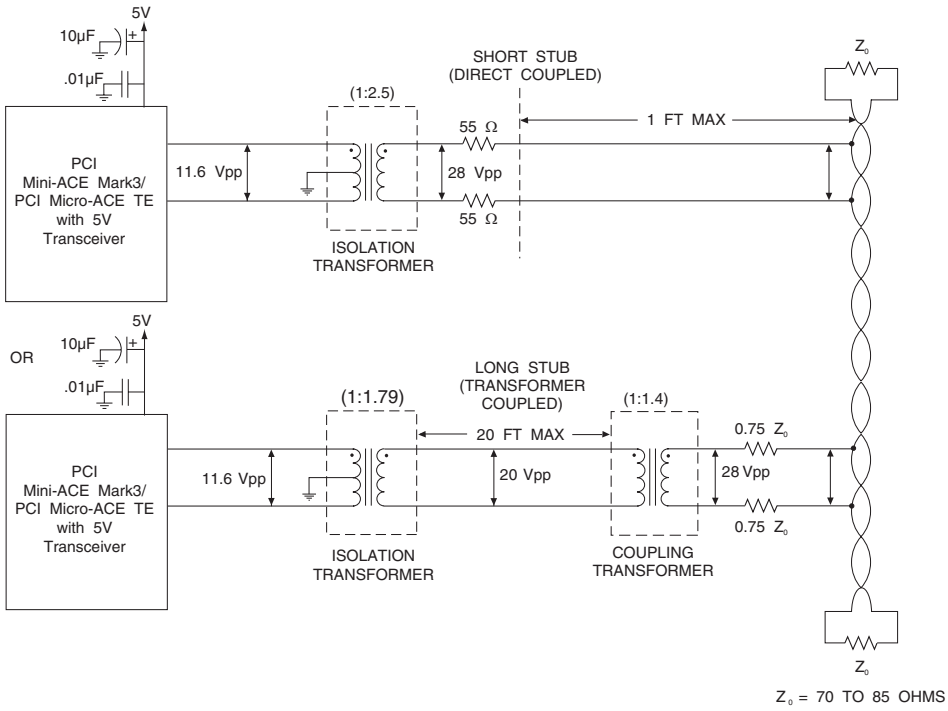


FIGURE 20. BU-65XXXX3/4 (5V TRANSCEIVER) INTERFACE TO MIL-STD-1553 BUS

TABLE 66. BTTC TRANSFORMERS FOR USE WITH +5.0 VOLT PCI Mini-ACE Mark3 / PCI MICRO-ACE-TE

BTTC PART NUMBER	# OF CHANNELS, CONFIGURATION	COUPLING RATIO DESCRIPTION	COUPLING RATIO (1:X)	MOUNTING	MAX HEIGHT	WIDTH (INCLUDING LEADS)	LENGTH (INCLUDING LEADS)
MLP-2005	Single	Direct	(1:2.5)	SMT	0.185"	0.4"	0.52"
MLP-3005	Single	Direct	(1:2.5)	Through Hole	0.185"	0.4"	0.4"
B-3230 (-30) #	Single	Direct	(1:2.5)	Through Hole	0.25"	0.35"	0.5"
MLP-2205	Single	Transformer	(1:1.79)	SMT	0.185"	0.4"	0.52"
MLP-3205	Single	Transformer	(1:1.79)	Through Hole	0.185"	0.4"	0.4"
B-3229 (-29) #	Single	Transformer	(1:1.79)	Through Hole	0.25"	0.35"	0.5"
HLP-6015 #	Single	Direct & Transformer	(1:2.5) & (1:1.79)	SMT	0.19"	0.63"	1.13"
B-3227 (-27) #	Single	Direct & Transformer	(1:2.5) & (1:1.79)	SMT	0.29"	0.63"	1.13"
MLP-3305	Single	Direct & Transformer	(1:2.5) & (1:1.79)	Through Hole	0.185"	0.4"	0.4"
B-3226 (-26) #	Single	Direct & Transformer	(1:2.5) & (1:1.79)	Through Hole	0.25"	0.625"	0.625"
HLP-6014 #	Single	Direct & Transformer	(1:2.5) & (1:1.79)	Flat Pack	0.19"	0.63"	1.13"
B-3231 (-31) #	Single	Direct & Transformer	(1:2.5) & (1:1.79)	Flat Pack	0.29"	0.63"	1.13"
DSS-2005	Dual (Side-by-Side)	Direct	(1:2.5)	SMT	0.13"	0.72"	0.96"
DSS-2205	Dual (Side-by-Side)	Transformer	(1:1.79)	SMT	0.13"	0.72"	0.96"
DSS-1005	Dual (Side-by-Side)	Direct & Transformer	(1:2.5) & (1:1.79)	SMT	0.165"	0.72"	0.96"

TABLE 66. BTTC TRANSFORMERS FOR USE WITH +5.0 VOLT PCI Mini-ACE Mark3 / PCI MICRO-ACE-TE (CONT.)							
BTTC PART NUMBER	# OF CHANNELS, CONFIGURATION	COUPLING RATIO DESCRIPTION	COUPLING RATIO (1:X)	MOUNTING	MAX HEIGHT	WIDTH (INCLUDING LEADS)	LENGTH (INCLUDING LEADS)
TSM-2005	Dual (Stacked)	Direct	(1:2.5)	SMT	0.32"	0.4"	0.52"
TSM-2205	Dual (Stacked)	Transformer	(1:1.79)	SMT	0.32"	0.4"	0.52"
TST-9117 #	Dual (Stacked)	Direct & Transformer	(1:2.5) & (1:1.79)	SMT	0.335"	1.125"	1.125"
TST-9107 #	Dual (Stacked)	Direct & Transformer	(1:2.5) & (1:1.79)	Through Hole	0.335"	0.625"	0.625"
TST-9127 #	Dual (Stacked)	Direct & Transformer	(1:2.5) & (1:1.79)	Flat Pack	0.335"	0.625"	0.625"

Notes:
1. All Transformers in the table above can be used with BU-6XXXXX3/6 (1553B transceivers).
2. Transformers identified with "#" in the table above are not recommended for use with the BU-6XXXXX4 (McAir-Compatable transceivers)

THERMAL MANAGEMENT FOR PCI MICRO-ACE TE (BGA PACKAGE)

Ball Grid Array (BGA) components necessitate that thermal management issues be considered early in the design stage for MIL-STD-1553 terminals. This is especially true if high transmitter duty cycles are expected. The temperature range specified for the PCI Micro-ACE TE devices refer to case temperature. Any duty cycle is acceptable as long as the case temperature is maintained within the extended industrial temperature range specified for the -Exx parts. See below for an explanation of the thermal management requirements for high transmitter duty cycles with the military temperature range components.

All PCI Micro-ACE TE devices incorporate multiple package connections (28-balls for 3.3V transceiver, 34 balls for 5V transceivers) which perform the dual function of transceiver circuit ground and thermal heat sink. Each transceiver has 14 or 17 contiguous balls arranged in a rectangle. Refer to FIGURE 21 and FIGURE 24 for a visual representation of the thermal ball locations. It is mandatory that these thermal balls be directly soldered to a circuit ground plane (a circuit trace is insufficient). Operation without an adequate ground/thermal plane is not recommended and extended exposure to these conditions may affect device reliability.

The purpose of this ground/thermal plane is to conduct the heat being generated by the transceivers within the package away from the PCI Micro-ACE-TE. Since the thermal balls are contiguous, a mini-plane can be created on the PCB top layer and thermal vias can then be sunk down thru the top-side mini-plane into the appropriate thermal plane.

The temperature of each chip within the PCI Micro-Ace TE must be maintained below its respective maximum operating junction temperature as specified in Table 1. The simplest method to ensure this is to attribute all internal power dissipation to the transceiver, use the θ_{Jx} numbers also specified in Table 1 to calculate the temperature rise at the transceiver, and ensure that the temperature at the transceiver never exceeds the lowest maximum operating junction temperature allowed for any internal component (135°C for the protocol chip).

The general equation for the heat rise from ambient to the source of heat inside a component (typically the transistor junctions) is $\Delta T=P*\theta$ where P is the power dissipation of the component and θ is the thermal impedance from the junctions to ambient. Here there are two heat paths to the ambient, up through the top of the case, and down through the PCB, so we have a pair of equations:

$$\Delta T = P_C*(\theta_{JC}+\theta_{CA}) = P_B*(\theta_{JB}+\theta_{BA}) \text{ and } P = P_C+P_B.$$

Where P_C is the portion of the component power which flows through the top of the case to the ambient, θ_{JC} is the thermal impedance of the component from the junctions to the top of the case, and θ_{CA} is the thermal impedance of the system from the top of the case to ambient. Similarly, P_B is the portion of the component power which flows through the bottom of the case into the PCB, θ_{JB} is the thermal impedance of the component from the transistor junctions to the board, and θ_{BA} is the thermal impedance of the system from the board under the component to ambient.

For the case of a BU-65843BC-102 used as a monitor terminal, P=0.19W and θ_{JB}=31.3°C/W. This can be simplified by assuming that no heat flows out through the top of the case and only measuring the rise above package temperature without considering the whole path to ambient (ignoring θ_{BA}). The equation thus simplifies to:

$$\Delta T = P*(\theta_{JB}) = 0.19*(31.3+0) = 5.9°C$$

With a package temperature of 125°, this leaves the junction temperature below the maximum of 135°C.

The transmit duty cycle of a remote terminal is typically under 25%, with a few exceptions for high bandwidth devices like data

loaders. Substituting the 25% duty cycle power (P=0.35W) into the equation above leads to a temperature rise of 10.955°C, which is just beyond the acceptable limit for a board temp of 125°C, so board temp would have to be limited to 124°C, or duty cycle would need to be limited below 25%.

For a bus controller, higher duty cycles are common, so it may be necessary to add some form of heat sink to remove heat from the top of the component as well. For a BU-65863BC-102 with a duty cycle of 100%, P=0.69W. If the cooling paths from the top and bottom of the case to the ambient are assumed to be equally effective, ignoring θ_{CA} and θ_{BA} and setting the temperatures at both the top and bottom of the component to be the same, then the equations become:

$$\Delta T = P_C*(20.8) = P_B*(31.3)$$

And:

$$0.69 = P_C+P_B$$

Which turns into:

$$P_C = 0.69-P_B$$

Substituting for P_C and θ_{Jx} in the equation for ΔT, we get:

$$\Delta T = (0.69-P_B)*(20.8) = P_B*(31.3)$$

$$14.352-20.8*P_B = 31.3*P_B$$

$$13.936 = 52.1*P_B$$

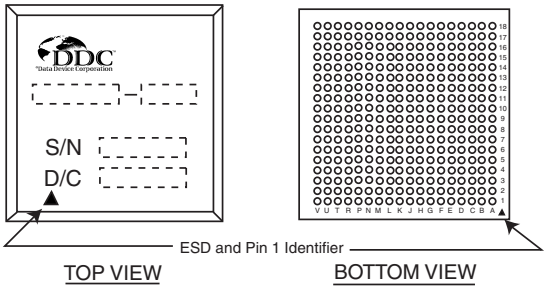
$$P_B = 0.275$$

Substituting this result back into the ΔT equation, we get:

$$\Delta T = 0.2999*26.5 = 8.6°C$$

So as long as both the top and bottom of the case are maintained below 125°C, using heat sinks if necessary, the junction temperatures will remain within the acceptable limits.

For applications where high duty cycle operation is required at high ambient temperature, DDC also provides a thermal model that can be used with the FloTherm modeling tool from Mentor Graphics to assign power dissipation numbers to each internal component and determine the resulting operating junction temperature of each, allowing the assurance of proper operation without requiring excessively conservative estimates that can hurt performance and increase costs.



Notes:
1) For BU-65843B8/BU-65863B8, balls D3, D4, D5, E3, E4, E5, F1, F2, F3, F4, F5, G3, G4, G5, L3, L4, L5, M3, M4, M5, N1, N2, N3, N4, N5, P3, P4, P5 must be connected to a thermal plane to maintain recommended operating temperature.
2) For BU-65843B3/BU-65863B3, D3, D4, D5, E2, E3, E4, E5, F3, F4, F5, G2, G3, G4, G5, H3, H4, H5, P11, P12, P13, P14, P15, R11, R12, R13, R14, R15, T11, T12, T13, T14, T15, U12, U14 must be connected to a thermal plane to maintain recommended operating temperature

FIGURE 21. THERMAL BALL LOCATIONS FOR PCI MICRO-ACE-TE (BGA PACKAGE)

TABLE 67. POWER AND GROUND, CQFP				
SIGNAL NAME	BU-65743X3/X4 BU-65843X3/X4 BU-65863X3/X4	BU-65743X8/X9 BU-65843X8/X9 BU-65863X8/X9	BU-65743X0 BU-65843X0 BU-65863X0	DESCRIPTION
	PIN	PIN	PIN	
+ 5.0V_Xcvr	10	-	-	+ 5.0 Volt Transceiver Power
+ 3.3V_Xcvr	-	10	-	+3.3 Volt Transceiver Power
+ 3.3V_Logic	30,51,69	30, 51, 69	10, 30, 51, 69	Logic Power
Gnd_Xcvr	22, 79	22, 79	-	Transceiver Ground
Gnd_Logic	31, 50, 70	31, 50, 70	22, 79, 31, 50, 70	Logic Ground

NOTE: Logic ground and transceiver ground are **NOT** tied together inside the package.

TABLE 68. POWER AND GROUND, BGA WITH 3.3V TRANSCEIVERS		
SIGNAL NAME	BU-65843B8 BU-65863B8	DESCRIPTION
	BALL	
3.3V_XCVR	A4, A5, B4, B5, J1, J2, J3, J4, J5, K1, K2, K3, K4, K5 , U4, U5, V4, V5	TRANSCEIVER POWER
3.3V_LOGIC	A8, A9, B8, B9, L16, L17, M16, M17, N12, N13, P12, P13, R6, R7, T6, T7, U6, U7, V6, V7	LOGIC POWER
GND_XCVR	D3, D4, D5, E3, E4, E5, F1, F2, F3, F4, F5, G3, G4, G5, L3, L4, L5, M3, M4, M5, N1, N2, N3, N4, N5, P3, P4, P5	TRANSCEIVER GROUND (THERMAL BALLS)
GND_LOGIC	E10, E11, E12, F10, F11, F12, G10, G11, G12, H10, H11, H12, R11, R12, R13, T11, T12, T13, U11, U12, U13	LOGIC GROUND

NOTE: Logic ground and transceiver ground are **NOT** tied together inside the package.

TABLE 69. POWER AND GROUND, BGA WITH 5V TRANSCEIVERS		
SIGNAL NAME	BU-65843B3 BU-65864B3	DESCRIPTION
	BALL	
5V_Vcc_CHA	F1, F2	TRANSCEIVER “A” POWER
5V_Vcc_CHB	U13, V13	TRANSCEIVER “B” POWER
5V_RAM	P4, R4	5V RAM **(BU-65864B3 ONLY)**
3.3V_LOGIC	A7, L1, L2, L15, L16, M3, P7, P9, R9, V8	LOGIC POWER
GND_XCVR	D3, D4, D5, E2, E3, E4, E5,F3, F4, F5, G2, G3, G4, G5, H3, H4, H5, P11, P12, P13, P14, P15, R11, R12, R13, R14, R15, T11, T12, T13, T14, T15, U12, U14	TRANSCEIVER GROUND (THERMAL BALLS)
GND_LOGIC	E12, E13, E14, F12, F13, F14, G12, G13, G14, H12, H13, H14	LOGIC GROUND

NOTE: Logic ground and transceiver ground **ARE** tied together inside the package.

TABLE 70. 1553 ISOLATION TRANSFORMER INTERFACE (BU-65XXXX8/X9/X3/X4 VERSIONS)				
SIGNAL NAME	PIN	5V	3V	DESCRIPTION
		BALL	BALL	
TX/RX-A (I/O)	3	D1, D2, E1	D1, D2, E1, E2	Analog Transmit/Receive Input/Outputs. Connect directly to 1553 isolation transformers. For BGA versions, connect all balls of the signal together.
$\overline{\text{TX/RX-A}}$ (I/O)	5	G1, H1, H2	G1, G2, H1, H2	
TX/RX-B (I/O)	15	U11, V11, V12	L1, L2, M1, M2	
$\overline{\text{TX/RX-B}}$ (I/O)	17	U15, V14, V15	P1, P2, R1, R2	

TABLE 71. INTERFACE TO EXTERNAL TRANSCEIVER (BU-65XXXF(G)0 VERSIONS)		
SIGNAL NAME	PIN	DESCRIPTION
TXDATA_A (O)	3	DIGITAL MANCHESTER BIPHASE TRANSMIT OUTPUTS, A BUS
$\overline{\text{TXDATA\_A}}$ (O)	5	
RXDATA_A (I)	8	DIGITAL MANCHESTER BIPHASE RECEIVE INPUTS, A BUS
$\overline{\text{RXDATA\_A}}$ (I)	4	
TX_INH_A_OUT (O)	11	DIGITAL OUTPUT TO INHIBIT EXTERNAL TRANSMITTER, A BUS
TXDATA_B (O)	15	DIGITAL MANCHESTER BIPHASE TRANSMIT OUTPUTS, B BUS
$\overline{\text{TXDATA\_B}}$ (O)	17	
RXDATA_B (I)	21	DIGITAL MANCHESTER BIPHASE RECEIVE INPUTS, B BUS
$\overline{\text{RXDATA\_B}}$ (I)	16	
TX_INH_B_OUT (O)	9	DIGITAL OUTPUT TO INHIBIT EXTERNAL TRANSMITTER, B BUS

TABLE 72. MANDATORY ADDITIONAL CONNECTIONS & INTERFACE TO EXTERNAL TRANSCEIVER (BGA'S ONLY)				
SIGNAL NAME	DESIGN USES INTERNAL TRANSCEIVERS	BU-65843B3 BU-65864B3	BU-65843B8 BU-65863B8	FOR USE WITH EXTERNAL TRANSCEIVERS "TRANSCEIVERLESS"
		BALL	BALL	
$\overline{\text{SNGL\_END}}$ (I)	No Connect "NC"	A15	D14	If $\overline{\text{SNGL\_END}}$ is connected to logic "0" the Manchester decoder inputs (RX_DATA_IN_X) will be configured to accept single-ended input signals (e.g.,MIL-STD-1773 fiber optic receiver outputs). If $\overline{\text{SNGL\_END}}$ is connected to logic "1," the decoder inputs will be configured to accept standard double-ended Manchester bi-phase input signals (i.e., MIL-STD-1553 receiver outputs).
TXINH_IN_A (I)	These two signals MUST be directly connected for normal "Built-In" transceiver operation.	A4	E7	Do NOT connect these two signals together. Connect TXINH_OUT (Digital transmit inhibit output) to the TX INH input of external MIL-STD-1553 transceivers. Asserted high to inhibit when not transmitting on the respective bus.
TXINH_OUT_A (O)		A5	E8	

NOTE: The BGA versions can be operated with either their internal transceivers or with external transceivers. When the devices are operated with their internal transceivers the customer must supply PCB traces that connect the device's "inputs to outputs" (within the correct column) as described in this table. For example, to operate the BU-65843B8/BU-65863B8 with their internal transceivers, PCB traces must connect E7 to E8, C7 to C8, D7 to D8, etc..

TABLE 72. MANDATORY ADDITIONAL CONNECTIONS & INTERFACE TO EXTERNAL TRANSCEIVER (BGA'S ONLY) (CONT)

SIGNAL NAME	DESIGN USES INTERNAL TRANSCEIVERS	BU-65843B3 BU-65864B3	BU-65843B8 BU-65863B8	FOR USE WITH EXTERNAL TRANSCEIVERS "TRANSCEIVERLESS"
		BALL	BALL	
TXDATA_IN_A (I)	These two signals MUST be directly connected for normal "Built-In" transceiver operation.	C8	C7	Do NOT connect these two signals together. Connect TXDATA_OUT (Digital manchester biphase transmit data output) directly to the corresponding input of a MIL-STD-1553 or MIL-STD-1773 (fiber optic) transceiver.
TXDATA_OUT_A (O)		B8	C8	
$\overline{\text{TXDATA\_IN\_A}}$ (I)	These two signals MUST be directly connected for normal "Built-In" transceiver operation.	C4	D7	Do NOT connect these two signals. Connect $\overline{\text{TXDATA\_OUT}}$ (Digital manchester biphase transmit data output) directly to the corresponding input of a MIL-STD-1553 or MIL-STD-1773 (fiber optic) transceiver.
$\overline{\text{TXDATA\_OUT\_A}}$ (O)		C5	D8	
$\overline{\text{RXDATA\_IN\_A}}$ (I)	These two signals MUST be directly connected for normal "Built-In" transceiver operation.	D10	G8	Do NOT connect these two signals together. Connect $\overline{\text{RXDATA\_IN}}$ (Digital manchester biphase receive data input) directly to the corresponding output of a MIL-STD-1553 or MIL-STD-1773 (fiber optic) transceiver.
$\overline{\text{RXDATA\_OUT\_A}}$ (O)		E10	G7	
RXDATA_IN_A (I)	These two signals MUST be directly connected for normal "Built-In" transceiver operation.	E9	H8	Do NOT connect these two signals together. Connect RXDATA_IN (Digital manchester biphase receive data input) directly to the corresponding output of a MIL-STD-1553 or MIL-STD-1773 (fiber optic) transceiver.
RXDATA_OUT_A (O)		F9	H7	
TXINH_IN_B (I)	These two signals MUST be directly connected for normal "Built-In" transceiver operation.	T8	N7	Do NOT connect these two signals together. Connect TXINH_OUT (Digital transmit inhibit output) to the corresponding input of external MIL-STD-1553 transceiver. Asserted high to inhibit when not transmitting on the respective bus.
TXINH_OUT_B (O)		R8	N8	
TXDATA_IN_B (I)	These two signals MUST be directly connected for normal "Built-In" transceiver operation.	R10	L7	Do NOT connect these two signals together. Connect TXDATA_OUT (Digital manchester biphase transmit data output) to the corresponding input of a MIL-STD-1553 or MIL-STD-1773 (fiber optic) transceiver.
TXDATA_OUT_B (O)		P10	L8	
$\overline{\text{TXDATA\_IN\_B}}$ (I)	These two signals MUST be directly connected for normal "Built-In" transceiver operation.	N12	M7	Do NOT connect these two signals together. Connect $\overline{\text{TXDATA\_OUT}}$ (Digital manchester biphase transmit data output) directly to corresponding inputs of a MIL-STD-1553 or MIL-STD-1773 (fiber optic) transceiver.
$\overline{\text{TXDATA\_OUT\_B}}$ (O)		M12	M8	
$\overline{\text{RXDATA\_IN\_B}}$ (I)	These two signals MUST be directly connected for normal "Built-In" transceiver operation.	M13	P10	Do NOT connect these two signals together. Connect $\overline{\text{RXDATA\_IN}}$ (Digital manchester biphase receive data input) directly to the corresponding output of a MIL-STD-1553 or MIL-STD-1773 (fiber optic) transceiver
$\overline{\text{RXDATA\_OUT\_B}}$ (O)		M14	P9	
RXDATA_IN_B (I)	These two signals MUST be directly connected for normal "Built-In" transceiver operation.	N13	R10	Do NOT connect these two signals together. Connect RXDATA_IN (Digital manchester biphase receive data input) directly to the corresponding output of a MIL-STD-1553 or MIL-STD-1773 (fiber optic) transceiver.
RXDATA_OUT_B (O)		N14	R9	

NOTE: The BGA versions can be operated with either their internal transceivers or with external transceivers. When the devices are operated with their internal transceivers the customer must supply PCB traces that connect the device's "inputs to outputs" (within the correct column) as described in this table. For example, to operate the BU-65843B8/BU-65863B8 with their internal transceivers, PCB traces must connect E7 to E8, C7 to C8, D7 to D8, etc..

TABLE 73. PROCESSOR INTERFACE CONTROL

SIGNAL NAME	PIN	BALL 3V	BALL 5V	DESCRIPTION
$\overline{\text{SSFLAG}}$ (I)/ EXT_TRIG (I)	20	U10	L9	Subsystem Flag (RT) or External Trigger (BC/Word Monitor) input. In RT mode with standard status word, if this input is asserted low, the Subsystem Flag bit will be set in the PCI MINI-ACE MARK3/MICRO-ACE TE's RT Status Word. If the $\overline{\text{SSFLAG}}$ input is logic "0" while bit 8 of Configuration Register #1 has been programmed to logic "1" (cleared), the Subsystem Flag RT Status Word bit will become logic "1", but bit 8 of Configuration Register #1, $\overline{\text{SUBSYSTEM FLAG}}$, will return logic "1" when read. That is, the sense on the $\overline{\text{SSFLAG}}$ input has no effect on the $\overline{\text{SUBSYSTEM FLAG}}$ register bit. This input has no meaning in RT mode with alternate status word. In the non-enhanced BC mode, this signal operates as an External Trigger input. In BC mode, if the external BC Start option is enabled (bit 7 of Configuration Register #1), a low to high transition on this input will issue a BC Start command, starting execution of the current BC frame. In the enhanced BC mode, during the execution of a Wait for External Trigger (WTG) instruction, the PCI Mini-ACE Mark3/Micro-ACE TE BC will wait for a low-to-high transition on EXT_TRIG before proceeding to the next instruction. In the Word Monitor mode, if the external trigger is enabled (bit 7 of Configuration Register #1), a low to high transition on this input will initiate a monitor start. (RT the monitor on low). In all modes this input operates as an external trigger, this signal should remain asserted for at least 4 1533_CLK ticks after it goes high. This input has no effect in Message Monitor mode.

TABLE 74. RT ADDRESS

SIGNAL NAME	PIN	BALL 3V	BALL 5V	DESCRIPTION
RTAD4 (MSB) (I)	80	A7	A10	RT Address inputs (5V tolerant). If bit 5 of Configuration Register #6, RT ADDRESS SOURCE, is programmed to logic "0" (default), then the PCI Mini-ACE Mark3/Micro-ACE TE's RT address is provided by means of these 5 input signals. In addition, if RT ADDRESS SOURCE is logic "0", the source of RT address parity is RTADP. There are many methods for using these input signals for designating the PCI Mini-ACE Mark3/Micro-ACE TE's RT address. For details, refer to the description of RT_AD_LAT. If RT ADDRESS SOURCE is programmed to logic "1", then the PCI Mini-ACE Mark3/Micro-ACE TE's source for its RT address and parity is under software control, when the SW writes to config reg #5 internal address bits 4-0 will be latched from PCI data bus bit AD5-1 and internal RTADP will be latched from PCI data bus bit AD0. In this case, the RTAD4-RTAD0 and RTADP signals are not used.
RTAD3 (I)	7	D10	C9	
RTAD2 (I)	2	C15	A8	
RTAD1 (I)	1	E6	B9	
RTAD0 (LSB) (I)	6	A6	C11	
RTADP (I)	13	E9	D6	Remote Terminal Address Parity. This input signal (5V tolerant) must provide an odd parity sum with RTAD4-RTAD0 in order for the RT to respond to non-broadcast commands. That is, there must be an odd number of logic "1"s from among RTAD-4-RTAD0 and RTADP
RT_AD_LAT (I)	12	D9	C7	RT Address Latch. Input signal (5V tolerant) used to control the PCI Mini-ACE Mark3/Micro-ACE TE's internal RT address latch. If RT_AD_LAT is connected to logic "0", then the PCI Mini-ACE Mark3/Micro-ACE TE RT is configured to accept a hardwired (transparent) RT address from RTAD4-RTAD0 and RTADP. If RT_AD_LAT is initially logic "0", and then transitions to logic "1", the values presented on RTAD4-RTAD0 and RTADP will be latched internally on the rising edge of RT_AD_LAT. If RT_AD_LAT is connected to logic "1", then the PCI Mini-ACE Mark3/Micro-ACE TE's RT address is latchable under host processor control. In this case, there are two possibilities: (1) If bit 5 of Configuration Register #6, RT ADDRESS SOURCE, is programmed to logic "0" (default), then the source of the RT Address is the RTAD4-RTAD0 and RTADP input signals; (2) If RT ADDRESS SOURCE is programmed to logic "1", then the source of the RT Address is the lower 6 bits of the PCI data bus, D5-D1 (for RTAD4-0) and D0 (for RTADP). In either of these two cases (with RT_AD_LAT = "1"), the processor will cause the RT address to be latched by: (1) writing bit 15 of Configuration Register #3, ENHANCED MODE, to logic "1"; (2) writing bit 3 of Configuration Register #4, LATCH RT ADDRESS WITH CONFIGURATION REGISTER #5, to logic "1"; and (3) writing to Configuration Register #5. In the case of RT ADDRESS SOURCE = "1", then the values of RT address and RT address parity must be written to the lower 6 bits of Configuration Register #5, via D5-D0. In the case where RT ADDRESS SOURCE = "0", the bit values presented on D5-D0 become "don't care".

TABLE 75. MISCELLANEOUS SIGNALS

SIGNAL NAME	PIN	BALL 3V	BALL 5V	DESCRIPTION
$\overline{\text{INCMD}}$ (O)/ $\overline{\text{MCRST}}$ (O)	19	C9	E8	In-command or Mode Code Reset. The function of this pin is controlled by bit 0 of Configuration Register #7, $\overline{\text{MODE CODE RESET}}$ / $\overline{\text{INCMD}}$ SELECT. If this register bit is logic "0" (default), $\overline{\text{INCMD}}$ will be active on this pin. For BC, RT, or Selective Message Monitor modes, $\overline{\text{INCMD}}$ is asserted low whenever a message is being processed by the PCI Mini-ACE Mark3/Micro-ACE TE. In Word Monitor mode, $\overline{\text{INCMD}}$ will be asserted low for as long as the monitor is online. For RT mode, if MODE CODE RESET/$\overline{\text{INCMD}}$ SELECT is programmed to logic "1", $\overline{\text{MCRST}}$ will be active. In this case, $\overline{\text{MCRST}}$ will be asserted low for two clock cycles following receipt of a Reset remote terminal mode command. In BC or Monitor modes, if MODE CODE RESET/$\overline{\text{INCMD}}$ SELECT is logic "1", this signal is inoperative; i.e., in this case, it will always output a value of logic "1".
TAG_CLK (I)	23	F14	D18	Input (5V tolerant) for optional external tag clock. No connection needed if internal tag clock is used. Maximum TAG_CLK frequency is 1/4th of the 1553_CLK input.
SLEEP_IN (I)	14	R4	--	Sleep input for both 3.3V transceivers. SLEEP_IN = 1 puts the 3.3V transceivers in sleep mode (receiver and transmitter disabled).
1553_CLK (I)	78	B7	D8	20 MHz, 16 MHz, 12 MHz, or 10 MHz clock input.
TX_INH A/B (I)	18	F8	F10	Transmitter inhibit input (5V tolerant) for the Channel A and Channel B MIL-STD-1553 transmitters. For normal operation, this input should be connected to logic "0". To force a shutdown of Channel A and Channel B, a value of logic "1" should be applied to the TX_INH input.
$\overline{\text{MSTCLR}}$ ($\overline{\text{RST}}$#) (I)	25	R18	B11	Master Clear. Negative true Reset input, normally asserted low following power turn-on. This input conforms to PCI $\overline{\text{RST}}$# convention.

TABLE 76. MISCELLANEOUS SIGNALS, BGA ONLY

<table>
<tr><th rowspan="2">SIGNAL NAME</th><th>BALL</th><th>BALL</th><th rowspan="2">DESCRIPTION</th></tr>
<tr><th>3V XCVR</th><th>5V XCVR</th></tr>
<tr><td rowspan="6">$\overline{\text{RTBOOT}}$ (I)</td><td rowspan="6">F7</td><td rowspan="6">C12</td><td colspan="3">If $\overline{\text{RTBOOT}}$ is connected to Logic "0" the PCI Micro ACE TE will initialize in RT mode with the Busy status word bit set following power turn on. Received data will not be stored because the “BUSY RECEIVE TRANSFER DISABLE” bit will also be set following power turn on. In addition, CLK_SEL_0 and CLK_SEL_1 are enabled and they select the divider for the 1553 clock circuitry:</td></tr>
<tr><td>CLK_SEL1</td><td>CLK_SEL0</td><td>1553 CLOCK FREQUENCY</td></tr>
<tr><td>0</td><td>0</td><td>10 MHz</td></tr>
<tr><td>0</td><td>1</td><td>20 MHz</td></tr>
<tr><td>1</td><td>0</td><td>12 MHz</td></tr>
<tr><td>1</td><td>1</td><td>16 MHz</td></tr>
<tr><td>CLK_SEL_0 (I)</td><td>L14</td><td>M18</td><td colspan="3">1553 CLOCK SELECT 0, ACTIVE ONLY WHEN $\overline{\text{RTBOOT}}$ = 0</td></tr>
<tr><td>CLK_SEL_1 (I)</td><td>E14</td><td>B15</td><td colspan="3">1553 CLOCK SELECT 1, ACTIVE ONLY WHEN $\overline{\text{RTBOOT}}$ = 0</td></tr>
</table>

TABLE 77. PCI BUS ADDRESS AND DATA SIGNALS				
SIGNAL NAME	**PIN**	**BALL 3V**	**BALL 5V**	**DESCRIPTION**
AD31 (I/O)	27	V9	D7	32-Bit PCI Bus Address / Data lines. Address and Data are multiplexed on the same pins. Each bus operation consists of an address phase followed by one or more data phases. Address phases are identified when the control signal FRAME# is asserted. Data transfers occur during those clock cycles in which the control signals IRDY# and TRDY# are both asserted.
AD30 (I/O)	28	T8	M10	
AD29 (I/O)	29	R17	L10	
AD28 (I/O)	32	P17	H16	
AD27 (I/O)	33	U8	E7	
AD26 (I/O)	34	N17	L11	
AD25 (I/O)	35	V8	N9	
AD24 (I/O)	36	P18	L18	
AD23 (I/O)	39	M18	K17	
AD22 (I/O)	40	J15	J16	
AD21 (I/O)	41	J18	G18	
AD20 (I/O)	42	K16	J17	
AD19 (I/O)	43	H18	G17	
AD18 (I/O)	44	K18	J18	
AD17 (I/O)	45	L18	K18	
AD16 (I/O)	46	K17	H17	
AD15 (I/O)	59	D16	D15	
AD14 (I/O)	60	E18	F16	
AD13 (I/O)	61	D17	D16	
AD12 (I/O)	62	B15	C15	
AD11 (I/O)	63	D18	D17	
AD10 (I/O)	64	A15	C14	
AD9 (I/O)	65	A14	A14	
AD8 (I/O)	67	B14	C13	
AD7 (I/O)	68	A12	A12	
AD6 (I/O)	71	B11	A11	
AD5 (I/O)	72	B6	J7	
AD4 (I/O)	73	A11	C10	
AD3 (I/O)	74	C12	C6	
AD2 (I/O)	75	C10	B7	
AD1 (I/O)	76	A10	A9	
AD0 (I/O) (LSB)	77	B10	B10	

TABLE 77. PCI BUS ADDRESS AND DATA SIGNALS (CONT)

SIGNAL NAME	PIN	BALL 3V	BALL 5V	DESCRIPTION
C/BE[3]# (I)	37	R8	J8	Bus Command and Byte Enables. These signals are multiplexed on the same pins. During the address phase of a bus operation, these pins identify the bus command, as shown in the table below. During the data phase of a bus operation, these pins are used as Byte Enables, with C/BE[0]# enabling byte 0 (LSB) and C/BE[3]# enabling byte 3 (MSB). The PCI Mini-ACE Mark3/Micro-ACE TE responds to the following PCI commands **C/BE[3:0]# — Description (during address phase)** 0 1 1 0 — Memory Read 0 1 1 1 — Memory Write 1 0 1 0 — Configuration Read 1 0 1 1 — Configuration Write 1 1 0 0 — Memory Read Multiple 1 1 1 0 — Memory Read Line 1 1 1 1 — Memory Write and Invalidate Note that the last three memory commands are aliased to the basic memory commands: Memory Read and Memory Write.
C/BE[2]# (I)	47	J17	H18	
C/BE[1]# (I)	58	E17	E15	
C/BE[0]# (I)	66	B12	B12	
PAR (I/O)	57	F16	F15	Parity. This signal is even parity across the entire AD[31:0] field along with the C/BE[3:0]# field. The parity is stable in the clock following the address phase and is sourced by the Bus Master. During the data phase for write operations, the Bus Master sources this signal on the clock following IRDY# active. During the data phase for read operations, this signal is sourced by the Target and is valid on the clock following TRDY# active. The PAR signal therefore has the same timing as AD[31:0], delayed by one clock.
PCI_CLK (I)	26	T10	M9	Clock input. The rising edge of this signal is the reference upon which all other clock signals are based, with the exception of RST# and INTA#. The maximum frequency accepted is 33 MHz and the minimum is 0 Hz.

TABLE 78. PCI CONTROL BUS SIGNALS (NOTE THAT ALL SIGNALS LISTED, EXCEPT INTA#, ARE SAMPLED ON THE RISING EDGE OF PCI_CLK)

SIGNAL NAME	PIN	BALL 3V	BALL 5V	DESCRIPTION
FRAME#(I)	48	G17	G15	Frame. This signal is driven by the current bus master and identifies both the beginning and duration of a bus operation. When FRAME# is first asserted, it indicates that a bus transaction is beginning and that valid addresses and a corresponding bus command are present on the AD[31:0] and C/BE[3:0] lines, qualified by PCI _CLK. When FRAME# is deasserted the transaction is in the final data phase or has been completed.
IRDY#(I)	49	H17	G16	Initiator Ready. This signal is sourced by the bus master and indicates that the bus master is able to complete the current data phase of a bus transaction. For write operations, it indicates that valid data is on the AD[31:0] pins. Wait states occur until both TRDY# and IRDY# are asserted together.
TRDY#(O)	52	G18	F18	Target Ready. This signal is sourced by the selected target and indicates that the target is able to complete the current data phase of a bus transaction. For read operations, it indicates that the target is providing valid data on the AD[31:0] pins. Wait states occur until both TRDY# and IRDY# are asserted together.
STOP#(O)	54	E16	E16	Stop. The Stop signal is sourced by the selected target and conveys a request to the bus master to stop the current transaction.
IDSEL#(I)	38	N18	K16	Initialization Device Select. This pin is used as a chip select during configuration read or write operations.
DEVSEL# (O)	53	F17	F17	Device Select. This signal is sourced by an active target upon decoding that its address and bus commands are valid. For bus masters, it indicates whether any device has decoded the current bus cycle.
PERR# (O)	55	F18	E18	Parity Error. This pin is used for reporting parity errors during the data portion of the bus transaction for all cycles except a Special Cycle. It is sourced by the agent receiving data and driven active two clocks following the detection of an error. This signal is driven inactive (high) two clocks prior to returning to the tri-state condition.
SERR# (O)	56	F15	E17	System Error. This pin is used for reporting address parity errors, data parity errors on Special Cycle commands, or any other condition having a catastrophic system impact.
INTA# (O)	24	J16	L17	Interrupt A. This pin is a level sensitive, active low interrupt to the host

TABLE 79. PCI MINI-ACE MARK3 PINOUT			
PIN#	**SIGNAL NAME**	**PIN#**	**SIGNAL NAME**
1	RTAD1	41	AD21
2	RTAD2	42	AD20
3	TX/RX A	43	AD19
4	DO NOT CONNECT, FACTORY TP	44	AD18
5	$\overline{\text{TX/RX\_A}}$	45	AD17
6	RTAD0	46	AD16
7	RTAD3	47	C/BE[2]#
8	DO NOT CONNECT, FACTORY TP	48	FRAME#
9	DO NOT CONNECT, FACTORY TP	49	IRDY#
10	3.3V_XCVR FOR BU-65XXF(G)8(9)-XXX 5VXCVR FOR BU-65XXF(G)3(4)-XXX	50	GND_LOGIC
		51	3.3V_LOGIC
		52	TRDY#
11	DO NOT CONNECT, FACTORY TP	53	DEVSEL#
12	RTAD_LAT	54	STOP#
13	RTAD_PAR	55	PERR#
14	SLEEP_IN	56	SERR#
15	TX/RX_B	57	PAR
16	DO NOT CONNECT, FACTORY TP	58	C/BE[1]#
17	$\overline{\text{TX/RX\_B}}$	59	AD15
18	TXINH_A/B	60	AD14
19	$\overline{\text{INCMD}}$ / $\overline{\text{MCRST}}$	61	AD13
20	$\overline{\text{SSFLAG}}$ / EXT_TRIG	62	AD12
21	DO NOT CONNECT, FACTORY TP	63	AD11
22	GND_XCVR	64	AD10
23	TAG_CLK	65	AD9
24	INTA#	66	C/BE[0]#
25	$\overline{\text{MSTCLR}}$	67	AD08
26	PCI_CLOCK	68	AD07
27	AD31	69	3.3V_LOGIC
28	AD30	70	GND_LOGIC
29	AD29	71	AD06
30	3.3V_LOGIC	72	AD05
31	GND_LOGIC	73	AD04
32	AD28	74	AD03
33	AD27	75	AD02
34	AD26	76	AD01
35	AD25	77	AD00
36	AD24	78	1553_CLK
37	C/BE[3]#	79	GND_XCVR
38	IDSEL	80	RTAD4
39	AD23		
40	AD22		

TABLE 80. PCI MICRO-ACE-TE BU-65843B8/BU-65863B8 (3.3V TRANSCEIVER) PINOUTS					
BALL	SIGNAL	NOTES	BALL	SIGNAL	NOTES
A1	NC		C10	AD02	
A2	NC		C11	NC	
A3	NC		C12	AD03	
A4	+3.3V_XCVR		C13	NC	
A5	+3.3V_XCVR		C14	NC	
A6	RTAD0		C15	RTAD2	
A7	RTAD4		C16	NC	
A8	+3.3V LOGIC		C17	NC	
A9	+3.3V LOGIC		C18	NC	
A10	AD01		D1	TX/RX-A	
A11	AD04		D2	TX/RX-A	
A12	AD07		D3	GND_XCVR /2/	Thermal Ball, Connects to Thermal Via
A13	NC		D4	GND_XCVR /2/	
A14	AD09		D5	GND_XCVR /2/	
A15	AD10		D6	NC	
A16	NC		D7	$\overline{\text{TXDATA\_IN\_A}}$ /1/	Connect to ball D8
A17	NC		D8	$\overline{\text{TXDATA\_OUT\_A}}$ /1/	Connect to ball D7
A18	NC		D9	RT_AD_LAT	
B1	NC		D10	RTAD3	
B2	NC		D11	NC	
B3	NC		D12	NC	
B4	+3.3V_XCVR		D13	NC	
B5	+3.3V_XCVR		D14	$\overline{\text{SNGL\_END}}$	
B6	AD05		D15	NC	
B7	1553_CLK		D16	AD15	
B8	+3.3V LOGIC		D17	AD13	
B9	+3.3V LOGIC		D18	AD11	
B10	AD00		E1	TX/RX_A	
B11	AD06		E2	TX/RX_A	
B12	C/BE[0]#		E3	GND/XCVR /2/	Thermal Ball, Connects to Thermal Via
B13	NC		E4	GND/XCVR /2/	
B14	AD08		E5	GND/XCVR /2/	
B15	AD12		E6	RTAD1	
B16	NC		E7	TXINH_IN_A /1/	Connect to ball E8
B17	NC		E8	TXINH_OUT_A /1/	Connect to ball E7
B18	NC		E9	RTADPAR	
C1	NC		E10	GND_LOGIC	
C2	NC		E11	GND_LOGIC	
C3	NC		E12	GND_LOGIC	
C4	NC		E13	NC	
C5	NC		E14	CLK_SEL_1	
C6	NC		E15	NC	
C7	TXDATA_IN_A /1/	Connect to ball C8	E16	STOP#	
C8	TXDATA_OUT_A /1/	Connect to ball C7	E17	C/BE[1]#	
C9	$\overline{\text{INCMD}}$ / $\overline{\text{MCRST}}$		E18	AD14	

TABLE 80. PCI MICRO-ACE-TE BU-65843B8/BU-65863B8 (3.3V TRANSCEIVER) PINOUTS (CONT)					
BALL	SIGNAL	NOTES	BALL	SIGNAL	NOTES
F1	GND_XCVR /2/	Thermal Ball, Connects to Thermal Via	H10	GND_LOGIC	
F2	GND_XCVR /2/		H11	GND_LOGIC	
F3	GND_XCVR /2/		H12	GND_LOGIC	
F4	GND_XCVR /2/		H13	NC	
F5	GND_XCVR /2/		H14	NC	
F6	NC		H15	NC	
F7	$\overline{\text{RTBOOT}}$		H16	NC	
F8	TX_INH A/B		H17	IRDY#	
F9	NC		H18	AD19	
F10	GND_LOGIC		J1	3.3V_XCVR	
F11	GND_LOGIC		J2	3.3V_XCVR	
F12	GND_LOGIC		J3	3.3V_XCVR	
F13	NC		J4	3.3V_XCVR	
F14	TAG_CLK		J5	3.3V_XCVR	
F15	SERR#L		J6	NC	
F16	PAR		J7	NC	
F17	DEVSEL#		J8	NC	
F18	PERR#		J9	NC	
G1	$\overline{\text{TX/RX\_A}}$		J10	NC	
G2	$\overline{\text{TX/RX\_A}}$		J11	NC	
G3	GND_XCVR /2/	Thermal Ball, Connects to Thermal Via	J12	NC	
G4	GND_XCVR /2/		J13	NC	
G5	GND_XCVR /2/		J14	NC	
G6	NC		J15	AD22	
G7	$\overline{\text{RXDATA\_OUT\_A}}$ /1/	Connect to ball G8	J16	INTA#	
G8	$\overline{\text{RXDATA\_IN\_A}}$ /1/	Connect to ball G7	J17	C/BE[2]#	
G9	NC		J18	AD21	
G10	GND_LOGIC		K1	3.3V_XCVR	
G11	GND_LOGIC		K2	3.3V_XCVR	
G12	GND_LOGIC		K3	3.3V_XCVR	
G13	NC		K4	3.3V_XCVR	
G14	NC		K5	3.3V_XCVR	
G15	NC		K6	NC	
G16	NC		K7	NC	
G17	FRAME#		K8	NC	
G18	TRDY#		K9	NC	
H1	$\overline{\text{TX/RX\_A}}$		K10	NC	
H2	$\overline{\text{TX/RX\_A}}$		K11	NC	
H3	NC		K12	NC	
H4	NC		K13	NC	
H5	NC		K14	NC	
H6	NC		K15	NC	
H7	RXDATA_OUT /1/	Connect to ball H8	K16	AD20	
H8	RXDATA_IN_A /1/	Connect to ball H7	K17	AD16	
H9	NC		K18	AD18	

TABLE 80. PCI MICRO-ACE-TE BU-65843B8/BU-65863B8 (3.3V TRANSCEIVER) PINOUTS (CONT)					
BALL	**SIGNAL**	**NOTES**	**BALL**	**SIGNAL**	**NOTES**
L1	TX/RX_B		N10	NC	
L2	TX/RX_B		N11	NC	
L3	GND_XCVR /2/	Thermal Ball, Connects to Thermal Via	N12	3.3V_LOGIC	
L4	GND_XCVR /2/		N13	3.3V_LOGIC	
L5	GND_XCVR /2/		N14	NC	
L6	NC		N15	NC	
L7	TXDATA_IN_B /1/	Connect to ball L8	N16	NC	
L8	TXDATA_OUT_B /1/	Connect to ball L7	N17	AD26	
L9	NC		N18	IDSEL	
L10	NC		P1	$\overline{\text{TX/RX\_B}}$	
L11	NC		P2	$\overline{\text{TX/RX\_B}}$	
L12	NC		P3	GND_XCVR /2/	Thermal Ball, Connects to Thermal Via
L13	NC		P4	GND_XCVR /2/	
L14	CLK_SEL_0		P5	GND_XCVR /2/	
L15	NC		P6	NC	
L16	3.3V_LOGIC		P7	NC	
L17	3.3V_LOGIC		P8	NC	
L18	AD17		P9	$\overline{\text{RXDATA\_OUT\_B}}$ /1/	Connect to ball P10
M1	TX/RX_B		P10	$\overline{\text{RXDATA\_IN\_B}}$ /1/	Connect to ball P9
M2	TX/RX_B		P11	NC	
M3	GND_XCVR /2/	Thermal Ball, Connects to Thermal Via	P12	3.3V_LOGIC	
M4	GND_XCVR /2/		P13	3.3V_LOGIC	
M5	GND_XCVR /2/		P14	NC	
M6	NC		P15	NC	
M7	$\overline{\text{TXDATA\_IN\_B}}$ /1/	Connect to ball M8	P16	NC	
M8	$\overline{\text{TXDATA\_OUT\_B}}$ /1/	Connect to ball M7	P17	AD28	
M9	NC		P18	AD24	
M10	NC		R1	$\overline{\text{TX/RX\_B}}$	
M11	NC		R2	$\overline{\text{TX/RX\_B}}$	
M12	NC		R3	NC	
M13	NC		R4	SLEEPIN	
M14	NC		R5	NC	
M15	NC		R6	3.3V_LOGIC	
M16	3.3V_LOGIC		R7	3.3V_LOGIC	
M17	3.3V_LOGIC		R8	C/BE[3]#	
M18	AD23		R9	RXDATA_OUT_B /1/	Connect to ball R10
N1	GND_XCVR /2/	Thermal Ball, Connects to Thermal Via	R10	RXDATA_IN_B /1/	Connect to ball R9
N2	GND_XCVR /2/		R11	GND_LOGIC	
N3	GND_XCVR /2/		R12	GND_LOGIC	
N4	GND_XCVR /2/		R13	GND_LOGIC	
N5	GND_XCVR /2/		R14	NC	
N6	NC		R15	NC	
N7	TXINH_IN_B /1/	Connect to ball N8	R16	NC	
N8	TXINH_OUT_B /1/	Connect to ball N7	R17	AD29	
N9	NC		R18	$\overline{\text{MSTCLR}}$ (RST#)	

TABLE 80. PCI MICRO-ACE-TE BU-65843B8/BU-65863B8 (3.3V TRANSCEIVER) PINOUTS (CONT)					
BALL	SIGNAL	NOTES	BALL	SIGNAL	NOTES
T1	NC		V8	AD25	
T2	NC		V9	AD31	
T3	NC		V10	NC	
T4	NC		V11	NC	
T5	NC		V12	NC	
T6	3.3V_LOGIC		V13	NC	
T7	3.3V_LOGIC		V14	NC	
T8	AD30		V15	NC	
T9	NC		V16	NC	
T10	PCI_CLK		V17	NC	
T11	GND_LOGIC		V18	NC	
T12	GND_LOGIC				
T13	GND_LOGIC				
T14	NC				
T15	NC				
T16	NC				
T17	NC				
T18	NC				
U1	NC				
U2	NC				
U3	NC				
U4	3.3V_XCVR				
U5	3.3V_XCVR				
U6	3.3V_LOGIC				
U7	3.3V_LOGIC				
U8	AD27				
U9	NC				
U10	SSFLAG/EXTTRIG				
U11	GND_LOGIC				
U12	GND_LOGIC				
U13	GND_LOGIC				
U14	NC				
U15	NC				
U16	NC				
U17	NC				
U18	NC				
V1	NC				
V2	NC				
V3	NC				
V4	3.3V_XCVR				
V5	3.3V_XCVR				
V6	3.3V_LOGIC				
V7	3.3V_LOGIC				

NOTES :

/1/ -LOGIC-TRANSCEIVER INTERCONNECT SIGNALS: CONSULT **Table 71**

/2/ - THERMAL BALL - MUST BE CONNECTED TO PWB THERMAL PLANE (28)

NC = **D**O **N**OT **C**ONNECT, NO USER CONNECTIONS TO THESE BALLS ALLOWED

TABLE 81. PCI MICRO-ACE-TE BU-65843B3/BU-65864B3 (5V TRANSCEIVER) PINOUTS					
BALL	SIGNAL	NOTES	BALL	SIGNAL	NOTES
A1	NC		C10	AD04	
A2	NC		C11	RTAD0	
A3	NC		C12	RT_BOOT	
A4	TXINH_IN_A /1/		C13	AD08	
A5	TXINH_OUT_A /1/		C14	AD10	
A6	NC		C15	AD12	
A7	+3.3V LOGIC		C16	NC	
A8	RTAD2		C17	NC	
A9	AD01		C18	NC	
A10	RTAD4		D1	TX/RX-A	
A11	AD06		D2	TX/RX-A	
A12	AD07		D3	GND_XCVR /2/	Thermal Ball, Connects to Thermal Via
A13	NC		D4	GND_XCVR /2/	
A14	AD09		D5	GND_XCVR /2/	
A15	SNGL_END		D6	RTAD_PAR	
A16	NC		D7	AD31	
A17	NC		D8	1553_CLK	
A18	NC		D9	NC	
B1	NC		D10	RXDATA_IN_A /1/	
B2	NC		D11	NC	
B3	NC		D12	NC	
B4	NC		D13	NC	
B5	NC		D14	NC	
B6	NC		D15	AD15	
B7	AD02		D16	AD13	
B8	TXDATA_OUT_A /1/		D17	AD11	
B9	RTAD1		D18	TAG_CLK	
B10	AD00		E1	TX/RX_A	
B11	MSTCLR (RST#)		E2	GND/XCVR /2/	Thermal Ball, Connects to Thermal Via
B12	C/BE[0]#		E3	GND/XCVR /2/	
B13	NC		E4	GND/XCVR /2/	
B14	NC		E5	GND/XCVR /2/	
B15	CLK_SEL1		E6	NC	
B16	NC		E7	AD27	
B17	NC		E8	INCMD / MCRST	
B18	NC		E9	RXDATA_IN_A /1/	
C1	NC		E10	RXDATA_OUT_A /1/	
C2	NC		E11	NC	
C3	NC		E12	GND_LOGIC	
C4	TXDATA_IN_A /1/		E13	GND_LOGIC	
C5	TXDATA_OUT_A /1/		E14	GND_LOGIC	
C6	AD03		E15	C/BE[1]#	
C7	RT_AD_LAT		E16	STOP#	
C8	TXDATA_IN_A /1/		E17	SERR#	
C9	RTAD3		E18	PERR#	

TABLE 81. PCI MICRO-ACE-TE BU-65843B3/BU-65864B3 (5V TRANSCEIVER) PINOUTS (CONT)					
BALL	SIGNAL	NOTES	BALL	SIGNAL	NOTES
F1	+5V VCC CH A		H10	NC	
F2	+5V VCC CH A		H11	NC	
F3	GND_XCVR /2/	Thermal Ball, Connects to Thermal Via	H12	GND_LOGIC	
F4	GND_XCVR /2/		H13	GND_LOGIC	
F5	GND_XCVR /2/		H14	GND_LOGIC	
F6	NC		H15	NC	RFU (JTAG)
F7	NC		H16	AD28	
F8	NC		H17	AD16	
F9	RXDATA_OUT_A /1/		H18	C/BE[2]#	
F10	TX_INH A/B		J1	NC	
F11	NC		J2	NC	
F12	GND_LOGIC		J3	NC	
F13	GND_LOGIC		J4	NC	
F14	GND_LOGIC		J5	NC	
F15	PAR		J6	NC	
F16	AD14		J7	AD05	
F17	DEVSEL#		J8	C/BE[3]#	
F18	TRDY#		J9	NC	
G1	$\overline{\text{TX/RX\_A}}$		J10	NC	
G2	GND_XCVR /2/	Thermal Ball, Connects to Thermal Via	J11	NC	
G3	GND_XCVR /2/		J12	NC	
G4	GND_XCVR /2/		J13	NC	
G5	GND_XCVR /2/		J14	NC	
G6	NC		J15	NC	RFU (JTAG)
G7	NC		J16	AD22	
G8	NC		J17	AD20	
G9	NC		J18	AD18	
G10	NC		K1	NC	
G11	NC		K2	NC	
G12	GND_LOGIC		K3	NC	
G13	GND_LOGIC		K4	NC	
G14	GND_LOGIC		K5	NC	
G15	FRAME#		K6	NC	
G16	IRDY#		K7	NC	
G17	AD19		K8	NC	
G18	AD21		K9	NC	
H1	$\overline{\text{TX/RX\_A}}$		K10	NC	
H2	$\overline{\text{TX/RX\_A}}$		K11	NC	
H3	GND_XCVR /2/	Thermal Ball, Connects to Thermal Via	K12	NC	
H4	GND_XCVR /2/		K13	NC	
H5	GND_XCVR /2/		K14	NC	RFU (JTAG)
H6	NC		K15	NC	RFU (JTAG)
H7	NC		K16	IDSEL	
H8	NC		K17	AD23	
H9	NC		K18	AD17	

TABLE 81. PCI MICRO-ACE-TE BU-65843B3/BU-65864B3 (5V TRANSCEIVER) PINOUTS (CONT)					
BALL	SIGNAL	NOTES	BALL	SIGNAL	NOTES
L1	3.3V_LOGIC		N10	NC	
L2	3.3V_LOGIC		N11	NC	
L3	NC		N12	TXDATA_IN_B /1/	
L4	NC		N13	RXDATA_IN_B /1/	
L5	NC		N14	RXDATA_OUT_B /1/	
L6	NC		N15	NC	
L7	NC		N16	NC	
L8	NC		N17	NC	
L9	SSFLAG / EXT_TRIG		N18	NC	
L10	AD29		P1	NC	
L11	AD26		P2	NC	
L12	NC		P3	NC	
L13	NC		P4	5V_RAM	5V RAM BU-65864B3 ONLY
L14	NC		P5	NC	
L15	3.3V_LOGIC		P6	NC	
L16	3.3V_LOGIC		P7	3.3V_LOGIC	
L17	INTA#		P8	NC	
L18	AD24		P9	3.3V_LOGIC	
M1	NC		P10	TXDATA_OUT_B /1/	
M2	NC		P11	GND_XCVR /2/	Thermal Ball, Connects to Thermal Via
M3	3.3V_LOGIC		P12	GND_XCVR /2/	
M4	NC		P13	GND_XCVR /2/	
M5	NC		P14	GND_XCVR /2/	
M6	NC		P15	GND_XCVR /2/	
M7	NC		P16	NC	
M8	NC		P17	NC	
M9	PCI_CLK		P18	NC	
M10	AD30		R1	NC	
M11	NC		R2	NC	
M12	TXDATA_OUT_B /1/		R3	NC	
M13	RXDATA_IN_B /1/		R4	5V_RAM	5V RAM BU-65864B3 ONLY
M14	RXDATA_OUT_B /1/		R5	NC	
M15	NC		R6	NC	
M16	NC	RFU (JTAG)	R7	NC	
M17	NC		R8	TXINH_OUT_B /1/	
M18	CLK_SEL_0		R9	3.3V_LOGIC	
N1	NC		R10	TXDATA_IN_B /1/	
N2	NC		R11	GND_XCVR	Thermal Ball, Connects to Thermal Via
N3	NC		R12	GND_XCVR	
N4	NC		R13	GND_XCVR	
N5	NC		R14	GND_XCVR	
N6	NC		R15	GND_XCVR	
N7	NC		R16	NC	
N8	NC		R17	NC	
N9	AD25		R18	NC	

TABLE 81. PCI MICRO-ACE-TE BU-65843B3/BU-65864B3 (5V TRANSCEIVER) PINOUTS (CONT)

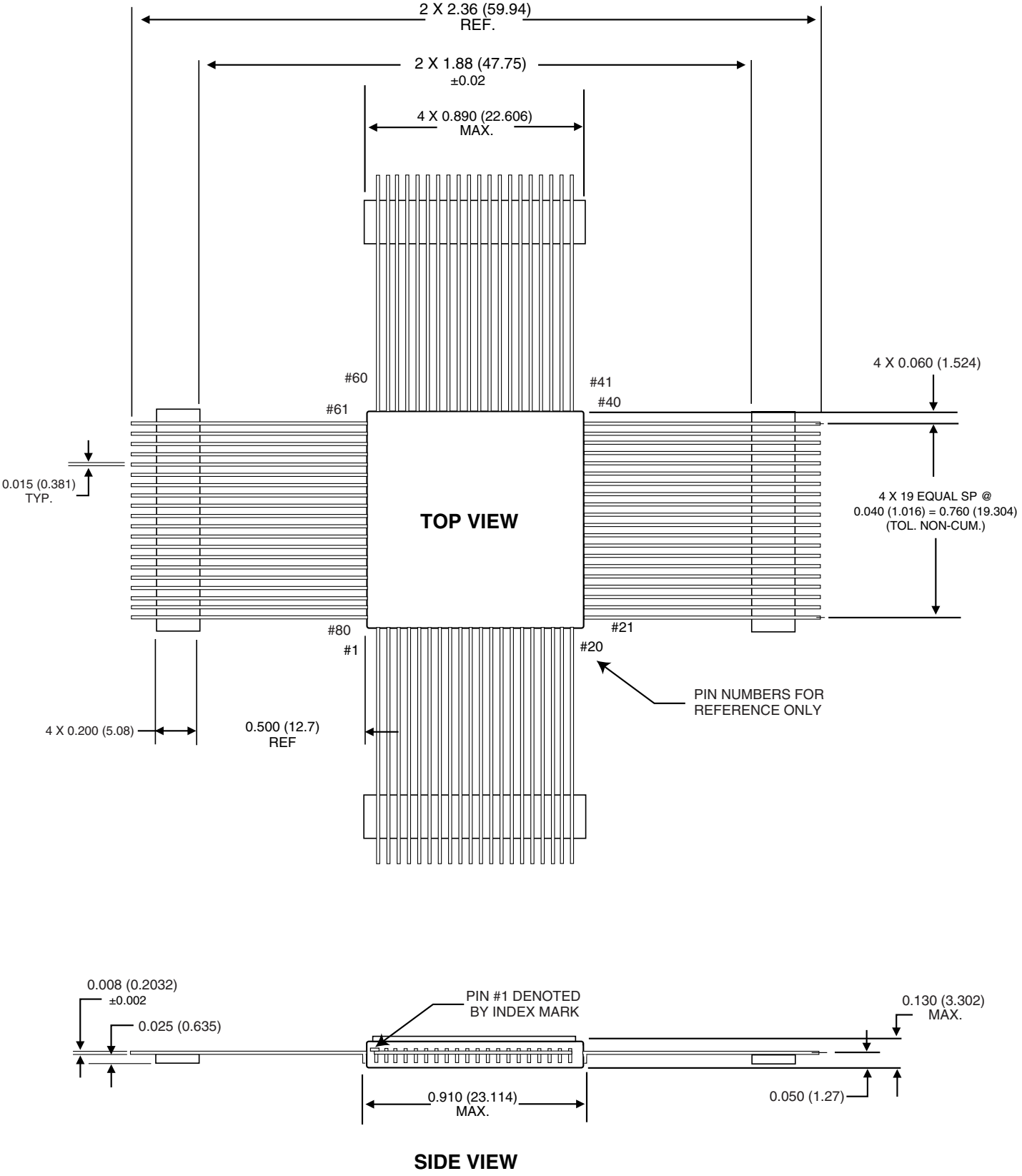
BALL	SIGNAL	NOTES	BALL	SIGNAL	NOTES
T1	NC		V10	NC	
T2	NC		V11	TX/RX_B	
T3	NC		V12	TX/RX_B	
T4	NC		V13	5V Vcc CHB	
T5	NC		V14	$\overline{\text{TX/RX\_B}}$	
T6	NC		V15	$\overline{\text{TX/RX\_B}}$	
T7	NC		V16	NC	
T8	TXINH_IN_B /1/		V17	NC	
T9	NC		V18	NC	
T10	NC				
T11	GND_XCVR	Thermal Ball, Connects to Thermal Via			
T12	GND_XCVR				
T13	GND_XCVR				
T14	GND_XCVR				
T15	GND_XCVR				
T16	NC				
T17	NC				
T18	NC				
U1	NC				
U2	NC				
U3	NC				
U4	NC				
U5	NC				
U6	NC				
U7	NC				
U8	NC				
U9	NC				
U10	NC				
U11	TX/RX_B				
U12	GND_XCVR	Thermal Ball, Connects to Thermal Via			
U13	5V Vcc CHB				
U14	GND_XCVR	Thermal Ball, Connects to Thermal Via			
U15	$\overline{\text{TX/RX\_B}}$				
U16	NC				
U17	NC				
U18	NC				
V1	NC				
V2	NC				
V3	NC				
V4	NC				
V5	NC				
V6	NC				
V7	NC				
V8	3.3V_LOGIC				
V9	NC				

NOTES:

/1/ -LOGIC-TRANSCEIVER INTERCONNECT SIGNALS: CONSULT **Table 71**

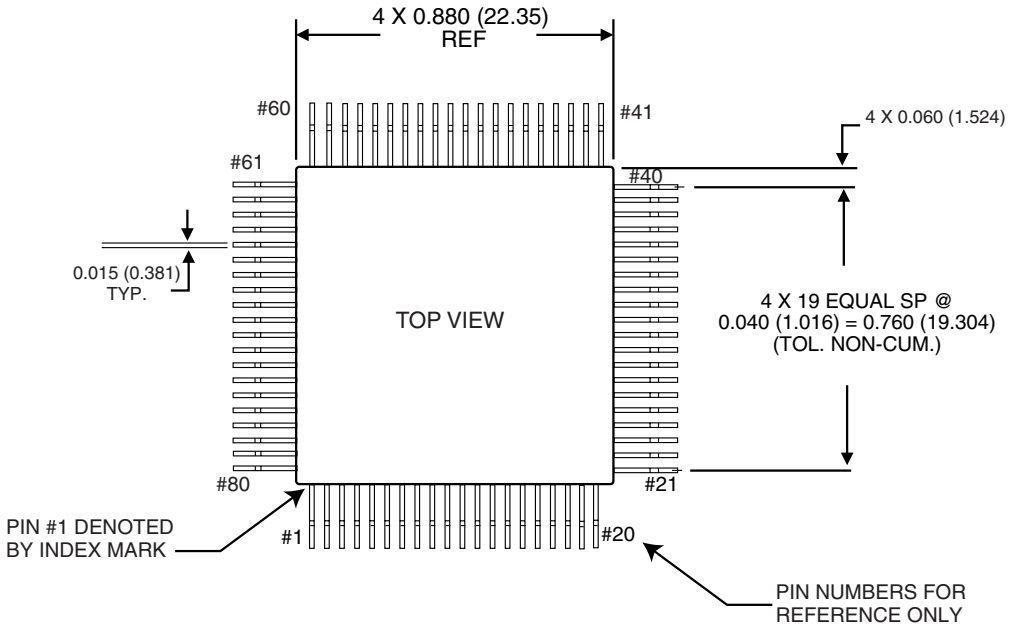
/2/ -THERMAL BALL - MUST BE CONNECTED TO PWB THERMAL PLANE (34)

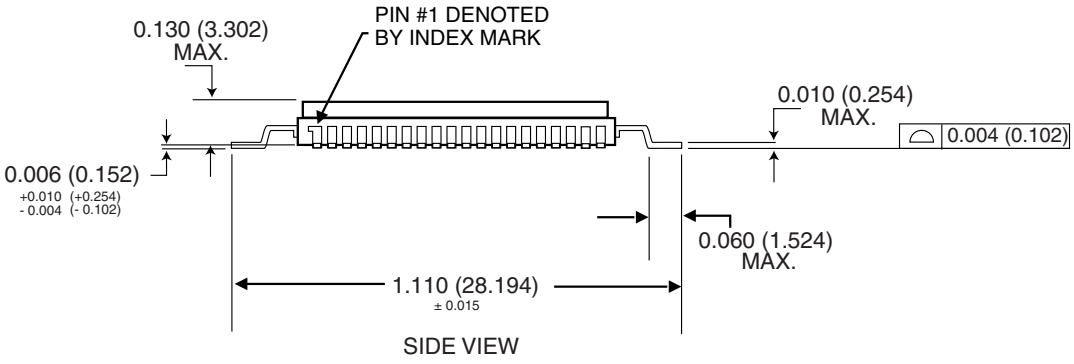
NC = **D**O **N**OT **C**ONNECT, NO USER CONNECTIONS TO THESE BALLS ALLOWED



Notes:
1) Dimensions are in inches (mm).

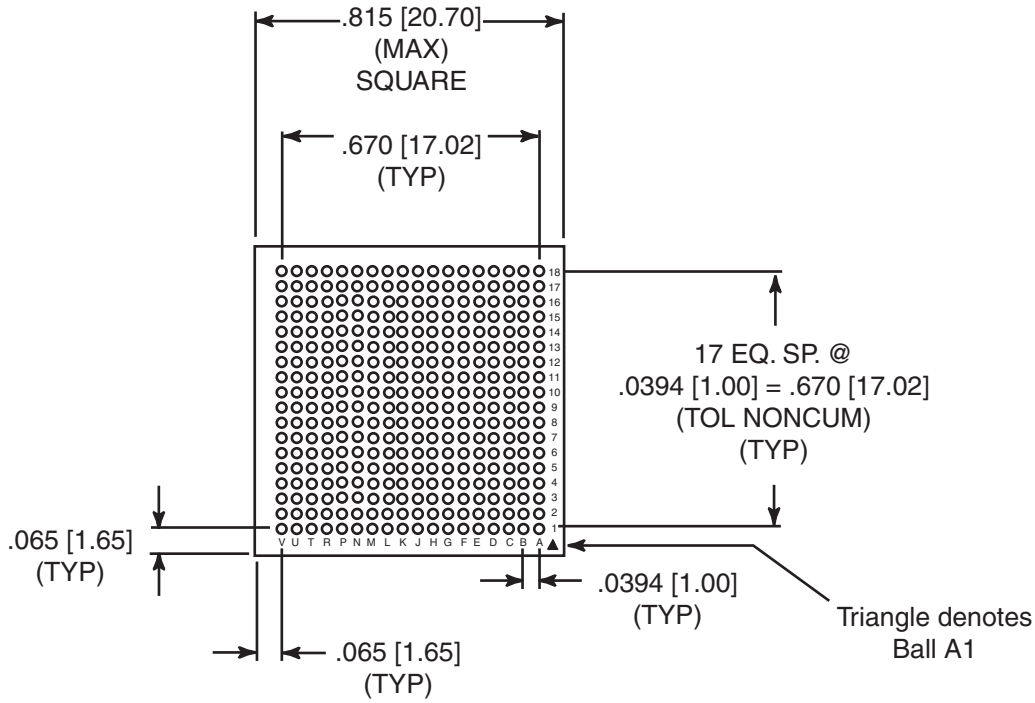
FIGURE 22. MECHANICAL OUTLINE DRAWING FOR 80-LEAD FLATPACK



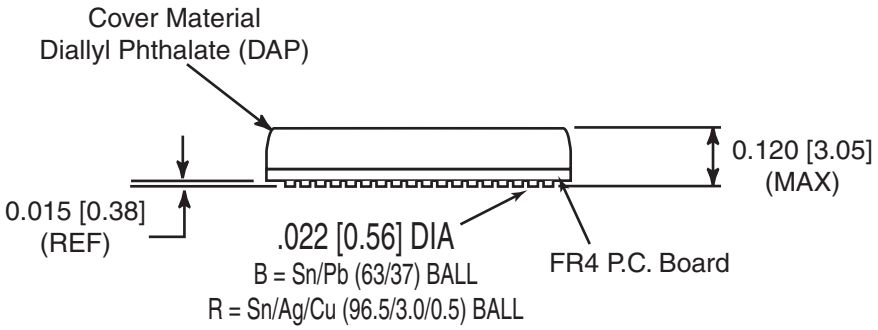


Notes:
1) Dimensions are in inches (mm).

FIGURE 23. MECHANICAL OUTLINE DRAWING FOR 80-PIN GULL LEAD PACKAGE



BOTTOM VIEW



SIDE VIEW

Notes:
1) Dimensions are in inches (mm).
2) Cover material: Diallyl Phthalate (DAP).
3) Base material: FR4 PC board.
4) Solder Ball Cluster to be centralized within ±.010 of outline dimensions.
5) The copper pads (324 places) on the bottom of the BGA package are .025" (0.635 mm) in diameter prior to processing. Final ball size is .022" (0.56 mm) after processing (typical).

FIGURE 24. MECHANICAL OUTLINE DRAWING FOR 324 BALL BGA PACKAGE

ORDERING INFORMATION FOR PCI MINI-ACE MARK3

BU-6586 3F3-120X

Supplemental Process Requirements:
- S = Pre-Cap Source Inspection
- L = 100% Pull Test
- Q = 100% Pull Test and Pre-Cap Source Inspection
- K = One Lot Date Code
- W = One Lot Date Code and Pre-Cap Source Inspection
- Y = One Lot Date Code and 100% Pull Test
- Z = One Lot Date Code, Pre-Cap Source Inspection and 100% Pull Test
- Blank = None of the Above

Test Criteria:
- 0 = Standard Testing
- 1 = X-Ray
- 2 = MIL-STD-1760 Amplitude Compliant (not available with McAir compatible Outputs) See transceiver 4, 9 & D options
- 3 = MIL-STD-1760 and X-Ray

Process Requirements:
- 0 = Standard DDC practices, no Burn-In
- 1 = MIL-PRF-38534 Compliant (note 2)
- 2 = B (note 1)
- 3 = MIL-PRF-38534 Compliant (note 2) with PIND Testing
- 4 = MIL-PRF-38534 Compliant (note 2) with Solder Dip
- 5 = MIL-PRF-38534 Compliant (note 2) with PIND Testing and Solder Dip
- 6 = B (note 1) with PIND Testing
- 7 = B (note 1) with Solder Dip
- 8 = B (note 1) with PIND Testing and Solder Dip
- 9 = Standard DDC Processing with Solder Dip, no Burn-In (see table on next page)

Temperature Range/Data Requirements:
- 1 = -55°C to +125°C
- 2 = -40°C to +85°C
- 3 = 0°C to +70°C
- 4 = -55°C to +125°C with Variables Test Data
- 5 = -40°C to +85°C with Variables Test Data
- 6 = Custom Part (Reserved)
- 7 = Custom Part (Reserved)
- 8 = 0°C to +70°C with Variables Test Data

Voltage/Transceiver Option:
- 0 = Transceiverless (contact factory for availability)
- 3 = +5.0 Volts rise/fall times = 100 to 300 ns (-1553B)
- 4 = +5.0 Volts rise/fall times = 200 to 300 ns (-1553B and McAir compatible) Note: Not available with "MIL-STD-1760 Amplitude Compliant Outputs")
- 8 = +3.3 Volts rise/fall times = 100 to 300 ns (-1553B) (note 4)
- 9 = +3.3 Volts rise/fall times = 200 to 300 ns (-1553B and McAir compatible) Note: Not available with "MIL-STD-1760 Amplitude Compliant Outputs") (note 4)
- C = +3.3 Volts rise/fall times = 100 to 300 ns (-1553B) (note 5)
- D = +3.3 Volts rise/fall times = 200 to 300 ns (-1553B and McAir compatible. Note: Not available with "MIL-STD-1760 Amplitude Compliant Outputs") (note 5)

Package Type:
- F = 80-Lead Flat Pack
- G = 80-Lead "Gull Wing" (Formed Lead)

Logic / RAM Voltage
- 3 = 3.3 Volt

PCI-Mini-ACE/Mark3 Product Type: (See Product Matrix on Page 75)
- BU-6574 = RT only with 4K X 16 RAM
- BU-6584 = BC /RT / MT with 4K x 16 RAM
- BU-6586 = BC /RT / MT with 64K x 17 RAM

Notes:
1. Standard DDC processing with burn-in and full temperature test. See table on next page.
2. MIL-PRF-38534 product grading is designated with the following dash numbers:
   Class H is a -11X, 13X, 14X, 15X, 41X, 43X, 44X, 45X
   Class G is a -21X, 23X, 24X, 25X, 51X, 53X, 54X, 55X
   Class D is a -31X, 33X, 34X, 35X, 81X, 83X, 84X, 85X
3. The above products contain tin-lead solder finish as applicable to solder dip requirements.
4. Transformer center-tap connected to +3.3V_XCVR, see FIGURE 18 (Obsolete)
5. Transformer center-tap connected to GND, see FIGURE 19

ORDERING INFORMATION FOR PCI MICRO-ACE-TE*

BU-6XXX3BX-E0X

Test Criteria:
0 = 18V Amplitude. Only available with “Voltage transceiver option = 4”
2 = MIL-STD-1760 Amplitude Compliant, Standard

Process Requirements:
0 = Standard DDC practices, no Burn-In

Temperature Range/Data Requirements:
E = -40°C to +100°C
1 = -55°C to +125°C (only available with transceiver option C)

Voltage/Transceiver Option:
3 = +5.0 Volts rise/fall times = 100 to 300 ns (-1553B)
4 = +5.0 Volts 200 to 300 ns rise/fall times, -1553 and McAir compatible
(not available with “Test Criteria option = 2”)
8 = +3.3 Volts rise/fall times = 100 to 300 ns (-1553B) (note 3)
C = +3.3 Volts rise/fall times = 100 to 300 ns (-1553B) (note 4)

Package Type:
B = 324-ball BGA Package
R = RoHS Compliant 324-ball BGA Package

Logic / RAM Voltage:
3 = 3.3 Volt
4 = 3.3 Volt Logic, 5.0 Volt RAM (for BU-65864, 64K x 17 RAM Voltage is always +5.0V)

Product Type: (See Product Matrix)
BU-6584 = PCI BC/RT/MT with 4K x 16 RAM
BU-6586 = PCI BC/RT/MT with 64K x 17 RAM

Note : Unless otherwise specified, these products contains tin-lead solder.
*See PCI-MICRO-ACE-TE Product Matrix for valid ordering options

ACCESSORIES:

BU-64863B8-600

MICRO-ACE-TE (324 Ball BGA) Mechanical Sample, with "daisy chain" connections of alternating balls, for use in environmental (mechanical / thermal) integrity testing.

STANDARD DDC PROCESSING FOR HYBRID AND MONOLITHIC HERMETIC PRODUCTS		
TEST	MIL-STD-883	
	METHOD(S)	CONDITION(S)
INSPECTION	2009, 2010, 2017, and 2032	—
SEAL	1014	A and C
TEMPERATURE CYCLE	1010	C
CONSTANT ACCELERATION	2001	3000g
BURN-IN	1015 (note 1), 1030 (note 2)	TABLE 1

Notes:
1. For Process Requirement "B*" (refer to ordering information), devices may be non-compliant with MIL-STD-883, Test Method 1015, Paragraph 3.2. Contact factory for details.
2. When applicable.
3. Transformer center-tap connected to +3.3V_XCVR, see FIGURE 18 (Obsolete)
4. Transformer center-tap connected to GND, see FIGURE 19

STANDARD DDC PROCESSING FOR BGA PRODUCTS		
TEST	MIL-STD-883	
	METHOD(S)	CONDITION(S)
INSPECTION	2010, 2017, and 2032	—
TEMPERATURE CYCLE	1010	B

PCI-MINI-ACE MARK3 PRODUCT MATRIX				
PART NUMBER	LOGIC VOLTAGE	MEMORY	RAM VOLTAGE	TRANSCEIVER VOLTAGE
BU-65743X3	3.3V	4K x 16	3.3V	5.0V
BU-65743X4	3.3V	4K x 16	3.3V	5.0V
BU-65743XC	3.3V	4K x 16	3.3V	3.3V
BU-65743XD	3.3V	4K x 16	3.3V	3.3V
BU-65843X3	3.3V	4K x 16	3.3V	5.0V
BU-65843X4	3.3V	4K x 16	3.3V	5.0V
BU-65843XC	3.3V	4K x 16	3.3V	3.3V
BU-65843XD	3.3V	4K x 16	3.3V	3.3V
BU-65863X3	3.3V	64K x 17	3.3V	5.0V
BU-65863X4	3.3V	64K x 17	3.3V	5.0V
BU-65863XC	3.3V	64K x 17	3.3V	3.3V
BU-65863XD	3.3V	64K x 17	3.3V	3.3V

PCI-MICRO-ACE TE PRODUCT MATRIX					
PART NUMBER	SPECIAL ORDER MIN QTY MAY APPLY	LOGIC VOLTAGE	MEMORY	RAM VOLTAGE	TRANSCEIVER VOLTAGE
BU-65843B3-E02		3.3V	4K x 16	3.3V	5.0V
BU-65843BC-X02	X	3.3V	4K x 16	3.3V	3.3V
BU-65864B(R)3-E02		3.3V	64K x 17	5.0V	5.0V
BU-65863BC-X02	X	3.3V	64K x 17	3.3V	3.3V
BU-65864B(R)4-E00		3.3V	64K x 17	5.0V	5.0V

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EN9100:2009, JIS Q9100:2009
FILE NO. 10001296 ASH09

RECORD OF CHANGE

For BU-65743 Data Sheet

Revision	Date	Pages	Description
W	6/2009	30, 32, 33, 35, 50, 51	Removed “old” double-buffered references. Replaced table 65. Added a new Table (Table 66).
Y	11/2009	62, 65, 67, 72	Changed "Package Type" ordering description FROM: R = Lead Free 324-ball BGA Package TO: R = RoHS Compliant 324-ball BGA Package Added not bars to R1 R2 of table 80 and G1, H1, H2, U15, V14, V15 of table 81
AA	4/2010	5, 48, 50	Edit to Soldering section of table 1. Edit to table 65 and Figure 18.
AB			
AC	6/2011	47, 48, 49, 50, 71, 72	Updated Figures 18 and 20. Added Figure 19 (BU-64XXXXC/D). Incremented all following Figure numbers. Update to Figure 20. Replaced Table 65. Added Options “C” and “D”, and notes 4 and 5 to Ordering Information for PCI Mini-ACE Mark3. Added Option “C” and notes to Ordering Information for PCI Micro-ACE-TE
AD	2/2012	2 - 6, 50 - 53	Changed transformer ratio from “1:2.038” to “1:2.07” in Figure 1, Figure 19, and pages 50 and 52. Table 1: Added BU-65X43XC/D-XXX and BU-65863XC/D-XXX to Power Supply Requirements (3.3V Transceiver). Added BU-65X43XC/D-XXX and BU-65863XC/D-XXX to Power Dissipation (3.3V Transceiver). Added BU-65XX3XC/D-XXX to Power Dissipation (Hottest Die 3.3V Transceiver).
AE	8/2013	3, 5, 53, 54, 75, 76	Table 1 edits to add “8”, “9”, “C” & “D” options and Thermal section specs. Expanded Thermal Management section on pages 53 and 54, Added Version “1” temperature range to PCI Micro-ACE-TE order info on page 75, Edits to tables on page 76
AF	5/2014	5	edit solder temperature in spec table