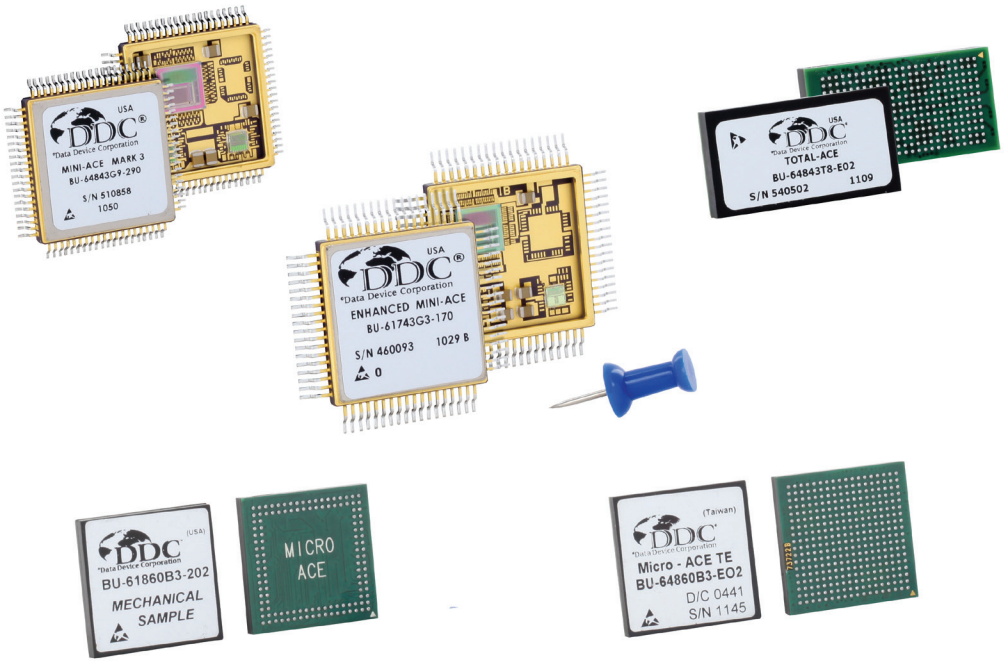
# Enhanced Miniature Advanced Communications Engine User's Guide

©Data Device Corporation

**Model: BU-6186X**




## Volume 2 - Hardware Reference

DDC's Enhanced Mini-ACE family of MIL-STD-1553 terminals provide complete interfaces between a host processor and 1553 bus. These terminals integrate a dual transceiver, protocol logic, and 4K or 64K words of RAM.

### Enhanced Mini-ACE Family:

- Enhanced Mini-ACE®
- Micro-ACE®
- Mini-ACE® Mark3
- Micro-ACE®-TE
- Total-ACE®

**For more information:** www.ddc-web.com/EMA

# DDC's Data Networking Solutions

## MIL-STD-1553 | ARINC 429 | Fibre Channel

As the leading global supplier of data bus components, cards, and software solutions for the military, commercial, and aerospace markets, DDC's data bus networking solutions encompass the full range of data interface protocols from MIL-STD-1553 and ARINC 429 to USB, and Fibre Channel, for applications utilizing a spectrum of form-factors including PMC, PCI, Compact PCI, PC/104, ISA, and VME/VXI.

DDC has developed its line of high-speed Fibre Channel and Extended 1553 products to support the real-time processing of field-critical data networking netween sensors, compute notes, data storage displays, and weapons for air, sea, and ground military vehicles.

Whether employed in increased bandwidth, high-speed serial communications, or traditional avionics and ground support applications, DDC's data solutions fufill the expanse of military requirements including reliability, determinism, low CPU utilization, real-time performance, and ruggedness within harsh environments. Out use of in-house intellectual property ensures superior mutli-generational support, independent of the life cycles of commercial devices. Moreover, we maintain software compatibility between product generations to protect our customers' investments in software development, system testing, and end-product qualification.

### *MIL-STD-1553*

DDC provides an assortment of quality MIL-STD-1553 commercial, military, and COTS grade cards and components to meet your data conversion and data interface needs. DDC supplies MIL-STD-1553 board level products in a variety of form factors including AMC, USB, PCI, cPCI, PCI-104, PCMCIA, PMC, PC/104, PC/104-Plus, VME/VXI, and ISAbus cards. Our 1553 data bus board solutions are integral elements of military, aerospace, and industrial applications. Our extensive line of military and space grade components provide MIL-STD-1553 interface solutions for microprocessors, PCI buses, and simple systems. Our 1553 data bus solutions are designed into a global network of aircraft, helicopter, and missle programs.

### *ARINC 429*

DDC also has a wide assortment of quality ARINC-429 commercial, military, and COTS grade cards and components, which will meet your data conversion and data interface needs. DDC supplies ARINC-429 board level products in a variety of form factors including AMC, USB, PCI, PMC, PCI-104, PC/104 Plus, and PCMCIA boards. DDC's ARINC 429 components ensure the accurate and reliable transfer of flight-critical data. Our 429 interfaces support data bus development, validation, and the transfer of flight-critical data aboard commercial aerospace platforms.

### *Fibre Channel*

DDC has developed its line of high-speed Fibre Channel network access controllers and switches to support the real-time processing demands of field-critical data networking between sensors, computer nodes, data storage, displays, and weapons, for air, sea, and ground military vehicles. Fibre Channel's architecture is optimized to meet the performance,reliability, and demanding environmental requirements of embedded, real time, military applications, and designed to endure the multi-decade life cycle demands of military/aerospace programs.

# ENHANCED MINIATURE ADVANCED COMMUNICATIONS ENGINE (ENHANCED MINI-ACE® SERIES) USER'S GUIDE VOLUME 2 – HARDWARE REFERENCE

## MN-6186X-002



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| Revision | Date | Pages | Description |
|---|---|---|---|
| A | 3/2003 | All | Reformatted |
| B | 8/2004 | All | Major Revision, See MarCom for Markup |
| A | 8/2005 | All | Major Revision, Volume 2 now a stand alone Manual returning to an A revision. |
| B | 1/2007 | All | Updated Figures 12, 41, and 42<br>Updated Tables 17 & 18<br>Volume 3 (Appendices) added to Volume 2, with Appendix E intentionally left blank |
| C | 6/2007 | All | Updated Tables 20, 21, 32 and 33<br>Moved footnote referencing Table 22 and Figure 46 under Fig 46 to Fig 45 referencing Tables 20 and 21 and Figures 45 and 46.<br>Removed Southeast and West coast contact info. |
| D | 11/2007 | 54 | T12 description corrected. |
| E | 2/2008 | 156 – 182 | Removed outline drawings, pinouts, and ordering information, as these details are maintained in the datasheet. |
| F | 12/2008 | Various | Addition of the AceXtreme product line. |
| G | 7/2011 | 4, 13, 15, 19, 21, 22, 23, 154, 160 | Figure 2 title change, text edits on pages 13, 19 and 21, added Figure 6, updated Figures 4, 9 and 10, updated Tables 41 and 42 |
| H | 8/2012 | All | Updated all images to a clearer format, new template applied to document. |
| J | 7/2016 | 31,32,34 | Updated section 9.2 and figure 15. |
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# 1 PREFACE

This manual uses typographical conventions to assist the reader in understanding the content. This section will define the text formatting used in the rest of the manual

## 1.1 Text Usage

- **BOLD**–indicates important information and table, figure, and chapter references.
- ***BOLD ITALIC***–designates DDC Part Numbers.
- `Courier New`–indicates code examples.
- <…> - indicates user-entered text or commands.

## 1.2 Special Handling and Cautions

The ***Enhanced Mini-ACE Series*** uses state-of-the-art components, and proper care should be used to ensure that the device will not be damaged by Electrical Static Discharge (ESD), physical shock, or improper power surges and that precautions are taken to avoid electrocution.


*Warnings: Turn off power to the computer hardware and unplug from wall.*

*NEVER insert or remove card with power turned on.*

*Ensure that standard ESD precautions are followed. As a minimum, one hand should be grounded to the power supply in order to equalize the static potential.*

*Do not store disks in environments exposed to excessive heat, magnetic fields or radiation.*

## 1.3 Trademarks

All trademarks are the property of their respective owners.

## 1.4 What is included in this manual?

This manual contains a complete description of hardware installation and use.

## 1.5 Technical Support

In the event that problems arise beyond the scope of this manual, you can contact DDC by the following:

US Toll Free Technical Support:
1-800-DDC-5757, ext. 7771

Outside of the US Technical Support:
1-631-567-5600, ext. 7771

Fax:
1-631-567-5758 to the attention of DATA BUS Applications

DDC Website:
www.ddc-web.com/ContactUs/TechSupport.aspx

Please note that the latest revisions of Software and Documentation are available for download at DDC's Web Site, www.ddc-web.com.

# 2 OVERVIEW

All references throughout this document to the “Enhanced Mini-ACE” shall be interpreted to include Enhanced Mini-ACE, Micro-ACE, Mini-ACE Mark3, Micro-ACE TE, and Total-ACE products. Any specific references to a unique series of components (i.e. Micro-ACE only) will utilize the component part number (i.e. BU-61740B, BU-61840B/61860B etc.).

The Enhanced Mini-ACE family (Enhanced Mini-ACE, Micro-ACE, Mini-ACE Mark 3, Micro-ACE TE, Total-ACE) of MIL-STD-1553 terminals provides complete interfaces between a host processor and a 1553 bus. All these terminals integrate dual transceiver, protocol logic, and 4K words or 64K words of RAM. Additionally, the Total-ACE integrates the isolation transformer(s) as well. The BC/RT/MT versions with 64K words of RAM include built-in RAM parity checking.

The Enhanced Mini-ACE is packaged in a choice of a 1.0-inch square Flat Pack or Gull Wing package, or a 0.815-inch square BGA package (Micro-ACE). The Mini-ACE Mark 3 is packaged in a choice of a 0.890-inch Flat Pack or Gull Wing package, or a 0.815-inch square BGA package (Micro-ACE-TE). The Total-ACE is packaged in a 1.100-inch x 0.600-inch rectangular, plastic BGA.

The Flat Pack or Gull Wing packaged Enhanced Mini-ACE provides footprint compatibility with the previous generation Mini-ACE (Plus) terminal.

All members of the Enhanced Mini-ACE series (Enhanced Mini-ACE, Micro-ACE, Mini-ACE Mark3, Micro-ACE-TE, and Total-ACE) provide software compatibility with the previous generation Mini-ACE (Plus) terminals, and the older ACE series.

The Enhanced Mini-ACE and Micro-ACE are powered by a choice 5V, or 5V/3.3V (3.3V logic). Multiprotocol support of MIL-STD-1553A/B and STANAG 3838, including versions incorporating McAir compatible transmitters, is provided. There is a choice of 10, 12, 16, or 20 MHz clocks.

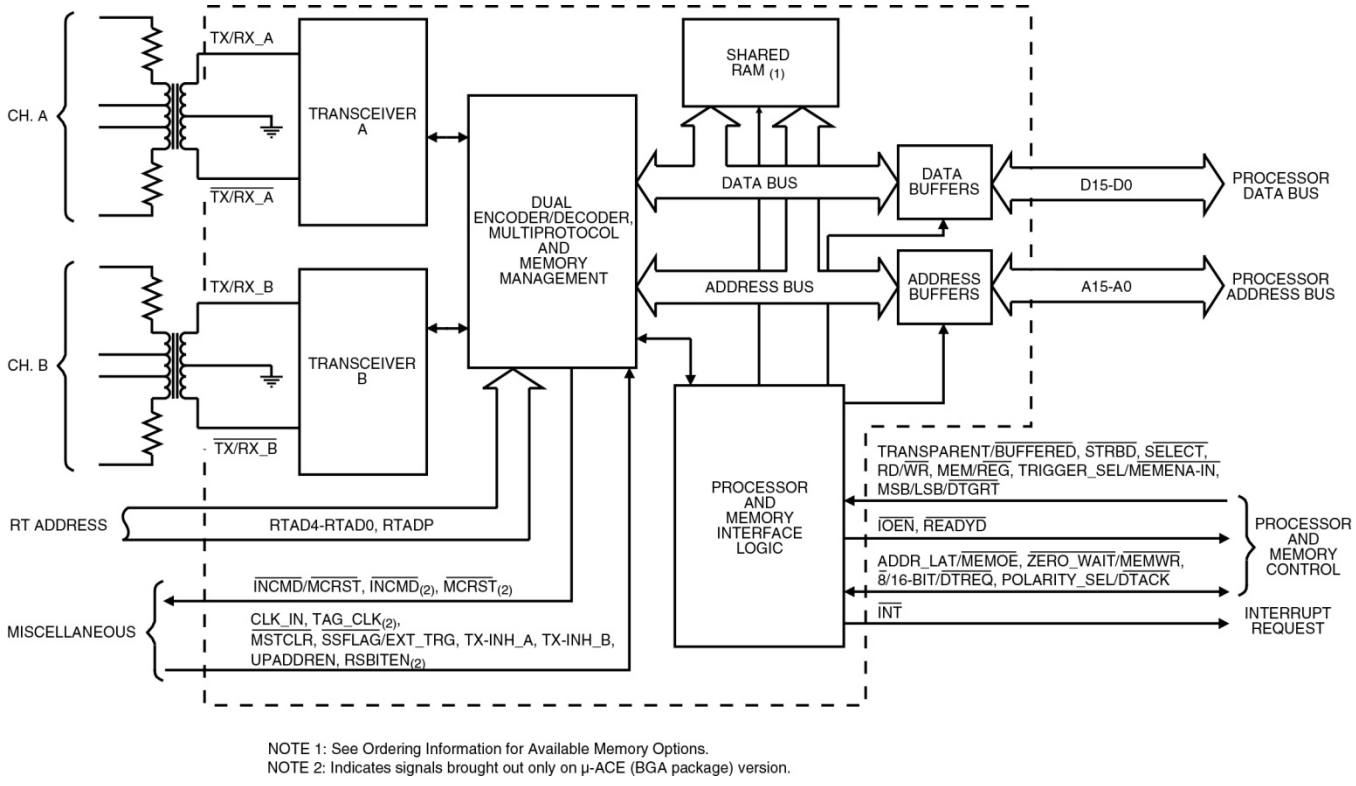
The Mini-ACE Mark3 and Micro-ACE-TE are powered by a choice of 3.3V/5V (logic), and 3.3V/5V (transceivers). (Certain combination restrictions apply. See datasheet for full ordering information). Multiprotocol support of MIL-STD-1553A/B and STANAG 3838, including versions incorporating McAir compatible transmitters, is provided. There is a choice of 10, 12, 16, or 20 MHz clocks.

The Total-ACE is an all 3.3V device (logic & transceivers) with integrated isolation transformers. (Certain combination restrictions apply. See datasheet for full ordering information). Multiprotocol support of MIL-STD-1553A/B and STANAG 3838, is provided. There is a choice of 10, 12, 16, or 20 MHz clocks.

BC features include a built-in engine, with a set of 20 instructions. This provides an autonomous means of implementing multi-frame message scheduling, message retry schemes, data double buffering, asynchronous message insertion, and reporting to the host CPU. The Enhanced Mini-ACE incorporates a fully autonomous built-in selftest, which provides comprehensive testing of the internal protocol logic and/or RAM.

The Enhanced Mini-ACE RT offers the same choices of subaddress buffering as ACE and Mini-ACE (Plus), along with a global circular buffering option, 50% rollover interrupt for circular buffers, an interrupt status queue, and an “Auto-boot” option to support MIL-STD-1760.

The Enhanced Mini-ACE terminals provide the same flexibility in host interface configurations as the Mini-ACE (Plus) terminals, and the older ACE series along with a reduction in the host processor’s worst-case holdoff time.




NOTE 1: See Ordering Information for Available Memory Options.
NOTE 2: Indicates signals brought out only on µ-ACE (BGA package) version.

**Figure 1. Enhanced Mini-ACE/Micro-ACE Series Block Diagram**

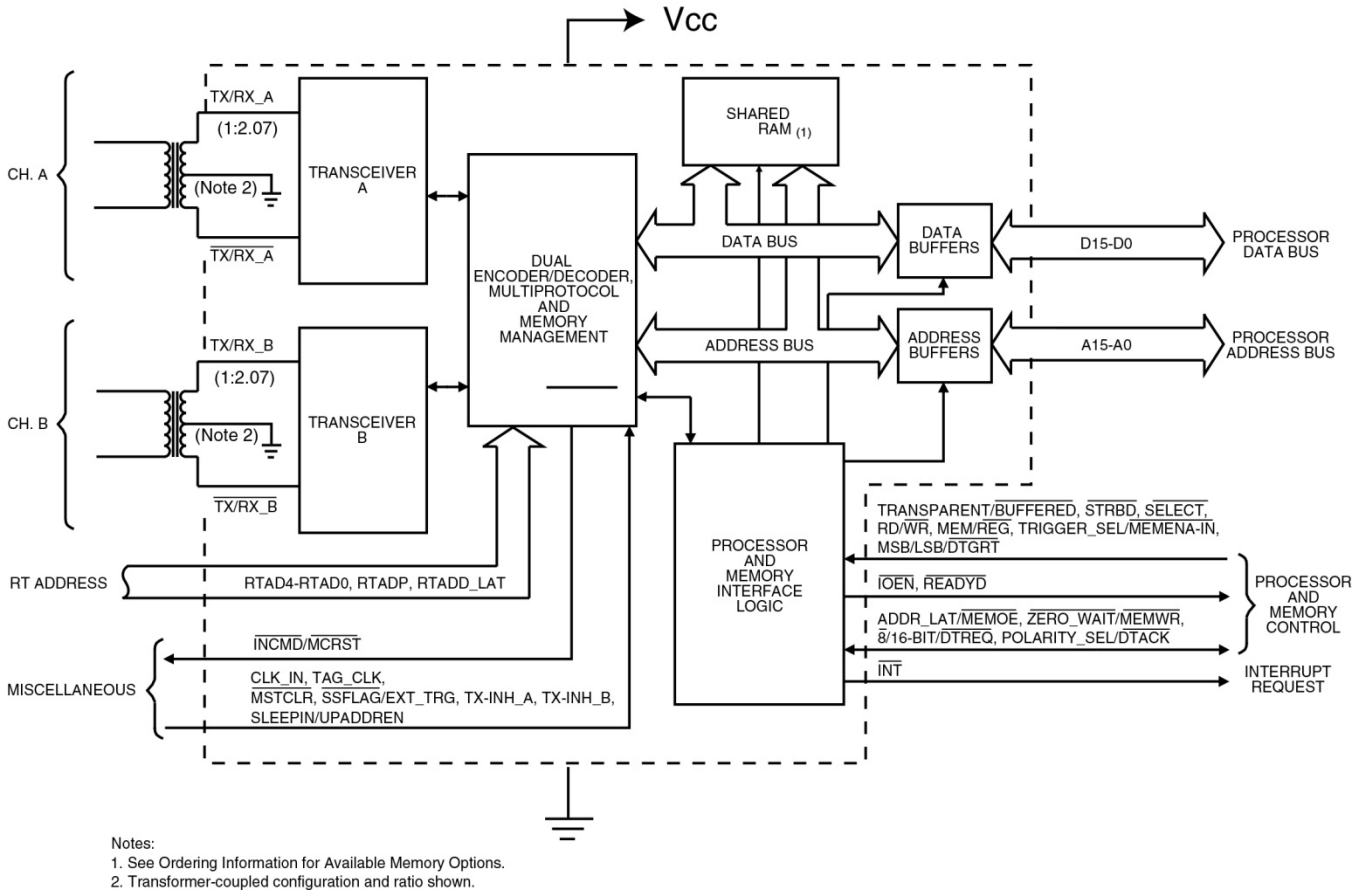



**Figure 2. Mini-ACE Mark3 and Micro-ACE-TE Block Diagram (shown with X8/9 Transceiver Option)**

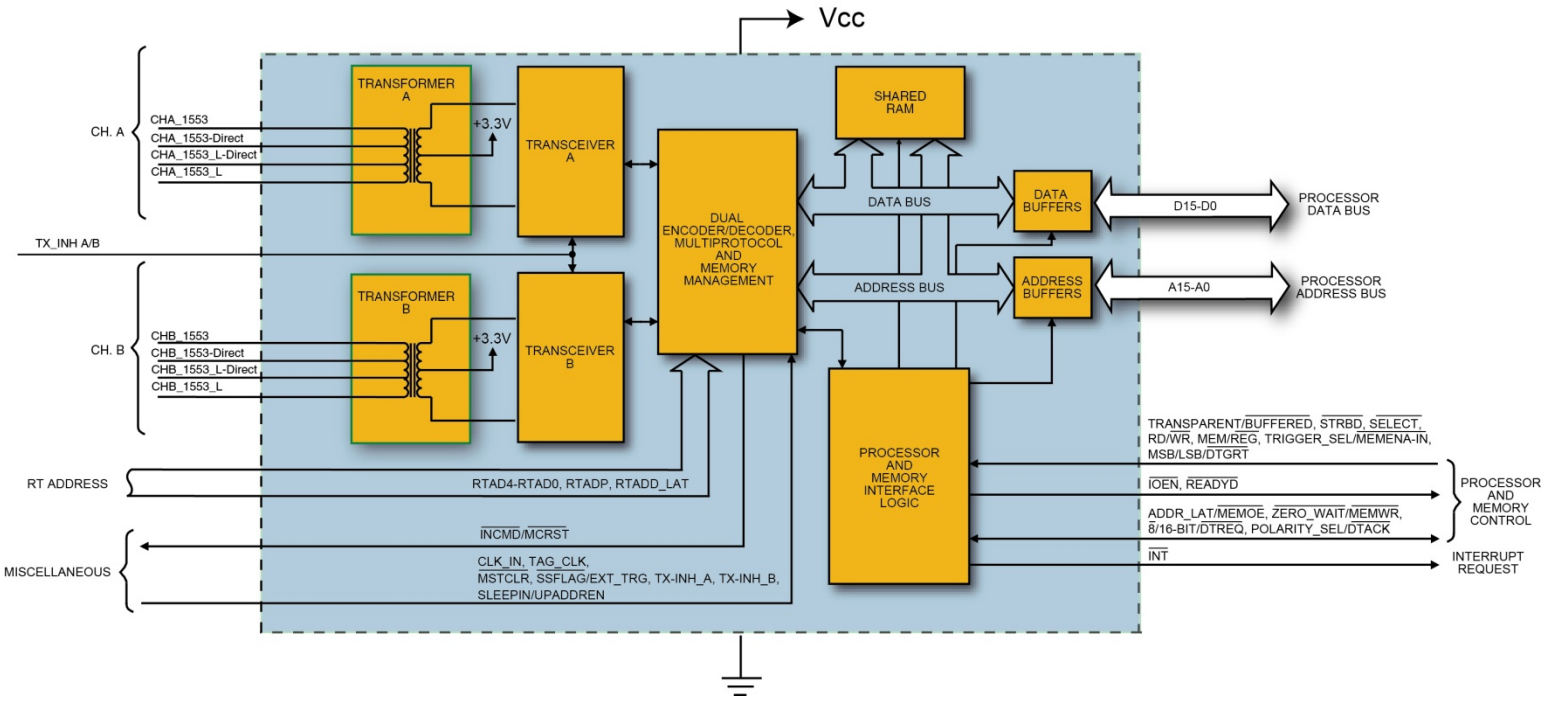



**Figure 3. Total-ACE Block Diagram**

# 3 DEVICE SPECIFICATIONS

The Latest Device Specifications for the Enhanced Mini-Ace/Micro-Ace and Mini-ACE Mark3/Micro-ACE TE, and Total-ACE are available at http://www.ddc-web.com:

For the latest Enhanced Mini-ACE/Micro-ACE information see BU-6174X/6184X/6186X Data Sheet

For the latest Mini-ACE Mark3/Micro-ACE-TE information see BU-6474X/6484X/6486X Data Sheet

For the latest Total-ACE information see BU-64843T Data Sheet

# 4 FUNCTIONAL OVERVIEW

The BU-61743/61745 RT, and BU-61843/61845/61864/61865 BC/RT/MT Enhanced Mini-ACE (BU-61740B RT, and BU-61840B/61860B BC/RT/MT Micro-ACE), BU-64743/64745 RT, and BU-64843/64845/64863 BC/RT/MT Mini-ACE Mark3 (BU-64840B/64843B/64860B/64863B BC/RT/MT Micro-ACE-TE) family of MIL-STD-1553 terminals comprise a complete integrated interface between a host processor and a MIL-STD-1553 bus.

The BU-61743/61745 RT, and BU-61843/61845/61864/61865 BC/RT/MT Enhanced Mini-ACE are packaged in a 1.0 inch square ceramic flat-pack package providing footprint (with four pin differences) compatibility with previous generation Mini-ACE terminals. The BU-64743/64745 RT, and BU-64843/64845/64863 BC/RT/MT Mini-ACE Mark3 are packaged in a 0.890 inch square ceramic flat-pack package.

The BU-61740B RT, and BU-61840B/61860B BC/RT/MT Micro-ACE and BU-64840B/64843B/64860B/64863B BC/RT/MT Micro-ACE-TE are packaged in a 0.815 inch square BGA package.

The Enhanced Mini-ACE series of hybrids provides software compatibility with the previous generation Mini-ACE terminals, as well as software compatibility with the older ACE series.

The Enhanced Mini-ACE RT provides complete multi-protocol support of MIL-STD-1553A/B/McAir and STANAG 3838. All versions integrate dual transceiver; along with protocol, host interface, memory management logic; and a minimum of 4K words of RAM. In addition, the BU-61864/61865/61860B/64863/64860B/64863B BC/RT/MT terminals include 64K words of internal RAM, with built-in parity checking.

The Enhanced Mini-ACE series includes 5V or 3.3V, voltage source transceivers for improved line driving capability, with options for MIL-STD-1760 and McAir compatibility. As a means of reducing power consumption, there are versions for which the logic is powered by 3.3V, rather than 5V. To provide further flexibility, the Enhanced Mini-ACE may operate with a choice of 10, 12, 16, or 20 MHz clock inputs.

One of the salient new features of the Enhanced Mini-ACE is its enhanced bus controller architecture. The Enhanced BC's highly autonomous message sequence control engine provides a means for offloading the host processor for implementing minor and major frame timing control; asynchronous message insertion; data block double buffering; bulk data transfers; and retry and bus switching strategy. For the purpose of performing messaging to the host processor, the Enhanced BC mode includes a General Purpose Queue, along with user-defined interrupts.

The Enhanced Mini-ACE is the latest device group in the ACE family. The term “enhanced” has also been used in earlier versions of the family to describe new features introduced at each stage. For backward compatibility reasons, the same terms and options have been maintained in the Enhanced Mini-ACE. The user will be aware of Enhanced Mode, set by bit 15 of Configuration Register (CR) # 3 along with the following optional features from earlier families:

| | |
|---|---|
| Enhanced RT Memory Management | CR#2 Bit #1 |
| Enhanced RT Interrupt Handling | CR#2 Bit #15 |
| Enhanced Mode Code Handling | CR#3 Bit #0 |
| Enhanced Mode Enable | CR#3 Bit #15 |
| Expanded BC Control Word Enable | CR#4 Bit #12 |

Plus for the latest devices:

| | |
|---|---|
| Enhanced BC | CR#6 Bit #15 |
| Enhanced Time Tag Synchronization | CR#7 Bit #2 |
| Enhanced BC Watchdog Timer Enable | CR#7 Bit #1 |

In many cases, the user may wish to enable most of these bits at initialization to have all available features active

A second major new feature of the Enhanced Mini-ACE is the incorporation of a fully autonomous built-in self-test. This test provides comprehensive testing of the internal protocol logic. A separate test verifies the operation of the internal RAM. Since the self-tests are fully autonomous, they eliminate the need for the host to write and read stimulus and response vectors.

The Enhanced Mini-ACE RT offers the same choices of single, double, and circular buffering for individual subaddresses as the ACE and Mini-ACE (Plus). New enhancements to the RT architecture include a global circular buffering option for multiple (or all) receive subaddresses, a 50% rollover interrupt for circular buffers, an interrupt status queue for logging up to 32 interrupt events, and an option to automatically initialize to RT mode with the busy bit set. The interrupt status queue and 50% rollover interrupt features are also included as improvements to the Enhanced Mini-ACE’s monitor architecture.

To minimize board space and "glue" logic, the Enhanced Mini-ACE terminals provide the same wide choice of host interface configurations as the ACE and Mini-ACE (Plus). This includes support of shared RAM interfaces to 16-bit or 8-bit processors, memory or port type interfaces, and multiplexed or non-multiplexed address/data buses; plus a DMA interface configuration.

Hermetic, ceramic packaged, Enhanced Mini-ACE series terminals are available in versions operating over the full military temperature range of -55 to +125°C. Available screened to MIL-PRF-38534C, these terminals are ideal for military and industrial processor-to-1553 applications.

## 4.1 Transceivers

The transceivers in the Enhanced Mini-ACE series of terminals are fully monolithic, requiring only a +5 or +3.3 volt power input. The transmitters are voltage sources, which provide improved line driving capability over current sources. This serves to improve performance on long buses with many taps. The transmitters also offer an option that satisfies the MIL-STD-1760 requirement for a minimum of 20 volts peak-to-peak, transformer coupled output.

Besides eliminating the demand for an additional power supply, the use of a +5V or +3.3V-only transceivers requires the use of a step-up, rather than a step-down, isolation transformer. This provides the advantage of higher terminal input impedance than is possible for a 15 volt or 12 volt transmitter. As a result, there is a greater margin for the input impedance test, mandated for the 1553 validation test. This characteristic allows for longer cable lengths between a system connector and the isolation transformers of an embedded 1553 terminal.

To provide compatibility to McAir specs, the Enhanced Mini-ACE is available with an option for transmitters with increased rise and fall times.

The receiver sections of the Enhanced Mini-ACE are fully compliant with MIL-STD-1553B Notice 2 in terms of front end over voltage protection, threshold, common mode rejection, and word error rate.

# 5 SIGNAL DESCRIPTIONS BY FUNCTIONAL GROUPS

For the latest Enhanced Mini-ACE/Micro-ACE information see BU-6174X/6184X/6186X Data Sheet

For the latest Mini-ACE Mark3/Micro-ACE-TE information see BU-6474X/6484X/6486X Data Sheet

For the latest Total-ACE information see BU-64843T Data Sheet

# 6 +5.0V TRANSCEIVER INTERFACE TO A MIL-STD-1553 BUS

Figure 4 illustrates the interface between the various +5.0V transceiver versions of the Enhanced Mini-ACE series and a MIL-STD-1553 bus. Connections for both direct (short stub) and transformer (long stub) coupling, as well as the peak-to-peak "Nominal" voltage levels that appear at various points (when transmitting), are as indicated in the figure.

Please see for +5.0V isolation transformer limitations and recommendations.

In accordance with MIL-STD-1553B, the turns ratio of the coupling transformer is required to be 1.0 to 1.4. For both coupling configurations, isolation resistors are required to be in series with each leg connecting to the 1553 bus. In the case of direct coupling, the value of the coupling resister is 55 ohms. For direct coupling, the isolation resistors are located within the 1553 BC, RT, or Monitor terminal. In the case of transformer coupled, the resistors are 0.75 $Z_0$ in value and are located in the bus coupler, rather than the BC, RT, or Monitor terminal. The isolation resistors protect the bus against short circuit conditions in the transformers, stubs, or terminal components.

For most system applications, transformer (stub) coupling is preferred over direct coupling. Some of the advantages of transformer coupling are:

(1) Looking from the 1553 bus towards the stub, the effect of the 1.4 to 1.0 stepdown of the coupling transformer will be to **double** the impedance of the stub/terminal combination, as seen by the bus. Since the stub impedance decreases as a function of stub length due to distributed cable capacitance, this doubling effect serves to reduce the amount of impedance loading on the bus by individual terminals. For this reason, stub coupled terminals may be located up to 20 feet from the bus; the distance for direct coupled terminals is limited to 12 inches.

(2) Looking from the isolation transformer down the stub (towards the bus), the impedance seen is $Z_0$. Therefore, the characteristic impedance of the stub cabling (78 ohms nominal) matches the stub's load impedance, minimizing reflections back toward the transmitter.

(3) In a direct-coupled terminal, the main bus is not protected against a short circuit in the stub cabling. For the transformer coupled case, the bus is protected against such a fault.

(4) A transformer coupled terminal provides improved DC and common mode isolation over a direct-coupled terminal.

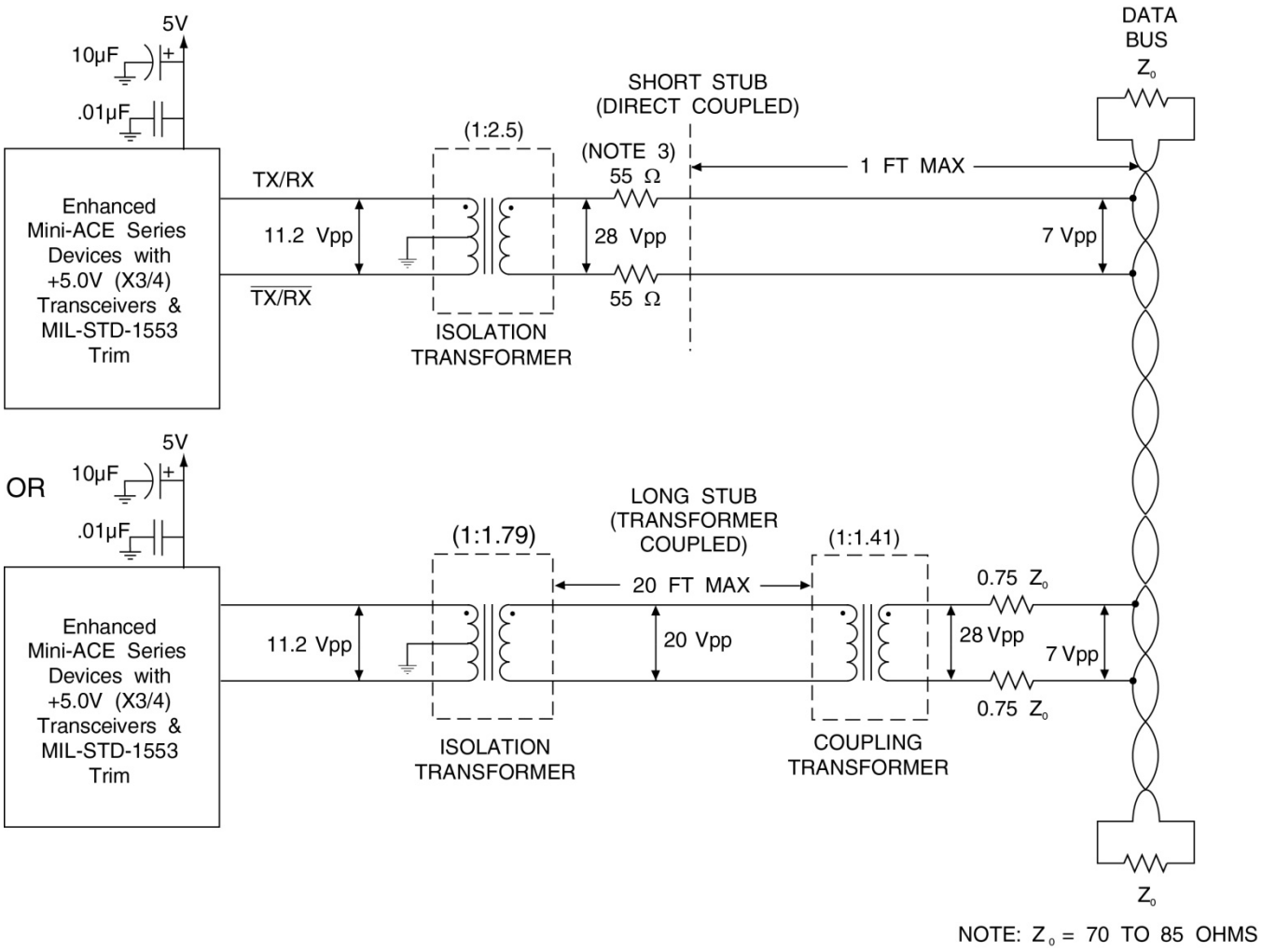



**Figure 4. Enhanced Mini-ACE Series Interface to 1553 Bus (+5.0V Transceivers [X3/4] & MIL-STD-1553 Trim shown)**

*Figure 4 Notes:*

1. *Shown for one or two redundant buses that interface to the Enhanced Mini-ACE.*

2. *Transmitted voltage level on 1553 bus is 6 Vp-p min, 7 Vp-p nominal, 9 Vp-p max.*

3. *Required tolerance on isolation resistors is 2%. Instantaneous power dissipation (when transmitted) is approximately 0.5W (typ), 0.8W (max).*

## 6.1 +5.0 Volt Isolation Transformers

Please see MN-6186X-003 Appendix A for +5.0V isolation transformer limitations and recommendations.

# 7 +3.3V TRANSCEIVER INTERFACE TO A MIL-STD-1553 BUS

Figure 5 and Figure 6 illustrate the interface between the various +3.3V transceiver versions of the Enhanced Mini-ACE series and a MIL-STD-1553 bus. Connections for both direct (short stub) and transformer (long stub) coupling, as well as the peak-to-peak “Nominal” voltage levels that appear at various points (when transmitting), are as indicated in the Figures.

Figure 7 illustrates the interface between the Total-ACE (with integrated isolation transformers) and a MIL-STD-1553 bus. Connections for transformer (long stub) coupling, as well as the peak-to-peak “Nominal” voltage levels that appear at various points (when transmitting), are as indicated in the Figure.

Please see +3.3V isolation transformer limitations and recommendations.

In accordance with MIL-STD-1553B, the turns ratio of the coupling transformer is required to be 1.0 to 1.4. For both coupling configurations, isolation resistors are required to be in series with each leg connecting to the 1553 bus. In the case of direct coupling, the value of the coupling resister is 55 ohms. For direct coupling, the isolation resistors are located within the 1553 BC, RT, or Monitor terminal. In the case of transformer coupled, the resistors are 0.75 $Z_0$ in value and are located in the bus coupler, rather than the BC, RT, or Monitor terminal. The isolation resistors protect the bus against short circuit conditions in the transformers, stubs, or terminal components.

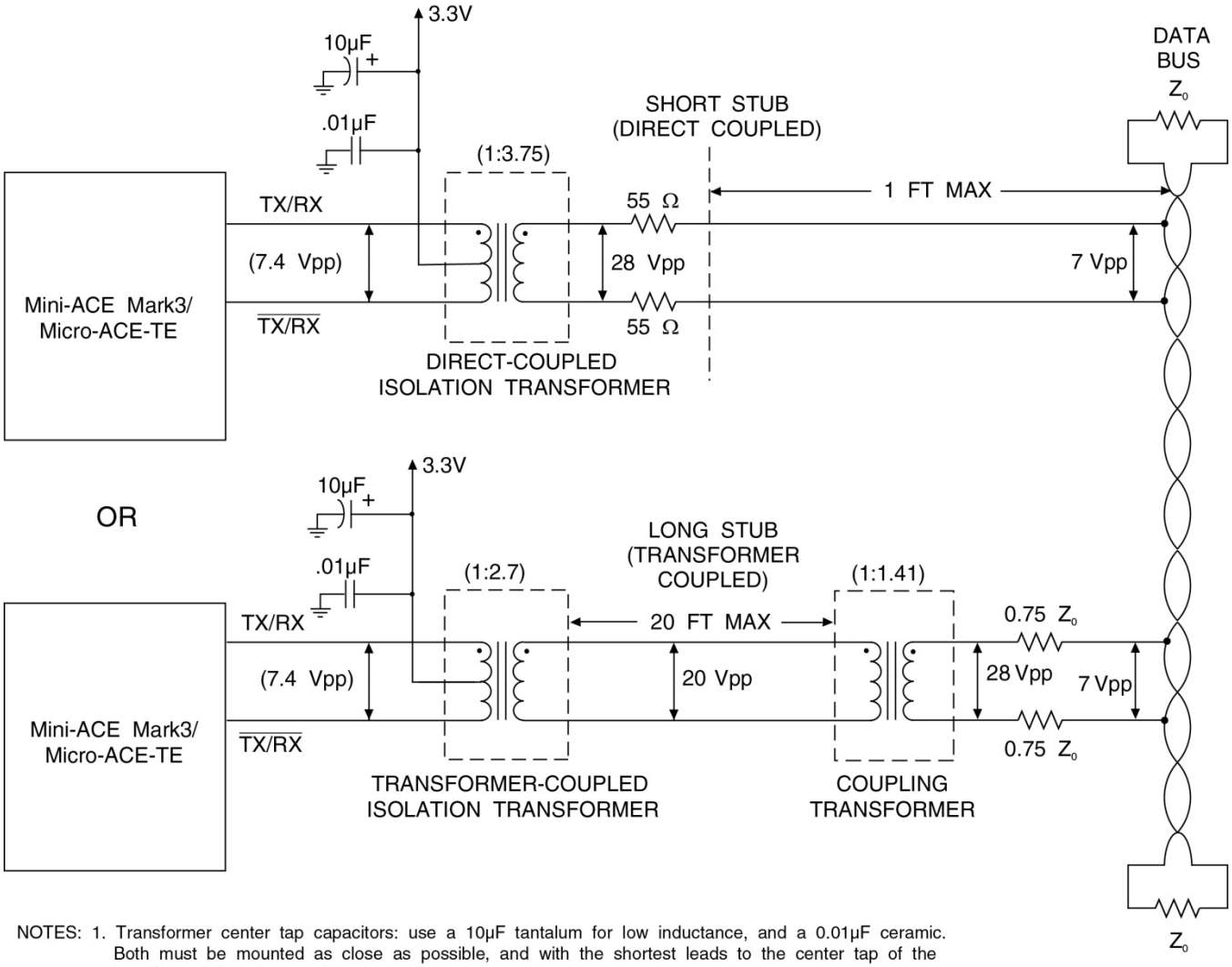
For most system applications, transformer (stub) coupling is preferred over direct coupling. Some of the advantages of transformer coupling are:

(1) Looking from the 1553 bus towards the stub, the effect of the 1.4 to 1.0 stepdown of the coupling transformer will be to **double** the impedance of the stub/terminal combination, as seen by the bus. Since the stub impedance decreases as a function of stub length due to distributed cable capacitance, this doubling effect serves to reduce the amount of impedance loading on the bus by individual terminals. For this reason, stub coupled terminals may be located up to 20 feet from the bus; the distance for direct coupled terminals is limited to 12 inches.

(2) Looking from the isolation transformer down the stub (towards the bus), the impedance seen is $Z_0$. Therefore, the characteristic impedance of the stub cabling (78 ohms nominal) matches the stub's load impedance, minimizing reflections back toward the transmitter.

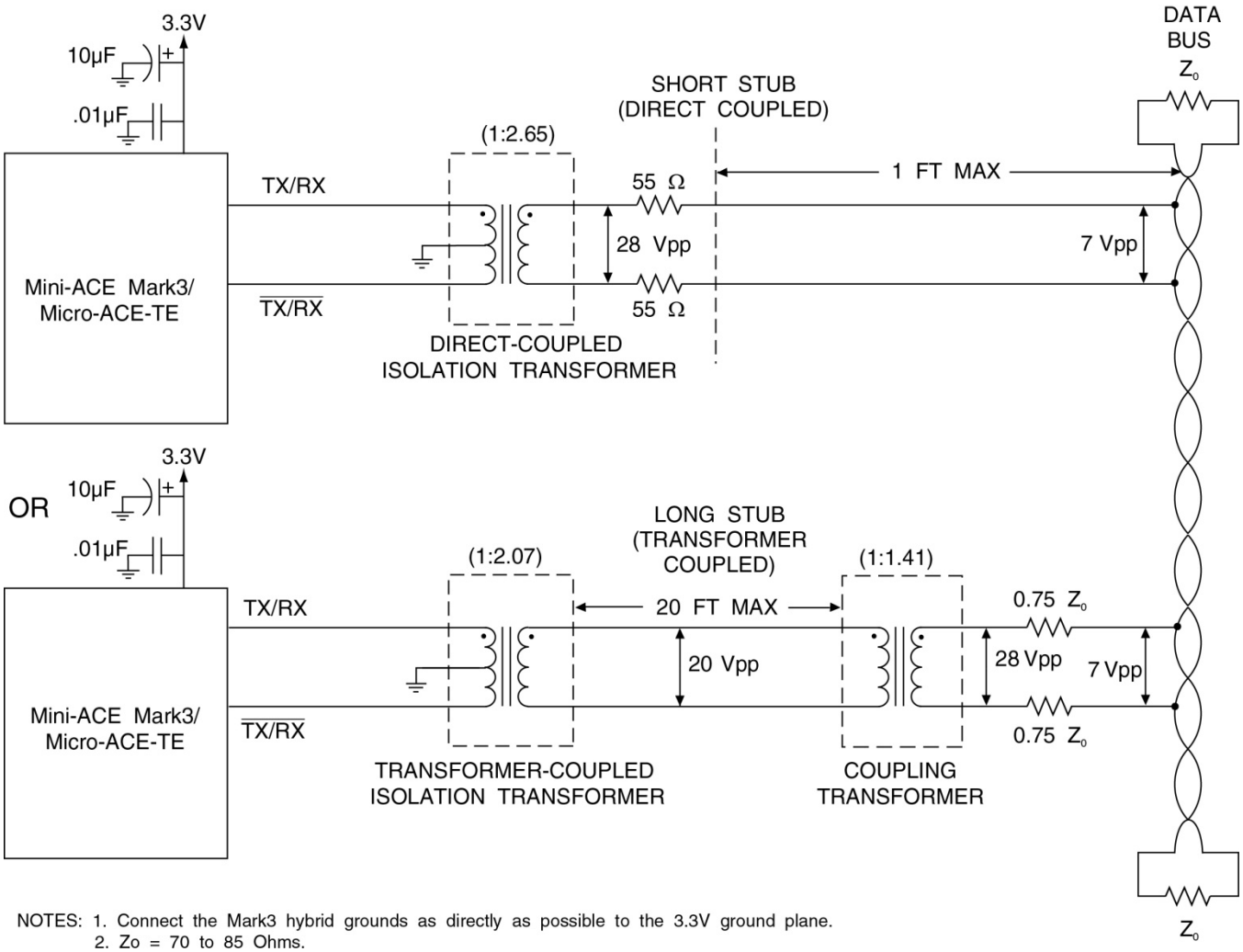
(3) In a direct-coupled terminal, the main bus is not protected against a short circuit in the stub cabling. For the transformer coupled case, the bus is protected against such a fault.

(4) A transformer coupled terminal provides improved DC and common mode isolation over a direct-coupled terminal.



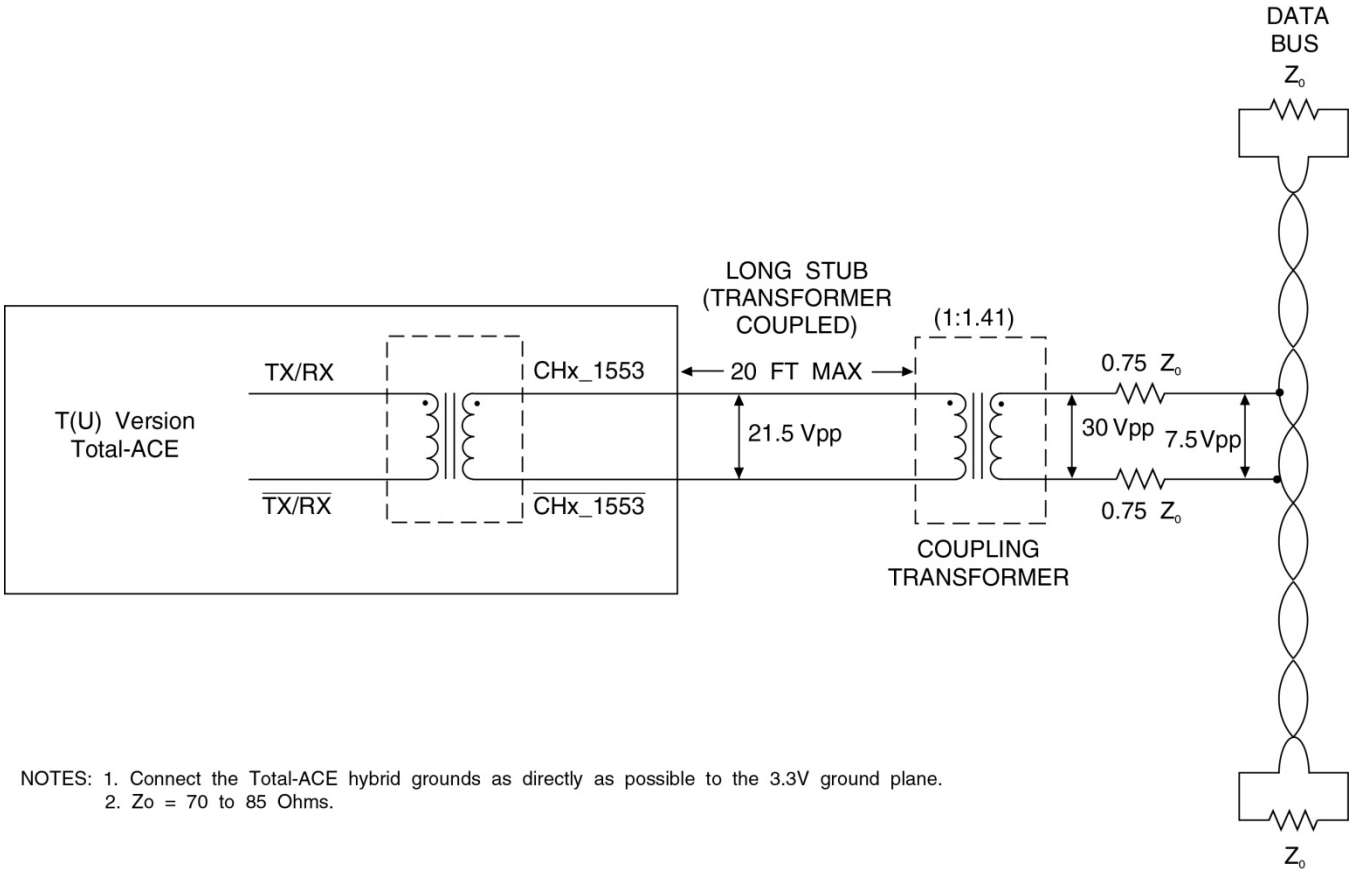

NOTES: 1. Transformer center tap capacitors: use a 10µF tantalum for low inductance, and a 0.01µF ceramic. Both must be mounted as close as possible, and with the shortest leads to the center tap of the transformer(s) and ground.
2. Connect the Mark3 hybrid grounds as directly as possible to the 3.3V ground plane.
3. Zo = 70 to 85 Ohms.

**Figure 5. Enhanced Mini-ACE Series Interface to 1553 Bus (+3.3V Transceivers [X8/9] & MIL-STD-1553 Trim shown)**




NOTES: 1. Connect the Mark3 hybrid grounds as directly as possible to the 3.3V ground plane.
2. Zo = 70 to 85 Ohms.

**Figure 6. Enhanced Mini-ACE Series Interface to 1553 Bus (+3.3V Transceivers [XC/D] & MIL-STD-1553 Trim shown)**




NOTES: 1. Connect the Total-ACE hybrid grounds as directly as possible to the 3.3V ground plane.
2. Zo = 70 to 85 Ohms.

**Figure 7. Total-ACE Series Interface to 1553 Bus (+3.3V Transceivers [X8] & MIL-STD-1553 Trim shown)**

## 7.1 +3.3 Volt Isolation Transformers

Please see MN-6186X-003 Appendix A for +3.3V isolation transformer limitations and recommendations.

# 8 THERMAL MANAGEMENT FOR MICRO-ACE AND MIRCO-ACE-TE (BGA PACKAGE)

Ball Grid Array (BGA) components necessitate that thermal management issues be considered early in the design stage for MIL-STD-1553 terminals. This is especially true if high transmitter duty cycles are expected. The temperature range specified for DDC's Micro-ACE, Micro-ACE-TE, and Total-ACE device refers to the temperature at the ball, not the case.

All Micro-ACE, Micro-ACE-TE, and Total-ACE devices incorporate multiple package connections that perform the dual function of transceiver circuit ground and thermal heat sink. **Refer to datasheet pinout tables for thermal ball connection locations.** It is mandatory that these thermal balls be directly soldered to a circuit ground/thermal plane (a circuit trace is insufficient). Operation without an adequate ground/thermal plane is not recommended and extended exposure to these conditions may affect device reliability.

The purpose of this ground/thermal plane is to conduct the heat being generated by the transceivers within the package and conduct this heat away from the Micro-ACE, Micro-ACE-TE, and Total-ACE. In general, the circuit ground and thermal (chassis) ground are not the same ground plane. It is acceptable for these balls to be directly soldered to a ground plane but it must be located in close physical and thermal proximity (0.003" pre-preg layer recommended) to the thermal plane.

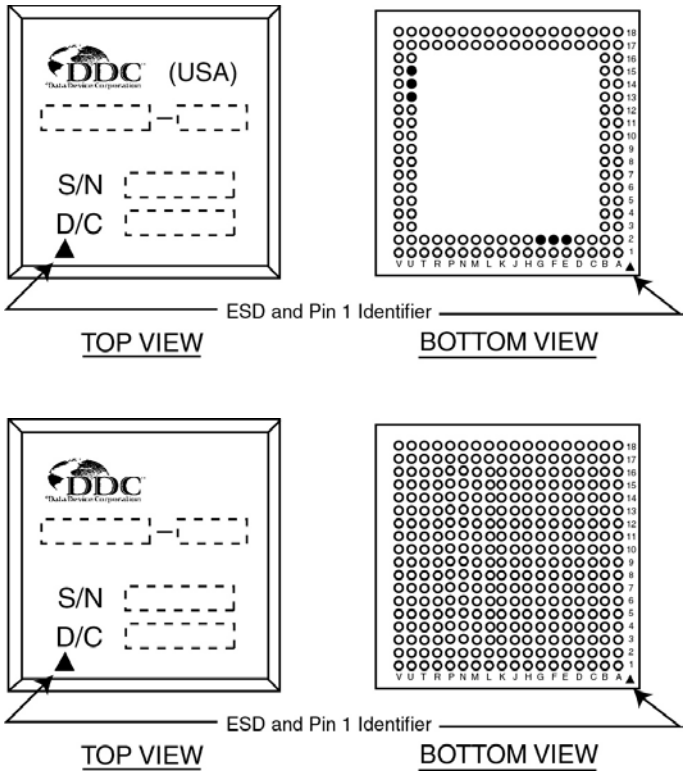



**Figure 8. Ball Locations for Micro-ACE-TE and Micro-ACE (BGA Packages)**

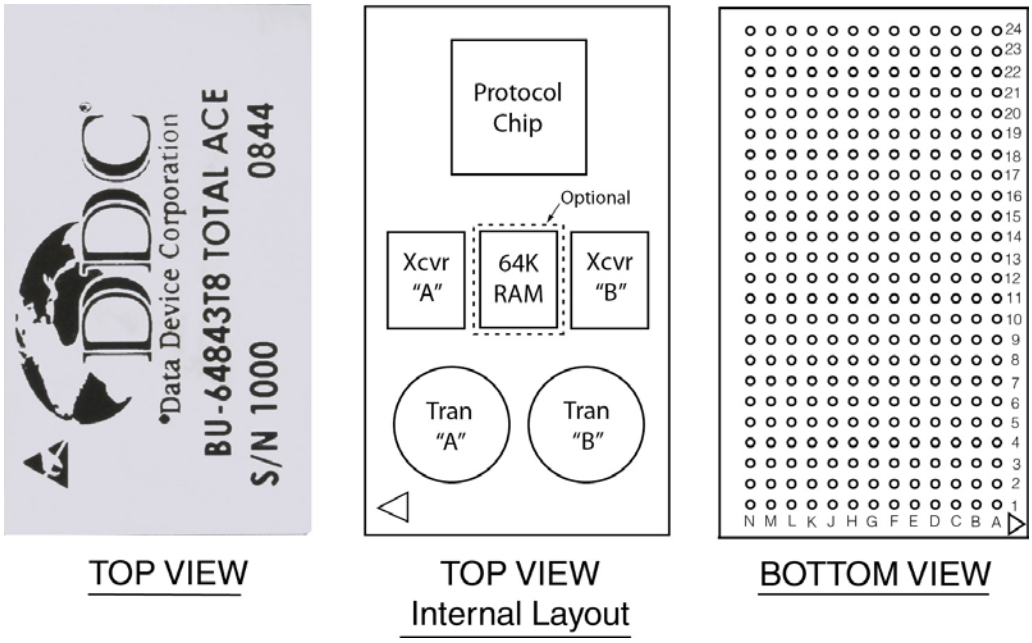



**Figure 9. Ball Locations for Total-ACE (BGA Package)**

## 8.1 Power Supply and PC Board Considerations

With regard to the Enhanced Mini-ACE terminal and the associated isolation Transformers (Note: Total-ACE features integral isolation transformers), there are a number of important factors to consider relating to component placement, circuit routing, and power distribution. Some of these factors include:

**(1) Power and Ground Distribution:**

Any resistance will result in power supply input voltage drops, which can lower the transmitter output voltage below the minimum level required by MIL-STD-1553. It is important to minimize the power distribution impedance along the transceivers high current path.

For devices with X3/4 (+5V) or XC/D (+3.3V) transceivers, the high current path (while transmitting) is from the positive voltage supply into the device, through the transmitter output stage, through one leg of the isolation transformer to the grounded transformer primary winding center tap (see Figure 10).

For devices with X8/9 (+3.3V) transceivers, the high current path (while transmitting) is from the +3.3 volt supply into the transformer primary winding center tap, through one leg of the isolation transformer, through the transmitter output stage and the device GROUND pins (see Figure 11).

It is important to realize that in both cases the high current path is through (and includes) the transformer primary winding center tap. A worst-case analysis should ensure that with minimum supply voltage (and calculated voltage drops), the voltage delivered between device power supply pins (Vcc or Gnd) and the center tap of the respective transformer will be no less than the specified minimum voltage of 4.75V (X3/4 option) or 3.15V (X8/9/C/D option).

In some cases, excessive transmitting voltage drops can be reduced by means of larger decoupling capacitors, but it is best to minimize these voltage drops at the PCB design stage with low resistance conductors.

**(2) Component & Signal Spacing:**

Avoid running 1553 analog signal traces in close proximity to other analog or digital signals on the board (especially those running in parallel) as severe crosstalk can increase the receiver's bit error rate, zero-crossing distortion, or common mode rejection beyond that allowed by MIL-STD-1553.

Isolation transformers should be placed as close as is physically possible to the respective TX/RX pins on the device. This serves to minimize crosstalk from other signals in addition to minimizing the voltage drop in the traces. The trace lengths of the complementary, input/output signal pairs should also be minimized and closely matched in length as well.

**(3) Power & Ground Planes:**

As is the rule in all high-speed digital circuits, it is good practice to incorporate ground and power supply planes under the MIL-STD-1553 device, Bi-Phase data output lines (out of device transceivers) and Isolation transformers.

Isolation transformer secondary output traces to the bus (or stub) should not have ground or power planes under them.

Distributed capacitance tends to lower the input impedance of the terminal as seen from the 1553 bus. MIL-STD-1553 requires there be a minimum input impedance of 2kΩ for direct-coupled and 1kΩ for transformer-coupled (stub) terminals. It is likely that the terminal will not meet this requirement if there are ground or power planes under the isolation transformer secondary output traces to the bus (or stub).

***IMPORTANT NOTE:***

*It is very important that there be ground and/or power supply planes underneath the MIL-STD-1553 device, the Bi-Phase data output lines (out of device transceivers) and Isolation transformers.*

*There should NOT be any ground or power planes beneath the TX/RX signals emanating from the isolation transformer secondary output winding to any connector or cables leaving the board.*

**(4) Analog and Digital Grounds:**

The BU-61743/61745 RT, and BU-61843/61845/61864/61865 BC/RT/MT Enhanced Mini-ACE (BU-61740B RT, and BU-61840B/61860B BC/RT/MT Micro-ACE) logic and transceiver grounds ARE connected together inside the hybrid.

The BU-64743/64745 RT, and BU-64843/64845/64863 BC/RT/MT Mini-ACE Mark3 (BU-64840B/64843B/64860B/64863B BC/RT/MT Micro-ACE-TE) and BU-64843T Total-ACE, logic and transceiver grounds are NOT connected together inside the hybrid.

**(5) Decoupling Capacitors:**

Two relatively small ceramic capacitors (0.1µf), with both low Effective Series Resistance (ESR) and low Effective Series Inductance (ESL), are generally necessary for the LOGIC & RAM power inputs as well as the transceiver power inputs on the device. These reduce the high-frequency power supply noise that may result from the 1MHz and 2MHz current pulses drawn by the transceivers.

A 10µf tantalum capacitor located at the device transceiver power inputs is usually sufficient to compensate for voltage drops due to the increased current requirement (100s of mA) while transmitting.

If the voltage at the device transceiver power inputs is greater than the required minimum when not transmitting, but less than the minimum when transmitting, then a larger tantalum capacitor may be necessary to sustain the power input voltage above the minimum level while transmitting. This capacitor could be sized by a process of trial and error while the transceiver is transmitting 32 data word (worst case) messages at duty cycles representing typical system operation.

**(6) Location of the Clock Oscillator:**

The Clock Oscillator should be located as close as physically possible to the clock input pin on the device.

**(7) In Summary:**

For all devices, two, 0.1µf ceramic decoupling capacitor on both LOGIC & RAM power inputs.

For devices, with X3/4/C/D transceivers, DDC recommends a 10µf tantalum capacitor in parallel with a 0.1µf ceramic capacitor (see Figure 10).

For devices with X8/9 transceivers, DDC recommends a 1.0µf tantalum capacitor in parallel with a 0.1µf ceramic capacitor (see Figure 11).

These capacitors should be located as close as possible to the Vcc input pads and should be sufficient for most applications.

Additionally, for devices with X8/9 transceivers, a 10µf tantalum capacitor in parallel with a .01µf ceramic capacitor must be located as close as possible to the center tap of the transceiver isolation transformer.

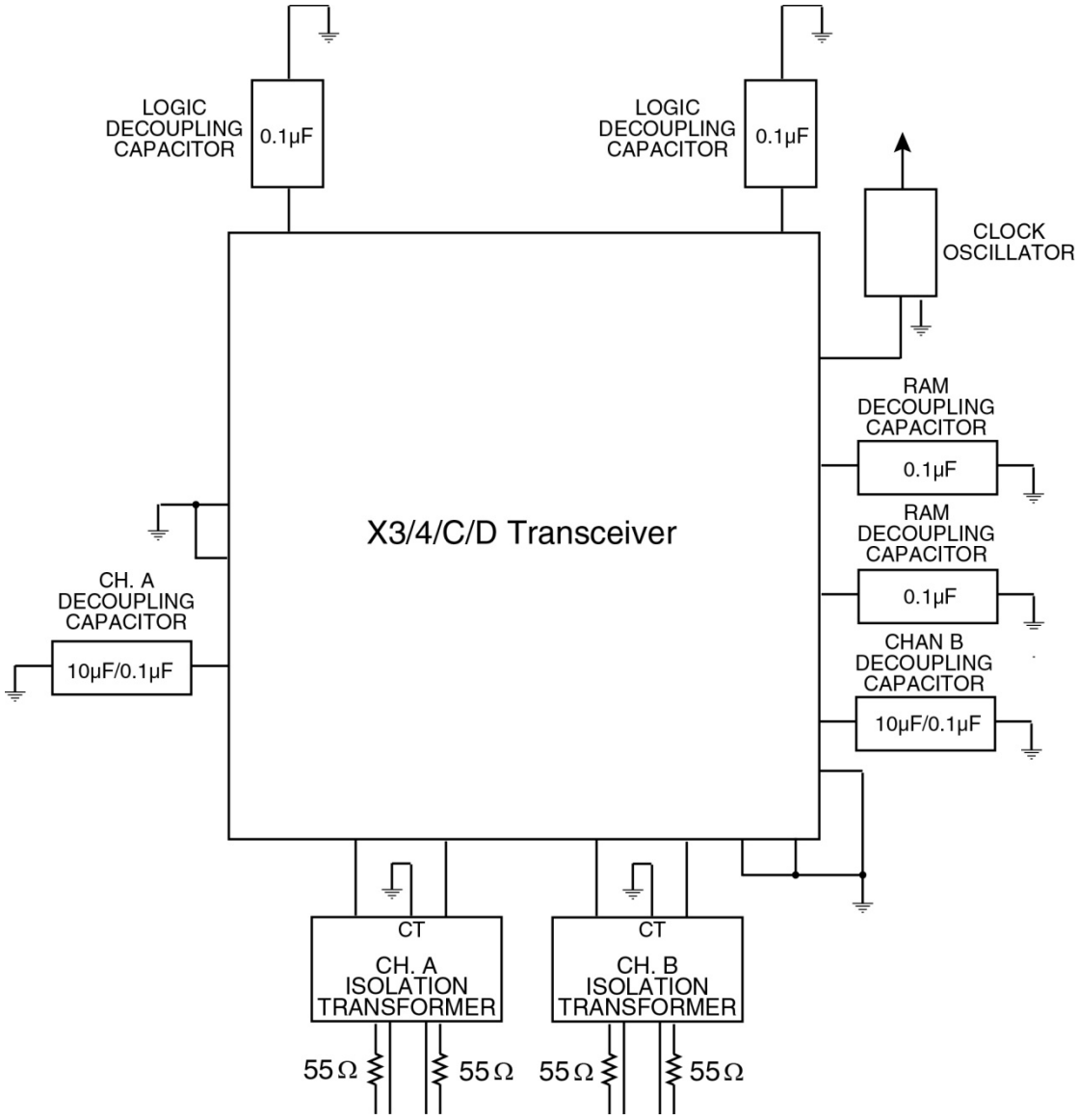



**Figure 10. P.C. Board Layout Example: X3/4/C/D Transceiver**

*Figure 10 Notes:*

1. *Physical spacing between Enhanced Mini-ACE® and isolation transformers must be kept to a minimum.*

2. *There must be ground and/or power supply planes underneath the device, the Bi-Phase data output lines (out of device transceivers) and isolation transformers.*

3. *There should not be any ground or power supply planes underneath the TX/RX signals emanating from the isolation transformers secondary output winding to any connector or cables leaving the board.*

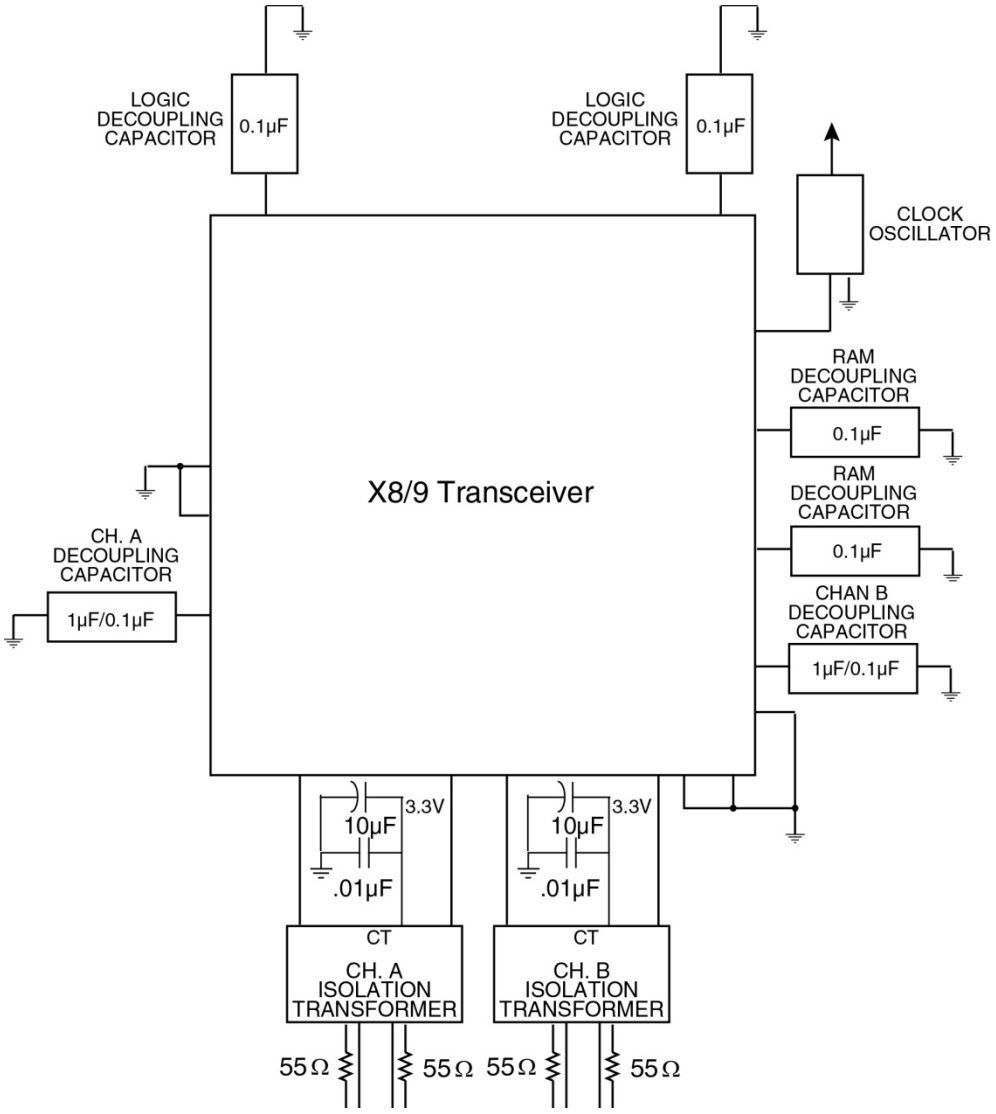



**Figure 11. P.C. Board Layout Example: X8/9 Transceiver**

*Figure 11Notes:*

1. *Physical spacing between Enhanced Mini-ACE® and isolation transformers must be kept to a minimum.*
2. *There must be ground and/or power supply planes underneath the device, the Bi-Phase data output lines (out of device transceivers) and isolation transformers.*
3. *There should not be any ground or power planes beneath the TX/RX signals emanating from the isolation transformers secondary output winding to any connector or cables leaving the board.*
4. *The two isolation transformers are an integral part of the Total-ACE®.*

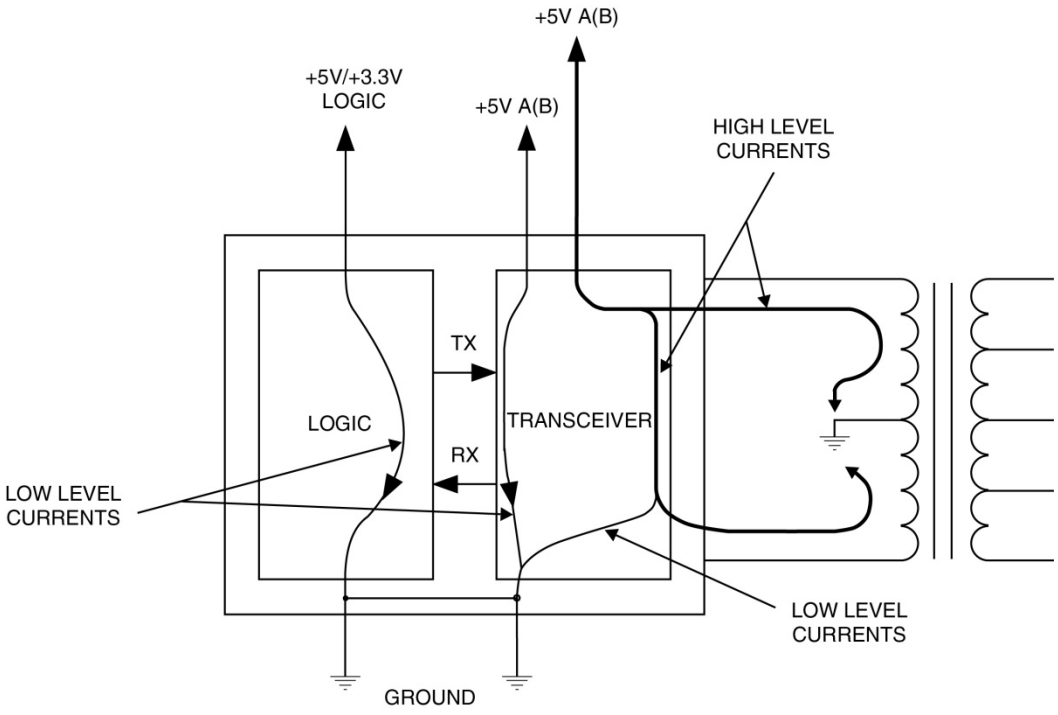



**Figure 12. Power/Ground Current Distribution for +5V Transceivers (X3/4 Option)**

## 8.2 Simplified Equivalent Circuit of Transceiver

Refer to the circuit illustrated in Figure 13. $V_{in}$ is defined to be the rated minimum output voltage from the power supply. $R_d$ is the series resistance of the power distribution path to the transceiver power inputs. This includes resistance in the power supply return path, from the transformer center tap, as well as the power input path.

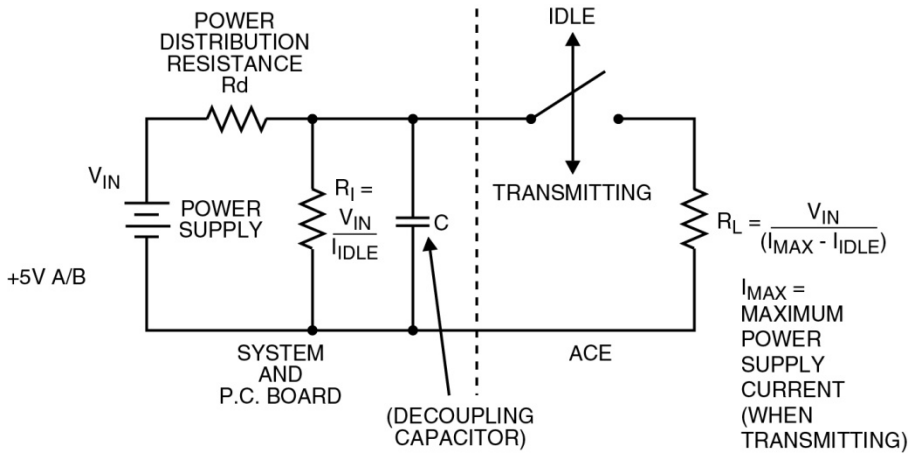



**Figure 13. Simplified Equivalent Circuit of Enhanced Mini-ACE Terminal**

## 8.3 Isolation Transformer Interface to System Connector

The general practice in connecting the stub side of a transformer (or direct) coupled terminal to an external system connector is to make use of 78 ohm twisted-pair shielded cable. This minimizes impedance discontinuities. The decision of whether to isolate or make connections between the center tap of the isolation transformer's secondary, the stub shield, the bus shield, and/or chassis ground must be made on a system basis, as determined by an analysis of EMI/RFI and lightning considerations. In most systems, the secondary center tap is **not** grounded. In some systems, it is specified that the 1553 terminal's input impedance must be measured at the system connector. This is despite the fact that the MIL-STD-1553B requirement is for it to be measured looking directly in from the bus side of the isolation transformer. The effect of a relatively long stub cable will be to reduce the measured impedance. If this reduces the impedance below the required level of 1000 ohms (for transformer-coupled stubs), it is sometimes possible to increase the impedance somewhat by using a pair of coax wires (with the shields ungrounded), rather than a single twisted/shielded pair, for the stub connections. The effect on the rest of the system performance of the bus signals coupled from the ungrounded shielded cables must be considered as a tradeoff against the increased terminal impedance.

## 8.4 Simulated Bus (Lab Bench) Interconnections

For purposes of software development and system integration, it is generally not necessary to integrate the required couplers, terminators, etc., that comprise a complete MIL-STD-1553B bus. In most instances, a simplified electrical configuration will suffice. The interconnection methods illustrated in Figure 14 allows the device to be interfaced over a "simulated bus" to simulation and test equipment. The length of this “simulated bus” should not exceed 5 feet. It is important to note that the termination resistors indicated are necessary (if not already present within the test/simulation equipment) in order to ensure reliable communications between the device and the simulation/test equipment. As illustrated In Figure 14, the 78Ω and 39 Ω termination resistors should be physically located as close as possible to the test/simulation equipment.

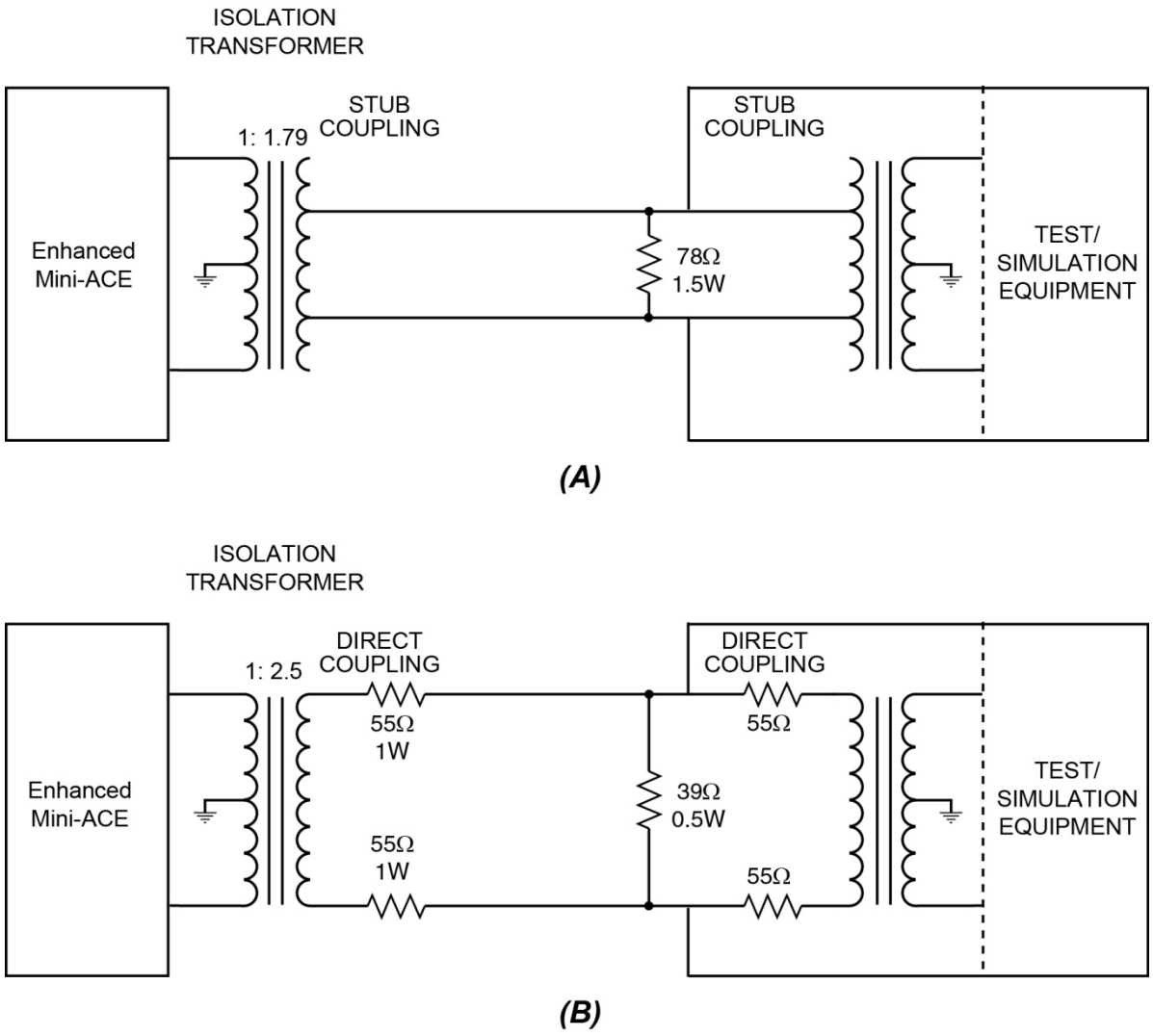



**Figure 14. Simulated Bus Interconnections**

*Figure 14 Note:*

*(A) Transformer Coupled Enhanced Mini-ACE-to-Transformer Coupled Equipment*

*(B) Direct Coupled Enhanced Mini-ACE-to-Direct Coupled Equipment*

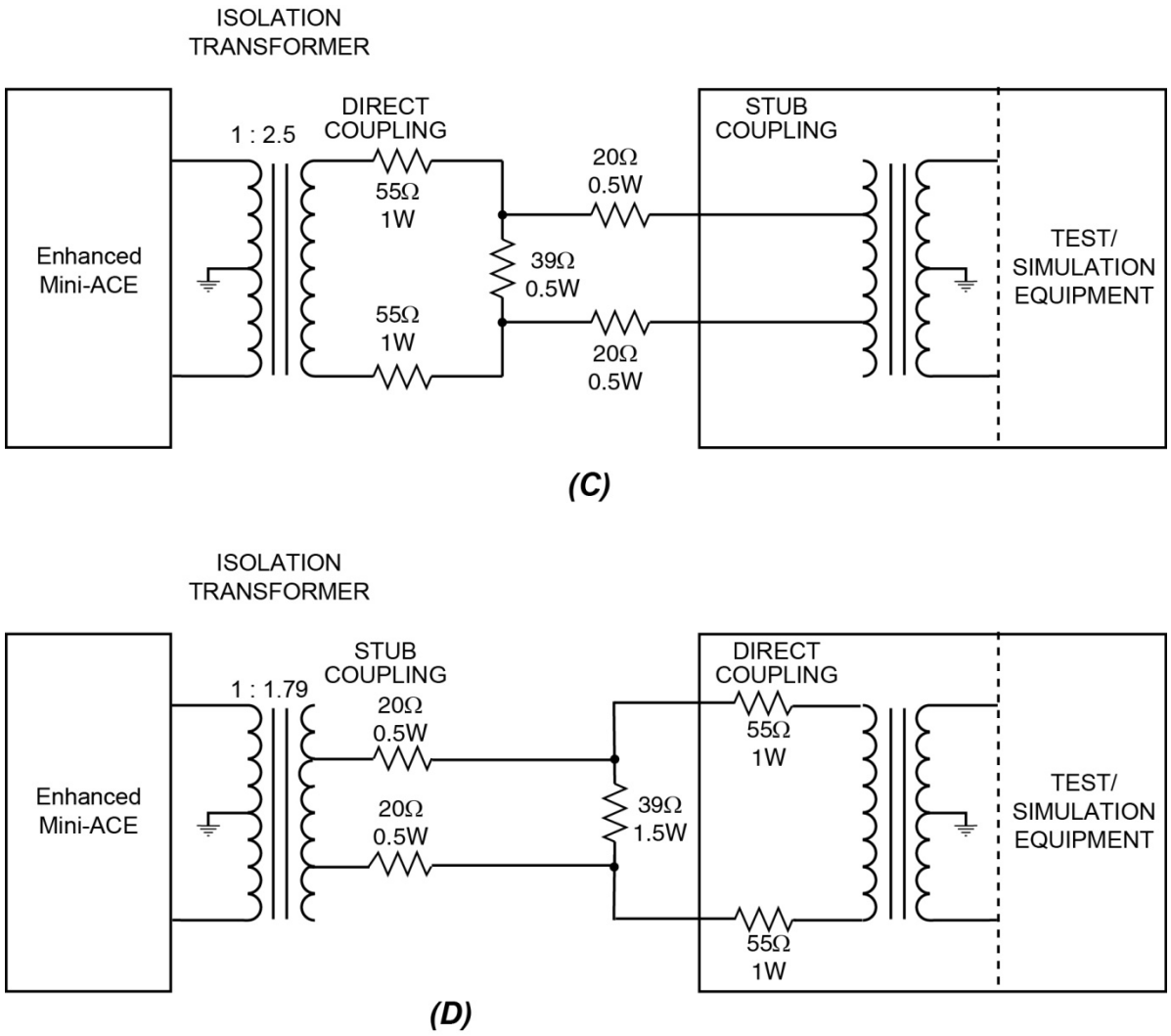



**Figure 14. Simulated Bus Interconnections**

*Figure 14 Note:*

*(C) Direct Coupled Enhanced Mini-ACE-to-Transformer Coupled Equipment*

*(D) Transformer Coupled Enhanced Mini-ACE-to-Transformer Coupled Equipment*

## 8.5 Logic Compatibility

The Enhanced Mini-ACE's logic signals provide compatibility with both TTL and CMOS type systems. In addition, the BU-61XX**3(4)** versions of the Enhanced Mini-ACE, which operates from a 3.3V logic supply, provides tolerance to external 5 volt logic. That is, the absolute maximum rating for “Logic Input Voltage” for versions of Enhanced Mini-ACE operating from either +5V or +3.3V logic power is 6.0V. To enable this, the Enhanced Mini-ACE’s input and I/O pad cells include clamping diodes to LOGIC GROUND, but do **not** include clamping diodes to $V_{CC}$-LOGIC.

The output and I/O signals are capable of sourcing and sinking up to 3.4 mA.

There are active “pull-up” type current sources from $V_{CC}$ on all of the inputs and I/O signals except for the clock input, CLK_IN. The value of these current sources is specified for a range of 50 to 350 µA.

There are Schmidt triggers on all digital input signals (including I/Os), including the clock input. All input signals (and the inputs on I/O signals) except for CLK_IN are TTL type, with $V_{IL}$= 0.7V max, $V_{IH}$= 2.1V min, and a minimum Schmidt hysteresis window of 0.4V. CLK_IN is a CMOS type input signal, with a $V_{IL}$ of 0.2•$V_{CC}$max, a $V_{IH}$ of 0.8•$V_{CC}$ min, and a minimum Schmidt hysteresis window of 1 volt.

# 9 HOST PROCESSOR AND MEMORY INTERFACE

The Enhanced Mini-ACE provides a great deal of flexibility for interfacing to a host processor and optional external memory. As shown in Figure 15, there are 14 control signals (13 for the Mini-ACE series terminals), 6 of which are dual purpose, for the processor/memory interface. Figure 15 through Figure 20 illustrate six of the configurations that may be used for interfacing an Enhanced Mini-ACE to a host processor bus. The various possible configurations serve to reduce to an absolute minimum the amount of "glue" logic required to interface to 8-, 16-, and 32_bit processor buses. In addition, features are included to facilitate interfacing to processors that do not have a "wait state" type of handshake acknowledgment. Finally, the Enhanced Mini-ACE supports a reliable interface to an external dual port RAM. This type of interface minimizes the portion of the available processor bandwidth required to access its internal 1553 RAM.

## 9.1 Address Mapping: Words vs. Bytes

It is important to note that with respect to the Enhanced Mini-ACE's address bus, A15 through A0, all address mapping is **word oriented**, rather than byte oriented. Although there are a few exceptions, inherent address mapping for most standard 8-, 16-, and 32-bit microprocessors is **byte oriented**. This difference in mapping convention must be taken into account when assigning pointer values and making CPU accesses to the Enhanced Mini-ACE's internal data structures (stack, lookup tables, data tables, etc.) in the Enhanced Mini-ACE's shared RAM address space. That is, in terms of the CPU's memory map, the address of these data structures, relative to the Enhanced Mini-ACE's base memory address, will be **double** the value of the pointer that is stored in the Enhanced Mini-ACE’s shared RAM.

For interfacing to most 16-bit microprocessors, the processor's A1 signal connects to the Enhanced Mini-ACE's A0 pin, processor A2 connects to the Enhanced Mini-ACE's A1 pin, etc. For interfacing to an 8-bit microprocessor, the processor A0 output connects to the Enhanced Mini-ACE's MSB/LSB input, the processor's A1 output connects to the Enhanced Mini-ACE's A0 pin, processor A2 connects to the Enhanced Mini-ACE's A1 pin, etc.

While the Enhanced Mini-ACE's internal shared RAM is intended primarily for the buffering of 1553 messages and related pointer data, it is important to noted that there is **no restriction** prohibiting the use of this RAM for general purpose program memory or "scratchpad" data memory.

## 9.2 16-Bit Buffered Mode

The 16-bit buffered mode (Figure 15) is the most common interface configuration used. It provides a direct, shared RAM interface to a 16-bit or 32-bit microprocessor.

In this mode, the Enhanced Mini-ACE's internal address and data buffers provide the necessary isolation between the host processor's address and data buses and the corresponding internal memory buses.

Depending on which version of Enhanced Mini-ACE, Mini-ACE Mark3, Micro-ACE(TE), or Total-ACE is used, there may be either 4K X 16 or RAM or 64X 16 of RAM. For a version with 4K X 16 of RAM, the upper address signals A15-A12 may be either connected to the host address bus, hardwired to logic ‘0’ or ‘1’, or left disconnected. For a version with 64K X 16 of RAM, all 16 address signals A15-A0 should be connected to the host address bus.

In the shared RAM configuration, the processor **always** has access to its own buses. That is, the Enhanced Mini-ACE will **never** request the use of the CPU buses. This provides the advantage of allowing the Enhanced Mini-ACE to access its buffer RAM while the CPU is able to **simultaneously** use its buses to access its memory or I/O. In this way, a shared RAM interface utilizes less of the CPU's bandwidth than does a DMA interface.

In the 16-bit buffered mode, note that TRANSPARENT/BUFFERED* is strapped to logic "0," while 16/8*-BIT is connected to logic "1." The input signal ADDR_LAT may be used to demultiplex the address bus. For examples, for some Intel microprocessors (i.e., Intel 80186), the CPU's ALE output should be connected to ADDR_LAT. If not used, ADDR_LAT should be connected to logic "1."The logic sense of the RD/WR* control input is selectable by means of the POLARITY_SEL input. For example, POLARITY_SEL should be connected to logic "1" to write on RD/WR* low for Motorola 680X0 processors; POLARITY_SEL should be connected to logic "0" to write on RD/WR* high for Intel i960 series processors. By strapping the input signal ZERO_WAIT* to logic "1," the Enhanced Mini-ACE may be interfaced to processors that have an acknowledge type of handshake input to accommodate hardware controlled wait states; most current processor chips have such an input. For this type of processor, the Enhanced Mini-ACE will assert its READYD* output low only after it has latched data to be written or has presented data to be read on D15-D0. In the nonzero wait mode, the host processor terminates the transfer cycle by releasing STRBD* high after the Enhanced Mini-ACE has asserted READYD* low.

By strapping ZERO_WAIT* to logic "0," it is possible to easily interface the Enhanced Mini-ACE to processors that **do not** have an acknowledge type of handshake input. An example of such a processor is Analog Device's ADSP2101 DSP chip. In this configuration, the processor can clear its strobe output (the Enhanced Mini-ACE's STRBD* input) before the access to the Enhanced Mini-ACE has been completed (before READYD* goes low).

In the buffered configuration, the host initiates an access to the Enhanced Mini-ACE's internal RAM or registers by asserting the signals SELECT*, STRBD*, MEM/REG*, and RD/WR*. SELECT* and MEM/REG* are generally the outputs of an address

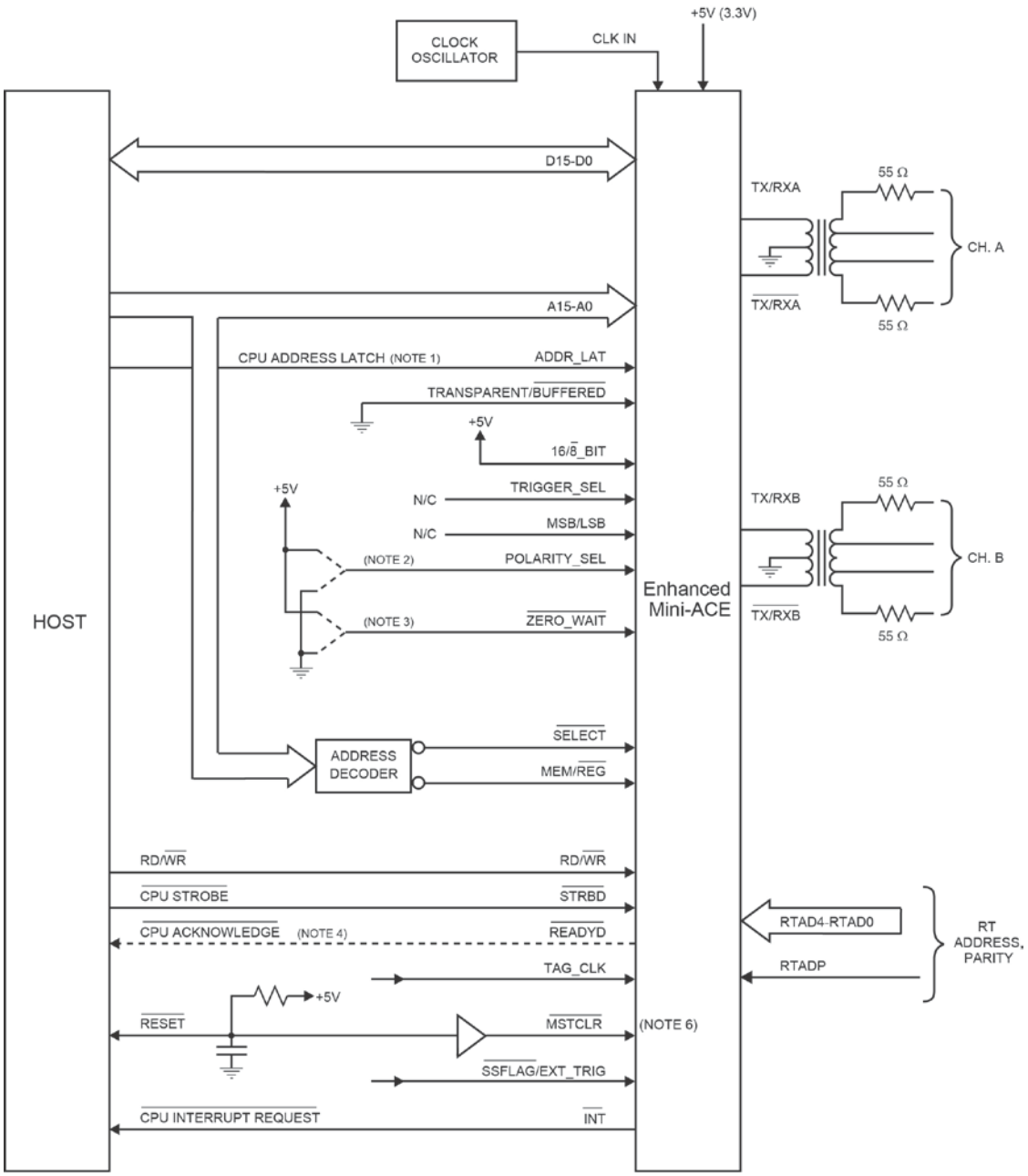
decoder. SELECT* must be asserted low to access the Enhanced Mini-ACE's RAM or registers. MEM/REG* must be presented high for memory access and low for register access. If POLARITY_SEL is logic "1," RD/WR* must be presented high to read and low to write; if POLARITY_SEL is logic "0," RD/WR* must be presented low to read and high to write. STRBD* is the main processor control input to the Enhanced Mini-ACE to control the length of an access cycle.

## 9.3 Zero Wait Configuration

Some microprocessors **do not** have a "strobe/acknowledge" type of handshake mechanism. In this case, the Enhanced Mini-ACE's "zero wait" interface configuration may be used by strapping ZERO_WAIT* to logic "0." In this mode, the CPU is able to release STRBD* high **before** the Enhanced Mini-ACE's READYD* output transitions from high to low and back to high. The low-to-high transition of READYD* indicates the end of the Enhanced Mini-ACE's internal transfer cycle. This mode takes advantage of the Enhanced Mini-ACE's internal address and data latches and added control logic and serves to minimize the amount of "glue" logic required.

In the 16-bit zero wait mode, the CPU writes a word by presenting the address and data for the word to be written on A15-A0 and D15-D0 respectively. To implement a single zero wait read operation, the host processor must perform **two** read accesses to the Enhanced Mini-ACE. During the first access, the address and transfer type indication (memory or register) of the location to be read must be asserted on A15-A0 and MEM/REG*, respectively. The data read on D15-D0 during this cycle **should be ignored ("thrown away")**. During the **second** read access, the Enhanced Mini-ACE presents the data corresponding to the address presented on the **first** access on D15-D0. If the CPU performs a multi-word read burst, the address for the **next** word should be presented on A15-A0 on the same cycle that data is read from D15-D0. That is, for a multi-word read transfer, the address presented should always be **one location ahead** of that of the data being read.

In the zero wait mode, STRBD* must be asserted low for a minimum of 20 ns. Reference Figure 35 **and** Figure 40. If STRBD* is not sampled low for two rising edges of the clock input CLK_IN, READYD* will go low within 40 ns after the rising edge of STRBD*. If STRBD* is sampled low for two rising edges of CLK_IN, READYD* will go low within 40 ns after the second rising clock edge. In either case, the Enhanced Mini-ACE's internal transfer cycle will not begin until after the second rising edge of CLK_IN **and** STRBD* is returned to logic "1." When the Enhanced Mini-ACE initiates the internal transfer, it asserts the output signal IOEN* low for four clock cycles. When the Enhanced Mini-ACE completes the internal transfer cycle, IOEN* clears high. One-half clock cycle after IOEN* goes high, the Enhanced Mini-ACE acknowledges completion of the transfer by re-asserting READYD* high. In the zero wait mode, the CPU can determine if the Enhanced Mini-ACE has completed its transfer cycle by polling the value of the READYD* output.




NOTES:

1. CPU ADDRESS LATCH SIGNAL PROVIDED BY PROCESSORS WITH MULTIPLEXED ADDRESS/DATA BUSES. FOR PROCESSORS WITH NON-MULTIPLEXED ADDRESS AND DATA BUSSES, ADDR_LAT SHOULD BE CONNECTED TO +5V.
2. IF POLARITY_SEL = "1", RD/$\overline{WR}$ IS HIGH TO READ, LOW TO WRITE.
   IF POLARITY_SEL = "0", RD/$\overline{WR}$ IS LOW TO READ, HIGH TO WRITE.
3. $\overline{ZERO\_WAIT}$ SHOULD BE STRAPPED TO LOGIC "1" FOR NON-ZERO WAIT INTERFACE AND TO LOGIC "0" FOR ZERO WAIT INTERFACE.
4. CPU ACKNOWLEDGE PROCESSOR INPUT ONLY FOR NON-ZERO WAIT TYPE OF INTERFACE.
6. THE RISE TIME FOR MSTCLR MUST BE LESS THAN 10µS IN ORDER TO ENSURE CORRECT INITIALIZATION OF THE ENHANCED MINI-ACE'S TRANSCEIVERS.

**Figure 15. Interconnection Diagram for 16-Bit Buffered Mode**

## 9.4 16-Bit Transparent Mode

Similar to the 16-bit buffered mode, the 16-bit transparent mode (Figure 16) supports a shared RAM interface to a host CPU. The transparent mode offers the advantage of allowing the buffer RAM size to be expanded to up to 64K words, using external RAM. For BU-61864(5), which contain 64K of internal RAM, the user may operate in transparent mode, but the combination of internal and external RAM must not exceed 64K words.

A disadvantage of the transparent mode is that external address and data buffers are required to isolate the processor buses from the Enhanced Mini-ACE buses. In the transparent mode, the host is able to access up to 64K of external RAM. Like the buffered mode, the host is able to use its data/address buses while the Enhanced Mini-ACE **simultaneously** accesses its internal or external shared RAM. Note that in the transparent configuration, external tri-state buffers are required to isolate the CPU's data/address buses from the Enhanced Mini-ACE's RAM buses. Table 1 summarizes the operation of the Enhanced Mini-ACE's tri-state address and data bus buffers for the 16-bit buffered and transparent modes.

**Table 1. Operation Of Address and Data Buffers For 16-Bit Interfaces**

| TRANSPARENT/BUFFERED MODE | CPU/1553 ACCESS | READ/WRITE | INT/EXT RAM (NOTE 1) | ADDRESS BUFFERS | DATA BUFFERS |
|---|---|---|---|---|---|
| Buffered | CPU | WRITE | INT | → | → |
| Buffered | CPU | READ | INT | → | ← |
| Buffered | 1553 | WRITE | INT | Hi-Z | Hi-Z |
| Buffered | 1553 | READ | INT | Hi-Z | HiZ |
| Transparent | CPU | WRITE | INT | → | → |
| Transparent | CPU | WRITE | EXT | → | Hi-Z |
| Transparent | CPU | READ | INT | → | → |
| Transparent | CPU | READ | EXT | → | Hi-Z |
| Transparent | 1553 | WRITE | INT | ← | ← |
| Transparent | 1553 | WRITE | EXT | ← | ← |
| Transparent | 1553 | READ | INT | ← | ← |
| Transparent | 1553 | READ | EXT | ← | ← |

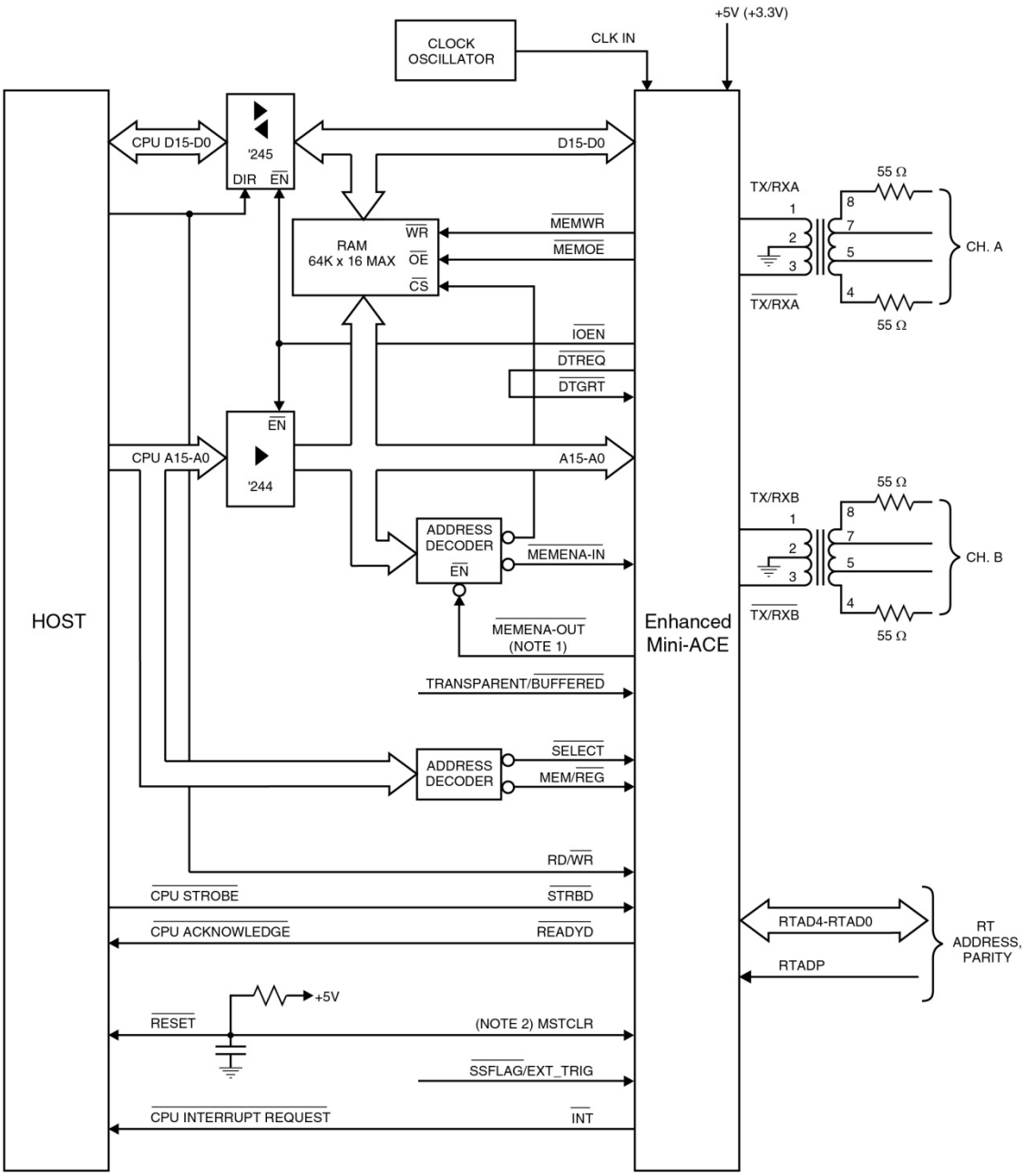
| Table 1. Operation Of Address and Data Buffers For 16-Bit Interfaces | | | | | |
|---|---|---|---|---|---|
| **TRANSPARENT/BUFFERED MODE** | **CPU/1553 ACCESS** | **READ/WRITE** | **INT/EXT RAM (NOTE 1)** | **ADDRESS BUFFERS** | **DATA BUFFERS** |

Table 1 Notes:

1. The Enhanced Mini-ACE distinguishes between internal (INT) and external (EXT) RAM by means of the input signal MEMENA-IN*. MEMENA-IN* is low for internal RAM access, high for external RAM access.
2. " $\longrightarrow$ " indicates buffers enabled in direction from external processor bus towards internal memory bus.
3. " $\longleftarrow$ " indicates buffers enabled in direction from internal memory bus towards external processor bus.
4. " Hi-Z" indicates buffers are in high impedance (tri-state) condition in both directions.

In the transparent mode (reference Figure 16), the memory control signals, MEMWR* and MEMENA-IN* must be connected to the respective control inputs of external RAM.

The external RAM $\overline{CS}$ signal (the external address decoder input) may be derived by logically OR'ing DTACK* and IOEN* {i.e., $\overline{CS}$ (low) = $\overline{DTACK}$ (low) or $\overline{IOEN}$ (low)}. If the Enhanced Mini-ACE's internal RAM is used, the address decoder output to select this RAM must be connected to the Enhanced Mini-ACE's MEMENA-IN* input. If the Enhanced Mini-ACE's internal RAM is not used, MEMENA-IN* must be connected to logic "1." As shown in the figure, the Enhanced Mini-ACE's IOEN* output should be connected to the tri-state enable inputs of the external address and data buffers. In the transparent mode, there is an extra clock cycle (four, instead of the three in buffered mode) between the falling edge of IOEN* and the falling edge of the acknowledge (handshake) output READYD*. This extra time is provided to accommodate the enable times and propagation delays associated with the external tri-state buffers.




NOTES:

1. MEMENA-OUT IS NOT AVAILABLE ON THE ENHANCED MINI-ACE SERIES TERMINALS BUT MAY BE REPLACED BY LOGICALLY OR'ING DTACK WITH IOEN.
2. THE RISE TIME FOR MSTCLR MUST BE LESS THAN 10 mS IN ORDER TO ENSURE CORRECT INITIALIZATION OF THE ENHANCED MINI-ACE'S TRANSCEIVERS.

**Figure 16. Interconnection Diagram for 16-Bit Transparent Mode (Shown with +5V Transceiver)**

## 9.5 16-Bit Dual Port RAM Interface

A modified version of the transparent mode involves the use of external dual port RAM, rather than conventional static RAM (Reference Figure 17). This allows the host to access RAM very quickly (the only limitation is essentially the RAM speed); the Enhanced Mini-ACE arbitration delays are eliminated in this instance. The worst case delay time occurs only during simultaneous access by the host CPU and the Enhanced Mini-ACE to the same memory address; in general, this will occur very rarely and the delay is limited to approximately 250 ns.

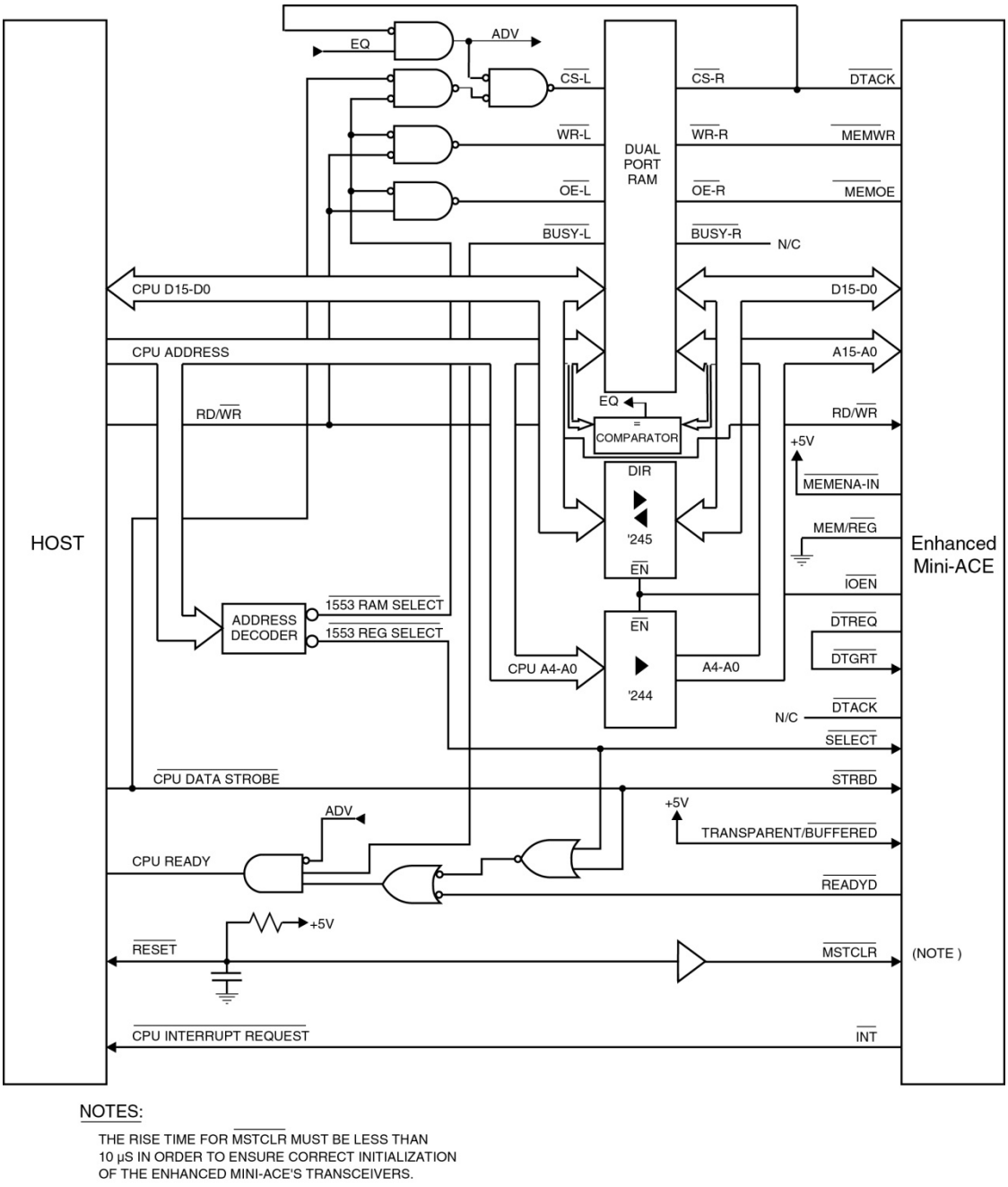
In the dual port RAM interface, one side of the RAM is accessed by the host CPU, while the other side is accessed by the Enhanced Mini-ACE's "1553" logic, by means of the memory control signals. Note that tri-state buffers are required on the address and data buses in order for the CPU to be able to access the Enhanced Mini-ACE's internal registers. Note that the Enhanced Mini-ACE input signal MEM/REG* is hardwired to logic "0," and SELECT* is connected to the address decoder output 1553 REG SELECT* to enable the register accesses. The signal CPU READY is asserted low (indicating "not ready") under either of two conditions:

When the dual port RAM's BUSY-L* output is asserted, indicating that the host tried to access the same location currently being accessed by the 1553 logic. Note that with most dual port RAM chips, a "Busy" condition will only result when both sides are performing an access to the same address location.

CPU READY will be asserted low during the time of a register access, prior to the completion of the Enhanced Mini-ACE's transfer cycle. That is, during the time that the SELECT* and STRBD* inputs are asserted low, but before READYD* is asserted low.

***IMPORTANT NOTE:***

*In this configuration, the dual port RAM's BUSY-R* output is not connected. As a result, it is important to note that the length of the pulse (low) presented on the dual port RAM's CS-L* input (derived from the CPU's CPU DATA STROBE* output) must be less than 100 ns. If CS-L* is asserted low for too long, it may cause the Enhanced Mini-ACE's "1553" logic to miss a transfer cycle. This could have the effect of corrupting a 1553 message (on an Enhanced Mini-ACE read cycle) or causing the Enhanced Mini-ACE to not store a word in the dual port RAM (on an Enhanced Mini-ACE write cycle).*




NOTES:

THE RISE TIME FOR $\overline{\text{MSTCLR}}$ MUST BE LESS THAN 10 µS IN ORDER TO ENSURE CORRECT INITIALIZATION OF THE ENHANCED MINI-ACE'S TRANSCEIVERS.

**Figure 17. Interconnection Diagram for 16-Bit Dual Port RAM Mode**

## 9.6 16-Bit DMA Mode

Figure 18 illustrates the connections for the 16-bit Direct Memory Access (DMA) mode. In this configuration, use of the address and data buses is arbitrated by the host processor, rather than by the Enhanced Mini-ACE. The arbitration involves the three DMA control signals Request (DTREQ*), Grant (DTGRT*), and Acknowledge (DTACK*). The DMA interface allows the Enhanced Mini-ACE to interface to large amounts of system RAM. For system address spaces greater than 64K words, it is necessary for the host processor to provide a page register for the upper address bits (above A15) when the Enhanced Mini-ACE accesses the RAM (DTACK* is asserted low).

The internal RAM is accessible through the standard Enhanced Mini-ACE interface (SELECT*, STRBD*, READYD*, etc). The host CPU may access external RAM by means of the Enhanced Mini-ACE's arbitration logic and output control signals, as illustrated in Figure 18. Alternatively, control of the RAM may be multiplexed between the host processor and the Enhanced Mini-ACE, as shown in Figure 19. The latter requires the use of external logic, but allows the processor to access the RAM directly at the full access speed of the RAM, rather than waiting for the Enhanced Mini-ACE handshake acknowledge output (READYD*).

In the DMA configuration, the host processor controls access to the address and data buses by means of a request/grant/acknowledge handshake. Refer to Figure 18. When the 1553 terminal needs to transfer a word or block of words to RAM, it requests use of the buses from the host CPU by asserting its DTREQ* (Data Transfer Request) output low. When the host CPU completes its current instruction cycle, it relinquishes use of the buses by asserting DTGRT* (Data Transfer Grant) low. When the Enhanced Mini-ACE samples DTGRT* low on a rising edge of CLK_IN, it asserts DTACK* (Data Transfer Acknowledge) low to indicate that the Enhanced Mini-ACE has accepted control of the buses.

For the configuration in Figure 18, the ENABLE input to the address decoder is formulated by logically OR'ing DTACK* and IOEN* as shown, that is, ENABLE* (low) = DTACK* (low) or IOEN* (low). For the configuration in Figure 19, DTACK* ( **not** gated with IOEN*) is used to enable the Enhanced Mini-ACE's external RAM access. In either case, the resulting signal can be connected to an external address decoder to derive MEMENA-IN* for internal RAM access, or CS* input(s) to external RAM. DTACK* will remain asserted for four clock cycles (200 ns at 20 MHz, 250 ns at 16 MHz, 333 ns at 12 MHz, 400 ns at 10 MHz) to complete a single-word transfer cycle. For a read cycle, the Enhanced Mini-ACE output MEMOE* (Memory Output Enable) is asserted low; for a write cycle, MEMWR* (Memory Write) is asserted low. For a multiword transfer cycle during a Start-of-Message (SOM), End-of-Message (EOM), or BC Retry sequences, DTACK* will remain asserted for an additional [4•(number of words)] clock cycles; either MEMOE* or MEMWR* will be asserted for each word cycle.

In the DMA configuration, the host has two mechanisms for accessing external RAM. As shown in Figure 18, the host can access the RAM by means of the Enhanced Mini-ACE's control signals SELECT*, STRBD*, MEM/REG*. RD/WR*, READYD*, MEMWR* and MEMOE*. While this requires no external control logic, it does entail about 250 ns of processor bandwidth to complete an access. This time allows the Enhanced Mini-ACE to arbitrate between 1553 and CPU accesses, and between internal and external RAM access and to enable internal tri-state buffers. Alternatively, in the configuration of Figure 19, the host processor's access time to read or write the external RAM is reduced by means of the extra logic gates shown. The only limitations are the CPU's strobe width, the access time of the RAM, and the gate delays. Note that in this configuration, the host must still activate the signals SELECT*, STRBD*, etc. in order to access the Enhanced Mini-ACE's internal registers.

## 9.7 Handshake Timeout

In the DMA or transparent modes, the host processor must allow the Enhanced Mini-ACE's 1553 logic to gain access to the system address and data buses to read and write memory. In order to ensure that words are transferred to/from RAM when required during the processing of 1553 messages, the CPU must provide the Enhanced Mini-ACE access to the system buses within the allotted time. The allotted time is 10.5 µs when using a 20 MHz clock input, 10 µs when using a 16 MHz clock input, 9 µs when using a 12 MHz clock, and 8.5 µs when using a 10 MHz clock input. If the CPU fails to provide access within the allotted time, the Enhanced Mini-ACE will be unable to transfer a word or burst of words.

A Handshake Timeout can occur on Data Word Transfers in all modes, and during Start-of-Message (SOM) sequences in RT or Message Monitor modes.

Note that a Handshake Timeout condition will **not** occur during the following transfer sequences: BC Start-of-Message (SOM), End-of-Message (EOM), and Retry sequences; Word Monitor start sequence; RT End-of-Message (EOM) sequence; and Message Monitor End-of-Message (EOM) sequence.

The handshake timer will expire in either of two circumstances:

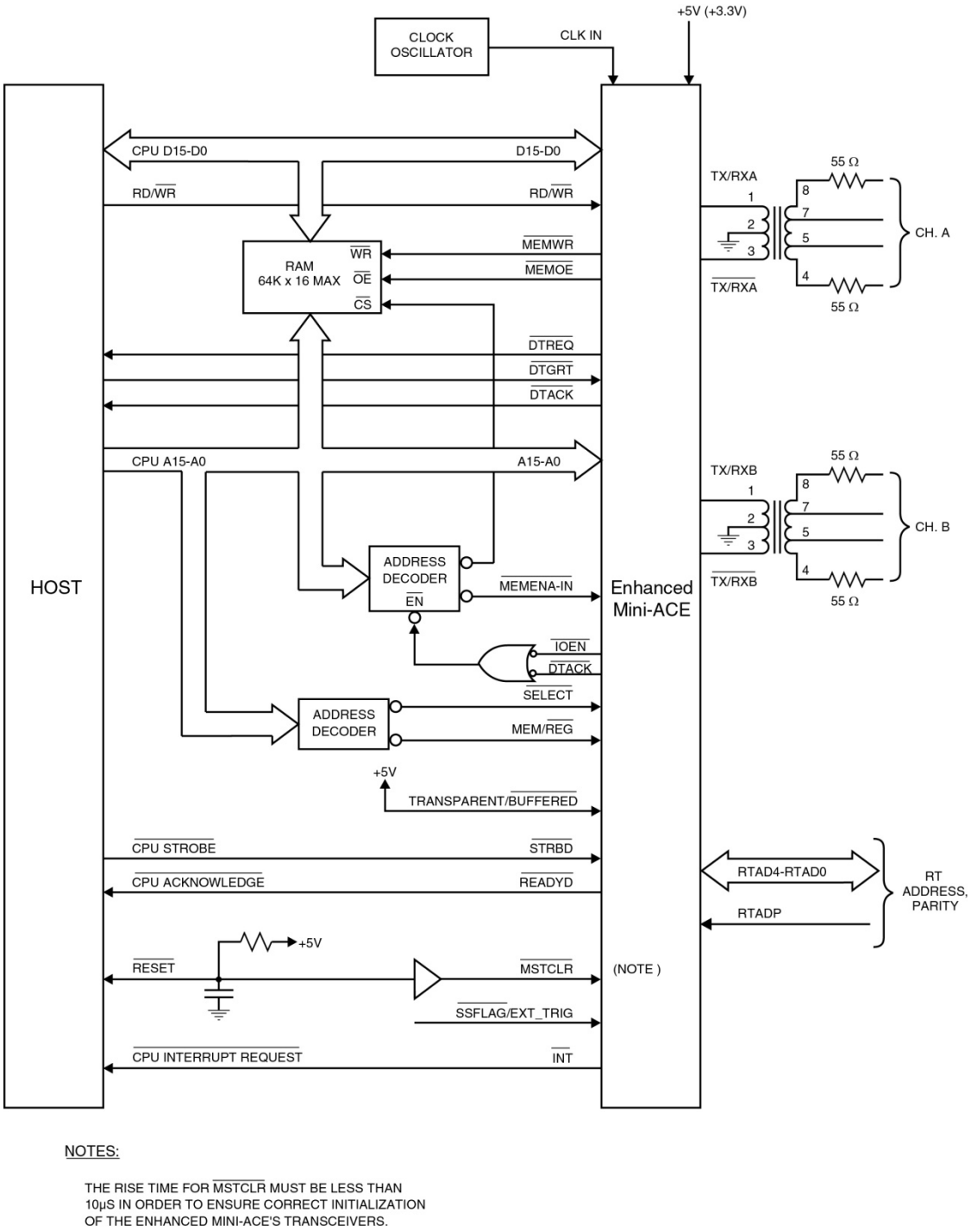
(1) In the DMA configuration, if the host processor did not assert DTGRT* (low) within the allotted time after the Enhanced Mini-ACE asserted its DTREQ* output (low); or

(2) In transparent mode (includes the DMA configuration), if the processor kept STRBD* asserted (low) for longer than the allotted time after the Enhanced Mini-ACE asserted its READYD* acknowledge output low.

The effects of a handshake timeout are as follows:

- In BC, RT, or Selective Monitor modes, the processing of the current message is immediately terminated. In BC or RT modes, if the Enhanced Mini-ACE is transmitting on the 1553 bus in BC or RT modes, the transmission is terminated. The current received Data Word and any subsequent Data Words will not be stored to the Enhanced Mini-ACE shared RAM.
- In RT mode, the Enhanced Mini-ACE **will continue** to monitor received data words for error conditions (encoding, parity, etc.) after a Handshake Timeout condition has occurred. Any detected errors will be flagged in the Block Status Word, Interrupt Status Register, and RT BIT Word Register.
- In BC mode, the processing of a frame of messages is terminated and not re-started.
- In Word Monitor mode, the Enhanced Mini-ACE will not store the current "Word/ID Word" pair, but will continue to store subsequent word pairs.
- In BC, RT, or Selective Monitor modes, the EOM and ERROR FLAG bits will be set in the Block Status Word for the current message.
- If enabled, a HANDSHAKE FAILURE interrupt request will be issued, and the HANDSHAKE FAILURE bit will be set to logic "1" in the Interrupt Status register.
- In RT mode, the HANDSHAKE FAILURE bit will be set in the RT Built-In-Test (BIT) Word.
- If a Handshake Failure occurs during an RT Start-of-Message (SOM) transfer sequence, the entire message will be ignored.

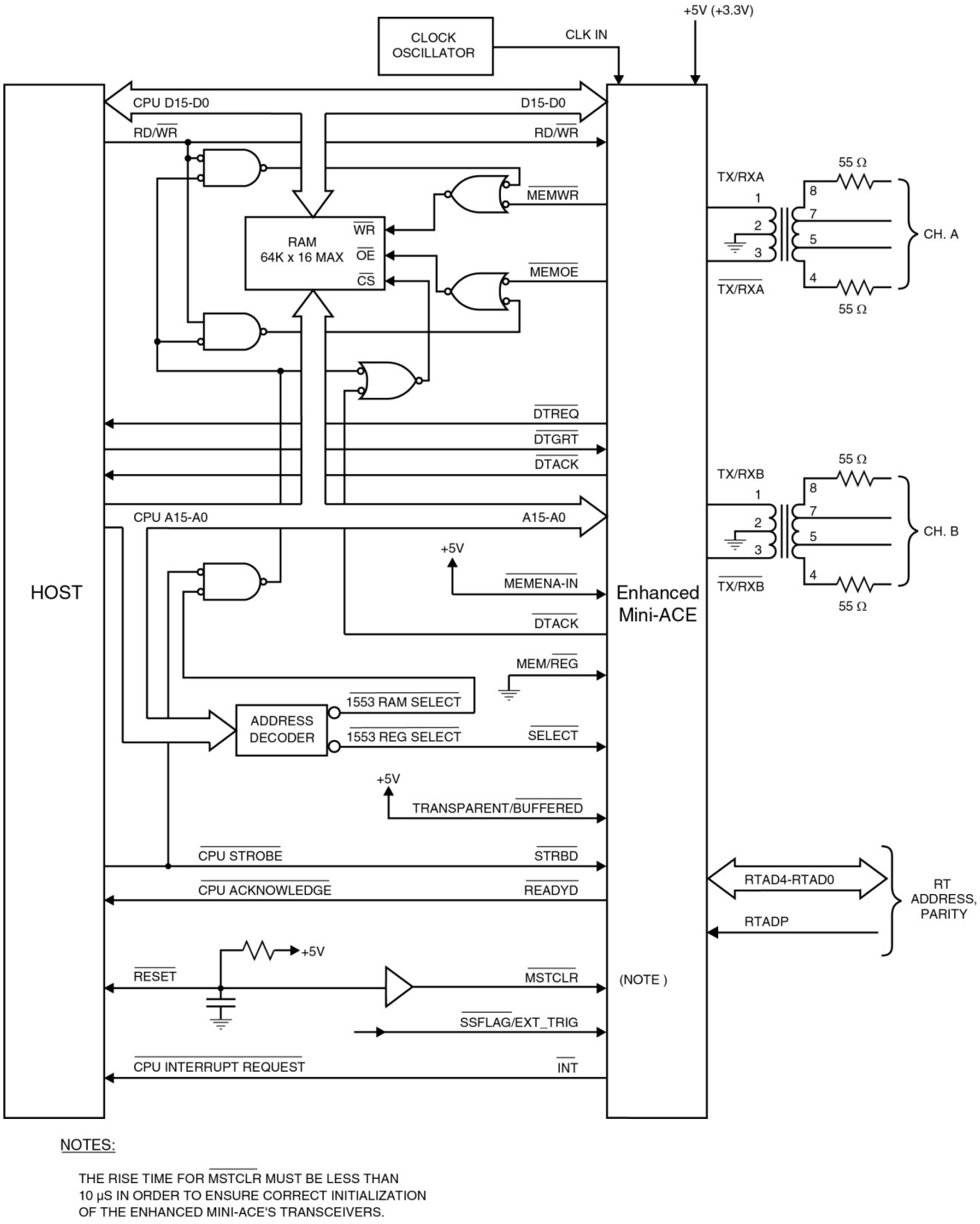
***Note:*** *A handshake timeout cannot occur in the buffered mode configuration.*




NOTES:

THE RISE TIME FOR $\overline{\text{MSTCLR}}$ MUST BE LESS THAN 10μS IN ORDER TO ENSURE CORRECT INITIALIZATION OF THE ENHANCED MINI-ACE'S TRANSCEIVERS.

**Figure 18. Interconnection Diagram for 16-Bit DMA Mode (Shown with +5V Transceiver)**




NOTES:

THE RISE TIME FOR $\overline{\text{MSTCLR}}$ MUST BE LESS THAN 10 µS IN ORDER TO ENSURE CORRECT INITIALIZATION OF THE ENHANCED MINI-ACE'S TRANSCEIVERS.

**Figure 19. 16-Bit DMA with External Logic to Reduce CPU Access Time (Shown with +5V Transceiver)**

## 9.8 8-Bit Buffered Mode

Figure 20 illustrates the 8-bit buffered mode. This interface allows a direct connection to 8-bit microprocessors and 8-bit micro controllers. As in the 16-bit buffered configuration, the buffered RAM is limited to the Enhanced Mini-ACE's internal RAM (4K words on BU-61743(5)/61843(5), and 64K words on BU-61864(5)). In the 8-bit mode, the host CPU accesses the Enhanced Mini-ACE's internal registers and RAM by means of a pair of 8-bit registers embedded in the Enhanced Mini-ACE interface.

The 8-bit interface may be further configured by means of three strappable inputs: ZERO_WAIT*, POLARITY_SEL, and TRIGGER_SEL.In the 8-bit buffered mode, the input 16/8*-BIT must be strapped to logic "0" and the CPU's data bus must be connected to both D15-D8 and D7-D0. The LSB of the processor address bus (processor A0) must be connected to the input MSB/LSB for upper/lower byte selection. The processor's A1 output connects to the Enhanced Mini-ACE's A0 input, processor A2 to Enhanced Mini-ACE A1, etc.

The programmable inputs POLARITY_SEL and TRIGGER_SEL allow the Enhanced Mini-ACE terminals to accommodate the different byte ordering conventions (big/little endian) and "A0" logic sense implemented by different 8-bit processor families. For example, a Motorola 6809 writes upper data first to the lower (usually even) address location, followed by lower data to the next highest (usually odd numbered) location. By contrast, an Intel 8088 will first write lower data to the lower (usually even numbered) address location and then write the upper byte to the next highest (usually odd numbered) address. If the POLARITY_SEL input signal is connected to logic "1" in the 8-bit nonzero wait mode, then the MSB/LSB input signal will select the most significant byte when low and the least significant byte when high.

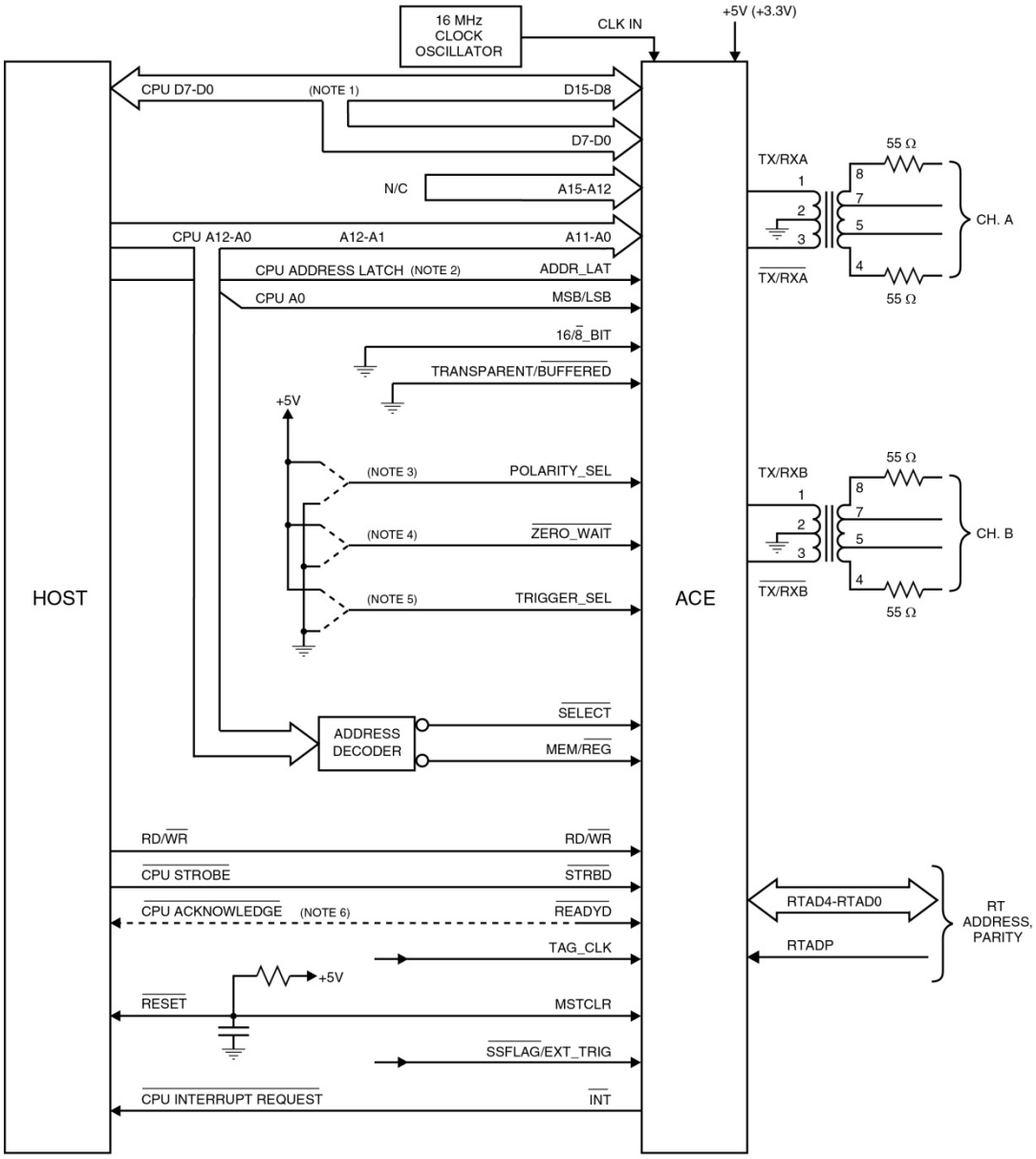
When the POLARITY_SEL input signal is connected to logic "0," the MSB/LSB input signal will select the least significant byte when low and the most significant byte when high. Therefore, a Motorola 6809 would require that the POLARITY_SEL input be connected to logic "1," while an Intel 8088 would require a logic "0" on POLARITY_SEL.The TRIGGER_SEL input will control the order in which bytes are transferred to or from the Enhanced Mini-ACE. This is important because the Enhanced Mini-ACE performs 16-bit internal transfers.

For the case of a write operation, the host processor will write 8 bits of a 16-bit word to the Enhanced Mini-ACE. The Enhanced Mini-ACE will store this byte in an internal data latch. The host processor will then present the other 8 bits of the word. At this point in time, the Enhanced Mini-ACE will "trigger" an internal 16-bit transfer, with half of the data being presented from the CPU data bus, while the other half (written during the previous CPU cycle) is presented to the Enhanced Mini-ACE's RAM or register from the internal latch.

When operating in the nonzero wait mode, a logic "0" on the TRIGGER_SEL input will configure the Enhanced Mini-ACE to trigger an internal 16-bit transfer on the least significant byte transfer for a read access, and by the most significant byte transfer for a write access. A logic "1" on the TRIGGER_SEL input will configure the Enhanced Mini-ACE to trigger an internal 16-bit transfer on the most significant byte transfer for a read access, and by the least significant byte transfer for a write access. Therefore, a 6809 interface would require that the TRIGGER_SEL input be connected to logic "1," while an 8088 interface requires a logic "0."The operation of the ACE's 8-bit nonzero wait buffered mode is essentially the same as the 16-bit mode, with the following exceptions:

For a write cycle, the first byte is written to an internal latch; the second byte is written directly to a register or RAM location. When the second byte is written to register or RAM, the first byte is simultaneously transferred from the buffer register to register or RAM. The address (A15-A0 and MEM/REG*) is "don't care" during the first byte transfer, but must be valid during the second byte transfer. The handshake output READYD* is asserted low after both byte transfers.

For a read cycle in the "nonzero wait" mode, the first byte is read directly from register or RAM. While the first byte is read by the CP, the second byte is being stored in an internal latch. The processor may then read the second byte from the buffer. The address (A15-A0 and MEM/REG*) must be valid during the first byte read, but is "don't care" during the second byte read. The handshake output READYD* is asserted low after both byte transfers.




NOTES:

1. CPU D7-D0 CONNECTS TO BOTH D15-D8 AND D7-D0.
2. CPU ADDRESS LATCH SIGNAL PROVIDED BY PROCESSORS WITH MULTIPLEXED ADDRESS/DATA BUFFERS.
3. IF POLARITY_SEL = "1", THEN MSB/LSB SELECTS THE MOST SIGNIFICANT BYTE WHEN LOW, AND THE LEAST SIGNIFICANT BYTE WHEN HIGH.
   IF POLARITY_SEL = "0", THEN MSB/LSB SELECTS THE LEAST SIGNIFICANT BYTE WHEN LOW, AND THE MOST SIGNIFICANT BYTE WHEN HIGH.
4. ZERO WAIT SHOULD BE STRAPPED TO LOGIC "1" FOR NON-ZERO WAIT INTERFACE AND TO LOGIC "0" FOR ZERO WAIT INTERFACE.
5. OPERATION OF TRIGGER_SELECT INPUT IS AS FOLLOWS:
   FOR NON-ZERO WAIT INTERFACE (ZERO WAIT = "1"):
   IF TRIGGER_SEL = "1", THEN INTERNAL 16-BIT TRANSFERS ARE TRIGGERED BY THE MOST SIGNIFICANT BYTE TRANSFER READ ACCESSES AND BY THE LEAST SIGNIFICANT BYTE TRANSFER FOR WRITE ACCESSES.
   IF TRIGGER_SEL = "0", THEN INTERNAL 16-BIT TRANSFERS ARE TRIGGERED BY THE LEAST SIGNIFICANT BYTE TRANSFER FOR READ ACESSES AND BY THE MOST SIGNIFICANT BYT TRANSFER FOR WRITE ACCESSES.
   FOR ZERO WAIT INTERFACE (ZERO WAIT = "0"):
   IF TRIGGER_SEL = "1", THEN INTERNAL 16-BIT TRANSFERS ARE TRIGGERED BY THE LEAST SIGNIFICANT BYTE TRANSFER, FOR BOTH READ AND WRITE ACCESSES.
   IF TRIGGER_SEL = "0", THEN INTERNAL 16-BIT TRANSFERS ARE TRIGGERED BY THE MOST SIGNIFICANT BYTE TRANSFER, FOR BOTH READ AND WRITE ACCESES.
6. CPU ACKNOWLEDGE PROCESSOR INPUT ONLY FOR NON-ZERO WAIT TYPE OF INTERFACE.

**Figure 20. Interconnection Diagram for 8-Bit Buffered Mode (Shown with +5V Transceivers)**

21Table 2 provides a summary of the possible transfer sequences in the 8-bit nonzero wait mode.

**Table 2. Summary of 8-Bit Operation (Nonzero Wait Mode)**

| ZERO WAIT* | TRIGGER SELECT | POLARITYSELECT | RD/WR* | FIRST BYTE TRANSFER | SECOND BYTE TRANSFER |
|---|---|---|---|---|---|
| 1 | 1 | 1 | 1 | MSB/LSB = 0;<br>Valid A15-A0, MEM/REG*;<br>CPU ⟵ RAM 15-8;<br>Buffer 7-0 ⟵ RAM 7-0 | MSB/LSB = 1;<br>A15-A0, MEM/REG* = "Don't Care;<br>"CPU ⟵ Buffer 7-0 |
| 1 | 1 | 1 | 0 | MSB/LSB = 0;<br>A15-A0, MEM/REG* = "Don't Care;<br>"CPU ⟶ Buffer 15-8 | MSB/LSB = 1;<br>Valid A15-A0, MEM/REG*;<br>Buffer 15-8 ⟶ RAM 15-8;<br>CPU ⟶ RAM 7-0 |
| 1 | 1 | 0 | 1 | MSB/LSB = 1;<br>Valid A15-A0, MEM/REG*;<br>CPU ⟵ RAM 15-8;<br>Buffer 7-0 ⟵ RAM 7-0 | MSB/LSB = 0;<br>A15-A0, MEM/REG* = "Don't Care;<br>"CPU ⟵ Buffer 7-0 |
| 1 | 1 | 0 | 0 | MSB/LSB = 1;<br>A15-A0, MEM/REG* = "Don't Care;<br>"CPU ⟶ Buffer 15-8 | MSB/LSB = 0;<br>Valid A15-A0, MEM/REG*;<br>Buffer 15-8 ⟶ RAM 15-8;<br>CPU ⟶ RAM 7-0 |
| 1 | 0 | 1 | 1 | MSB/LSB = 1;<br>Valid A15-A0, MEM/REG*;<br>CPU ⟵ RAM 7-0;<br>Buffer 15-8 ⟵ RAM 15-8 | MSB/LSB = 0;<br>A15-A0, MEM/REG* = "Don't Care;<br>"CPU ⟵ Buffer 15-8 |
| 1 | 0 | 1 | 0 | MSB/LSB = 1;<br>A15-A0, MEM/REG* = "Don't Care;<br>"CPU ⟶ Buffer 7-0 | MSB/LSB = 0;<br>Valid A15-A0, MEM/REG*;<br>Buffer 7-0 ⟶ RAM 7-0;<br>CPU ⟶ RAM 15-8 |
| 1 | 0 | 0 | 1 | MSB/LSB = 0;<br>Valid A15-A0, MEM/REG*;<br>CPU ⟵ RAM 7-0;<br>Buffer 15-8 ⟵ RAM 15-8 | MSB/LSB = 1;<br>A15-A0, MEM/REG* = "Don't Care;<br>"CPU ⟵ Buffer 15-8 |
| 1 | 0 | 0 | 0 | MSB/LSB = 0;<br>A15-A0, MEM/REG* = "Don't Care;<br>"CPU ⟶ Buffer 7-0 | MSB/LSB = 1;<br>Valid A15-A0, MEM/REG*;<br>Buffer 7-0 ⟶ RAM 7-0;<br>CPU ⟶ RAM 15-8 |

## 9.9 8-Bit Zero Wait Mode

By connecting ZERO_WAIT* to logic "0" in the 8-bit buffered mode, the Enhanced Mini-ACE may be interfaced with minimal "glue" logic to micro controllers, such as the Intel 8051 series, that do not have an "acknowledge" type of handshake input. When performing a write transfer in the zero wait mode, the Enhanced Mini-ACE will begin the cycle in the same manner as the nonzero wait mode. The difference is that the Enhanced Mini-ACE will latch the data, address and control lines internally if the host processor terminates the transfer cycle (brings STRBD* high) before the Enhanced Mini-ACE has responded with the handshake acknowledge output (high-to-low transition of READYD*). The only constraint is that the host processor must not begin a new transfer to the Enhanced Mini-ACE until the Enhanced Mini-ACE has completed the previous internal transfer.

The operation of the READYD* output signal in the nonzero wait mode is to indicate when a transfer is complete. In the zero wait mode, however, READYD* indicates that a transfer is active. READYD* is normally high and will go low upon the start of the internal transfer, and will remain low until the internal transfer is complete. After the internal RAM or register transfer has been completed, $\overline{\text{READYD}}$ will revert to its high state.

The operation of the TRIGGER_SEL input in the 8-bit zero wait mode is similar to its operation in the 8-bit nonzero wait mode. The Enhanced Mini-ACE must be configured to trigger the internal transfer off of the proper byte transfer. A write operation is the same for both zero wait and nonzero wait, in that the Enhanced Mini-ACE will trigger the internal write when the second of two byte transfers is performed. An internal read transfer will be triggered after the host processor reads the second byte of a 2-byte read. This is in contrast to a nonzero wait read, in which the internal read is triggered on the first of a two byte access.

The write cycle for the 8-bit "zero wait" mode (ZERO_WAIT* = logic "0") is identical to that for the 8-bit "nonzero wait" mode, except for the operation of the READYD* output. In the "zero wait" mode, READYD* stays high during the entire first byte (nontriggering) transfer cycle. During the second byte transfer time (triggering transfer), READYD* stays high until STRBD* is either cleared high (after a minimum pulse width of 20 ns), or has been sampled low for two rising edges of the CLK_IN input. READYD* then goes low (indicating "not ready") and remains high until the internal 16-bit transfer of data between the ACE's internal latches and internal RAM or register has been completed.

When using the 8-bit (or 16-bit) "zero wait" mode, it is assumed there is no "acknowledge" input on the processor to connect the Enhanced Mini-ACE's READYD* output to. However, the CPU may still poll the READYD* output. **It should not initiate another transfer cycle to the ACE while READYD* is logic "0."** Alternatively, the CPU may insert software wait states between successive accesses

to the Enhanced Mini-ACE. The required wait time varies with the mode of operation and frequency of the clock input. Refer to Table 3 to determine the required minimum wait time.

**Table 3. Minimum Required Delay Times**

| MODE | @ 20 MHz | @ 16 MHz | @ 12 MHz | @ 10 MHz |
|---|---|---|---|---|
| Bus Controller (BC) | 1.9 µs | 2.4 µs | 3.1 µs | 3.8 µs |
| Remote Terminal(RT) | 3.9 µs | 4.9 µs | 6.4 µs | 7.7 µs |
| Word Monitor | 900 ns | 1.1 µs | 1.5 µs | 1.8 µs |
| Selective Message Monitor | 2.1 µs | 2.31 µs | 3.5 µs | 4.2 µs |

For the read cycle for the 8-bit "zero wait" mode: It is important to realize that for a given read cycle, the internal RAM address (including the value of MEM/REG*) is the address that was presented on the Enhanced Mini-ACE's address inputs (A15-A0) during the **second** byte read of the **previous** (word) READ cycle. Therefore, in order to read a word (two bytes) in this mode, the first byte read access is a "dummy cycle" as far as the data bus (D15-8, D7-D0) is concerned; however, the address (A15-A0 and MEM/REG*) for the first word to be read must be presented at this time.

That is, in order to initiate a series of word accesses, the CPU must first perform a "second byte transfer" read access (illustrated in Table 4) with the valid address and value of MEM/REG* for the first word presented. The data read during this transfer should be ignored ("thrown away"). The CPU should then perform the "first byte" and "second byte" read cycles to acquire the data from the address (including MEM/REG*) that was previously presented. As far as the Enhanced Mini-ACE is concerned, the address presented on A15-A0 and MEM/REG* is "Don't Care" during the "first byte" transfer. On the second byte transfer, the valid address for the **next** word to be read may be presented on A15-A0 and MEM/REG*. The CPU may then read the subsequent word by performing a first byte read, followed by a second byte read, etc.

Note that the READYD* output will remain high through the end of the first "zero wait" read cycle, but will transition to logic "0" during (or possibly after) the STRBD* pulse for the second byte read cycle. During the time that READYD* is logic "0", the RAM data for the address presented is transferred from the Enhanced Mini-ACE's internal RAM or register to the two internal 8-bit latches. When READYD* is re-asserted to logic "1" (2.6 µs max later with a 16 MHz clock), the CPU may then proceed to read the first byte, then the second byte.

Table 4 summarizes the possible transfer sequences for the 8-bit zero wait mode.

| Table 4. Summary of 8-Bit Operation (Zero Wait Mode) | | | | | |
|---|---|---|---|---|---|
| **ZEROWAIT** | **TRIGGER SELECT** | **POLARITY SELECT** | **RD/WR** | **FIRST BYTE TRANSFER** | **SECOND BYTE TRANSFER** |
| 0 | 1 | 1 | 1 | MSB/LSB = 0;<br>A15-A0, MEM/REG* = "Don't Care;<br>"CPU ⟵ Buffer 15-8<br>(Last A15-A0,MEM/REG*) | MSB/LSB = 1;<br>A15-A0 and MEM/REG* Valid for Next Word;<br>CPU ⟵ Buffer 7-0 (Last A15-A0, MEM/REG*);then,<br>Buffer 15-0 ⟵ RAM 15-0 |
| 0 | 1 | 1 | 0 | MSB/LSB = 0;A15-A0, MEM/REG* = "Don't Care;<br>"CPU ⟶ Buffer 15-8 | MSB/LSB = 1;<br>Valid A15-A0, MEM/REG*;<br>CPU ⟶ Buffer 7-0;then,<br>Buffer ⟶ RAM 15-0 |
| 0 | 1 | 0 | 1 | MSB/LSB = 1;<br>A15-A0, MEM/REG* = "Don't Care;<br>"CPU ⟵ Buffer 15-8 (Last A15-A0,MEM/REG*) | MSB/LSB = 0;<br>A15-A0 and MEM/REG* Valid for Next Word;<br>CPU ⟵ Buffer 7-0 (Last A15-A0, MEM/REG*);then,<br>Buffer 15-0 ⟵ RAM 15-0 |
| 0 | 1 | 0 | 0 | MSB/LSB = 1;<br>A15-A0, MEM/REG* = "Don't Care;<br>"CPU ⟶ Buffer 15-8 | MSB/LSB = 0;<br>Valid A15-A0, MEM/REG*;<br>CPU ⟶ Buffer 7-0;then,<br>Buffer ⟶ RAM 15-0 |
| 0 | 0 | 1 | 1 | MSB/LSB = 1;<br>A15-A0, MEM/REG* = "Don't Care;<br>"CPU ⟵ Buffer 7-0(Last A15-A0, MEM/REG*) | MSB/LSB = 0;<br>A15-A0 and MEM/REG* Valid for Next Word;<br>CPU ⟵ Buffer 15-8 (Last A15-A0, MEM/REG*);then,<br>Buffer 15-0 ⟵ RAM 15-0 |
| 0 | 0 | 1 | 0 | MSB/LSB = 1;<br>A15-A0, MEM/REG* = "Don't Care;<br>"CPU ⟶ Buffer 7-0 | MSB/LSB = 0;<br>Valid A15-A0, MEM/REG*;<br>CPU ⟶ Buffer 15-8;then,<br>Buffer ⟶ RAM 15-0 |
| 0 | 0 | 0 | 1 | MSB/LSB = 0;<br>A15-A0, MEM/REG* = "Don't Care;<br>"CPU ⟵ Buffer 7-0<br>(Last A15-A0,MEM/REG*) | MSB/LSB = 1;<br>A15-A0 and MEM/REG* Valid for Next Word;<br>CPU ⟵ Buffer 15-8 (Last A15-A0, MEM/REG*);then,<br>Buffer 15-0 ⟵ RAM 15-0 |

| Table 4. Summary of 8-Bit Operation (Zero Wait Mode) | | | | | |
|---|---|---|---|---|---|
| **ZEROWAIT** | **TRIGGER SELECT** | **POLARITY SELECT** | **RD/WR** | **FIRST BYTE TRANSFER** | **SECOND BYTE TRANSFER** |
| 0 | 0 | 0 | 0 | MSB/LSB = 0;<br>A15-A0, MEM/REG* = "Don't Care;<br>"CPU ⟶ Buffer 7-0 | MSB/LSB = 1;<br>Valid A15-A0, MEM/REG*;<br>CPU ⟶ Buffer 15-8;then,<br>Buffer ⟶ RAM 15-0 |

## 9.10 Control Logic

"Glue" control logic is generally required to provide conditioning between the processor's control signals and the Enhanced Mini-ACE's control signals. In many systems, this circuitry may be implemented into a programmable logic device (EPLD/FPGA). It is often possible to combine the address decoding and control logic glue functions in the same EPLD/FPGA device. One typical function of the glue logic is to formulate the Enhanced Mini-ACE's STRBD* input. This is a simple logical OR function for many processors that provides separate WRITE* and READ* strobe outputs. In addition, gating, inverting, and/or tri-state control logic is often needed between the Enhanced Mini-ACE's READYD* output and the processor's acknowledge input.

## 9.11 Interrupt Logic

In many cases, the interrupt request logic may be implemented in the same EPLD/FPGA with the address decoding and glue logic. The most common functions of this logic include providing tri-state or open collector INTERRUPT REQUEST outputs, clearing the request flip-flop, and providing interrupt vector responses.

## 9.12 Reset (MSTCLR*) Input

The Enhanced Mini-ACE may be placed in its power turn-on, or initialization state, following either a hardware or software reset. A hardware reset, which generally occurs following power turn-on, is caused by asserting the MSTCLR* input to logic "0" for at least 100ns of the Enhanced Mini-ACE's internal logic following a hardware, software, or "Reset RT" reset is summarized in Volume 1, Table 3, in the "REGISTERS" section of the User's Guide.

**Note that in order to ensure the correct initialization at the Enhanced Mini-ACE's transceivers, the rise time for $\overline{\text{MSTCLR}}$ must be less than 10 µs.**

## 9.13 Chip Select (SELECT*) Input

In all modes, a CPU transfer is initiated through the use of the input signals SELECT* and STRBD*. The Enhanced Mini-ACE will begin a CPU transfer upon sampling both SELECT* and STRBD* low on a rising clock edge. A CPU transfer, once started (as indicated by a logic 0 output on the IOEN* output signal), will remain active until the STRBD* input returns to a logic 1 state.

## 9.14 Bit Buffered, Nonzero Wait Mode Interface Timing

Figure 22 and Figure 23 illustrate the timing for the host processor to access the Enhanced Mini-ACE's internal RAM or registers in the 16_bit, nonzero wait buffered mode. Figure 22 illustrates the 16_bit buffered, nonzero wait state mode read cycle timing, while Figure 23 shows the 16_bit, buffered, nonzero wait state mode write cycle timing.

During a CPU transfer cycle, the signals $\overline{\text{STRBD}}$ and $\overline{\text{SELECT}}$ must be sampled low on the rising edge of the system clock to request access to the Enhanced Mini-ACE internal shared RAM. The transfer will begin on the first rising system clock edge when ($\overline{\text{SELECT}}$ **and** $\overline{\text{STRBD}}$) is low **and** the 1553 protocol/memory management unit is not accessing the internal RAM. The start of the transfer is indicated by the falling edge of the output signal $\overline{\text{IOEN}}$. The signals MEM/$\overline{\text{REG}}$ and RD/$\overline{\text{WR}}$ are latched internally on the first falling clock edge after the start of the transfer cycle. The address inputs are latched internally on the first rising clock edge after the signal $\overline{\text{IOEN}}$ goes low. Note that the address lines may be latched at any time using the ADDR_LAT input signal.

The output signal $\overline{\text{READYD}}$ will be asserted low on the third rising clock edge after $\overline{\text{IOEN}}$ goes low for read transfers or the second rising clock edge for write transfers. The assertion of $\overline{\text{READYD}}$ low indicates to the host processor that read data is available on the parallel data bus (D15-D0), or that write data has been stored. At this time, the CPU should bring the signal $\overline{\text{STRBD}}$ high, completing the transfer cycle.

| Table 5. CPU Reading RAM/Registers (16-Bit, Buffered, Non-Zero Wait Mode) | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| REF | DESCRIPTION | NOTES | 5V LOGIC | | | 3.3V LOGIC | | | UNITS |
| | | | MIN | TYP | MAX | MIN | TYP | MAX | |
| t1 | $\overline{\text{SELECT}}$ and $\overline{\text{STRBD}}$ low setup time prior to clock rising edge | 2, 9 | 10 | | | 15 | | | ns |
| t2 | $\overline{\text{SELECT}}$ and $\overline{\text{STRBD}}$ low to $\overline{\text{IOEN}}$ low (uncontended access @ 20 MHz) | 2, 6 | | | 100 | | | 105 | ns |
| | (contended access, with ENHANCED CPU ACCESS = “0” @ 20 MHz) | 2, 6 | | | 3.6 | | | 3.6 | µs |
| | (contended access, with ENHANCED CPU ACCESS = “1” @ 20 MHz) | 2, 6 | | | 515 | | | 520 | ns |
| | (uncontended access @ 16 MHz) | 2, 6 | | | 112 | | | 117 | ns |
| | (contended access, with ENHANCED CPU ACCESS = “0” @ 16 MHz) | 2, 6 | | | 4.6 | | | 2.8 | µs |
| | (contended access, with ENHANCED CPU ACCESS = “1” s @ 16 MHz) | 2, 6 | | | 630 | | | 635 | ns |
| | (uncontended access @ 12 MHz) | 2, 6 | | | 133 | | | 138 | ns |
| | (contended access, with ENHANCED CPU ACCESS = “0” @ 12 MHz) | 2, 6 | | | 6.0 | | | 6.0 | µs |
| | (contended access, with ENHANCED CPU ACCESS = “1” @ 12 MHz) | 2, 6 | | | 815 | | | 820 | ns |
| | (uncontended access @ 10 MHz) | 2, 6 | | | 150 | | | 155 | ns |
| | (contended access, with ENHANCED CPU ACCESS = “0” @ 10 MHz) | 2, 6 | | | 7.2 | | | 7.2 | µs |
| | (contended access, with ENHANCED CPU ACCESS = “1” @ 10 MHz) | 2, 6 | | | 965 | | | 970 | ns |
| t3 | Time for MEM/$\overline{\text{REG}}$ and RD/$\overline{\text{WR}}$ to become valid following $\overline{\text{SELECT}}$ and $\overline{\text{STRBD}}$ low (@ 20 MHz) | 3,4,5,7 | | | 15 | | | 10 | ns |
| | @ 16 MHz | 3,4,5,7 | | | 21 | | | 16 | ns |
| | @ 12 MHz | 3,4,5,7 | | | 32 | | | 27 | ns |
| | @ 10 MHz | 3,4,5,7 | | | 40 | | | 35 | ns |
| t4 | Time for Address to become valid following $\overline{\text{SELECT}}$ and $\overline{\text{STRBD}}$ low (@ 20 MHz) | | | | 17 | | | 12 | ns |
| | @ 16 MHz | | | | 30 | | | 25 | ns |
| | @ 12 MHz | | | | 50 | | | 45 | ns |
| | @ 10 MHz | | | | 67 | | | 62 | ns |
| t5 | CLOCK IN rising edge delay to $\overline{\text{IOEN}}$ falling edge | 6 | | | 40 | | | 40 | ns |
| t6 | $\overline{\text{SELECT}}$ hold time following $\overline{\text{IOEN}}$ falling | 2 | 0 | | | 0 | | | ns |
| t7 | MEM/$\overline{\text{REG}}$, RD/$\overline{\text{WR}}$ setup time prior to CLOCK IN falling edge | 3,4,5,7 | 10 | | | 15 | | | ns |
| t8 | MEM/$\overline{\text{REG}}$, RD/$\overline{\text{WR}}$ hold time following CLOCK IN falling edge | 3,4,5,7 | 30 | | | 30 | | | ns |

| Table 5. CPU Reading RAM/Registers (16-Bit, Buffered, Non-Zero Wait Mode) | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| REF | DESCRIPTION | NOTES | 5V LOGIC | | | 3.3V LOGIC | | | UNITS |
| | | | MIN | TYP | MAX | MIN | TYP | MAX | |
| t9 | Address valid setup time prior to CLOCK IN rising edge | 7,8 | 30 | | | 35 | | | ns |
| t10 | Address hold time following CLOCK IN rising edge | 7,8,9 | 30 | | | 30 | | | ns |
| t11 | $\overline{\text{IOEN}}$ falling delay to $\overline{\text{READYD}}$ falling (@ 20 MHz) | 6,9 | 135 | 150 | 165 | 135 | 150 | 165 | ns |
| | @ 16 MHz | 6,9 | 170 | 187.5 | 205 | 170 | 187.5 | 205 | ns |
| | @ 12 MHz | 6,9 | 235 | 250 | 265 | 235 | 250 | 265 | ns |
| | @ 10 MHz | 6,9 | 285 | 300 | 315 | 285 | 300 | 300 | ns |
| t12 | Output Data valid prior to $\overline{\text{READYD}}$ falling (@20 MHz) | 6 | 21 | | | 11 | | | ns |
| | @ 16 MHz | 6 | 33 | | | 23 | | | ns |
| | @ 12 MHz | 6 | 54 | | | 44 | | | ns |
| | @ 10 MHz | 6 | 71 | | | 61 | | | ns |
| t13 | CLOCK IN rising edge delay to $\overline{\text{READYD}}$ falling | 6 | | | 40 | | | 40 | ns |
| t14 | $\overline{\text{READYD}}$ falling to $\overline{\text{STRBD}}$ rising release time | | | | ∞ | | | ∞ | ns |
| t15 | $\overline{\text{STRBD}}$ rising edge delay to $\overline{\text{IOEN}}$ rising edge and $\overline{\text{READYD}}$ rising edge | 6 | | | 30 | | | 40 | ns |
| t16 | Output Data hold time following $\overline{\text{STRBD}}$ rising edge | | 0 | | | 0 | | | ns |
| t17 | $\overline{\text{STRBD}}$ rising delay to output data tri-state | | | | 40 | | | 40 | ns |
| t18 | $\overline{\text{STRBD}}$ high hold time from $\overline{\text{READYD}}$ rising | | 0 | | | 0 | | | ns |
| t19 | CLOCK IN rising edge delay to output data valid | | | | 40 | | | 40 | ns |

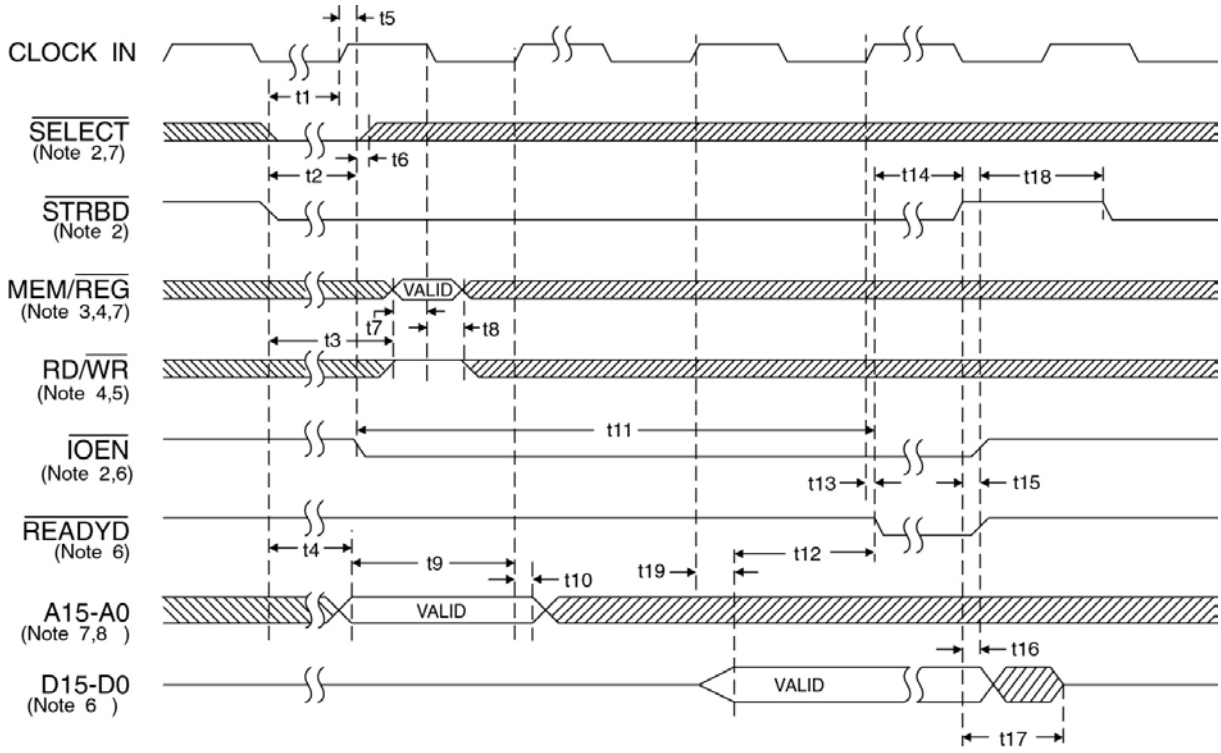



**Figure 22. CPU Reading RAM/Registers (16-Bit, Buffered, Nonzero Wait)**

Notes: ForTable 5 and Figure 22

1. For the 16-bit buffered nonzero wait configuration, TRANSPARENT/$\overline{\text{BUFFERED}}$ must be connected to logic "0". $\overline{\text{ZERO\_WAIT}}$ and DTREQ / 16/8 must be connected to logic "1". The inputs TRIGGER_SEL and MSB/LSB may be connected to either +5V or ground.
2. $\overline{\text{SELECT}}$ and $\overline{\text{STRBD}}$ may be tied together. $\overline{\text{IOEN}}$ goes low on the first rising CLK edge when $\overline{\text{SELECT}}$ • $\overline{\text{STRBD}}$ is sampled low (satisfying t1) and the Enhanced Mini-ACE's protocol/memory management logic is not accessing the internal RAM. When this occurs, $\overline{\text{IOEN}}$ goes low, starting the transfer cycle. After $\overline{\text{IOEN}}$ goes low, $\overline{\text{SELECT}}$ may be released high.
3. MEM/$\overline{\text{REG}}$ must be presented high for memory access, low for register access.
4. MEM/$\overline{\text{REG}}$ and RD/$\overline{\text{WR}}$ are buffered transparently until the first falling edge of CLK after $\overline{\text{IOEN}}$ goes low. After this CLK edge, MEM/$\overline{\text{REG}}$ and RD/$\overline{\text{WR}}$ become latched internally.
5. The logic sense for RD/$\overline{\text{WR}}$ in the diagram assumes that POLARITY_SEL is connected to logic "1." If POLARITY_SEL is connected to logic "0," RD/$\overline{\text{WR}}$ must be asserted low to read.
6. The timing for $\overline{\text{IOEN}}$, READYD and D15-D0 assumes a 50 pf load. For loading above 50 pf, the validity of $\overline{\text{IOEN}}$, READYD, and D15-D0 is delayed by an additional 0.14 ns/pf typ, 0.28 ns/pf max.
7. The timing for A15-A0, MEM/$\overline{\text{REG}}$ and $\overline{\text{SELECT}}$ assumes that ADDR-LAT is connected to logic "1." Refer to Address Latch timing for additional details.
8. The address bus A15-A0 is internally buffered transparently until the first rising edge of CLK after $\overline{\text{IOEN}}$ goes low. After this CLK edge, A15-A0 becomes latched internally.
9. Setup time given for use in worst case timing calculations. None of the Enhanced Mini-ACE input signals are required to be synchronized to the system clock. When $\overline{\text{SELECT}}$ and $\overline{\text{STRBD}}$ do not meet the setup time of t1, but occur during the setup window of an internal flip-flop, an additional clock cycle will be inserted between the falling clock edge that latches MEM/REG and RD/WR and the rising clock edge that latches the Address (A15-A0). When this occurs, the delay from IOEN falling to READYD falling (t11) increases by one clock cycle and the address hold time (t10) must be increased be one clock cycle.

| Table 6. CPU Writing RAM/Registers (16-Bit, Buffered, Nonzero Wait Mode) | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| REF | DESCRIPTION | NOTES | 5V LOGIC | | | 3.3V LOGIC | | | UNITS |
| | | | MIN | TYP | MAX | MIN | TYP | MAX | |
| t1 | $\overline{\text{SELECT}}$ and $\overline{\text{STRBD}}$ low setup time prior to clock rising edge | 2, 10 | 10 | | | 15 | | | ns |
| t2 | $\overline{\text{SELECT}}$ and $\overline{\text{STRBD}}$ low to $\overline{\text{IOEN}}$ low (uncontended access @ 20 MHz) | 2, 6 | | | 100 | | | 105 | ns |
| | (contended access, with ENHANCED CPU ACCESS = “0” @ 20 MHz) | 2, 6 | | | 3.6 | | | 3.6 | µs |
| | (contended access, with ENHANCED CPU ACCESS = “1” @ 20 MHz) | 2, 6 | | | 465 | | | 470 | ns |
| | (uncontended access @ 16 MHz) | 2, 6 | | | 112 | | | 117 | ns |
| | (contended access, with ENHANCED CPU ACCESS = “0” @ 16 MHz) | 2, 6 | | | 4.6 | | | 2.8 | µs |
| | (contended access, with ENHANCED CPU ACCESS = “1” @ 16 MHz) | 2, 6 | | | 565 | | | 570 | ns |
| | (uncontended access @ 12 MHz) | 2, 6 | | | 133 | | | 138 | ns |
| | (contended access, with ENHANCED CPU ACCESS = “0” @ 12 MHz) | 2, 6 | | | 6.0 | | | 6.0 | µs |
| | (contended access, with ENHANCED CPU ACCESS = “1” @ 12 MHz) | 2, 6 | | | 732 | | | 737 | ns |
| | (uncontended access @ 10 MHz) | 2, 6 | | | 150 | | | 155 | ns |
| | (contended access, with ENHANCED CPU ACCESS = “0” @ 10 MHz) | 2, 6 | | | 7.2 | | | 7.2 | µs |
| | (contended access, with ENHANCED CPU ACCESS = “1” @ 10 MHz) | 2, 6 | | | 865 | | | 870 | ns |
| t3 | Time for MEM/$\overline{\text{REG}}$ and RD/$\overline{\text{WR}}$ to become valid following $\overline{\text{SELECT}}$ and $\overline{\text{STRBD}}$ low (@ 20 MHz) | 3,4,5,7 | | | 15 | | | 10 | ns |
| | @ 16 MHz | 3,4,5,7 | | | 21 | | | 16 | ns |
| | @ 12 MHz | 3,4,5,7 | | | 32 | | | 27 | ns |
| | @ 10 MHz | 3,4,5,7 | | | 40 | | | 35 | ns |
| t4 | Time for Address to become valid following $\overline{\text{SELECT}}$ and $\overline{\text{STRBD}}$ low (@ 20 MHz) | | | | 17 | | | 12 | ns |
| | @ 16 MHz | | | | 30 | | | 25 | ns |
| | @ 12 MHz | | | | 50 | | | 45 | ns |
| | @ 10 MHz | | | | 67 | | | 62 | ns |
| t5 | Time for data to become valid following $\overline{\text{SELECT}}$ and $\overline{\textit{STRBD}}$ low (@ 20 MHz) | | | | 37 | | | 32 | ns |
| | @ 16 MHz | | | | 50 | | | 45 | ns |
| | @ 12 MHz | | | | 70 | | | 65 | ns |
| | @ 10 MHz | | | | 87 | | | 82 | ns |

| Table 6. CPU Writing RAM/Registers (16-Bit, Buffered, Nonzero Wait Mode) | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| REF | DESCRIPTION | NOTES | 5V LOGIC | | | 3.3V LOGIC | | | UNITS |
| | | | MIN | TYP | MAX | MIN | TYP | MAX | |
| t6 | Clock in rising edge delay to $\overline{\text{IOEN}}$ falling edge | 6 | | | 40 | | | 40 | ns |
| t7 | $\overline{\text{SELECT}}$ hold time following $\overline{\text{IOEN}}$ falling | 2 | 0 | | | 0 | | | ns |
| t8 | MEM/$\overline{\text{REG}}$, RD/$\overline{\text{WR}}$ setup time prior to CLOCK IN falling edge | 3,4,5,7 | 10 | | | 15 | | | ns |
| t9 | MEM/$\overline{\text{REG}}$, RD/$\overline{\text{WR}}$ setup time following CLOCK IN falling edge | 3,4,5,7 | 30 | | | 35 | | | ns |
| t10 | Address valid setup time prior to CLOCK IN rising edge | 7,8 | 30 | | | 35 | | | ns |
| t11 | Data valid setup time prior to CLOCK IN rising edge | | 10 | | | 15 | | | ns |
| t12 | Address valid hold time following CLOCK IN rising edge | 7,8,9 | 30 | | | 30 | | | ns |
| t13 | Data valid hold time following CLOCK IN rising edge | 9 | 10 | | | 15 | | | ns |
| t14 | $\overline{\text{IOEN}}$ falling delay to $\overline{\text{READYD}}$ falling @ 20 MHz | 6,9 | 85 | 100 | 115 | 85 | 100 | 115 | ns |
| | @ 16 MHz | 6,9 | 110 | 125 | 140 | 110 | 125 | 140 | ns |
| | @ 12 MHz | 6,9 | 152 | 167 | 182 | 152 | 167 | 182 | ns |
| | @ 10 MHz | 6,9 | 185 | 200 | 215 | 185 | 200 | 215 | ns |
| t15 | CLOCK IN rising edge delay to $\overline{\text{READYD}}$ falling | 6 | | | 40 | | | 40 | ns |
| t16 | $\overline{\text{READYD}}$ falling to $\overline{\text{STRBD}}$ rising release time | | | | ∞ | | | ∞ | ns |
| t17 | $\overline{\text{STRBD}}$ rising delay to $\overline{\text{IOEN}}$ rising edge and $\overline{\text{READYD}}$ rising edge | 6 | | | 30 | | | 40 | ns |
| t18 | $\overline{\text{STRBD}}$ high hold time from $\overline{\text{READYD}}$ rising | | 10 | | | 10 | | | ns |

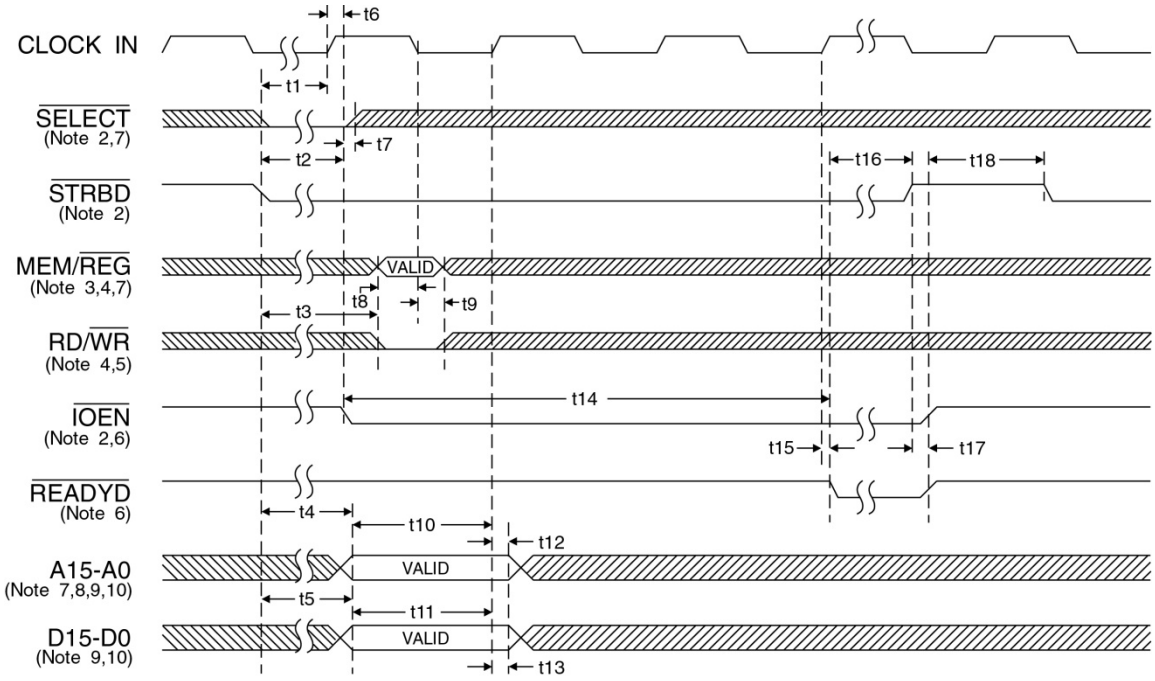



**Figure 23. CPU Writing RAM/Registers (16-Bit, Buffered, Nonzero Wait)**

Notes: For Table 6 and Figure 23

1. For the 16-bit buffered nonzero wait configuration TRANSPARENT/$\overline{\text{BUFFERED}}$ must be connected to logic "0", $\overline{\text{ZERO\_WAIT}}$ and $\overline{\text{DTREG}}$ / 16/$\overline{8}$ must be connected to logic "1". The inputs TRIGGER_SEL and MSB/LSB may be connected to either +5V or ground.
2. $\overline{\text{SELECT}}$ and $\overline{\text{STRBD}}$ may be tied together. $\overline{\text{IOEN}}$ goes low on the first rising CLK edge when $\overline{\text{SELECT}} \bullet \overline{\text{STRBD}}$ is sampled low (satisfying t1) and the Enhanced Mini-ACE's protocol/memory management logic is not accessing the internal RAM. When this occurs, $\overline{\text{IOEN}}$ goes low, starting the transfer cycle. After $\overline{\text{IOEN}}$ goes low, $\overline{\text{SELECT}}$ may be released high.
3. MEM/$\overline{\text{REG}}$ must be presented high for memory access, low for register access.
4. MEM/$\overline{\text{REG}}$ and RD/$\overline{\text{WR}}$ are buffered transparently until the first falling edge of CLK after $\overline{\text{IOEN}}$ goes low. After this CLK edge, MEM/$\overline{\text{REG}}$ and RD/$\overline{\text{WR}}$ become latched internally.
5. The logic sense for RD/$\overline{\text{WR}}$ in the diagram assumes that POLARITY_SEL is connected to logic "1." If POLARITY_SEL is connected to logic "0," RD/$\overline{\text{WR}}$ must be asserted high to write.
6. The timing for the $\overline{\text{IOEN}}$ and $\overline{\text{READYD}}$ outputs assumes a 50 pf load. For loading above 50 pf, the validity of $\overline{\text{IOEN}}$ and $\overline{\text{READYD}}$ is delayed by an additional 0.14 ns/pf typ, 0.28 ns/pf max.
7. The timing for A15-A0, MEM/$\overline{\text{REG}}$, and $\overline{\text{SELECT}}$ assumes that ADDR-LAT is connected to logic "1." Refer to Address Latch timing for additional details.
9. The address bus A15-A0 and data bus D15-D0 are internally buffered transparently until the first rising edge of CLK after $\overline{\text{IOEN}}$ goes low. After this CLK edge, A15-A0 and D15-D0 become latched internally.

Setup time given for use in worst case timing calculations. None of the Enhanced Mini-ACE input signals are required to be synchronized to the system clock. When $\overline{\text{SELECT}}$ and $\overline{\text{STRBD}}$ do not meet the setup time of t1, but occur during the setup time of an internal flip-flop, an additional clock cycle may be inserted between the falling clock edge that latches MEM/$\overline{\text{REG}}$ and RD/$\overline{\text{WR}}$ and the rising clock edge that latches the address (A15-A0) and data (D15-D0). When this occurs, the delay from $\overline{\text{IOEN}}$ falling to $\overline{\text{READYD}}$ falling (t14) increases by one clock cycle and the address and data hold time (t12 and t13) must be increased by one clock.

| Table 7. CPU Reading RAM/Registers (16-Bit, Buffered, Zero Wait Mode) | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| REF | DESCRIPTION | NOTES | 5V Logic | | | 3.3V Logic | | | UNITS |
| | | | MIN | TYP | MAX | MIN | TYP | MAX | |
| t1 | $\overline{\text{SELECT}}$ and $\overline{\text{STRBD}}$ low setup time prior to CLOCK IN rising | 10 | 10 | | | 15 | | | ns |
| t2 | $\overline{\text{SELECT}}$ and $\overline{\text{STRBD}}$ low minimum pulse width | | 20 | | | 20 | | | ns |
| t3 | $\overline{\text{SELECT}}$ and $\overline{\text{STRBD}}$ low delay to Data valid | 14 | | | 35 | | | 30 | ns |
| t4 | RD/$\overline{\text{WR}}$ setup time prior to $\overline{\text{SELECT}}$ and $\overline{\text{STRBD}}$ low | | 10 | | | 10 | | | ns |
| t5 | RD/$\overline{\text{WR}}$ high delay to Data valid | 14 | | | 35 | | | 30 | ns |
| t6A | Address setup time prior to $\overline{\text{STRBD}}$ rising | 11 | 10 | | | 10 | | | ns |
| t6B | Address setup time prior to CLOCK IN rising | 12 | 10 | | | 10 | | | ns |
| t7A | MEM/$\overline{\text{REG}}$ setup time prior to $\overline{\text{STRBD}}$ rising | 11 | 10 | | | 10 | | | ns |
| t7B | MEM/$\overline{\text{REG}}$ setup time prior to CLOCK IN rising | 12 | 10 | | | 10 | | | ns |
| t8A | $\overline{\text{SELECT}}$ low hold time following $\overline{\text{STRBD}}$ rising | 11 | 0 | | | 0 | | | ns |
| t8B | $\overline{\text{SELECT}}$ low hold time following CLOCK IN rising | 12 | 25 | | | 25 | | | ns |
| t9A,B | $\overline{\text{STRBD}}$ rising setup time prior to CLOCK IN rising | 10 | 15 | | | 20 | | | ns |
| t10A | MEM/$\overline{\text{REG}}$ and RD/WR* hold time following $\overline{\text{STRBD}}$ rising | 11 | 20 | | | 20 | | | ns |
| t10B | MEM/$\overline{\text{REG}}$ and RD/WR* hold time following CLOCK IN rising | 12 | 25 | | | 25 | | | ns |
| t11A | $\overline{\text{STRBD}}$ rising delay to $\overline{\text{READYD}}$ low | 11 | | | 30 | | | 30 | ns |
| t11B | CLOCK IN rising delay to $\overline{\text{READYD}}$ low | 12 | | | 35 | | | 30 | ns |
| t12A | Address hold time following $\overline{\text{STRBD}}$ rising | 11 | 20 | | | 20 | | | ns |
| t12B | Address hold time following CLOCK IN rising | 12 | 25 | | | 25 | | | ns |
| t13 | Output Data hold time following $\overline{\text{STRBD}}$ rising | | 0 | | | 0 | | | ns |
| t14 | $\overline{\text{STRBD}}$ rising delay to Data tri-state | | | | 35 | | | 30 | ns |
| t15 | $\overline{\text{STRBD}}$ rising delay to start of next transfer (uncontended access @20 MHz) | 13 | 320 | | | 320 | | | ns |
| | (Contended access, with ENHANCED CPU ACCESS = “0” @ 20 MHz) | 13 | 3.9 | | | 3.9 | | | us |
| | (Contended access, with ENHANCED CPU ACCESS = “1” @ 20 MHz) | 13 | 650 | | | 650 | | | ns |
| | $\overline{\text{STRBD}}$ rising delay to start of next transfer (uncontended access @16 MHz) | 13 | 395 | | | 395 | | | ns |
| | (Contended access, with ENHANCED CPU ACCESS = “0” @ 16 MHz) | 13 | 4.9 | | | 4.9 | | | us |
| | (Contended access, with ENHANCED CPU ACCESS = “1” @ 16 MHz) | 13 | 800 | | | 800 | | | ns |

| Table 7. CPU Reading RAM/Registers (16-Bit, Buffered, Zero Wait Mode) | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| REF | DESCRIPTION | NOTES | 5V Logic | | | 3.3V Logic | | | UNITS |
| | | | MIN | TYP | MAX | MIN | TYP | MAX | |
| | $\overline{STRBD}$ rising delay to start of next transfer (uncontended access @12 MHz) | 13 | 520 | | | 520 | | | ns |
| | (Contended access, with ENHANCED CPU ACCESS = "0" @ 12 MHz) | 13 | 6.5 | | | 6.5 | | | us |
| | (Contended access, with ENHANCED CPU ACCESS = "1" @ 12 MHz) | 13 | 1050 | | | 1050 | | | ns |
| | $\overline{STRBD}$ rising delay to start of next transfer (uncontended access @10 MHz) | 13 | 620 | | | 620 | | | ns |
| | (Contended access, with ENHANCED CPU ACCESS = "0" @ 10 MHz) | 13 | 7.8 | | | 7.8 | | | us |
| | (Contended access, with ENHANCED CPU ACCESS = "1" @ 10 MHz) | 13 | 1250 | | | 1250 | | | ns |
| t16 | $\overline{STRBD}$ rising delay to $\overline{IOEN}$ falling (uncontended access @20 MHz) | | | | 105 | | | 105 | ns |
| | (Contended access, with ENHANCED CPU ACCESS = "0" @ 20 MHz) | | | | 3.6 | | | 3.6 | us |
| | (Contended access, with ENHANCED CPU ACCESS = "1" @ 20 MHz) | | | | 350 | | | 350 | ns |
| | $\overline{STRBD}$ rising delay to $\overline{IOEN}$ falling (uncontended access @16 MHz) | | | | 130 | | | 130 | ns |
| | (Contended access, with ENHANCED CPU ACCESS = "0" @ 16 MHz) | | | | 4.5 | | | 4.5 | us |
| | (Contended access, with ENHANCED CPU ACCESS = "1" @ 16 MHz) | | | | 438 | | | 438 | ns |
| | $\overline{STRBD}$ rising delay to $\overline{IOEN}$ falling (uncontended access @12 MHz) | | | | 172 | | | 172 | ns |
| | (Contended access, with ENHANCED CPU ACCESS = "0" @ 12 MHz) | | | | 6.0 | | | 6.0 | us |
| | (Contended access, with ENHANCED CPU ACCESS = "1" @ 12 MHz) | | | | 583 | | | 583 | ns |
| | $\overline{STRBD}$ rising delay to $\overline{IOEN}$ falling (uncontended access @10 MHz) | | | | 205 | | | 205 | ns |
| | (Contended access, with ENHANCED CPU ACCESS = "0" @ 10 MHz) | | | | 7.2 | | | 7.2 | us |
| | (Contended access, with ENHANCED CPU ACCESS = "1" @ 10 MHz) | | | | 700 | | | 700 | ns |
| t17 | CLOCK IN rising to $\overline{IOEN}$ low | 2 | | | 40 | | | 30 | ns |
| t18 | $\overline{IOEN}$ low pulse width for RAM read (@20 MHz) | | 185 | 200 | 215 | 185 | 200 | 215 | ns |
| | $\overline{IOEN}$ low pulse width for REGISTER read (@20 MHz) | | 185 | 200 | 215 | 185 | 200 | 215 | ns |
| | $\overline{IOEN}$ low pulse width for RAM read (@16 MHz) | | 235 | 250 | 265 | 235 | 250 | 265 | ns |
| | $\overline{IOEN}$ low pulse width for REGISTER read (@16 MHz) | | 235 | 250 | 265 | 235 | 250 | 265 | ns |
| | $\overline{IOEN}$ low pulse width for RAM read (@12 MHz) | | 315 | 333 | 350 | 315 | 333 | 350 | ns |
| | $\overline{IOEN}$ low pulse width for REGISTER read (@12 MHz) | | 315 | 333 | 350 | 315 | 333 | 350 | ns |
| | $\overline{IOEN}$ low pulse width for RAM read (@10 MHz) | | 385 | 400 | 415 | 385 | 400 | 415 | ns |
| | $\overline{IOEN}$ low pulse width for REGISTER read (@10 MHz) | | 385 | 400 | 415 | 385 | 400 | 415 | ns |
| t19 | CLOCK IN rising delay to $\overline{IOEN}$ rising | | | | 35 | | | 30 | ns |

| Table 7. CPU Reading RAM/Registers (16-Bit, Buffered, Zero Wait Mode) | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| REF | DESCRIPTION | NOTES | 5V Logic | | | 3.3V Logic | | | UNITS |
| | | | MIN | TYP | MAX | MIN | TYP | MAX | |
| t20 | CLOCK IN falling delay to $\overline{\text{READYD}}$ rising | | | | 35 | | | 30 | ns |
| t21 | $\overline{\text{READYD}}$ high delay to start of next transfer ( $\overline{\text{STRBD}}$ falling) | | 0 | | | 0 | | | ns |

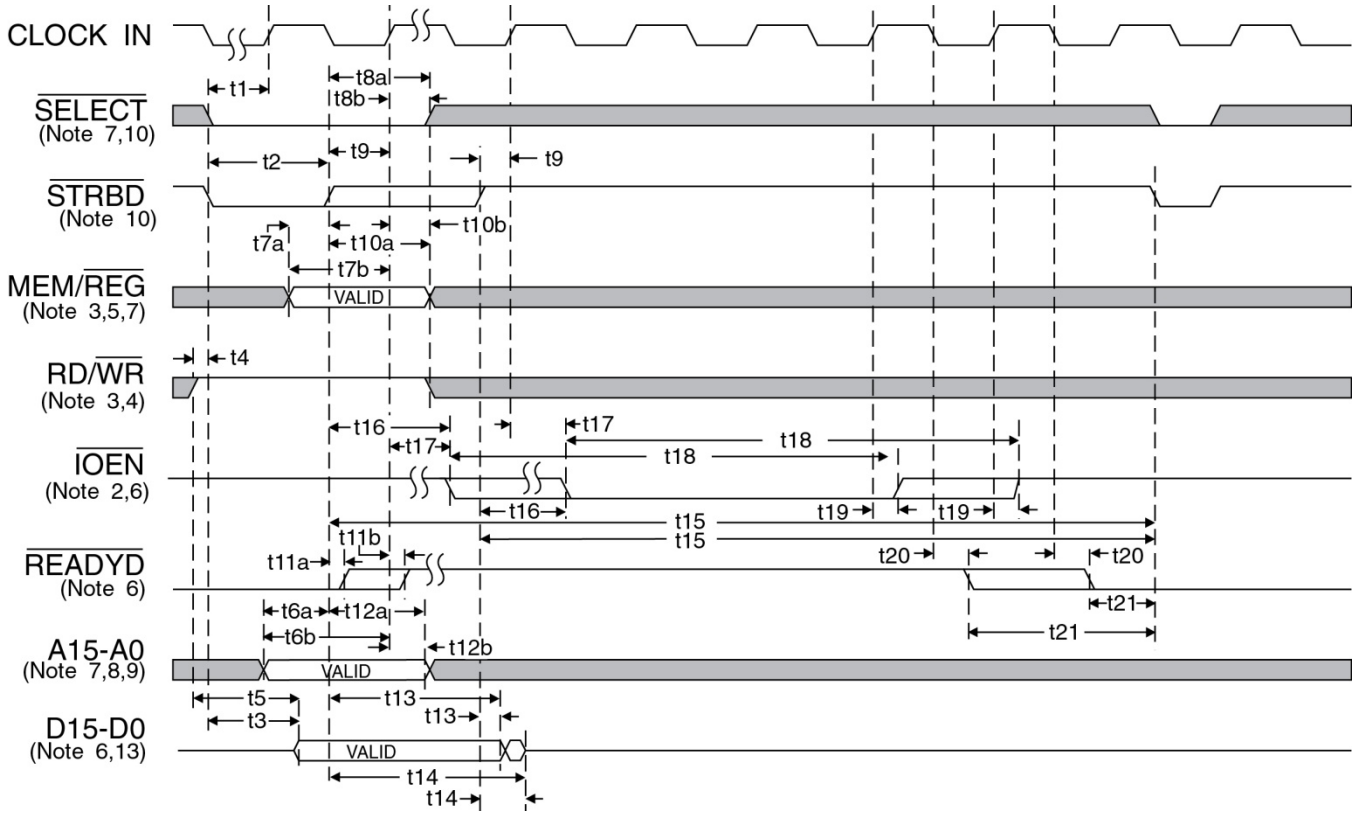



**Figure 24. CPU Reading RAM/Registers (16-Bit, Buffered, Zero Wait)**

Notes for Table 7 and Figure 24

1. For the 16-bit buffered configuration, the inputs TRIGGER_SEL and MSB/LSB may be connected to +5V or GND. For the zero wait interface, $\overline{\text{ZERO\_WAIT}}$ must be connected to logic "0."
2. $\overline{\text{IOEN}}$ goes low on the first rising CLK edge when $\overline{\text{READYD}}$ is low and $\overline{\text{STRBD}}$ is sampled high (satisfying t9 setup time) and the Enhanced Mini-ACE protocol/memory management logic is not accessing the internal RAM. When this occurs, $\overline{\text{IOEN}}$ goes low, starting the internal transfer.
3. MEM/$\overline{\text{REG}}$ and RD/$\overline{\text{WR}}$ are buffered transparently until latched by $\overline{\text{STRBD}}$ rising or second rising clock edge.
4. The logic sense for RD/$\overline{\text{WR}}$ in the diagram assumes that POLARITY_SEL is connected to logic "1." If POLARITY_SEL is connected to logic "0," RD/$\overline{\text{WR}}$ must be asserted low to read.
5. Data output is ready from register/RAM address referenced by the value of MEM/$\overline{\text{REG}}$ and A15-A0 from the previous read cycle.
6. The timing for $\overline{\text{IOEN}}$, $\overline{\text{READYD}}$ and D15-D0 assumes a 50 pf load. For loading above 50 pf, the validity of $\overline{\text{IOEN}}$, $\overline{\text{READYD}}$, and D15-D0 is delayed by an additional 0.14 ns/pf typ, 0.28 ns/pf max.
7. Timing for A15-A0, MEM/$\overline{\text{REG}}$, and $\overline{\text{SELECT}}$ assumes ADDR-LAT is connected to logic "1." Refer to Address Latch timing for additional details. Internal RAM is accessed by A15 through A0 (64K RAM Versions) or A11 through A0 (4K RAM Versions). Registers are accessed by A4 through A0.
9. The address bus A15-A0 is internally buffered transparently until latched by $\overline{\text{STRBD}}$ rising or second rising clock edge. To implement a single zero wait read operation, the host processor must perform two read accesses to the Enhanced Mini-ACE. During the first access, the address and transfer type indication (memory or register) of the location to be read must be asserted on A15-A0 and MEM/$\overline{\text{REG}}$, respectively. The data read on D15-D0 during this cycle should be ignored ("thrown away"). During the second read access, the Enhanced Mini-ACE presents the data corresponding to the address presented on the first access on D15-D0. If the CPU performs a multi-word read burst, the address for the next word should be presented on A15-A0 on the same cycle that data is read from D15-D0. That is, for a multi-word read transfer, the address presented should always be one location ahead of that of the data being read.
10. Setup time given for use in worst case timing calculations. These signals do not have to be synchronized to the system clock. Removal of $\overline{\text{SELECT}}$ prior to being latched on the second rising clock edge will have the same effect as $\overline{\text{STRBD}}$ rising. For Enhanced Mini-ACE applications, transfer will not start until $\overline{\text{SELECT}}$ and $\overline{\text{STRBD}}$ are both low. $\overline{\text{SELECT}}$ must go low prior to the second rising clock edge after $\overline{\text{STRBD}}$ goes low or transfer will be blocked.
11. For the case in which $\overline{\text{STRBD}}$ goes high before second rising clock edge in which $\overline{\text{SELECT}}$ is low and $\overline{\text{STRBD}}$ is low.
12. For the case in which $\overline{\text{STRBD}}$ is low and $\overline{\text{SELECT}}$ is low for a minimum of two rising clock edges for the Enhanced Mini-ACE.
13. After $\overline{\text{STRBD}}$ is brought high and $\overline{\text{READYD}}$ asserted low, $\overline{\text{STRBD}}$ MUST be kept low until $\overline{\text{READYD}}$ returns high.
14. Valid data will be present on D15-D0 only after $\overline{\text{SELECT}}$, $\overline{\text{STRBD}}$ and RD/$\overline{\text{WR}}$ propagation delays (t3 and t5) are met.

| Table 8. CPU Writing RAM/Registers (16-Bit, Buffered, Zero Wait Mode) | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| REF | DESCRIPTION | NOTES | 5V LOGIC | | | 3.3V LOGIC | | | UNITS |
| | | | MIN | TYP | MAX | MIN | TYP | MAX | |
| t1 | $\overline{\text{SELECT}}$ and $\overline{\text{STRBD}}$ low setup time prior to CLOCK IN rising | 10 | 10 | | | 15 | | | ns |
| t2 | $\overline{\text{SELECT}}$ and $\overline{\text{STRBD}}$ low minimum pulse width | | 20 | | | 20 | | | ns |
| t3 | RD/$\overline{\text{WR}}$ setup time prior to $\overline{\text{SELECT}}$ and $\overline{\text{STRBD}}$ low | | 10 | | | 10 | | | ns |
| t4A | Address setup time prior to $\overline{\text{STRBD}}$ rising | 12 | 10 | | | 10 | | | ns |
| t4B | Address setup time prior to CLOCK IN rising | 13 | 10 | | | 10 | | | ns |
| t5A | Data setup time prior to $\overline{\text{STRBD}}$ rising | 12 | 10 | | | 15 | | | ns |
| t5B | Data setup time prior to CLOCK IN rising | 13 | 10 | | | 10 | | | ns |
| t6A | MEM/$\overline{\text{REG}}$ setup time prior to $\overline{\text{STRBD}}$ rising | 12 | 10 | | | 10 | | | ns |
| t6B | MEM/$\overline{\text{REG}}$ setup time prior to CLOCK IN rising | 13 | 10 | | | 10 | | | ns |
| t7A | $\overline{\text{SELECT}}$ low hold time following $\overline{\text{STRBD}}$ rising | 12 | 0 | | | 0 | | | ns |
| t7B | $\overline{\text{SELECT}}$ low hold time following CLOCK IN rising | 13 | 25 | | | 25 | | | ns |
| t8 | $\overline{\text{STRBD}}$ rising setup time prior to CLOCK IN rising | 10 | 15 | | | 20 | | | ns |
| t9A | MEM/$\overline{\text{REG}}$ and RD/$\overline{\text{WR}}$ hold time following $\overline{\text{STRBD}}$ rising | 12 | 20 | | | 20 | | | ns |
| t9B | MEM/$\overline{\text{REG}}$ and RD/$\overline{\text{WR}}$ hold time following CLOCK IN rising | 13 | 25 | | | 25 | | | ns |
| t10A | $\overline{\text{STRBD}}$ rising delay to $\overline{\text{READYD}}$ low | 12 | | | 30 | | | 30 | ns |
| t10B | CLOCK IN rising delay to $\overline{\text{READYD}}$ low | 13 | | | 35 | | | 30 | ns |
| t11A | Address hold time following $\overline{\text{STRBD}}$ rising | 12 | 20 | | | 20 | | | ns |
| t11B | Address hold time following CLOCK IN rising | 13 | 25 | | | 25 | | | ns |
| t12A | Input Data hold time following $\overline{\text{STRBD}}$ rising | 12 | 20 | | | 20 | | | ns |
| t12B | Input Data hold time following CLOCK IN rising | 13 | 25 | | | 25 | | | ns |
| t13 | $\overline{\text{STRBD}}$ rising delay to $\overline{\text{IOEN}}$ falling (uncontended access @20 MHz) | | | | 105 | | | 105 | ns |
| | (Contended access, with ENHANCED CPU ACCESS = “0” @ 20 MHz) | | | | 3.6 | | | 3.6 | us |
| | (Contended access, with ENHANCED CPU ACCESS = “1” @ 20 MHz) | | | | 350 | | | 350 | ns |
| | $\overline{\text{STRBD}}$ rising delay to $\overline{\text{IOEN}}$ falling (uncontended access @16 MHz) | | | | 130 | | | 130 | ns |
| | (Contended access, with ENHANCED CPU ACCESS = “0” @ 16 MHz) | | | | 4.5 | | | 4.5 | us |
| | (Contended access, with ENHANCED CPU ACCESS = “1” @ 16 MHz) | | | | 438 | | | 438 | ns |
| | $\overline{\text{STRBD}}$ rising delay to $\overline{\text{IOEN}}$ falling (uncontended access @12 MHz) | | | | 172 | | | 172 | ns |

| Table 8. CPU Writing RAM/Registers (16-Bit, Buffered, Zero Wait Mode) | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| REF | DESCRIPTION | NOTES | 5V LOGIC | | | 3.3V LOGIC | | | UNITS |
| | | | MIN | TYP | MAX | MIN | TYP | MAX | |
| | (Contended access, with ENHANCED CPU ACCESS = “0” @ 12 MHz) | | | | 6.0 | | | 6.0 | us |
| | (Contended access, with ENHANCED CPU ACCESS = “1” @ 12 MHz) | | | | 583 | | | 583 | ns |
| | $\overline{\text{STRBD}}$ rising delay to $\overline{\text{IOEN}}$ falling (uncontended access @10 MHz) | | | | 205 | | | 205 | ns |
| | (Contended access, with ENHANCED CPU ACCESS = “0” @ 10 MHz) | | | | 7.2 | | | 7.2 | us |
| | (Contended access, with ENHANCED CPU ACCESS = “1” @ 10 MHz) | | | | 700 | | | 700 | ns |
| t14 | $\overline{\text{STRBD}}$ rising delay to start of next transfer (uncontended access @20 MHz) | 14 | 320 | | | 320 | | | ns |
| | (Contended access, with ENHANCED CPU ACCESS = “0” @ 20 MHz) | 14 | 3.9 | | | 3.9 | | | us |
| | (Contended access, with ENHANCED CPU ACCESS = “1” @ 20 MHz) | 14 | 650 | | | 650 | | | ns |
| | $\overline{\text{STRBD}}$ rising delay to start of next transfer (uncontended access @16 MHz) | 14 | 395 | | | 395 | | | ns |
| | (Contended access, with ENHANCED CPU ACCESS = “0” @ 16 MHz) | 14 | 4.9 | | | 4.9 | | | us |
| | (Contended access, with ENHANCED CPU ACCESS = “1” @ 16 MHz) | 14 | 800 | | | 800 | | | ns |
| | $\overline{\text{STRBD}}$ rising delay to start of next transfer (uncontended access @12 MHz) | 14 | 520 | | | 520 | | | ns |
| | (Contended access, with ENHANCED CPU ACCESS = “0” @ 12 MHz) | 14 | 6.5 | | | 6.5 | | | us |
| | (Contended access, with ENHANCED CPU ACCESS = “1” @ 12 MHz) | 14 | 1050 | | | 1050 | | | ns |
| | $\overline{\text{STRBD}}$ rising delay to start of next transfer (uncontended access @10 MHz) | 14 | 620 | | | 620 | | | ns |
| | (Contended access, with ENHANCED CPU ACCESS = “0” @ 10 MHz) | 14 | 7.8 | | | 7.8 | | | us |
| t15 | CLOCK IN rising to $\overline{\text{IOEN}}$ low | 2 | | | 40 | | | 30 | ns |
| t16 | $\overline{\text{IOEN}}$ low pulse width for RAM read (@20 MHz) | | 185 | 200 | 215 | 185 | 200 | 215 | ns |
| | $\overline{\text{IOEN}}$ low pulse width for REGISTER read (@20 MHz) | | 185 | 200 | 215 | 185 | 200 | 215 | ns |
| | $\overline{\text{IOEN}}$ low pulse width for RAM read (@16 MHz) | | 235 | 250 | 265 | 235 | 250 | 265 | ns |
| | $\overline{\text{IOEN}}$ low pulse width for REGISTER read (@16 MHz) | | 235 | 250 | 265 | 235 | 250 | 265 | ns |
| | $\overline{\text{IOEN}}$ low pulse width for RAM read (@12 MHz) | | 315 | 333 | 350 | 315 | 333 | 350 | ns |

| Table 8. CPU Writing RAM/Registers (16-Bit, Buffered, Zero Wait Mode) | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| REF | DESCRIPTION | NOTES | 5V LOGIC | | | 3.3V LOGIC | | | UNITS |
| | | | MIN | TYP | MAX | MIN | TYP | MAX | |
| | $\overline{IOEN}$ low pulse width for REGISTER read (@12 MHz) | | 315 | 333 | 350 | 315 | 333 | 350 | ns |
| | $\overline{IOEN}$ low pulse width for RAM read (@10 MHz) | | 385 | 400 | 415 | 385 | 400 | 415 | ns |
| | $\overline{IOEN}$ low pulse width for REGISTER read (@10 MHz) | | 385 | 400 | 415 | 385 | 400 | 415 | ns |
| t17 | CLOCK IN rising delay to $\overline{IOEN}$ rising | | | | 35 | | | 30 | ns |
| t18 | CLOCK IN falling delay to $\overline{READYD}$ rising | | | | 35 | | | 30 | ns |
| t19 | $\overline{READYD}$ high delay to start of next transfer ( $\overline{STRBD}$ falling) | | 0 | | | 0 | | | ns |

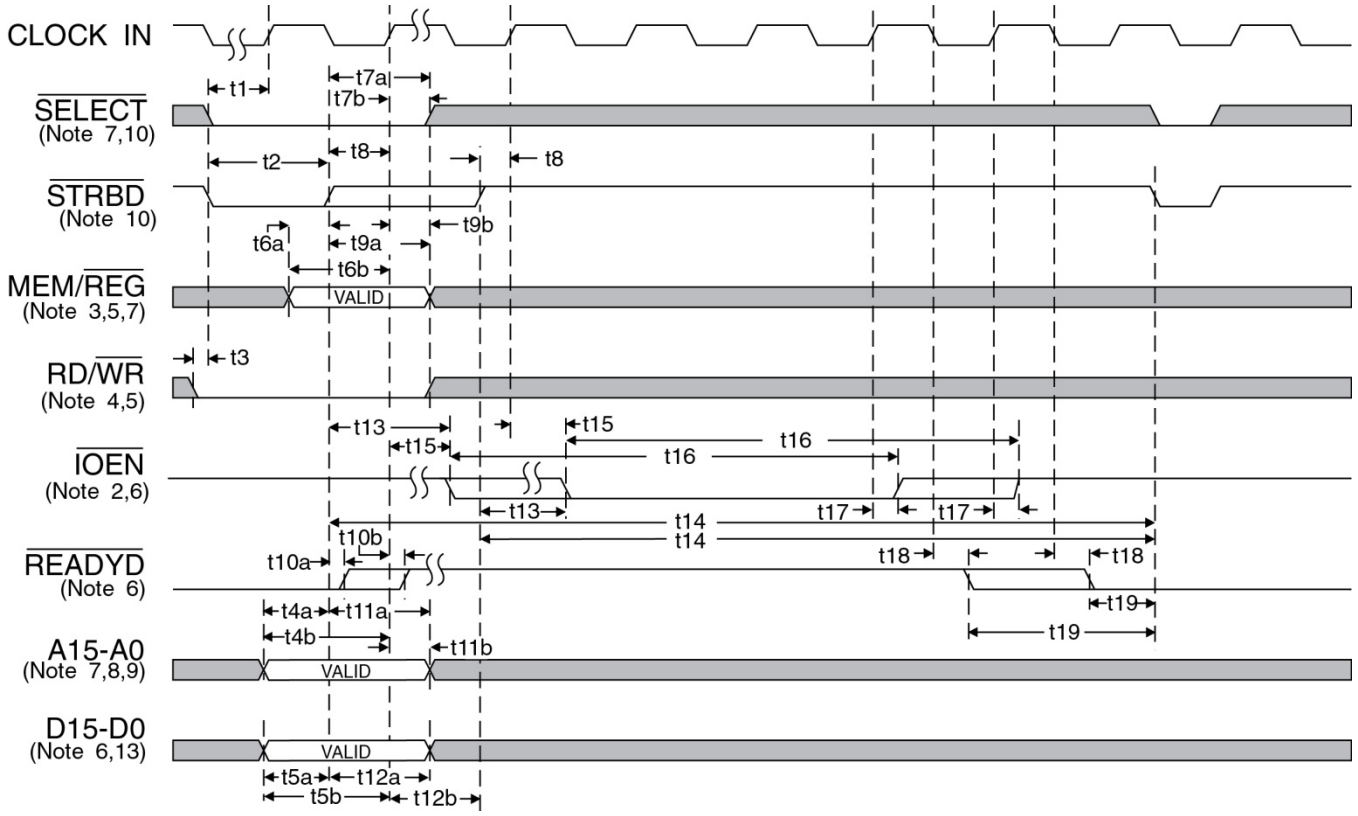



**Figure 25. CPU Writing RAM/Registers (16-Bit, Buffered, Zero Wait)**

**Notes for Table 8 and Figure 25**

1. For the 16-bit buffered configuration, the inputs TRIGGER_SEL and MSB/LSB may be connected to +5V or GND. For the zero wait interface, $\overline{\text{ZERO\_WAIT}}$ must be connected to logic "0."
2. $\overline{\text{IOEN}}$ goes low on the first rising CLK edge when $\overline{\text{READYD}}$ is low and $\overline{\text{STRBD}}$ is sampled high (satisfying t9 setup time) and the Enhanced Mini-ACE protocol/memory management logic is not accessing the internal RAM. When this occurs, $\overline{\text{IOEN}}$ goes low, starting the internal transfer.
3. MEM/$\overline{\text{REG}}$ must be presented high for memory access, low for register access.
4. MEM/$\overline{\text{REG}}$ and RD/$\overline{\text{WR}}$ are buffered transparently until latched by $\overline{\text{STRBD}}$ rising or second CLK edge. The logic sense for RD/$\overline{\text{WR}}$ in the diagram assumes that POLARITY_SEL is connected to logic "1." If POLARITY_SEL is connected to logic "0," RD/$\overline{\text{WR}}$ must be asserted high to write. The timing for $\overline{\text{IOEN}}$ and $\overline{\text{READYD}}$ outputs assumes a 50 pf load. For loading above 50 pf, the validity of $\overline{\text{IOEN}}$ and $\overline{\text{READYD}}$ is delayed by an additional 0.14 ns/pf typ, 0.28 ns/pf max.
7. Timing for A15-A0, MEM/$\overline{\text{REG}}$, and $\overline{\text{SELECT}}$ assumes ADDR-LAT is connected to logic "1." Refer to Address Latch timing for additional details.
8. Internal RAM is accessed by A15 through A0 (64K RAM Versions) or A11 through A0 (4K RAM Versions). Registers are accessed by A4 through A0.
9. The address bus A15-A0 is internally buffered transparently until latched by $\overline{\text{STRBD}}$ rising or second rising clock edge. The data bus starts to track when $\overline{\text{SELECT}}$ and $\overline{\text{STRBD}}$ are low until $\overline{\text{STRBD}}$ rises or second rising clock edge. To implement a single zero wait read operation, the host processor must perform two read accesses to the Enhanced Mini-ACE. During the first access, the address and transfer type indication (memory or register) of the location to be read must be asserted on A15-A0 and MEM/$\overline{\text{REG}}$, respectively. The data read on D15-D0 during this cycle should be ignored ("thrown away"). During the second read access, the Enhanced Mini-ACE presents the data corresponding to the address presented on the first access on D15-D0. If the CPU performs a multi-word read burst, the address for the next word should be presented on A15-A0 on the same cycle that data is read from D15-D0. That is, for a multi-word read transfer, the address presented should always be one location ahead of that of the data being read.
10. Setup time given for use in worst case timing calculations. These signals do not have to be synchronized to the system clock. Removal of $\overline{\text{SELECT}}$ prior to being latched on the second rising clock edge will have the same effect as STRBD* rising. For Enhanced Mini-ACE applications, transfer will not start until $\overline{\text{SELECT}}$ and $\overline{\text{STRBD}}$ are both low. $\overline{\text{SELECT}}$ must go low prior to the second rising clock edge after $\overline{\text{STRBD}}$ goes low or transfer will be blocked.
11. Data Bus will be actively driven when $\overline{\text{SELECT}}$ is low, $\overline{\text{STRBD}}$ is low and RD/$\overline{\text{WR}}$ is high. To prevent a bus crash between the host driving the Data Bus and the Enhanced Mini-ACE driving the Data Bus, RD/$\overline{\text{WR}}$ must be setup prior to $\overline{\text{SELECT}}$ low and $\overline{\text{STRBD}}$ low.
12. For the case in which $\overline{\text{STRBD}}$ goes high before second rising clock edge in which $\overline{\text{SELECT}}$ is low and $\overline{\text{STRBD}}$ is low. For case in which $\overline{\text{STRBD}}$ is low and $\overline{\text{SELECT}}$ is low for a minimum of two rising clock edges.
14. After $\overline{\text{STRBD}}$ is brought high and $\overline{\text{READYD}}$ asserted low, $\overline{\text{STRBD}}$ MUST be kept low until $\overline{\text{READYD}}$ returns high.

**Table 9. CPU Reading RAM/Registers (Transparent Mode)**

| REF | DESCRIPTION | 5V Logic | | | | 3.3V Logic | | | |
|---|---|---|---|---|---|---|---|---|---|
| | | NOTES | MIN | TYP | MAX | MIN | TYP | MAX | UNITS |
| t1 | $\overline{\text{SELECT}}$ and $\overline{\text{STRBD}}$ low setup time prior to CLOCK IN rising | 1 | 10 | | | 15 | | | ns |
| t2 | $\overline{\text{SELECT}}$ and $\overline{\text{STRBD}}$ low delay to $\overline{\text{IOEN}}$ low (uncontended access @20 MHz) | | | | 100 | | | 105 | ns |
| | $\overline{\text{SELECT}}$ and $\overline{\text{STRBD}}$ low delay to $\overline{\text{IOEN}}$ low (Contended access @ 20 MHz) | | | | 3.6 | | | 3.6 | us |
| | $\overline{\text{SELECT}}$ and $\overline{\text{STRBD}}$ low delay to $\overline{\text{IOEN}}$ low (uncontended access @16 MHz) | | | | 112 | | | 117 | ns |
| | $\overline{\text{SELECT}}$ and $\overline{\text{STRBD}}$ low delay to $\overline{\text{IOEN}}$ low (Contended access @ 16 MHz) | | | | 4.6 | | | 4.6 | us |
| | $\overline{\text{SELECT}}$ and $\overline{\text{STRBD}}$ low delay to $\overline{\text{IOEN}}$ low (uncontended access @12 MHz) | | | | 133 | | | 138 | ns |
| | $\overline{\text{SELECT}}$ and $\overline{\text{STRBD}}$ low delay to $\overline{\text{IOEN}}$ low (Contended access @ 12 MHz) | | | | 6.0 | | | 6.0 | us |
| | $\overline{\text{SELECT}}$ and $\overline{\text{STRBD}}$ low delay to $\overline{\text{IOEN}}$ low (uncontended access @10 MHz) | | | | 150 | | | 155 | ns |
| | $\overline{\text{SELECT}}$ and $\overline{\text{STRBD}}$ low delay to $\overline{\text{IOEN}}$ low (Contended access @ 10 MHz) | | | | 7.2 | | | 7.2 | us |
| t3 | CLOCK IN rising edge delay to $\overline{\text{IOEN}}$ falling | | | | 40 | | | 40 | ns |
| t4 | $\overline{\text{SELECT}}$ low hold time following $\overline{\text{IOEN}}$ falling | | 0 | | | 0 | | | ns |
| t5 | MEM/$\overline{\text{REG}}$ and RD/$\overline{\text{WR}}$ setup time prior to CLOCK IN falling | | 10 | | | 15 | | | ns |
| t6 | MEM/$\overline{\text{REG}}$ and RD/$\overline{\text{WR}}$ hold time following CLOCK IN falling | | 30 | | | 30 | | | ns |
| t7 | $\overline{\text{IOEN}}$ falling delay to $\overline{\text{READYD}}$ falling reading INT. RAM (@20 MHz) | | 185 | 200 | 215 | 185 | 200 | 215 | ns |
| | $\overline{\text{IOEN}}$ falling delay to $\overline{\text{READYD}}$ falling reading REG. or EXT. RAM (@20 MHz) | | 185 | 200 | 215 | 185 | 200 | 215 | ns |
| | $\overline{\text{IOEN}}$ falling delay to $\overline{\text{READYD}}$ falling reading INT. RAM (@16 MHz) | | 235 | 250 | 265 | 235 | 250 | 265 | ns |
| | $\overline{\text{IOEN}}$ falling delay to $\overline{\text{READYD}}$ falling reading REG. or EXT. RAM (@16 MHz) | | 235 | 250 | 265 | 235 | 250 | 265 | ns |
| | $\overline{\text{IOEN}}$ falling delay to $\overline{\text{READYD}}$ falling reading INT. RAM (@12 MHz) | | 315 | 333 | 350 | 315 | 333 | 350 | ns |
| | $\overline{\text{IOEN}}$ falling delay to $\overline{\text{READYD}}$ falling reading REG. or EXT. RAM (@12 MHz) | | 315 | 333 | 350 | 315 | 333 | 350 | ns |

## Table 9. CPU Reading RAM/Registers (Transparent Mode)

| REF | DESCRIPTION | 5V Logic | | | | 3.3V Logic | | | |
|---|---|---|---|---|---|---|---|---|---|
| | | NOTES | MIN | TYP | MAX | MIN | TYP | MAX | UNITS |
| | $\overline{\text{IOEN}}$ falling delay to $\overline{\text{READYD}}$ falling reading INT. RAM (@10 MHz) | | 385 | 400 | 415 | 385 | 400 | 415 | ns |
| | $\overline{\text{IOEN}}$ falling delay to $\overline{\text{READYD}}$ falling reading REG. or EXT. RAM (@10 MHz) | | 385 | 400 | 415 | 385 | 400 | 415 | ns |
| t8 | CLOCK IN rising delay to $\overline{\text{DTACK}}$ low | | | | 40 | | | 40 | ns |
| t9 | $\overline{\text{MEMENA\_IN}}$ setup time prior to CLOCK IN rising | | 10 | | | 10 | | | ns |
| t10 | $\overline{\text{MEMENA\_IN}}$ hold time following CLOCK IN rising | | 30 | | | 30 | | | ns |
| t11 | CLOCK IN rising delay to $\overline{\text{MEMOE}}$ falling | | | | 40 | | | 40 | ns |
| t12 | Address setup time prior to CLOCK IN rising | | 30 | | | 35 | | | ns |
| t13 | Address hold time following CLOCK IN rising | | 30 | | | 30 | | | ns |
| t14 | CLOCK IN rising to Output Data valid | | | | 40 | | | 40 | ns |
| t15 | CLOCK IN rising delay to $\overline{\text{READYD}}$ falling | | | | 40 | | | 40 | ns |
| t16 | $\overline{\text{STRBD}}$ release time following $\overline{\text{READYD}}$ falling (Internal RAM @20 MHz) | | | | 4.2 | | | 4.2 | us |
| | $\overline{\text{STRBD}}$ release time following $\overline{\text{READYD}}$ falling (External RAM @20 MHz) | | | | 4.2 | | | 4.2 | us |
| | $\overline{\text{STRBD}}$ release time following $\overline{\text{READYD}}$ falling (Internal RAM @16 MHz) | | | | 3.6 | | | 3.6 | us |
| | $\overline{\text{STRBD}}$ release time following $\overline{\text{READYD}}$ falling (External RAM @16 MHz) | | | | 3.6 | | | 3.6 | us |
| | $\overline{\text{STRBD}}$ release time following $\overline{\text{READYD}}$ falling (Internal RAM @12 MHz) | | | | 3.0 | | | 3.0 | us |
| | $\overline{\text{STRBD}}$ release time following $\overline{\text{READYD}}$ falling (External RAM @12 MHz) | | | | 3.0 | | | 3.0 | us |
| | $\overline{\text{STRBD}}$ release time following $\overline{\text{READYD}}$ falling (Internal RAM @10 MHz) | | | | 2.7 | | | 2.7 | us |
| | $\overline{\text{STRBD}}$ release time following $\overline{\text{READYD}}$ falling (External RAM @10 MHz) | | | | 2.7 | | | 2.7 | us |
| t17 | $\overline{\text{STRBD}}$ rising dly to $\overline{\text{IOEN}}$ rising, $\overline{\text{READYD}}$ rising, $\overline{\text{DTACK}}$ rising, $\overline{\text{MEMOE}}$ rising | | | | 30 | | | 40 | ns |
| t18 | Output Data hold time following $\overline{\text{STRBD}}$ rising | | 0 | | | 0 | | | ns |
| t19 | $\overline{\text{STRBD}}$ rising delay to Output Data tri-state | | | | 40 | | | 40 | ns |

| Table 9. CPU Reading RAM/Registers (Transparent Mode) | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| REF | DESCRIPTION | 5V Logic | | | | 3.3V Logic | | | |
| | | NOTES | MIN | TYP | MAX | MIN | TYP | MAX | UNITS |
| t20 | $\overline{\text{READYD}}$ rising delay to $\overline{\text{STRBD}}$ falling (delay to start of next transfer cycle) | | 0 | | | 0 | | | ns |

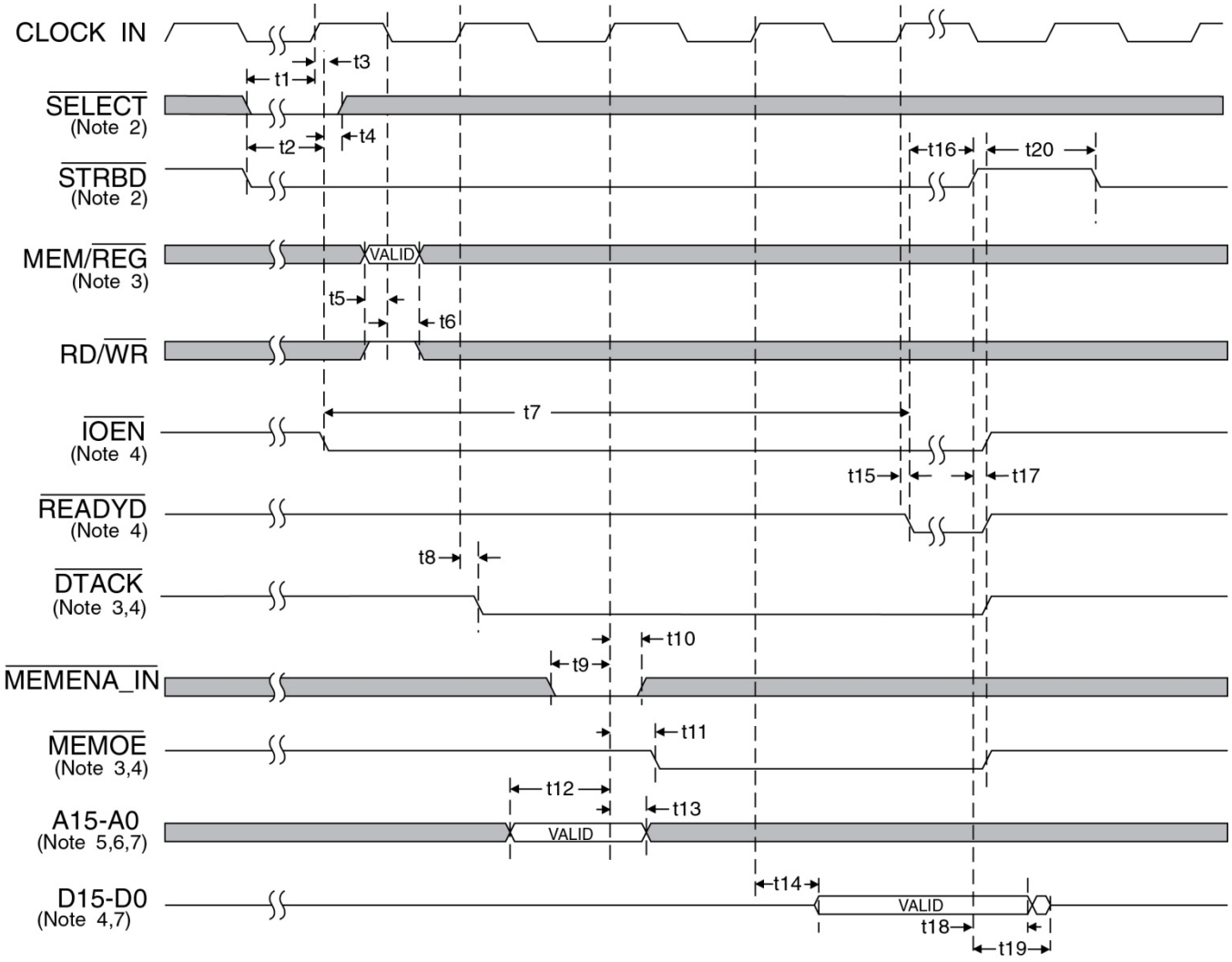



**Figure 26. CPU Reading RAM/Registers (Transparent Mode)**

Notes for Table 9 and Figure 26

1. Setup time given for use in worst case timing calculations. These signals do not have to be synchronized to the system clock.
2. $\overline{\text{SELECT}}$and $\overline{\text{STRBD}}$ may be tied together. $\overline{\text{IOEN}}$ goes low on the first rising CLK edge when $\overline{\text{SELECT}}$and $\overline{\text{STRBD}}$ are sampled low (satisfying t1) and the Enhanced Mini-ACE protocol/memory management logic is not actively performing a DMA transfer (i.e., $\overline{\text{DTACK}}$ is logic 1). When this occurs, $\overline{\text{IOEN}}$ goes low, starting the transfer cycle. After $\overline{\text{IOEN}}$ goes low, $\overline{\text{SELECT}}$ may be released high.
3. The timing diagram illustrates the CPU reading RAM. For register reads from the Enhanced Mini-ACE (MEM/$\overline{\text{REG}}$ input = logic 0) the $\overline{\text{DTACK}}$ and $\overline{\text{MEMOE}}$ output signals are not asserted, and therefore maintain a logic "1" level.
4. The timing for $\overline{\text{IOEN}}$, $\overline{\text{READYD}}$, $\overline{\text{DTACK}}$, $\overline{\text{MEMOE}}$, and D15-D0 assumes a 50 pf load. For loading above 50 pf, the validity of $\overline{\text{IOEN}}$, $\overline{\text{READYD}}$, $\overline{\text{DTACK}}$, $\overline{\text{MEMOE}}$, and D15-D0 is delayed by an additional 0.14 ns/pf typical, 0.28 ns/pf max.
5. Internal RAM is accessed by A15 through A0 (64K RAM Versions) or A11 through A0 (4K RAM Versions). Registers are accessed by A4 through A0.
6. The address bus A15-A0 is internally buffered transparently until the second rising edge of CLOCK_IN after $\overline{\text{IOEN}}$ goes low. After this CLOCK_IN edge, A15-A0 become latched internally.
7. For read operations from external memory, the address (A15-A0) must be held longer to meet the hold time requirements of the external memory used. The data bus (D15-D0) will remain in tri-state. D15-D0 will only be driven by the external RAM. All data bus timing will now be dependent on the external RAM used.

## Table 10. CPU Writing RAM/Registers (Transparent Mode)

| REF | DESCRIPTION | Notes | 5V Logic | | | 3.3V Logic | | | UNITS |
|---|---|---|---|---|---|---|---|---|---|
| | | | MIN | TYP | MAX | MIN | TYP | MAX | |
| t1 | $\overline{\text{SELECT}}$ and $\overline{\text{STRBD}}$ low setup time prior to CLOCK IN rising | 1 | 10 | | | 15 | | | ns |
| t2 | $\overline{\text{SELECT}}$ and $\overline{\text{STRBD}}$ low delay to $\overline{\text{IOEN}}$ low (uncontended access, @ 20 MHz) | | | | 100 | | | 105 | ns |
| | $\overline{\text{SELECT}}$ and $\overline{\text{STRBD}}$ low delay to $\overline{\text{IOEN}}$ low (Contended access, @ 20 MHz) | | | | 3.6 | | | 3.6 | us |
| | $\overline{\text{SELECT}}$ and $\overline{\text{STRBD}}$ low delay to $\overline{\text{IOEN}}$ low (Uncontended access, @ 16 MHz) | | | | 112 | | | 117 | ns |
| | $\overline{\text{SELECT}}$ and $\overline{\text{STRBD}}$ low delay to $\overline{\text{IOEN}}$ low (Contended access,@ 16 MHz) | | | | 4.6 | | | 4.6 | us |
| | $\overline{\text{SELECT}}$ and $\overline{\text{STRBD}}$ low delay to $\overline{\text{IOEN}}$ low (Uncontended access, @12 MHz) | | | | 133 | | | 138 | ns |
| | $\overline{\text{SELECT}}$ and $\overline{\text{STRBD}}$ low delay to $\overline{\text{IOEN}}$ low (Contended access, @ 12 MHz) | | | | 6.0 | | | 6.0 | us |
| | $\overline{\text{SELECT}}$ and $\overline{\text{STRBD}}$ low delay to $\overline{\text{IOEN}}$ low (Uncontended access, @ 10 MHz) | | | | 150 | | | 155 | ns |
| | $\overline{\text{SELECT}}$ and $\overline{\text{STRBD}}$ low delay to $\overline{\text{IOEN}}$ low (Contended access, @ 10 MHz) | | | | 7.2 | | | 7.2 | us |
| t3 | CLOCK IN rising edge delay to $\overline{\text{IOEN}}$ falling | | | | 40 | | | 40 | ns |
| t4 | $\overline{\text{SELECT}}$ low hold time following $\overline{\text{IOEN}}$ falling | | 0 | | | 0 | | | ns |
| t5 | MEM/$\overline{\text{REG}}$ and RD/$\overline{\text{WR}}$ setup time prior to CLOCK IN falling | | 10 | | | 15 | | | ns |
| t6 | MEM/$\overline{\text{REG}}$ and RD/$\overline{\text{WR}}$ hold time following CLOCK IN falling | | 30 | | | 30 | | | ns |
| t7 | $\overline{\text{IOEN}}$ falling delay to $\overline{\text{READYD}}$ falling (@ 20 MHz) | | 185 | 200 | 215 | 185 | 200 | 215 | ns |
| | $\overline{\text{IOEN}}$ falling delay to $\overline{\text{READYD}}$ falling (@ 16 MHz) | | 235 | 250 | 265 | 235 | 250 | 265 | ns |
| | $\overline{\text{IOEN}}$ falling delay to $\overline{\text{READYD}}$ falling (@ 12 MHz) | | 315 | 333 | 350 | 315 | 333 | 350 | ns |
| | $\overline{\text{IOEN}}$ falling delay to $\overline{\text{READYD}}$ falling (@ 10 MHz) | | 385 | 400 | 415 | 385 | 400 | 415 | ns |
| t8 | CLOCK IN rising delay to $\overline{\text{DTACK}}$ low | | | | 35 | | | 30 | ns |
| t9 | $\overline{\text{MEMENA\_IN}}$ setup time prior to CLOCK IN rising | | 5 | | | 10 | | | ns |
| t10 | $\overline{\text{MEMENA\_IN}}$ hold time following CLOCK IN rising | | 30 | | | 25 | | | ns |
| t11 | CLOCK IN rising delay to $\overline{\text{MEMWR}}$ falling | | | | 40 | | | 30 | ns |
| t12 | Address setup time prior to CLOCK IN rising | | 30 | | | 10 | | | ns |
| t13 | Address hold time following CLOCK IN rising | | 30 | | | 25 | | | ns |
| t14 | Input Data setup time prior to CLOCK IN rising | | 10 | | | 10 | | | ns |
| t15 | Input Data hold time following CLOCK IN rising | | 30 | | | 25 | | | ns |
| t16 | $\overline{\text{MEMWR}}$ low pulse width (@20 MHz) | | 37 | | 62 | 37 | | 62 | ns |
| | $\overline{\text{MEMWR}}$ low pulse width (@16 MHz) | | 50 | | 75 | 50 | | 75 | ns |
| | $\overline{\text{MEMWR}}$ low pulse width (@12 MHz) | | 70 | | 95 | 70 | | 95 | ns |
| | $\overline{\text{MEMWR}}$ low pulse width (@10 MHz) | | 87 | | 112 | 87 | | 112 | ns |

| Table 10. CPU Writing RAM/Registers (Transparent Mode) | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| REF | DESCRIPTION | Notes | 5V Logic | | | 3.3V Logic | | | UNITS |
| | | | MIN | TYP | MAX | MIN | TYP | MAX | |
| t17 | CLOCK IN rising delay to $\overline{\text{MEMWR}}$ rising | | | | 30 | | | 30 | ns |
| t18 | CLOCK IN rising delay to $\overline{\text{READYD}}$ falling | | | | 35 | | | 30 | ns |
| t19 | $\overline{\text{STRBD}}$ release time following $\overline{\text{READYD}}$ falling (@20 MHz) | | | | 4.2 | | | 4.2 | us |
| | $\overline{\text{STRBD}}$ release time following $\overline{\text{READYD}}$ falling (@16 MHz) | | | | 3.6 | | | 3.6 | us |
| | $\overline{\text{STRBD}}$ release time following $\overline{\text{READYD}}$ falling (@12 MHz) | | | | 3.0 | | | 3.0 | us |
| | $\overline{\text{STRBD}}$ release time following $\overline{\text{READYD}}$ falling (@10 MHz) | | | | 2.7 | | | 2.7 | us |
| t20 | $\overline{\text{STRBD}}$ rising delay to $\overline{\text{IOEN}}$ rising, $\overline{\text{READYD}}$ rising, and $\overline{\text{DTACK}}$ rising | | | | 30 | | | 35 | ns |
| t21 | $\overline{\text{READYD}}$ rising delay to $\overline{\text{STRBD}}$ falling (delay to start of next transfer cycle) | | 0 | | | 0 | | | ns |

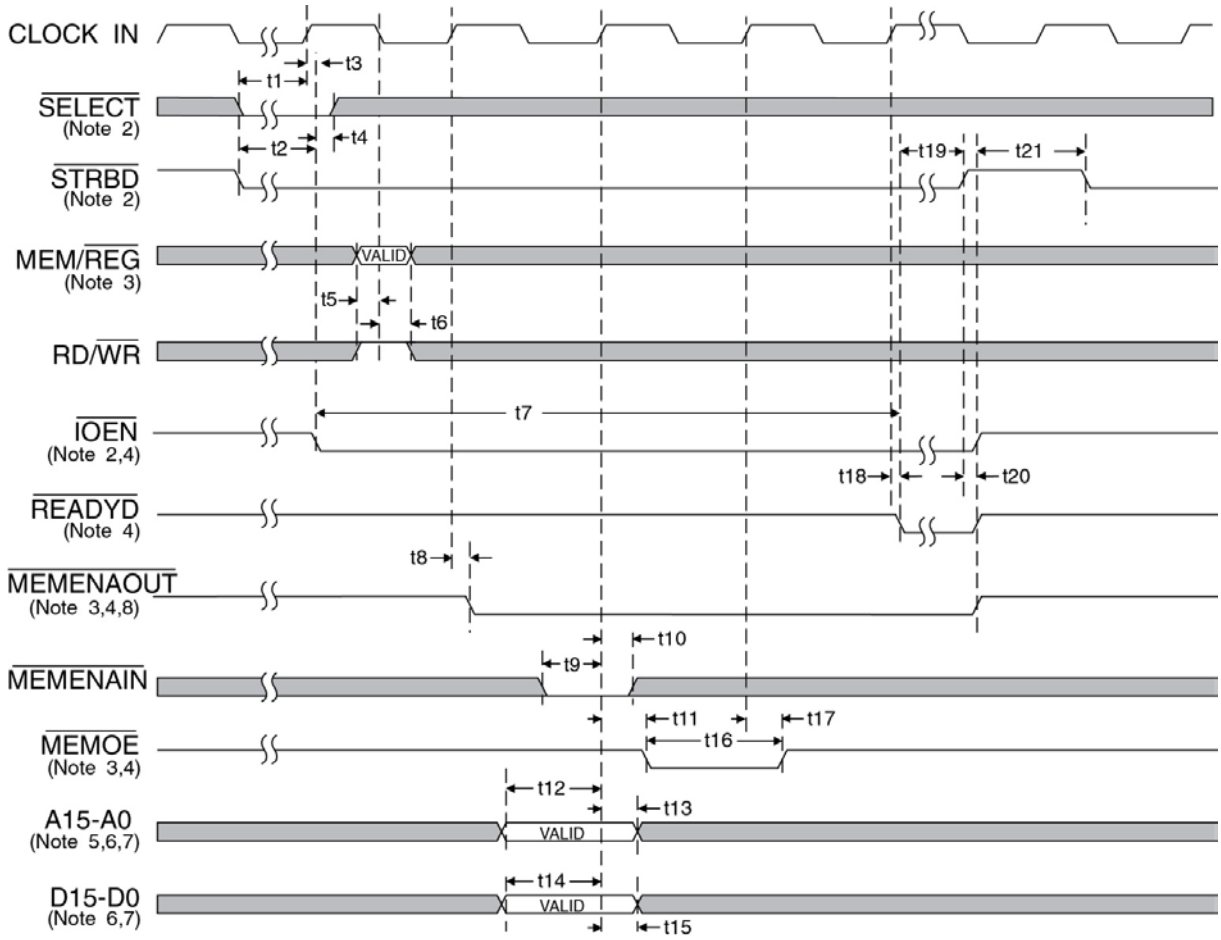



**Figure 27. CPU Writing RAM/Registers (Transparent Mode)**

Notes for Table 10 and Figure 27

1. Setup time given for use in worst case timing calculations. These signals do not have to be synchronized to the system clock.
2. $\overline{\text{SELECT}}$and $\overline{\text{STRBD}}$ may be tied together. $\overline{\text{IOEN}}$ goes low on the first rising CLK edge when $\overline{\text{SELECT}}$and $\overline{\text{STRBD}}$ is sampled low (satisfying t1) and the Enhanced Mini-ACE protocol/memory management logic is not active performing a DMA transfer (i.e., $\overline{\text{DTACK}}$ is logic 1). When this occurs, $\overline{\text{IOEN}}$ goes low, starting the transfer cycle. After $\overline{\text{IOEN}}$ goes low, $\overline{\text{SELECT}}$ may be released high.
3. The timing diagram illustrates the CPU writing to RAM. For register writes, the Enhanced Mini-ACE (MEM/$\overline{\text{REG}}$ input = logic 0) the $\overline{\text{DTACK}}$ and $\overline{\text{MEMWR}}$ output signals are not asserted, and therefore maintain a logic "1" level.
4. The timing for $\overline{\text{IOEN}}$, $\overline{\text{READYD}}$, $\overline{\text{DTACK}}$, and $\overline{\text{MEMWR}}$ assumes a 50 pf load. For loading above 50 pf, the validity of $\overline{\text{IOEN}}$, $\overline{\text{READYD}}$, $\overline{\text{DTACK}}$, and $\overline{\text{MEMWR}}$ is delayed by an additional 0.14 ns/pf typical, 0.28 ns/pf max.
5. Internal RAM is accessed by A15 through A0 (64K RAM Versions) or A11 through A0 (4K RAM Versions). Registers are accessed by A4 through A0.
6. The address bus A15-A0 and data bus D15-D0 are internally buffered transparently until the second rising edge of CLOCK_IN after $\overline{\text{IOEN}}$ goes low. After this CLOCK_IN edge, A15-A0 and D15-D0 become latched internally.
7. For write operation to external memory, the address (A15-A0) and data (D15-D0) must be held longer to meet the hold time requirements of the external memory used.

| Table 11. CPU Reading RAM/Registers (8-Bit NonZero Wait Mode) | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| REF | DESCRIPTION | NOTES | 5V LOGIC | | | 3.3V LOGIC | | | UNITS |
| | | | MIN | TYP | MAX | MIN | TYP | MAX | |
| t1 | $\overline{\text{SELECT}}$ and $\overline{\text{STRBD}}$ low setup time prior to clock rising edge | 2, 12 | 10 | | | 15 | | | ns |
| t2 | $\overline{\text{SELECT}}$ and $\overline{\text{STRBD}}$ low to $\overline{\text{IOEN}}$ low (uncontended access @ 20 MHz) | 2, 6 | | | 100 | | | 105 | ns |
| | (Contended access, with ENHANCED CPU ACCESS = “0” @ 20 MHz) | 2, 6 | | | 2.2 | | | 2.2 | µs |
| | (Contended access, with ENHANCED CPU ACCESS = “1” @ 20 MHz) | 2, 6 | | | 350 | | | 355 | ns |
| | (Uncontended access @ 16 MHz) | 2, 6 | | | 112 | | | 117 | ns |
| | (Contended access, with ENHANCED CPU ACCESS = “0” @ 16 MHz) | 2, 6 | | | 2.8 | | | 2.8 | µs |
| | (Contended access, with ENHANCED CPU ACCESS = “1” @ 16 MHz) | 2, 6 | | | 425 | | | 430 | ns |
| | (Uncontended access @ 12 MHz) | 2, 6 | | | 133 | | | 138 | ns |
| | (Contended access, with ENHANCED CPU ACCESS = “0” @ 12 MHz) | 2, 6 | | | 3.7 | | | 3.7 | µs |
| | (Contended access, with ENHANCED CPU ACCESS = “1” @ 12 MHz) | 2, 6 | | | 550 | | | 555 | ns |
| | (Uncontended access @ 10 MHz) | 2, 6 | | | 150 | | | 155 | ns |
| | (Contended access, with ENHANCED CPU ACCESS = “0” @ 10 MHz) | 2, 6 | | | 4.4 | | | 4.4 | µs |
| | (Contended access, with ENHANCED CPU ACCESS = “1” @ 10 MHz) | 2, 6 | | | 650 | | | 655 | ns |
| t3 | Address valid setup time prior to CLOCK IN rising edge | | 30 | | | 35 | | | ns |
| t4 | $\overline{\text{SELECT}}$ hold time following $\overline{\text{IOEN}}$ falling | 2 | 0 | | | 0 | | | ns |
| t5 | MEM/$\overline{\text{REG}}$, RD/$\overline{\text{WR}}$, MSB/LSB setup time prior to CLOCK IN falling edge | 3,4,5,10 ,11 | 10 | | | 15 | | | ns |
| t6 | MEM/$\overline{\text{REG}}$, RD/$\overline{\text{WR}}$, MSB/LSB hold time following CLOCK IN falling edge | 3,4,5,10 ,11 | 30 | | | 30 | | | ns |
| t7 | Address hold time following CLOCK IN rising edge | 9 | 30 | | | 30 | | | ns |
| t8 | $\overline{\text{IOEN}}$ falling delay to $\overline{\text{READYD}}$ falling (@ 20 MHz) | 6 | 185 | 200 | 215 | 185 | 200 | 215 | ns |
| | @ 16 MHz | 6 | 235 | 250 | 265 | 235 | 250 | 265 | ns |
| | @ 12 MHz | 6 | 318 | 333 | 348 | 318 | 333 | 348 | ns |
| | @ 10 MHz | 6 | 385 | 400 | 415 | 385 | 400 | 415 | ns |
| t9 | Output Data valid prior to $\overline{\text{READYD}}$ falling (@20 MHz) | 6,10,11 | 22 | | | 12 | | | ns |
| | @ 16 MHz | 6,10,11 | 33 | | | 23 | | | ns |
| | @ 12 MHz | 6,10,11 | 54 | | | 44 | | | ns |
| | @ 10 MHz | 6,10,11 | 72 | | | 62 | | | ns |

| Table 11. CPU Reading RAM/Registers (8-Bit NonZero Wait Mode) | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| REF | DESCRIPTION | NOTES | 5V LOGIC | | | 3.3V LOGIC | | | UNITS |
| | | | MIN | TYP | MAX | MIN | TYP | MAX | |
| t10 | CLOCK IN rising edge delay to $\overline{\text{READYD}}$ falling | 6 | | | 40 | | | 40 | ns |
| t11 | $\overline{\text{READYD}}$ falling to $\overline{\text{STRBD}}$ rising release time | 6 | | | ∞ | | | ∞ | ns |
| t12 | $\overline{\text{STRBD}}$ rising edge delay to $\overline{\text{IOEN}}$ rising edge and $\overline{\text{READYD}}$ rising edge | 6 | | | 30 | | | 40 | ns |
| t13 | Output Data hold time following $\overline{\text{STRBD}}$ rising edge | | 0 | | | 0 | | | ns |
| t14 | $\overline{\text{STRBD}}$ rising delay to output data tri-state | | | | 40 | | | 40 | ns |
| t15 | $\overline{\text{STRBD}}$ high hold time from $\overline{\text{READYD}}$ rising | | 0 | | | 0 | | | ns |
| t16 | CLOCK IN rising edge delay to $\overline{\text{IOEN}}$ falling edge | | | | 40 | | | 40 | ns |
| t17 | CLOCK IN rising edge delay to output data valid | | | | 40 | | | 40 | ns |

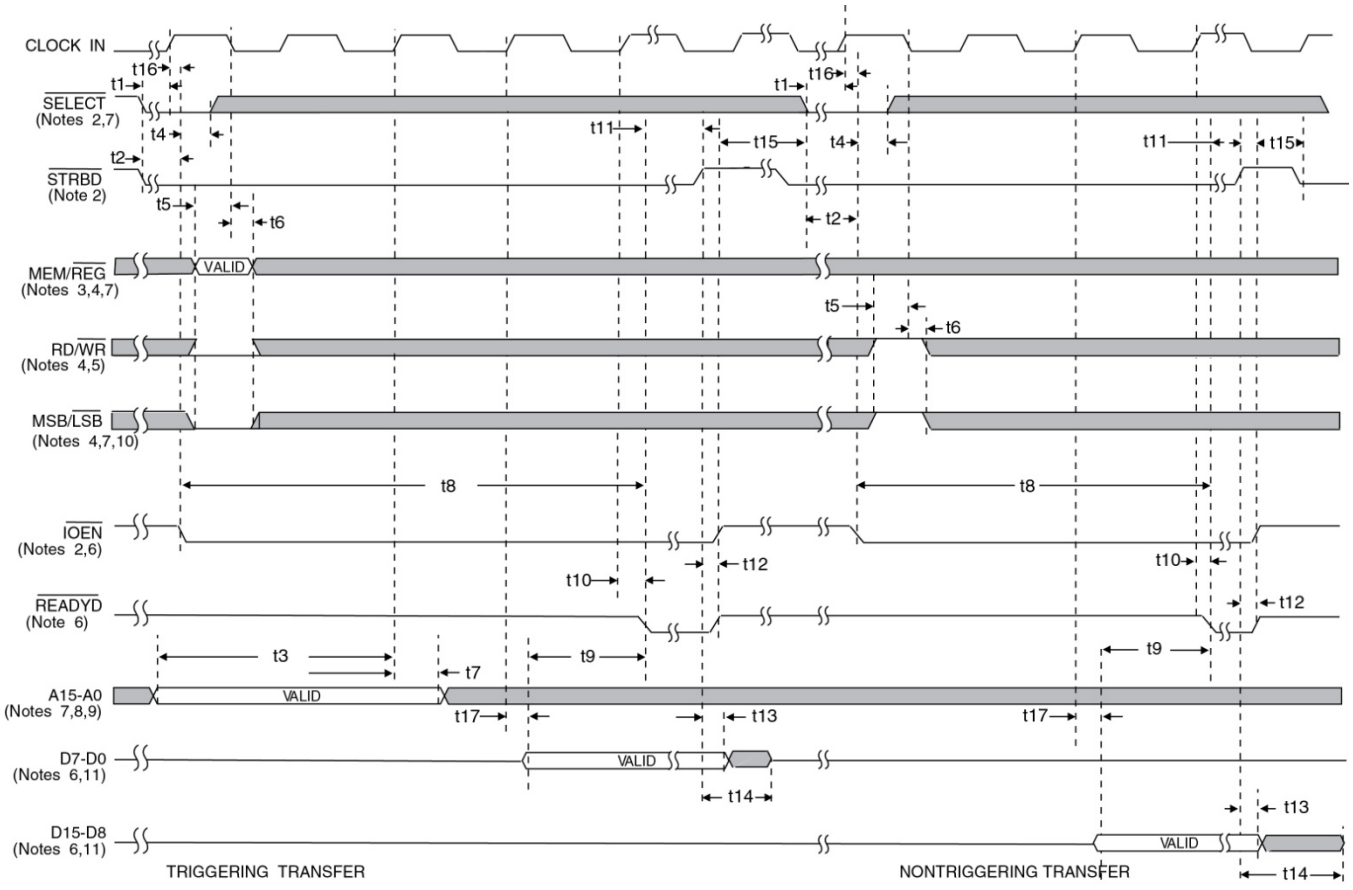



**Figure 28. CPU Reading RAM/Registers (8-Bit, Nonzero Wait)**

Notes for Table 11 and Figure 24

1. For 8-bit nonzero wait interface, TRANSPARENT/$\overline{\text{BUFFERED}}$ and 16/$\overline{8}$/$\overline{\text{DTREQ}}$ must be connected to logic "0". must be connected to logic "1".
2. $\overline{\text{SELECT}}$ and $\overline{\text{STRBD}}$ may be tied together. $\overline{\text{IOEN}}$ goes low on the first rising CLK edge when $\overline{\text{SELECT}}$ and $\overline{\text{STRBD}}$ are both sampled low (satisfying $t_1$) and the Enhanced Mini-ACE protocol/memory management logic is not accessing the internal RAM. When this occurs, $\overline{\text{IOEN}}$ goes low, starting the transfer cycle. After $\overline{\text{IOEN}}$ goes low, $\overline{\text{SELECT}}$ may be released high.
3. MEM/$\overline{\text{REG}}$ must be presented high for memory access, low for register access. MEM/$\overline{\text{REG}}$ is a "don't care" for non-triggering transfers.
4. MEM/$\overline{\text{REG}}$, MSB/$\overline{\text{LSB}}$ and RD/$\overline{\text{WR}}$ are buffered transparently until the first falling edge of CLK after $\overline{\text{IOEN}}$ goes low. After CLK edge, MEM/$\overline{\text{REG}}$, MSB/$\overline{\text{LSB}}$ and RD/$\overline{\text{WR}}$ become latched internally.
5. RD/$\overline{\text{WR}}$ must be presented high for read accesses and low for write accesses. The logic sense for RD/$\overline{\text{WR}}$ does not depend the state of the POL_SEL input in the 8-bit mode.
6. The timing for $\overline{\text{IOEN}}$, $\overline{\text{READYD}}$ and D15-D0 assumes a 50 pf load. For loading above 50 pf, the validity of $\overline{\text{IOEN}}$, $\overline{\text{READYD}}$, and D15-D0 is delayed by an additional 0.14 ns/pf typ, 0.28 ns/pf max.
7. Timing for A15-A0, MEM/$\overline{\text{REG}}$, $\overline{\text{SELECT}}$ and MSB/$\overline{\text{LSB}}$ assumes ADDR_LAT is connected to logic "1." Refer to Address timing for additional details.
8. Internal RAM is accessed by A15 through A0 (64K RAM Versions) or A11 through A0 (4K RAM Versions). Registers are accessed by A4 through A0.
9. The address bus A15-A0 is internally buffered transparently until the first rising edge of CLK after $\overline{\text{IOEN}}$ goes low. After this CLK edge, A15-A0 become latched internally.
10. The polarity of the MSB/$\overline{\text{LSB}}$ input signal assumes that the POL_SEL input signal is connected to logic "0." If POL_SEL is connected to logic "1," MSB/$\overline{\text{LSB}}$ will be high for LSB transfers and low for MSB transfers.
11. The order of the consecutive byte transfers assumes that the TRIG_SEL input signal is connected to logic "0." The actual transfer from the internal RAM or Register takes place during the "triggering transfer" (LSB in this case). If TRIG_SEL is connected to logic "1," the order of the byte transfers would be MSB followed by LSB and the triggering transfer would be the MSB.
12. Setup time given for use in worst case timing calculations. None of the Enhanced Mini-ACE input signals are required to be synchronized to the system clock.

| Table 12. CPU Writing RAM/Registers (8-Bit, NonZero Wait Mode) | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| REF | DESCRIPTION | NOTES | 5V LOGIC | | | 3.3V LOGIC | | | UNITS |
| | | | MIN | TYP | MAX | MIN | TYP | MAX | |
| t1 | $\overline{\text{SELECT}}$ and $\overline{\text{STRBD}}$ low setup time prior to clock rising edge | 2, 12 | 10 | | | 15 | | | ns |
| t2 | $\overline{\text{SELECT}}$ and $\overline{\text{STRBD}}$ low to $\overline{\text{IOEN}}$ low (uncontended access @ 20 MHz) | 2, 6 | | | 100 | | | 105 | ns |
| | (Contended access, with ENHANCED CPU ACCESS = “0” @ 20 MHz) | 2, 6 | | | 3.6 | | | 3.6 | µs |
| | (Contended access, with ENHANCED CPU ACCESS = “1” @ 20 MHz) | 2, 6 | | | 350 | | | 355 | ns |
| | (Uncontended access @ 16 MHz) | 2, 6 | | | 112 | | | 117 | ns |
| | (Contended access, with ENHANCED CPU ACCESS = “0” @ 16 MHz) | 2, 6 | | | 4.6 | | | 4.6 | µs |
| | (Contended access, with ENHANCED CPU ACCESS = “1” @ 16 MHz) | 2, 6 | | | 425 | | | 430 | ns |
| | (Uncontended access @ 12 MHz) | 2, 6 | | | 133 | | | 138 | ns |
| | (Contended access, with ENHANCED CPU ACCESS = “0” @ 12 MHz) | 2, 6 | | | 6.0 | | | 6.0 | µs |
| | (Contended access, with ENHANCED CPU ACCESS = “1” @ 12 MHz) | 2, 6 | | | 550 | | | 555 | ns |
| | (Uncontended access @ 10 MHz) | 2, 6 | | | 150 | | | 155 | ns |
| | (Contended access, with ENHANCED CPU ACCESS = “0” @ 10 MHz) | 2, 6 | | | 7.2 | | | 7.2 | µs |
| | (Contended access, with ENHANCED CPU ACCESS = “1” @ 10 MHz) | 2, 6 | | | 650 | | | 655 | ns |
| t3 | Address valid setup time prior to CLOCK IN rising edge | 7,8 | 30 | | | 35 | | | ns |
| t4 | $\overline{\text{SELECT}}$ hold time following $\overline{\text{IOEN}}$ falling | 2 | 0 | | | 0 | | | ns |
| t5 | MEM/$\overline{\text{REG}}$, RD/$\overline{\text{WR}}$, MSB/LSB setup time prior to CLOCK IN falling edge | 3,4,5,10,11 | 10 | | | 15 | | | ns |
| t6 | MEM/$\overline{\text{REG}}$, RD/$\overline{\text{WR}}$, MSB/LSB setup time following CLOCK IN falling edge | 3,4,5,10,11 | 30 | | | 30 | | | ns |
| t7 | Address and Data valid hold time following CLOCK IN rising edge | 9 | 30 | | | 30 | | | ns |
| t8 | $\overline{\text{IOEN}}$ falling delay to $\overline{\text{READYD}}$ falling @ 20 MHz | 6 | 135 | 150 | 165 | 135 | 150 | 165 | ns |
| | @ 16 MHz | 6 | 172.5 | 187.5 | 202.5 | 172.5 | 187.5 | 202.5 | ns |
| | @ 12 MHz | 6 | 235 | 250 | 265 | 235 | 250 | 265 | ns |
| | @ 10 MHz | 6 | 285 | 300 | 315 | 285 | 300 | 315 | ns |
| t9 | CLOCK IN rising edge delay to $\overline{\text{READYD}}$ falling | | | | 40 | | | 40 | ns |

| Table 12. CPU Writing RAM/Registers (8-Bit, NonZero Wait Mode) | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| REF | DESCRIPTION | NOTES | 5V LOGIC | | | 3.3V LOGIC | | | UNITS |
| | | | MIN | TYP | MAX | MIN | TYP | MAX | |
| t10 | $\overline{\text{READYD}}$ falling to $\overline{\text{STRBD}}$ rising release time | | | | ∞ | | | ∞ | ns |
| t11 | $\overline{\text{STRBD}}$ rising edge delay to $\overline{\text{IOEN}}$ rising edge and $\overline{\text{READYD}}$ rising edge | | | | 30 | | | 40 | ns |
| t12 | $\overline{\text{STRBD}}$ high hold time from $\overline{\text{READYD}}$ rising | | 10 | | | 10 | | | ns |
| t13 | Input Data valid setup time prior to CLOCK IN rising edge | | 10 | | | 15 | | | ns |
| t14 | Clock in rising edge delay to $\overline{\text{IOEN}}$ falling edge | | | | 40 | | | 40 | ns |

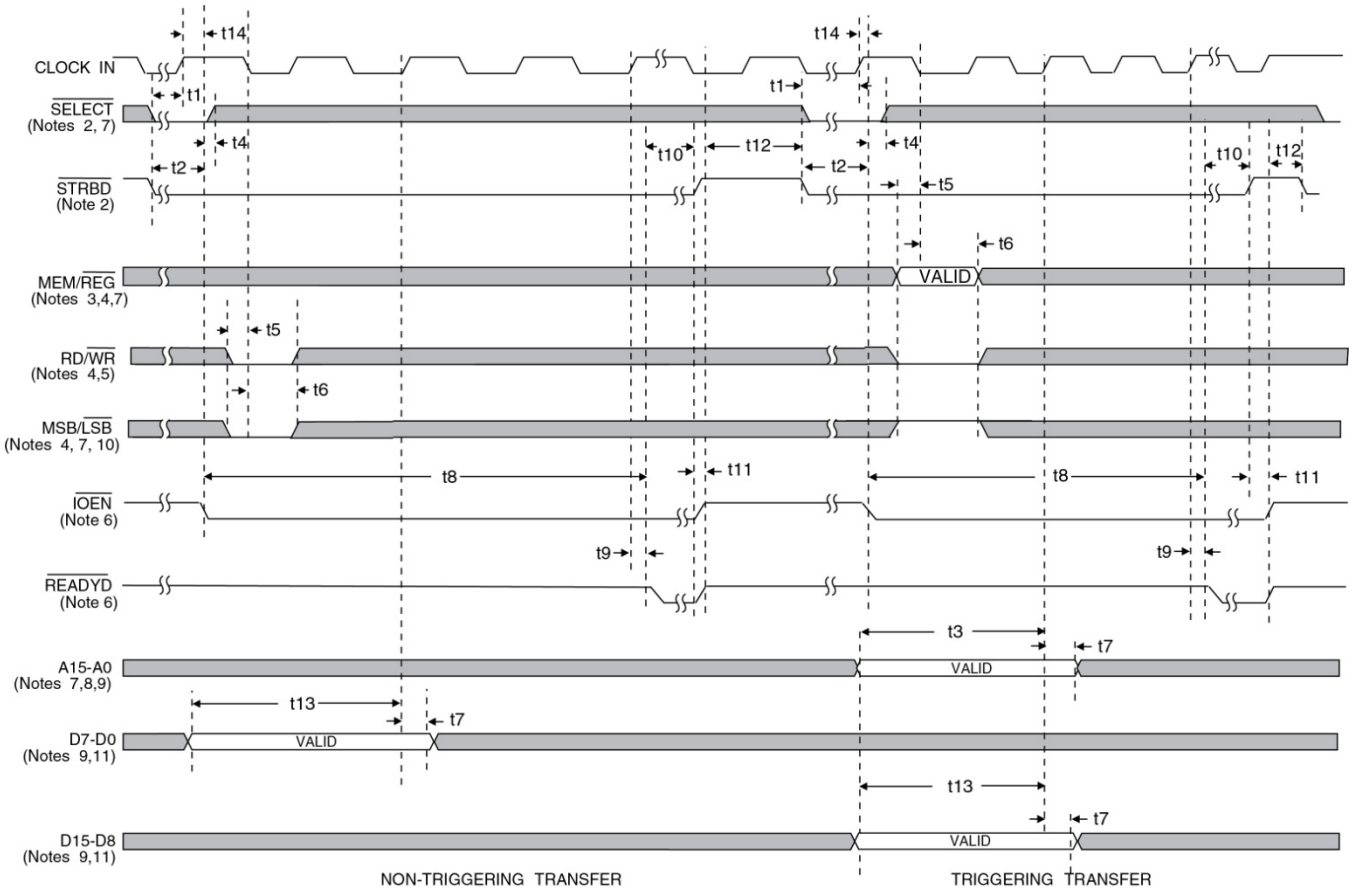



**Figure 29. CPU Writing RAM/Registers (8-Bit, Nonzero Wait)**

Notes for Table 12 and Figure 29

1. For 8-bit nonzero wait interface, TRANSPARENT/$\overline{\text{BUFFERED}}$ and 16/$\overline{8}$/$\overline{\text{DTREQ}}$ must be connected to logic "0." $\overline{\text{ZEROWAIT}}$ must be connected to logic "1."
2. $\overline{\text{SELECT}}$ and $\overline{\text{STRBD}}$ may be tied together. $\overline{\text{IOEN}}$ goes low on the first rising CLK edge when $\overline{\text{SELECT}}$ and $\overline{\text{STRBD}}$ are both sampled low (satisfying $t_2$) and the Enhanced Mini-ACE protocol/memory management logic is not accessing the internal RAM. When this occurs, $\overline{\text{IOEN}}$ goes low, starting the transfer cycle. After $\overline{\text{IOEN}}$ goes low, $\overline{\text{SELECT}}$ may be released high.
3. MEM/$\overline{\text{REG}}$ must be presented high for memory access, low for register access. MEM/$\overline{\text{REG}}$ is a "don't care" for non-triggering transfers.
4. MEM/$\overline{\text{REG}}$, MSB/$\overline{\text{LSB}}$, and RD/$\overline{\text{WR}}$ are buffered transparently until the first falling edge of CLK after $\overline{\text{IOEN}}$ goes low. After this CLK edge, MEM/$\overline{\text{REG}}$, MSB/$\overline{\text{LSB}}$, and RD/$\overline{\text{WR}}$ become latched internally.
5. RD/$\overline{\text{WR}}$ must be presented high for read accesses and low for write accesses. The logic sense for RD/$\overline{\text{WR}}$ does not depend on the state of the POL_SEL input in the 8-bit mode.
6. The timing for $\overline{\text{IOEN}}$ and $\overline{\text{READY}}$ outputs assumes a 50 pf load. For loading above 50 pf, the validity of $\overline{\text{IOEN}}$ and $\overline{\text{READY}}$ is delayed by an additional 0.14 ns/pf typ, 0.28 ns/pf max.
7. Timing for A15-A0, MEM/$\overline{\text{REG}}$, $\overline{\text{SELECT}}$ and MSB/$\overline{\text{LSB}}$ assumes ADDR_LAT is connected to logic "1." Refer to Address Latch timing for additional details.
8. Internal RAM is accessed by A15 through A0 (64K RAM Versions) or A11 through A0 (4K RAM Versions). Registers are accessed by A4 through A0.
9. The address bus A15-A0 and data bus D15-D0 are internally buffered transparently until the first rising edge of CLK after $\overline{\text{IOEN}}$ goes low. After this CLK edge, A15-A0 and D15-D0 become latched internally.
10. The polarity of the MSB/$\overline{\text{LSB}}$ input signal assumes that the POL_SEL input signal is connected to logic "0." If POL_SEL is connected to logic "1," MSB/$\overline{\text{LSB}}$ will be high for LSB transfers and low for MSB transfers.
11. The order of the consecutive byte transfers assumes that the TRIG_SEL input signal is connected to logic "0." The actual transfer to the internal RAM or Register takes place during the "triggering transfer" (MSB in this case). If TRIG_SEL is connected to logic "1," the order of the byte transfers would be MSB followed by LSB and the triggering transfer would LSB.
12. Setup time given for use in worst case timing calculations. None of the Enhanced Mini-ACE input signals are required to synchronized to the system clock.

| Table 13. CPU Reading RAM/Registers (8-Bit, Zero Wait Mode) | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| REF | DESCRIPTION | Notes | 5V Logic | | | 3.3V Logic | | | UNITS |
| | | | MIN | TYP | MAX | MIN | TYP | MAX | |
| t1 | RD/ $\overline{WR}$ and MSB/ $\overline{LSB}$ setup time prior to $\overline{STRBD}$ and $\overline{SELECT}$ falling | 11 | 10 | | | 15 | | | ns |
| t2 | $\overline{SELECT}$ and $\overline{STRBD}$ low setup time prior to CLOCK IN rising | 10 | 10 | | | 15 | | | ns |
| t3 | $\overline{SELECT}$ and $\overline{STRBD}$ low minimum pulse width | | 20 | | | 25 | | | ns |
| t4 | $\overline{SELECT}$ and $\overline{STRBD}$ low delay to Data valid | 14 | | | 35 | | | 40 | ns |
| t5 | RD/ $\overline{WR}$ and MSB/LSB delay to Data valid | 14 | | | 45 | | | 50 | ns |
| t6A | MEM/ $\overline{REG}$ setup time prior to $\overline{STRBD}$ rising | 11 | 10 | | | 10 | | | ns |
| t6B | MEM/ $\overline{REG}$ setup time prior to CLOCK IN rising | 12 | 10 | | | 10 | | | ns |
| t7A | MEM/ $\overline{REG}$ , RD/ $\overline{WR}$ , MSB/ $\overline{LSB}$ hold time following $\overline{STRBD}$ rising | 11 | 20 | | | 20 | | | ns |
| t7B | MEM/ $\overline{REG}$ , RD/ $\overline{WR}$ , MSB/ $\overline{LSB}$ hold time following CLOCK IN rising | 12 | 25 | | | 25 | | | ns |
| t8A | Address setup time prior to $\overline{STRBD}$ rising | 11 | 10 | | | 10 | | | ns |
| t8B | Address setup time prior to CLOCK IN rising | 12 | 10 | | | 10 | | | ns |
| t9A | Address hold time following $\overline{STRBD}$ rising | 11 | 20 | | | 20 | | | ns |
| t9B | Address hold time following CLOCK IN rising | 12 | 30 | | | 30 | | | ns |
| t10 | Output Data hold time following $\overline{STRBD}$ rising | | 0 | | | 0 | | | ns |
| t11 | $\overline{STRBD}$ rising delay to Data tri-state | | | | 35 | | | 40 | ns |
| t12 | $\overline{STRBD}$ rising delay to $\overline{IOEN}$ low (uncontended access @20 MHz) | | | | 107 | | | 112 | ns |
| | (Contended access, with ENHANCED CPU ACCESS = “0” @ 20 MHz) | | | | 3.6 | | | 3.6 | us |
| | (Contended access, with ENHANCED CPU ACCESS = “1” @ 20 MHz) | | | | 357 | | | 362 | ns |
| | $\overline{STRBD}$ rising delay to $\overline{IOEN}$ low (uncontended access @16 MHz) | | | | 120 | | | 125 | ns |
| | (Contended access, with ENHANCED CPU ACCESS = “0” @ 16 MHz) | | | | 4.6 | | | 4.6 | us |
| | (Contended access, with ENHANCED CPU ACCESS = “1” @ 16 MHz) | | | | 432 | | | 437 | ns |
| | $\overline{STRBD}$ rising delay to $\overline{IOEN}$ low (uncontended access @12 MHz) | | | | 140 | | | 145 | ns |
| | (Contended access, with ENHANCED CPU ACCESS = “0” @ 12 MHz) | | | | 6.0 | | | 6.0 | us |
| | (Contended access, with ENHANCED CPU ACCESS = “1” @ 12 MHz) | | | | 557 | | | 562 | ns |
| | $\overline{STRBD}$ rising delay to $\overline{IOEN}$ low (uncontended access @10 MHz) | | | | 157 | | | 162 | ns |
| | (Contended access, with ENHANCED CPU ACCESS = “0” @ 10 MHz) | | | | 7.2 | | | 7.2 | us |
| | (Contended access, with ENHANCED CPU ACCESS = “1” @ 10 MHz) | | | | 657 | | | 662 | ns |
| t13A | $\overline{STRBD}$ rising delay to $\overline{READYD}$ low | 11 | | | 30 | | | 30 | ns |
| t13B | CLOCK IN rising delay to $\overline{READYD}$ low | 12 | | | 35 | | | 35 | ns |

| Table 13. CPU Reading RAM/Registers (8-Bit, Zero Wait Mode) | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| REF | DESCRIPTION | Notes | 5V Logic | | | 3.3V Logic | | | UNITS |
| | | | MIN | TYP | MAX | MIN | TYP | MAX | |
| t14 | CLOCK IN rising to $\overline{\text{IOEN}}$ low | | | | 40 | | | 40 | ns |
| t15A | $\overline{\text{SELECT}}$ low hold time following $\overline{\text{STRBD}}$ rising | 11 | 0 | | | 0 | | | ns |
| t15B | $\overline{\text{SELECT}}$ low hold time following CLOCK IN rising | 12 | 25 | | | 25 | | | ns |
| t16 | $\overline{\text{STRBD}}$ rising setup time prior to CLOCK IN rising | 10 | 15 | | | 15 | | | ns |
| t17 | $\overline{\text{IOEN}}$ low pulse width for RAM read (@20 MHz) | | 185 | 200 | 215 | 185 | 200 | 215 | ns |
| | $\overline{\text{IOEN}}$ low pulse width for REGISTER read (@20 MHz) | | 185 | 200 | 215 | 185 | 200 | 215 | ns |
| | $\overline{\text{IOEN}}$ low pulse width for RAM read (@16 MHz) | | 235 | 250 | 265 | 235 | 250 | 265 | ns |
| | $\overline{\text{IOEN}}$ low pulse width for REGISTER read (@16 MHz) | | 235 | 250 | 265 | 235 | 250 | 265 | ns |
| | $\overline{\text{IOEN}}$ low pulse width for RAM read (@12 MHz) | | 315 | 333 | 350 | 315 | 333 | 350 | ns |
| | $\overline{\text{IOEN}}$ low pulse width for REGISTER read (@12 MHz) | | 315 | 333 | 350 | 315 | 333 | 350 | ns |
| | $\overline{\text{IOEN}}$ low pulse width for RAM read (@10 MHz) | | 385 | 400 | 415 | 385 | 400 | 415 | ns |
| | $\overline{\text{IOEN}}$ low pulse width for REGISTER read (@10 MHz) | | 385 | 400 | 415 | 385 | 400 | 415 | ns |
| t18 | $\overline{\text{STRBD}}$ rising delay to start of next transfer (uncontended access @20 MHz) | 13 | 320 | | | 325 | | | ns |
| | (Contended access, with ENHANCED CPU ACCESS = “0” @ 20 MHz) | 13 | 2.5 | | | 2.5 | | | us |
| | (Contended access, with ENHANCED CPU ACCESS = “1” @ 20 MHz) | 13 | 920 | | | 925 | | | ns |
| | $\overline{\text{STRBD}}$ rising delay to start of next transfer (uncontended access @16 MHz) | 13 | 395 | | | 400 | | | ns |
| | (Contended access, with ENHANCED CPU ACCESS = “0” @ 16 MHz) | 13 | 3.1 | | | 3.1 | | | us |
| | (Contended access, with ENHANCED CPU ACCESS = “1” @ 16 MHz) | 13 | 1.15 | | | 1.15 | | | us |
| | $\overline{\text{STRBD}}$ rising delay to start of next transfer (uncontended access @12 MHz) | 13 | 520 | | | 525 | | | ns |
| | (Contended access, with ENHANCED CPU ACCESS = “0” @ 12 MHz) | 13 | 4.1 | | | 4.1 | | | us |
| | (Contended access, with ENHANCED CPU ACCESS = “1” @ 12 MHz) | 13 | 1.52 | | | 1.52 | | | us |
| | $\overline{\text{STRBD}}$ rising delay to start of next transfer (uncontended access @10 MHz) | 13 | 620 | | | 625 | | | ns |
| | (Contended access, with ENHANCED CPU ACCESS = “0” @ 10 MHz) | 13 | 4.9 | | | 4.9 | | | us |
| | (Contended access, with ENHANCED CPU ACCESS = “1” @ 10 MHz) | 13 | 1.82 | | | 1.82 | | | us |
| t19 | CLOCK IN rising delay to $\overline{\text{IOEN}}$ rising | | | | 35 | | | 35 | ns |
| t20 | CLOCK IN falling delay to $\overline{\text{STRBD}}$ rising | | | | 35 | | | 35 | ns |
| t21 | $\overline{\text{STRBD}}$ rising delay to start of next transfer ($\overline{\text{SELECT}}$ and $\overline{\text{STRBD}}$ low) | | 20 | | | 20 | | | ns |

| Table 13. CPU Reading RAM/Registers (8-Bit, Zero Wait Mode) | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| REF | DESCRIPTION | Notes | 5V Logic | | | 3.3V Logic | | | UNITS |
| | | | MIN | TYP | MAX | MIN | TYP | MAX | |
| | trigger | | | | | | | | |
| t22 | $\overline{\text{READYD}}$ high to $\overline{\text{STRBD}}$ and $\overline{\text{SELECT}}$ low (Next transfer) | | 0 | | | 0 | | | ns |

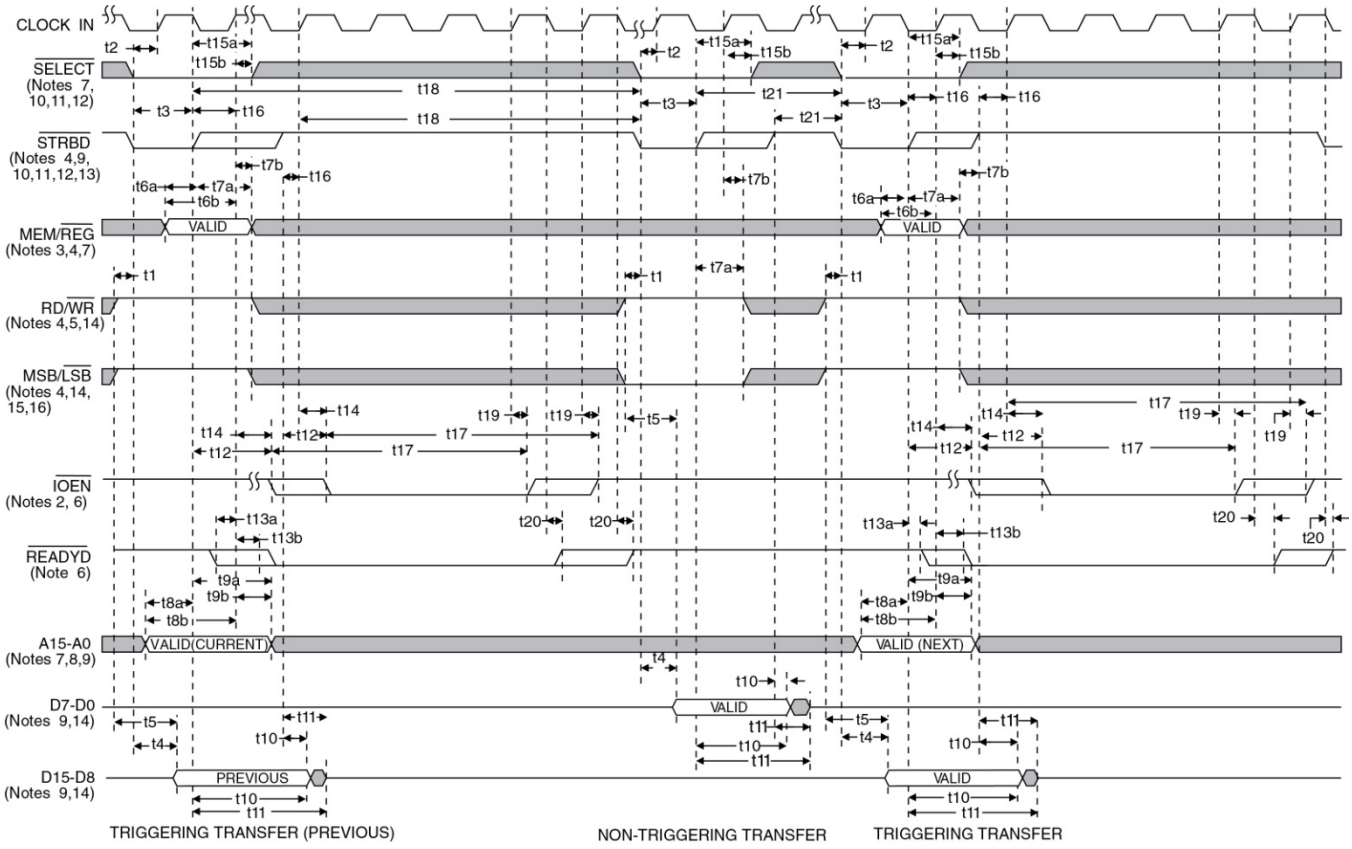



**Figure 30. CPU Reading RAM/Registers (8-Bit, Zero Wait)**

Notes for Table 13 and Figure 30

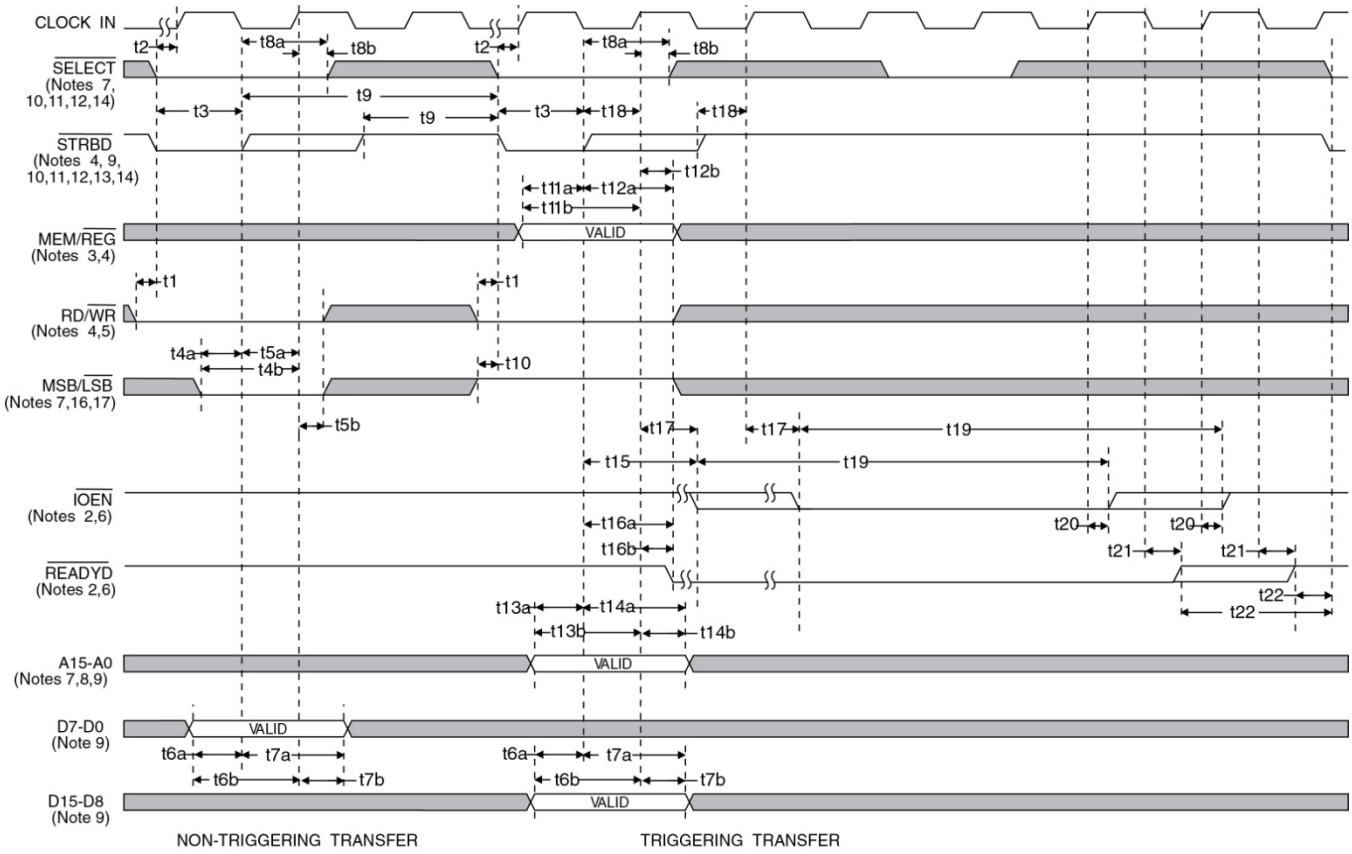
1. For 8-bit nonzero wait interface, TRANSPARENT/$\overline{\text{BUFFERED}}$, $\overline{\text{ZEROWAIT}}$ and 16/$\overline{8}$/$\overline{\text{DTREQ}}$ must be connected to logic "0."
2. $\overline{\text{IOEN}}$ goes low on the first rising CLK edge when $\overline{\text{READYD}}$ is high and $\overline{\text{STRBD}}$ is sampled high (satisfying t16 setup time) and the Enhanced Mini-ACE protocol/memory management logic is not accessing the internal RAM. When this occurs, $\overline{\text{IOEN}}$ goes low, starting the internal transfer.
3. MEM/$\overline{\text{REG}}$ must be presented high for memory access, low for register access.
4. MEM/$\overline{\text{REG}}$, MSB/$\overline{\text{LSB}}$, and RD/$\overline{\text{WR}}$ are buffered transparently until latched by $\overline{\text{STRBD}}$ rising or second rising CLK edge.
5. RD/$\overline{\text{WR}}$ must be presented high for read accesses and low for write accesses. The logic sense for RD/$\overline{\text{WR}}$ does not depend on the state of the POL_SEL input in the 8-bit mode.

6. The timing for $\overline{\text{IOEN}}$ and $\overline{\text{READYD}}$ outputs assumes a 50 pf load. For loading above 50 pf, the validity of $\overline{\text{IOEN}}$ and $\overline{\text{READYD}}$ is delayed by an additional 0.14 ns/pf typ, 0.28 ns/pf max.
7. Timing for A15-A0, MEM/$\overline{\text{REG}}$, MSB/$\overline{\text{LSB}}$, and $\overline{\text{SELECT}}$ assumes ADDR_LAT is connected to logic "1." Refer to Address Latch timing for additional details.
8. Internal RAM is accessed by A15 through A0 (64K RAM Versions) or A11 through A0 (4K RAM Versions). Registers are accessed by A4 through A0.
9. The address bus A15-A0 and data bus D15-D0 are internally buffered transparently until latched by $\overline{\text{STRBD}}$ rising or second CLK edge.
10. Setup time given for use in worst case timing calculations. These signals do not have to be synchronized to the system clock. Removal of $\overline{\text{SELECT}}$ prior to being latched on the second rising clock edge will have the same effect as $\overline{\text{STRBD}}$ rising. For Enhanced Mini-ACE applications, transfer will not start until $\overline{\text{SELECT}}$ and $\overline{\text{STRBD}}$ are both low. $\overline{\text{SELECT}}$ must go low prior to the second rising clock edge after STRBD* goes low or transfer will be blocked.
11. For the case in which $\overline{\text{STRBD}}$ goes high before the second rising clock edge in which $\overline{\text{SELECT}}$ is low and $\overline{\text{STRBD}}$ is low.
12. For the case in which $\overline{\text{STRBD}}$ is low and $\overline{\text{SELECT}}$ is low for a minimum of two rising clock edges.
13. For 8-Bit Zero Wait triggering transfers. After $\overline{\text{STRBD}}$ is brought high and $\overline{\text{READYD}}$ asserted low, $\overline{\text{STRBD}}$ **MUST** be kept low until $\overline{\text{READYD}}$ returns high.
14. Valid data will be present on the data bus only after $\overline{\text{SELECT}}$, $\overline{\text{STRBD}}$, MSB/$\overline{\text{LSB}}$ and RD/$\overline{\text{WR}}$ propagation delays (t3-t5) are met.
15. The polarity of the MSB/$\overline{\text{LSB}}$ input signal assumes that the POL_SEL input signal is connected to logic "0." If POL_SEL is connected to logic "1," MSB/$\overline{\text{LSB}}$ will be high for LSB transfers and low for MSB transfers.
16. The order of the consecutive byte transfers assumes that the TRIG_SEL input signal is connected to logic "0." The actual transfer to the internal RAM or Register takes place during the "triggering transfer" (MSB in this case). If TRIG_SEL is connected to logic "1," the order of the byte transfers would be MSB followed by LSB and the triggering transfer would be the LSB.

## Table 14. CPU Writing RAM/Registers (8-Bit, Zero Wait Mode)

| REF | DESCRIPTION | Notes | 5V Logic | | | 3.3V Logic | | | UNITS |
|---|---|---|---|---|---|---|---|---|---|
| | | | MIN | TYP | MAX | MIN | TYP | MAX | |
| t1 | RD/ $\overline{WR}$ setup prior to $\overline{SELECT}$ low and $\overline{STRBD}$ low | 11 | 10 | | | 10 | | | ns |
| t2 | $\overline{SELECT}$ and $\overline{STRBD}$ low setup time prior to CLOCK IN rising | 10 | 10 | | | 15 | | | ns |
| t3 | $\overline{SELECT}$ and $\overline{STRBD}$ low minimum pulse width | | 20 | | | 25 | | | ns |
| t4A | MSB/ $\overline{LSB}$ setup prior to $\overline{STRBD}$ rising | 12 | 20 | | | 20 | | | ns |
| t4B | MSB/ $\overline{LSB}$ setup prior to CLOCK IN rising | 14 | 20 | | | 20 | | | ns |
| t5A | MSB/ $\overline{LSB}$, RD/ $\overline{WR}$ hold timing following $\overline{STRBD}$ rising | 12 | 20 | | | 20 | | | ns |
| t5B | MSB/ $\overline{LSB}$, RD/ $\overline{WR}$ hold time following CLOCK IN rising | 14 | 25 | | | 25 | | | ns |
| t6A | Input Data setup prior to $\overline{STRBD}$ rising | 12 | 10 | | | 10 | | | ns |
| t6B | Input Data setup prior to CLOCK IN rising | 14 | 10 | | | 10 | | | ns |
| t7A | Input Data hold time following $\overline{STRBD}$ rising | 12 | 20 | | | 20 | | | ns |
| t7B | Input Data hold time following CLOCK IN rising | 14 | 25 | | | 25 | | | ns |
| t8A | $\overline{SELECT}$ low hold time following $\overline{STRBD}$ rising | 12 | 0 | | | 0 | | | ns |
| t8B | $\overline{SELECT}$ low hold time following CLOCK IN rising | 14 | 25 | | | 25 | | | ns |
| t9 | $\overline{STRBD}$ rising delay to start of next transfer ( $\overline{SELECT}$ low and $\overline{STRBD}$ low) | | 20 | | | 20 | | | ns |
| t10 | MSB/ $\overline{LSB}$ high setup prior to $\overline{SELECT}$ low and $\overline{STRBD}$ low | 17 | 10 | | | 10 | | | ns |
| t11A | MEM/ $\overline{REG}$ setup prior to $\overline{STRBD}$ rising | 12 | 10 | | | 10 | | | ns |
| t11B | MEM/ $\overline{REG}$ setup prior to CLOCK IN rising | 14 | 10 | | | 10 | | | ns |
| t12A | MEM/ $\overline{REG}$, RD/ $\overline{WR}$, MSB/ $\overline{LSB}$ hold time following $\overline{STRBD}$ rising | 12 | 20 | | | 20 | | | ns |
| t12B | MEM/ $\overline{REG}$, RD/ $\overline{WR}$, MSB/ $\overline{LSB}$ hold time following CLOCK IN rising | 14 | 25 | | | 25 | | | ns |
| t13A | Address setup prior to $\overline{STRBD}$ rising | 12 | 10 | | | 10 | | | ns |
| t13B | Address setup prior to CLOCK IN rising | 14 | 10 | | | 10 | | | ns |
| t14A | Address hold time following $\overline{STRBD}$ rising | 12 | 20 | | | 20 | | | ns |
| t14B | Address hold time following CLOCK IN rising | 14 | 30 | | | 30 | | | ns |
| t15 | $\overline{STRBD}$ rising delay to $\overline{IOEN}$ falling (uncontended access @20 MHz) | 13 | | | 107 | | | 112 | ns |
| | (Contended access, with ENHANCED CPU ACCESS = “0” @ 20 MHz) | 13 | | | 3.6 | | | 3.6 | us |
| | (Contended access, with ENHANCED CPU ACCESS = “1” @ 20 MHz) | 13 | | | 357 | | | 362 | ns |
| | $\overline{STRBD}$ rising delay to $\overline{IOEN}$ falling (uncontended access @16 MHz) | 13 | | | 120 | | | 125 | ns |
| | (Contended access, with ENHANCED CPU ACCESS = “0” @ 16 MHz) | 13 | | | 4.6 | | | 4.6 | us |
| | (Contended access, with ENHANCED CPU ACCESS = “1” @ 16 MHz) | 13 | | | 432 | | | 437 | ns |

| Table 14. CPU Writing RAM/Registers (8-Bit, Zero Wait Mode) | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| REF | DESCRIPTION | Notes | 5V Logic | | | 3.3V Logic | | | UNITS |
| | | | MIN | TYP | MAX | MIN | TYP | MAX | |
| | $\overline{\text{STRBD}}$ rising delay to $\overline{\text{IOEN}}$ falling (uncontended access @12 MHz) | 13 | | | 140 | | | 145 | ns |
| | (Contended access, with ENHANCED CPU ACCESS = “0” @ 12 MHz) | 13 | | | 6.0 | | | 6.0 | us |
| | (Contended access, with ENHANCED CPU ACCESS = “1” @ 12 MHz) | 13 | | | 557 | | | 562 | ns |
| | $\overline{\text{STRBD}}$ rising delay to $\overline{\text{IOEN}}$ falling (uncontended access @10 MHz) | 13 | | | 157 | | | 162 | ns |
| | (Contended access, with ENHANCED CPU ACCESS = “0” @ 10 MHz) | 13 | | | 7.2 | | | 7.2 | us |
| | (Contended access, with ENHANCED CPU ACCESS = “1” @ 10 MHz) | 13 | | | 657 | | | 662 | ns |
| t16A | $\overline{\text{STRBD}}$ rising delay to $\overline{\text{READYD}}$ falling | | | | 30 | | | 30 | ns |
| t16B | CLOCK IN rising delay to $\overline{\text{READYD}}$ falling | | | | 35 | | | 35 | ns |
| t17 | CLOCK IN rising delay to $\overline{\text{IOEN}}$ falling | | | | 40 | | | 40 | ns |
| t18 | $\overline{\text{STRBD}}$ high setup prior to CLOCK IN rising | | 15 | | | 15 | | | ns |
| t19 | $\overline{\text{IOEN}}$ low pulse width for RAM write (@20 MHz) | | 185 | 200 | 215 | 185 | 200 | 215 | ns |
| | $\overline{\text{IOEN}}$ low pulse width for REGISTER write (@20 MHz) | | 185 | 200 | 215 | 185 | 200 | 215 | ns |
| | $\overline{\text{IOEN}}$ low pulse width for RAM write (@16 MHz) | | 235 | 250 | 265 | 235 | 250 | 265 | ns |
| | $\overline{\text{IOEN}}$ low pulse width for REGISTER write (@16 MHz) | | 235 | 250 | 265 | 235 | 250 | 265 | ns |
| | $\overline{\text{IOEN}}$ low pulse width for RAM write (@12 MHz) | | 315 | 333 | 350 | 315 | 333 | 350 | ns |
| | $\overline{\text{IOEN}}$ low pulse width for REGISTER write (@12 MHz) | | 315 | 333 | 350 | 315 | 333 | 350 | ns |
| | $\overline{\text{IOEN}}$ low pulse width for RAM write (@10 MHz) | | 385 | 400 | 415 | 385 | 400 | 415 | ns |
| | $\overline{\text{IOEN}}$ low pulse width for REGISTER write (@10 MHz) | | 385 | 400 | 415 | 385 | 400 | 415 | ns |
| t20 | CLOCK IN rising delay to $\overline{\text{IOEN}}$ rising | | | | 35 | | | 35 | ns |
| t21 | CLOCK IN falling delay to $\overline{\text{READYD}}$ rising | | | | 35 | | | 35 | ns |
| t22 | $\overline{\text{READYD}}$ high to $\overline{\text{STRBD}}$ and $\overline{\text{SELECT}}$ low (Next transfer) | | 0 | | | 0 | | | ns |




## Figure 31. CPU Writing RAM/Registers (8-Bit, Zero Wait)

Notes for Table 14 and Figure 31

1. For 8-bit zero wait interface, TRANSPARENT/$\overline{\text{BUFFERED}}$, $\overline{\text{ZEROWAIT}}$ and 16/$\overline{8}$/$\overline{\text{DTREQ}}$ must be connected to logic "0."
2. $\overline{\text{IOEN}}$ goes low on the first rising CLK edge when $\overline{\text{READYD}}$ is high and $\overline{\text{STRBD}}$ is sampled high (satisfying t18 setup time) and the Enhanced Mini-ACE protocol/memory management logic is not accessing the internal RAM. When this occurs, $\overline{\text{IOEN}}$ goes low, starting the internal transfer.
3. MEM/$\overline{\text{REG}}$ must be presented high for memory access, low for register access.
4. MEM/$\overline{\text{REG}}$, MSB/$\overline{\text{LSB}}$, and RD/$\overline{\text{WR}}$ are buffered transparently until latched by $\overline{\text{STRBD}}$ rising or second rising CLK edge.
5. RD/$\overline{\text{WR}}$ must be presented high for read accesses and low for write accesses. The logic sense for RD/$\overline{\text{WR}}$ does not depend on the state of the POL_SEL input in the 8-bit mode.
6. The timing for $\overline{\text{IOEN}}$ and $\overline{\text{READYD}}$ outputs assumes a 50 pf load. For loading above 50 pf, the validity of $\overline{\text{IOEN}}$ and $\overline{\text{READYD}}$ is delayed by an additional 0.14 ns/pf typ, 0.28 ns/pf max.
7. Timing for A15-A0, MEM/$\overline{\text{REG}}$, MSB/$\overline{\text{LSB}}$ and $\overline{\text{SELECT}}$ assumes ADDR_LAT is connected to logic "1." Refer to Address Latch timing for additional details.
8. Internal RAM is accessed by A15 through A0 (64K RAM Versions) or A11 through A0 (4K RAM Versions).Registers are accessed by A4 through A0.
9. The address A15-A0 and data D15-D0 are internally buffered transparently until latched by $\overline{\text{STRBD}}$ rising or the second rising clock edge.

10. Setup time given for use in worst case timing calculations. These signals do not have to be synchronized to the system clock. Removal of $\overline{\text{SELECT}}$ effect as $\overline{\text{STRBD}}$ are both low. $\overline{\text{SELECT}}$ must go low prior to the second clock rising edge after $\overline{\text{STRBD}}$ goes low or transfer will be blocked.
11. Data Bus will be actively driven when $\overline{\text{SELECT}}$ is low, $\overline{\text{STRBD}}$ is low and RD/$\overline{\text{WR}}$ is high. To prevent a bus crash between the host driving the Data Bus and the Enhanced Mini-ACE driving the Data Bus, RD/$\overline{\text{WR}}$ must be setup prior to $\overline{\text{SELECT}}$ low and $\overline{\text{STRBD}}$ low.
12. For the case in which $\overline{\text{STRBD}}$ goes high before second rising clock edge in which $\overline{\text{SELECT}}$ is low and $\overline{\text{STRBD}}$ is low.
13. For 8-Bit Zero Wait triggering transfers. After $\overline{\text{STRBD}}$ is brought high and $\overline{\text{READYD}}$ asserted low, $\overline{\text{STRBD}}$ MUST be kept low until $\overline{\text{READYD}}$ returns high.
14. For the case in which $\overline{\text{STRBD}}$ is low and $\overline{\text{SELECT}}$ is low for a minimum of two rising clock edges.
15. $\overline{\text{IOEN}}$ will be asserted low following the first rising clock edge in which $\overline{\text{STRBD}}$ is high and the internal data bus is available.
16. The polarity of the MSB/$\overline{\text{LSB}}$ input signal assumes that the POL_SEL input signal is connected to logic "0." If POL_SEL is connected to logic "1," MSB/$\overline{\text{LSB}}$ will be high for LSB transfers and low for MSB transfers.
17. MSB/$\overline{\text{LSB}}$ must be setup prior to $\overline{\text{SELECT}}$ low and $\overline{\text{STRBD}}$ low to prevent an accidental write to the internal non-triggering byte data latch.
18. The order of the consecutive byte transfers assumes that the TRIG_SEL input signal is connected to logic "0." The actual transfer to internal RAM or register takes place during the "triggering transfer" (MSB in this case). If TRIG_SEL is connected to logic "1," the order of the byte transfers would be MSB followed by LSB and the triggering transfer would be the LSB.

## 9.15 Address Latch Timing

Figure 32 and Table 15 illustrate the operation and timing of the address input latches for the buffered interface mode. In the transparent mode, the address buffers, and $\overline{\text{SELECT}}$, MEM/$\overline{\text{REG}}$ inputs are always transparent (MSB/$\overline{\text{LSB}}$ not applicable). Since the transparent mode requires the use of external buffers, external address latches would be required to demultiplex a multiplexed address bus. In the buffered mode however, the Enhanced Mini-ACE's internal address may be used to perform the demultiplexing function. The operation of the address latches is controlled by means of the ADDR_LAT input. When ADDR_LAT is high, the latch outputs, which drive the Enhanced Mini-ACE's internal memory and control bus, transparently track the state of the address inputs A15 through A00, and the input signals $\overline{\text{SELECT}}$, MSB/$\overline{\text{LSB}}$, and MEM/$\overline{\text{REG}}$. When ADDR_LAT is low, the internal memory and control bus remain latched at the state of A15-A00, $\overline{\text{SELECT}}$, MSB/$\overline{\text{LSB}}$, and MEM/$\overline{\text{REG}}$ just prior to the falling edge of ADDR_LAT.

| Table 15. Address Latch Timing | | | | | |
|---|---|---|---|---|---|
| REF | DESCRIPTION | Enhanced Mini-ACE | | | UNITS |
| | | MIN | TYP | MAX | |
| t1 | ADDR_LAT pulse width | 20 | | | ns |
| t2 | ADDR_LAT high delay to internal signals valid | | | 10 | ns |
| t3 | Propagation delay from external input signals to internal signals valid | | | 10 | ns |
| t4 | Input setup time prior to falling edge of ADDR_LAT | 10 | | | ns |
| t5 | Input hold time following falling edge of ADDR_LAT | 20 | | | ns |

Table 15 Notes:

1. Applicable to buffered mode only. Address, $\overline{\text{SELECT}}$, and MEM/$\overline{\text{REG}}$ latches are always transparent in the transparent mode of operation.
2. Latches are transparent when ADDR_LAT is high. Internal values do not update when ADDR_LAT is low.
3. MSB/$\overline{\text{LSB}}$ input signal is applicable to 8-bit mode only (16/$\overline{8}$ input = logic "0"). MSB/$\overline{\text{LSB}}$ input is a "don't care" for 16-bit operation.

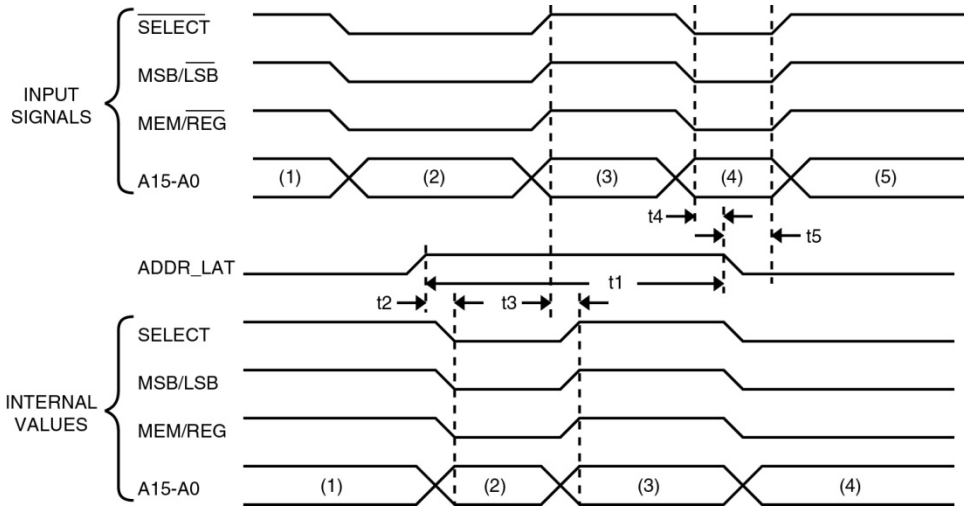



**Figure 32. Address Latch Timing**

## 9.16 Clock Input Considerations

### 9.16.1 Input Frequency

The Enhanced Mini-ACE may be operated from a 10MHz, 12MHz, 16MHz, or 20MHz clock input. In the default (power turn-on) state, the Enhanced Mini-ACE assumes a 16MHz clock input. As shown in Volume 1, Table 61 the frequency of CLOCK_IN input may be specified by writing to Configuration Registers 5 and 6. In addition, for 4K RAM versions of Enhanced Mini-ACE. The clock frequency may also be

designated by means of the UPADDREN, A15/CLK_SEL_2, and A14/CLK_SEL_0 input signals.

For compliance to the transmission rate accuracy spec of MIL-STD-1553B. The short term (1 second) frequency accuracy must be within ± 0.01%, with a long term accuracy of ± 0.1%. To comply to MIL-STD-1553A, the short term (1 second) accuracy must be to within ± 0.001%, with a long-term accuracy of ± 0.01%.

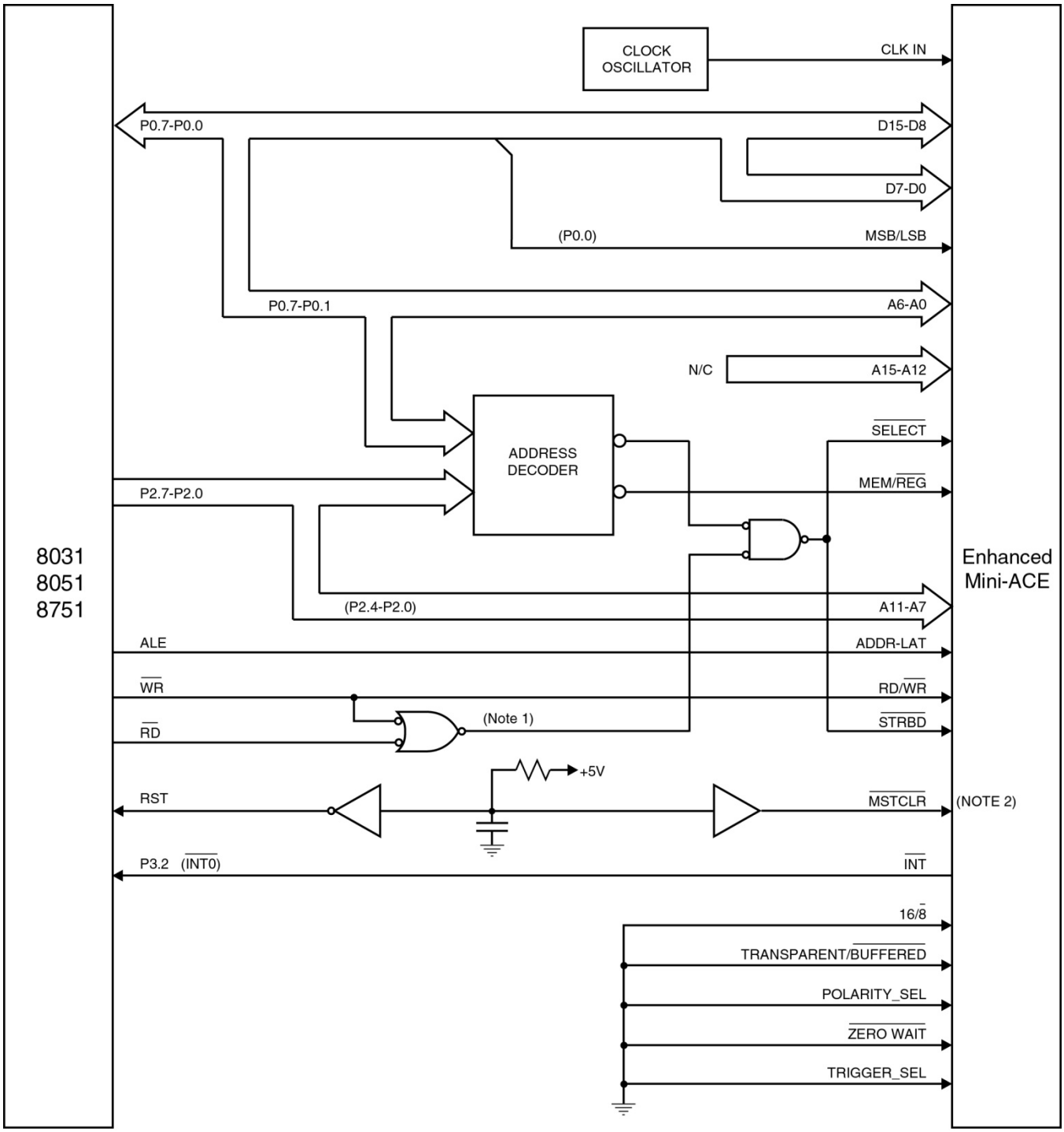
### 9.16.2 Double EdgeD MANCHESTER DECODER Sampling

The Enhanced Mini-ACE Manchester decoders operate by oversampling the digital input signal from the 1553 double-ended receivers on **every** edge (both rising and falling) of CLOCK_IN. To ensure reliable operation of the Manchester decoder, the duty cycle of the CLOCK_IN input signal must be in the range of 40% to 60%.

## 9.17 Sample Interfaces

### 9.17.1 INTEL 8051

Figure 33 illustrates a simplified interface drawing between an Intel 8051 and an Enhanced Mini-ACE. This interface is based on the Enhanced Mini-ACE's 8-bit buffered, zero wait interface. The 4K words (8K bytes) of Enhanced Mini-ACE internal RAM, map to Address range (Base Memory Address) (0000-1FFF). The 16 register locations (32 bytes) of the BU-65170/61580 map to address range (Base Register Address) (0000-001F), where BRA = Base Register Address. $\overline{\text{SELECT}}$ must be asserted low to access either RAM or register. MEM/$\overline{\text{REG}}$ must be asserted high to access RAM, low to access registers.




NOTE:
1. Select a gate such that the RD/WR setup time prior to SELECT and STRBD low is satisfied.
2. The rise time for MSTCLR must be less than 10 µs in order to ensure correct initialization of the Enhanced Mini-ACE's Transceivers.

**Figure 33. Intel 8051-to-Enhanced Mini-ACE Interface**

**Write accesses are performed as follows:**

1. Write lower data byte, with P0.0 (MSB/$\overline{\text{LSB}}$) = 0.
2. Write upper data byte, with P0.0 (MSB/$\overline{\text{LSB}}$) = 1.
   If additional write cycles are to be performed, wait the minimum time, then return to step 1. The minimum times are listed in Volume 1, TABLE 94.

**Read accesses are performed as follows:**

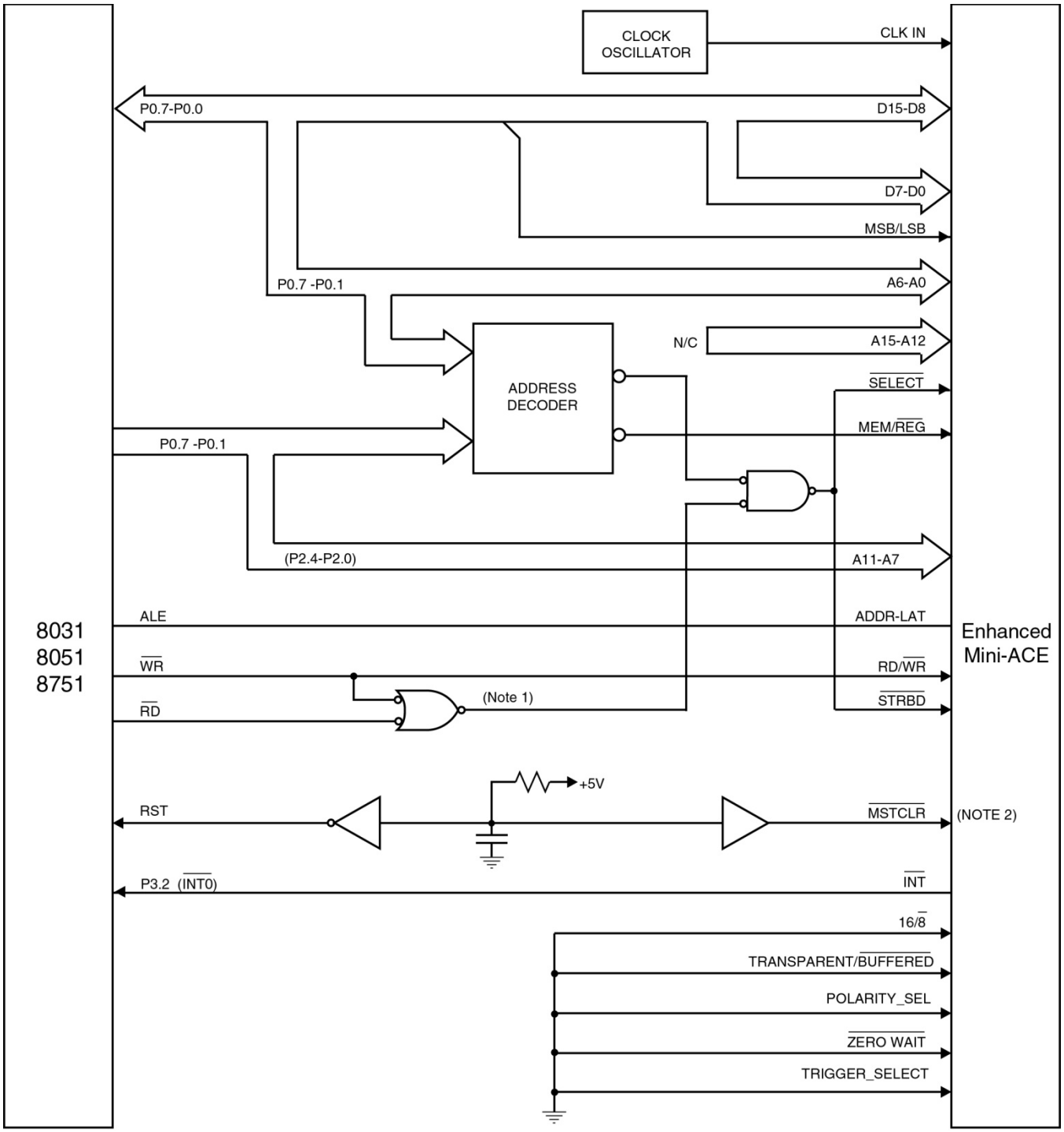
1. Perform a "dummy" read access to the upper data byte address (P0.0 (MSB/$\overline{\text{LSB}}$) = 1). Do not use the data byte accessed from this operation.
2. After waiting the minimum time (see Volume 1, TABLE 94), read the lower data byte, with P0.0 (MSB/$\overline{\text{LSB}}$) = 0.
3. While presenting the Address for the next word to be accessed (if any), read the upper byte, with P0.0 (MSB/$\overline{\text{LSB}}$) = 1.
   If there is a subsequent word to be read, repeat steps 2 and 3.

**Table 16. Minimum Required Delay Times**

| MODE | Enhanced Mini-ACE | | | |
|---|---|---|---|---|
| | @20MHz | @16MHz | @12MHz | @10MHz |
| **Bus Controller (BC)** | 1.9 µs | 2.4 µs | 3.1 µs | 3.8 µs |
| **Remote Terminal (RT)** | 3.9 µs | 4.9 µs | 6.4 µs | 7.7 µs |
| **Word Monitor** | 0.9 µs | 1.1 µs | 1.5 µs | 1.8 µs |
| **Selective Message Monitor** | 2.1 µs | 2.6 µs | 3.5 µs | 4.2 µs |

## 9.17.2 ADSP-2101

Figure 34 illustrates a simplified interface drawing between an Analog Devices ADSP-2101 and an Enhanced Mini-ACE. This interface takes advantage of the Enhanced Mini-ACE's 16-bit zero wait mode since the 2101 does not have an acknowledge handshake input. A restriction of the zero wait mode is that the processor may not begin a new transfer until the previous is complete. Therefore, the $\overline{\text{READYD}}$ output may optionally be read by the processor on the LSB of the data bus as a method of polling the Enhanced Mini-ACE to determine when the transfer is complete.




NOTE:
1. Select a gate such that the RD/WR* setup time prior to SELECT* and STRBD* low is satisfied.
2. The rise time for MSTCLR must be less than 10 µs in order to ensure correct initialization of the Enhanced Mini-ACE's Transceivers.

**Figure 34. ADSP-2101-to- ACE Interface**

## 9.17.3 MOTOROLA 68HC912-to-Enhanced Mini-ACE Interface

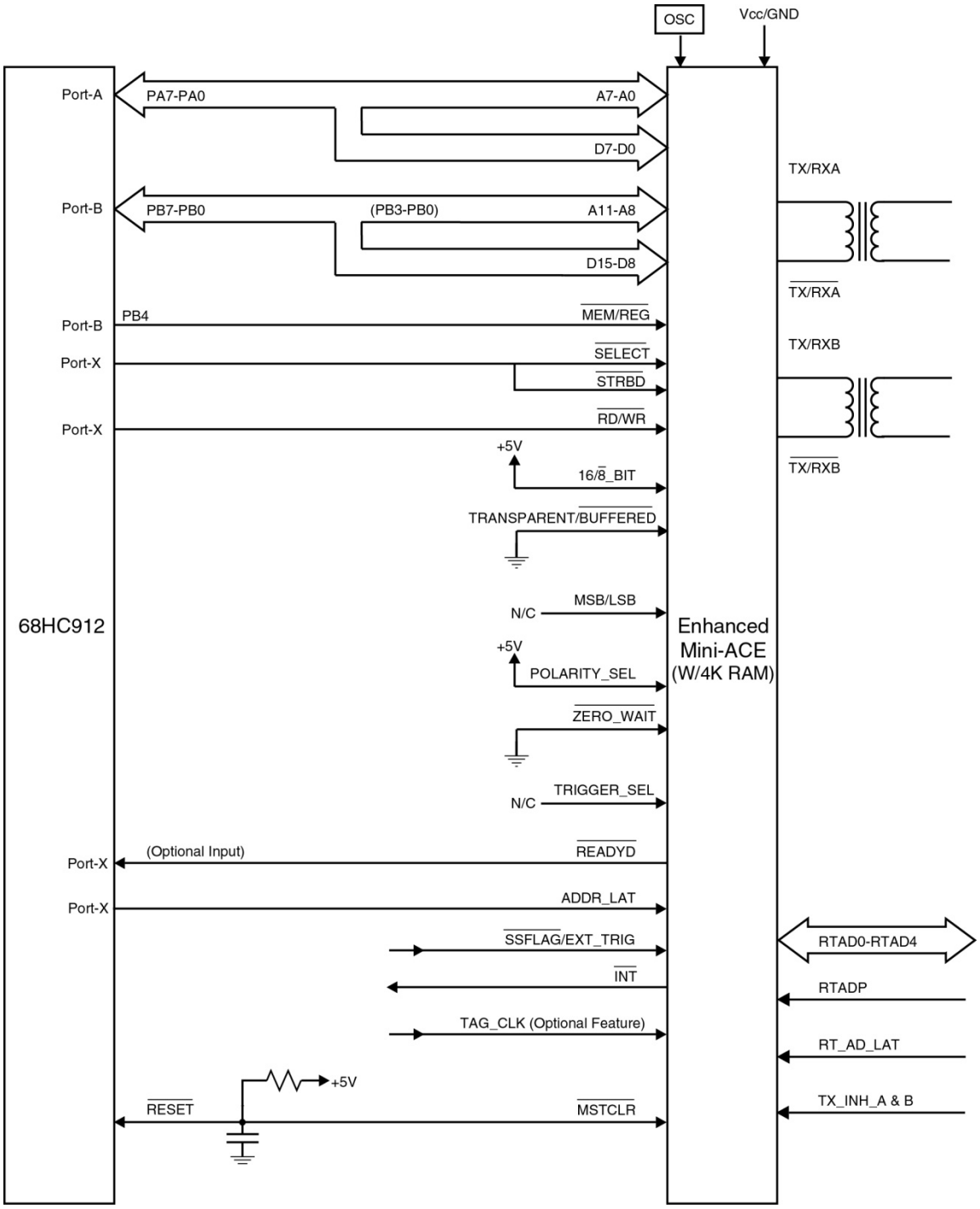
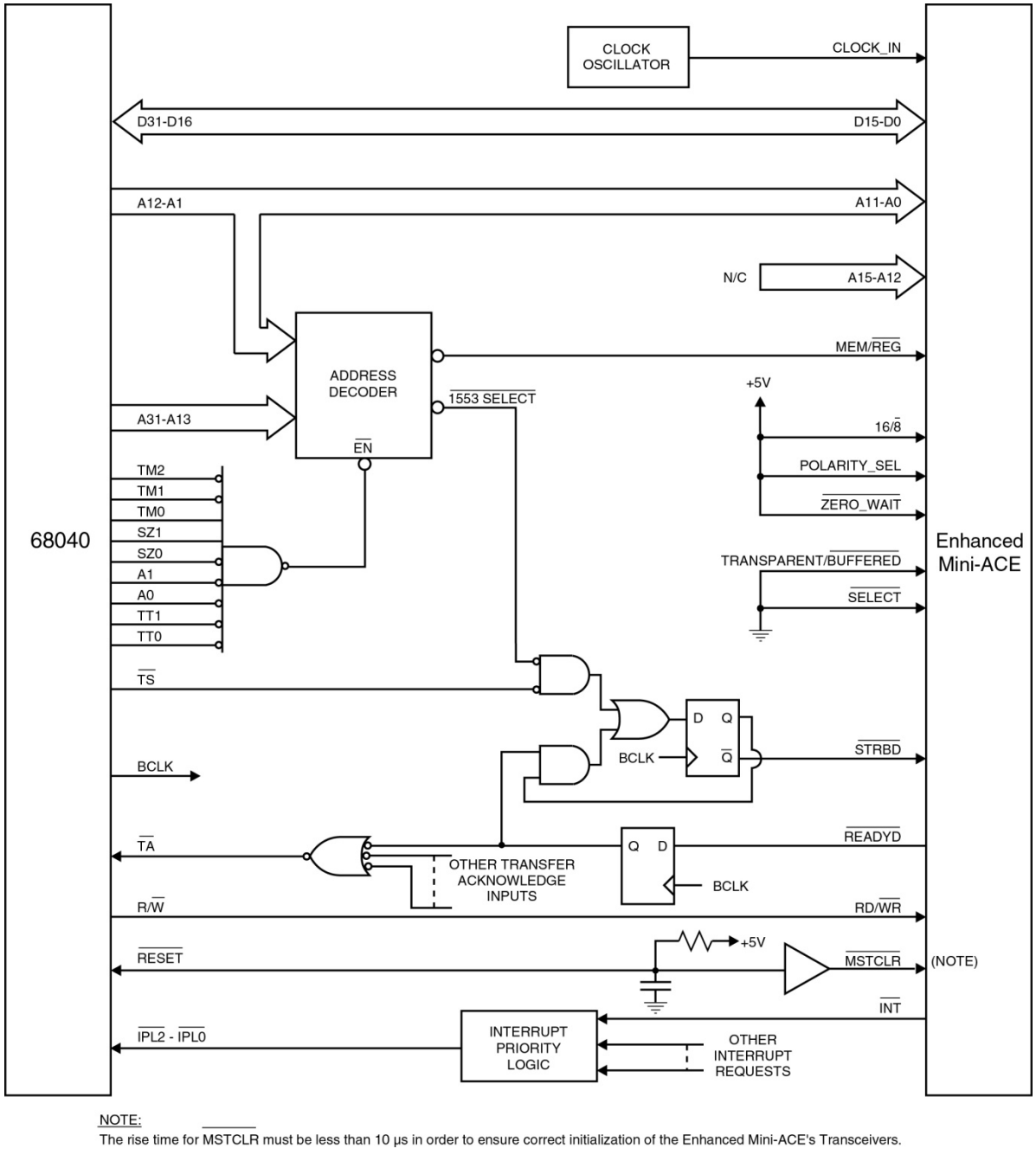



**Figure 35. Motorola 68HC912-to-Enhanced Mini-ACE Interface**

## 9.17.4 MOTOROLA 68040

Figure 36 illustrates a simplified interface drawing between a 68040 and an Enhanced Mini-ACE.

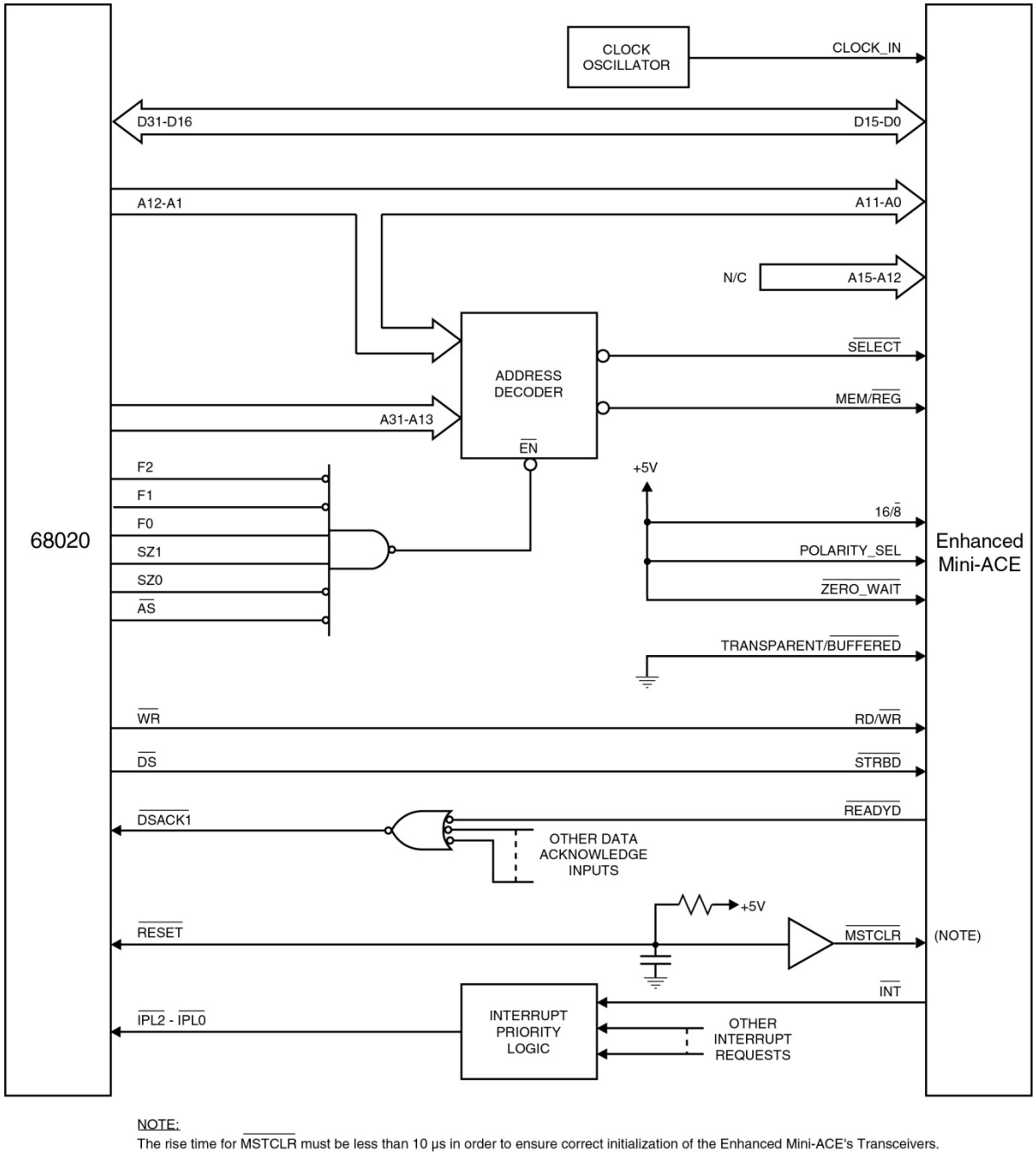



NOTE:
The rise time for MSTCLR must be less than 10 µs in order to ensure correct initialization of the Enhanced Mini-ACE's Transceivers.

**Figure 36. Motorola 68040-to-Enhanced Mini-ACE Interface**

## 9.17.5 MOTOROLA 68020

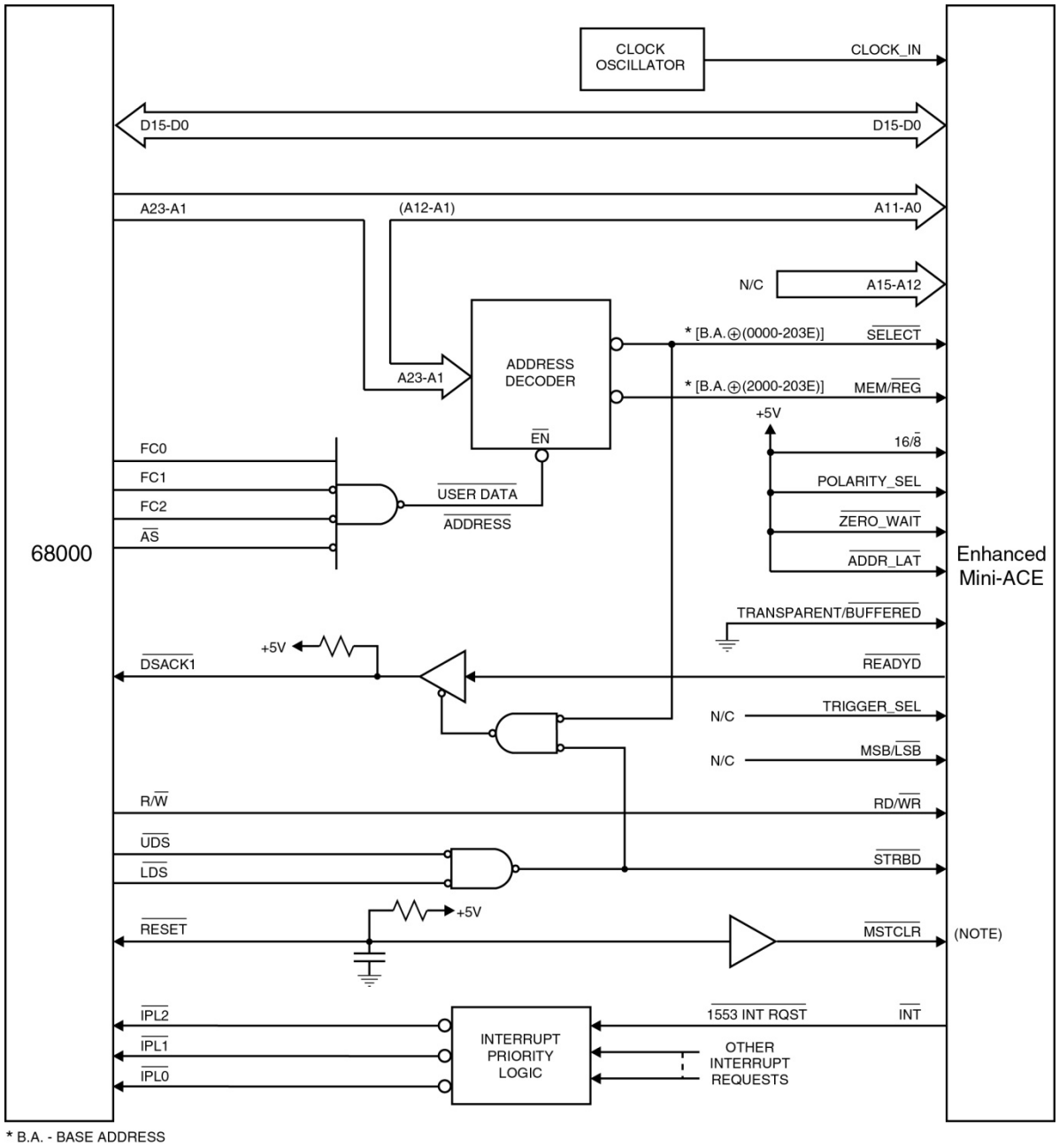
Figure 37 illustrates a simplified interface drawing between a 68020 and an Enhanced Mini-ACE.




NOTE:
The rise time for MSTCLR must be less than 10 µs in order to ensure correct initialization of the Enhanced Mini-ACE's Transceivers.

**Figure 37. Motorola 68020-to-Enhanced Mini-ACE Interface**

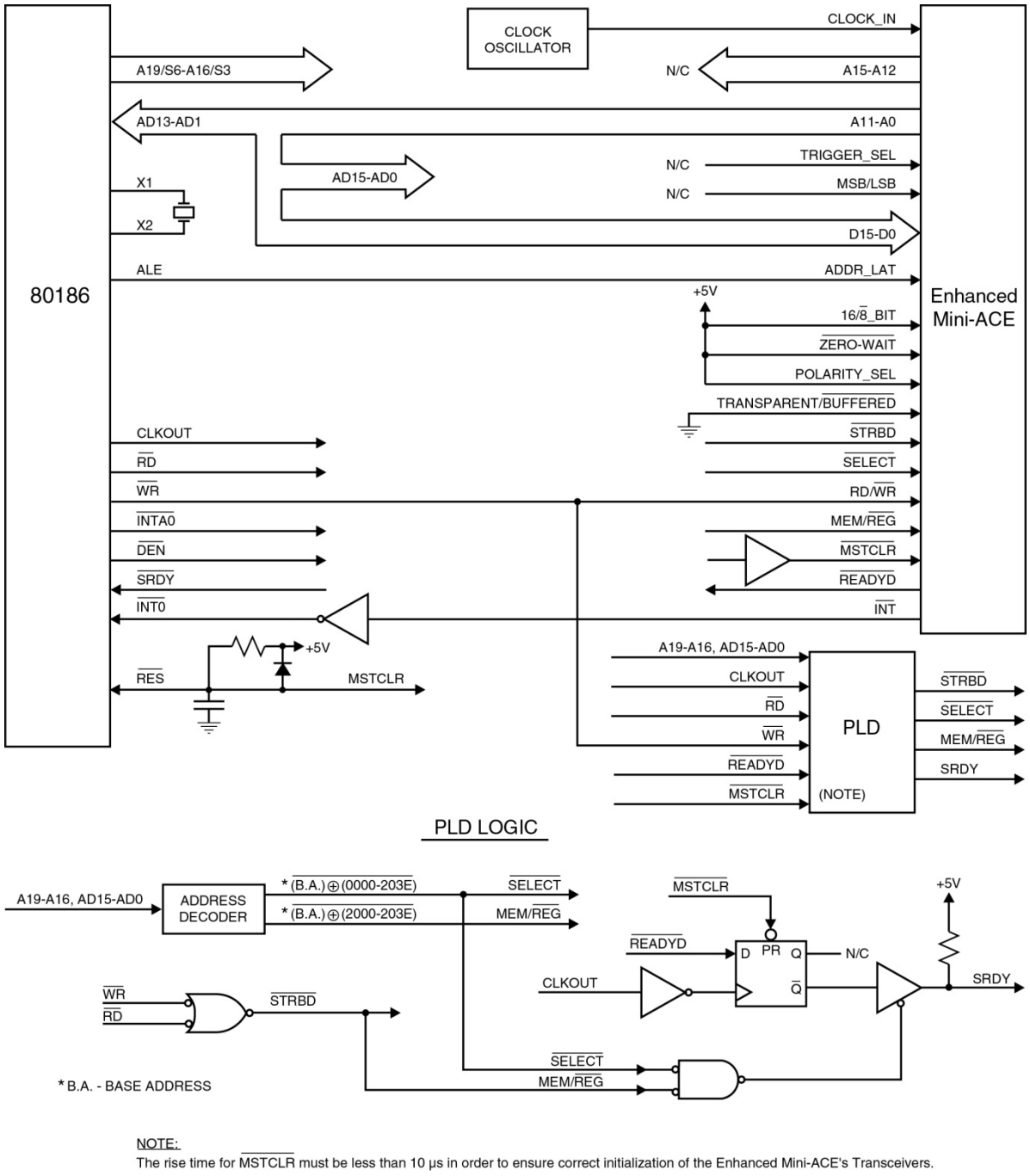
## 9.17.6 MOTOROLA 68000




NOTE:
The rise time for MSTCLR must be less than 10 µs in order to ensure correct initialization of the Enhanced Mini-ACE's Transceivers.

**Figure 38. Motorola 68000-to-Enhanced Mini-ACE Interface**

## 9.17.7 INTEL 80186




NOTE:
The rise time for MSTCLR must be less than 10 µs in order to ensure correct initialization of the Enhanced Mini-ACE's Transceivers.

**Figure 39. INTEL 80186-to-Enhanced Mini-ACE Interface**

## 9.17.8 INTEL 80286

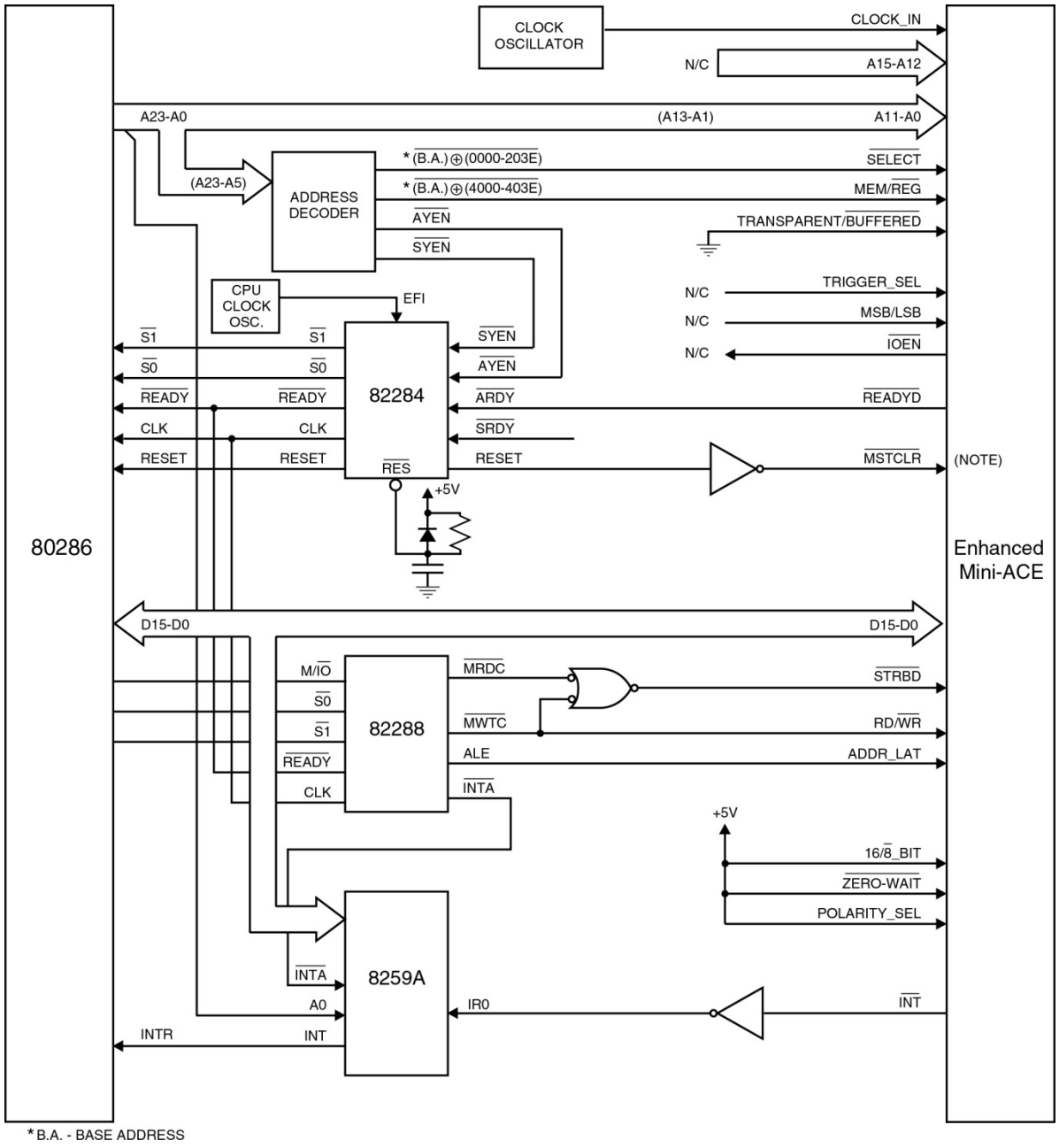
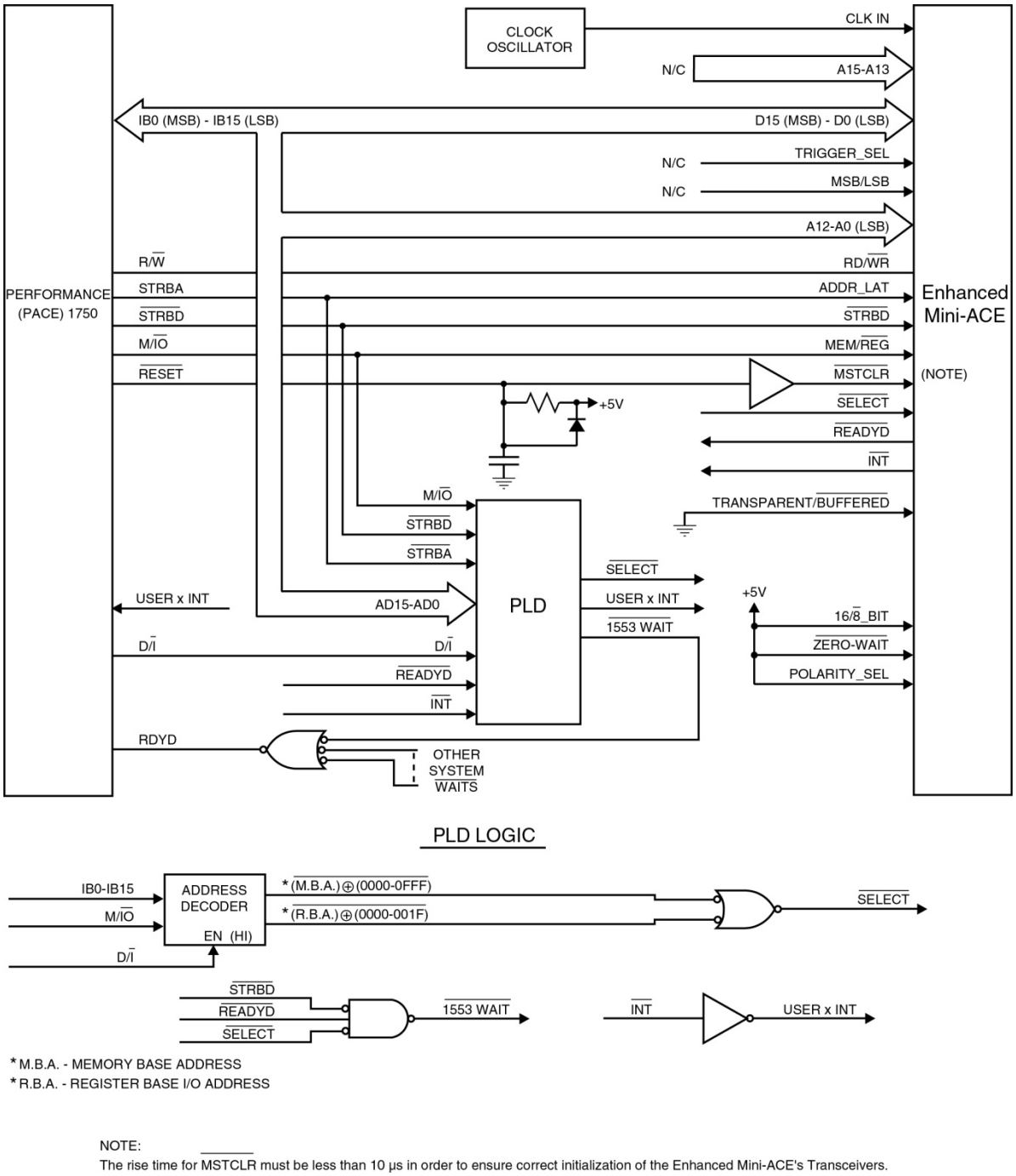



**Figure 40. INTEL 80286-to-Enhanced Mini-ACE Interface**

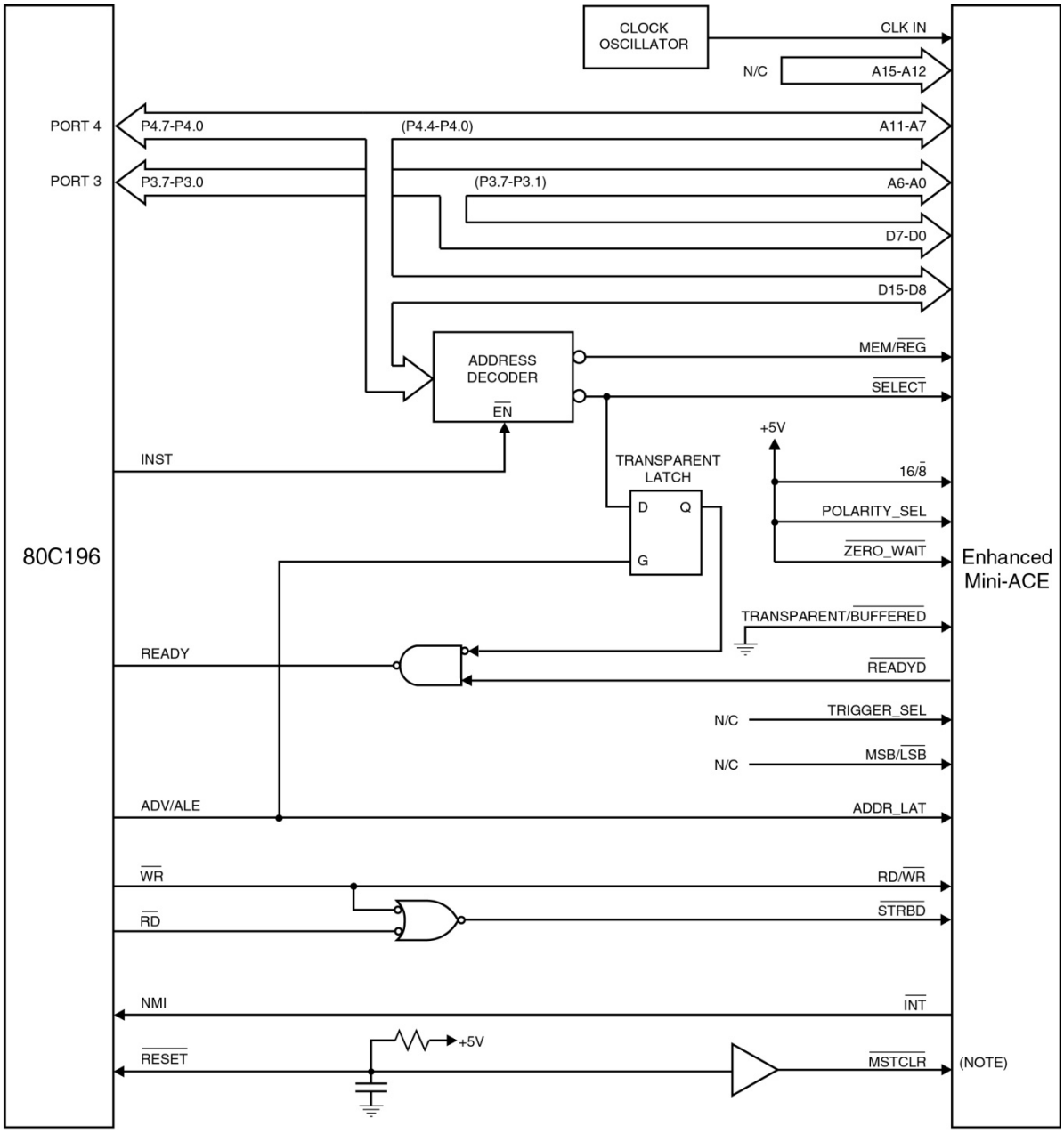
## 9.17.9 PERFORMANCE (PACE)




NOTE:
The rise time for MSTCLR must be less than 10 µs in order to ensure correct initialization of the Enhanced Mini-ACE's Transceivers.

**Figure 41. Performance (PACE) 1750-to-Enhanced Mini-ACE Interface**

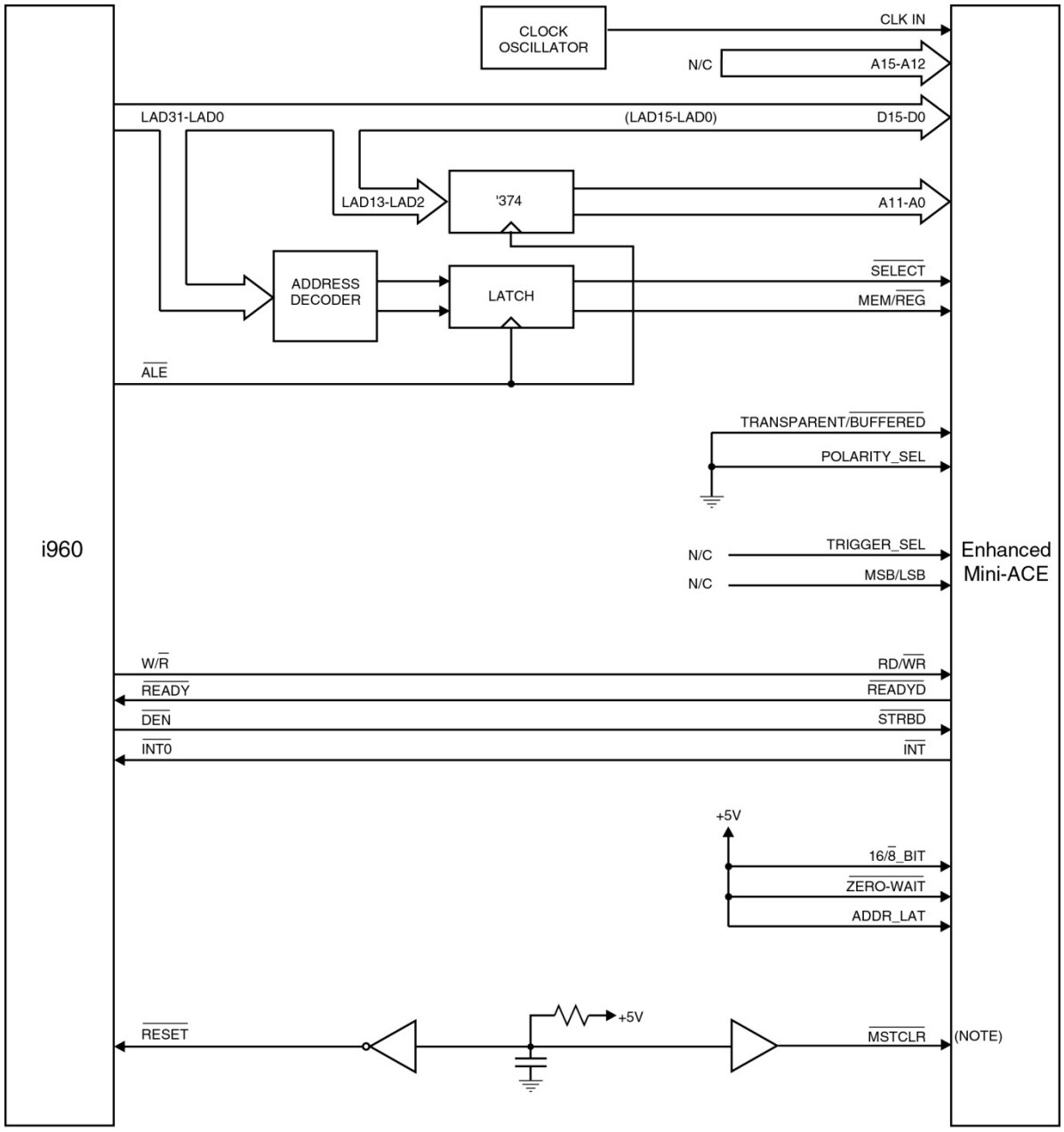
## 9.17.10 INTEL 80C196




NOTE:
The rise time for MSTCLR must be less than 10 µs in order to ensure correct initialization of the Enhanced Mini-ACE's Transceivers.

**Figure 42. INTEL 80C196-to-Enhanced Mini-ACE Interface**

### 9.17.11 INTEL i960




NOTE:
The rise time for MSTCLR must be less than 10 µs in order to ensure correct initialization of the Enhanced Mini-ACE's Transceivers.

**Figure 43. INTEL i960-to-Enhanced Mini-ACE Interface**

## 9.17.12 INTEL 80486

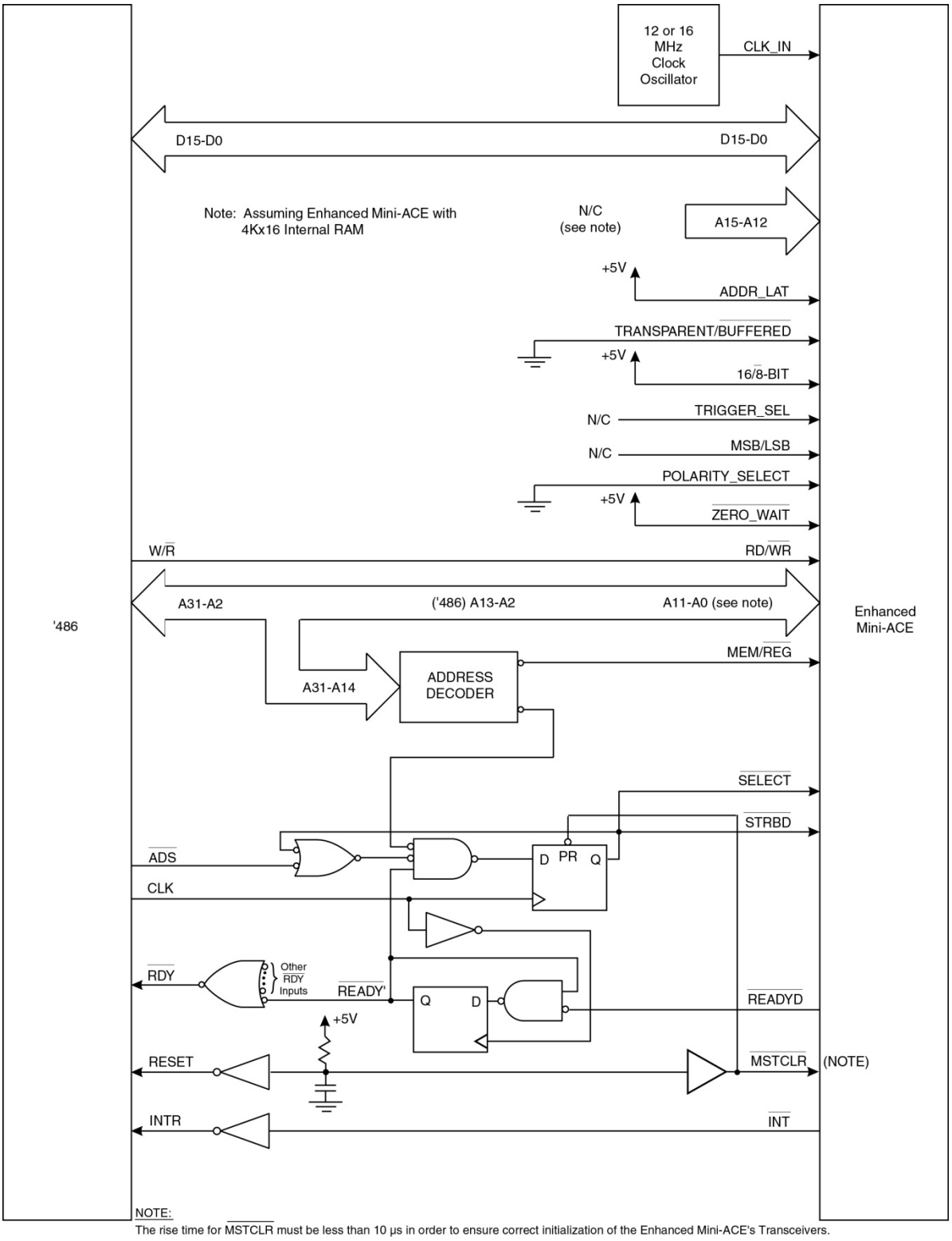
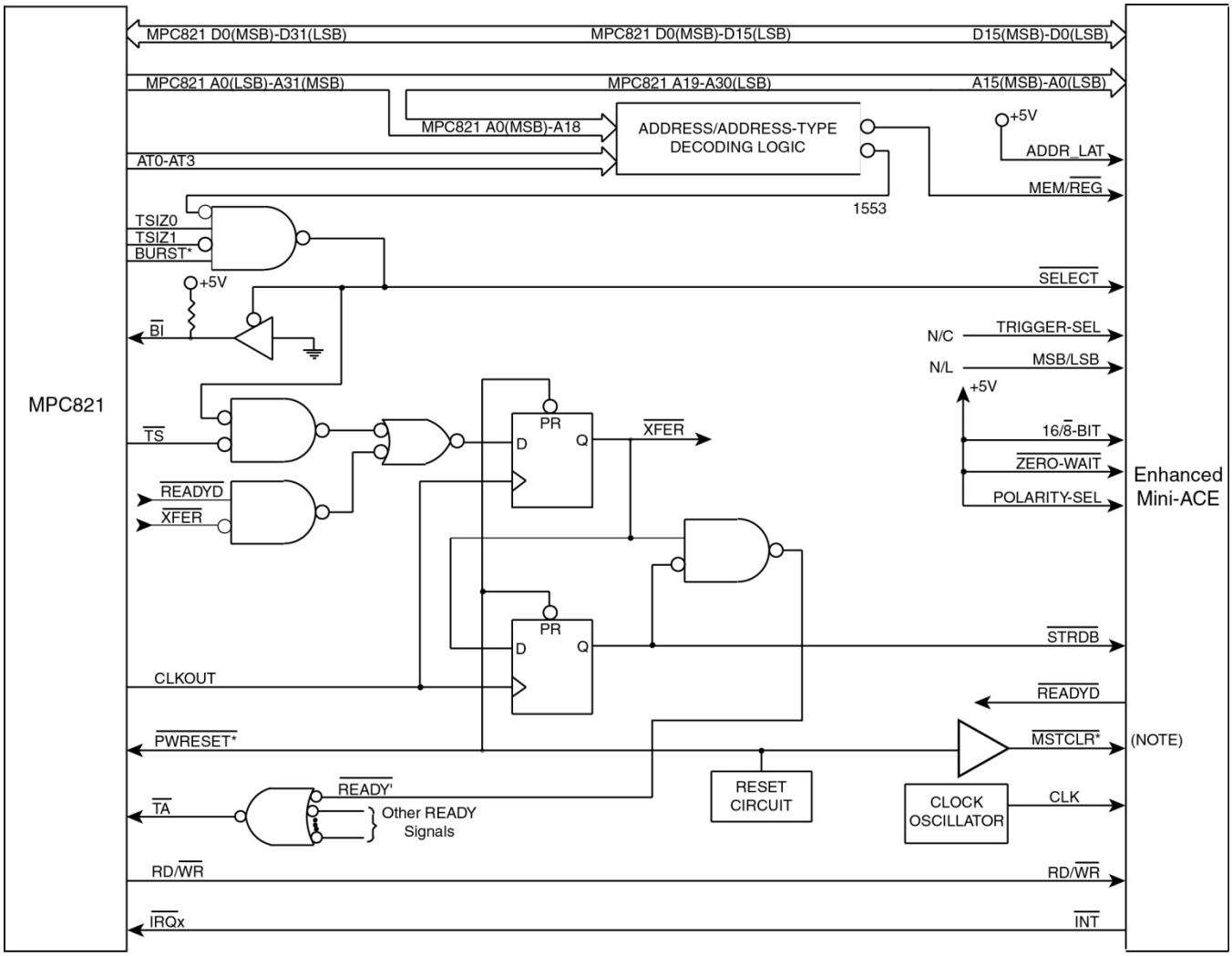



**Figure 44. INTEL 80486-to-Enhanced Mini-ACE Interface**

### 9.17.13 MOTOROLA MPC821




NOTE:
The rise time for MSTCLR must be less than 10 µs in order to ensure correct initialization of the Enhanced Mini-ACE's Transceivers.

**Figure 45. Motorola MPC821-to-Enhanced Mini-ACE Interface**

# 10 DETAILED DESCRIPTION OF 1553 MESSAGE SEQUENCES

## 10.1 General RAM Transfer Timing

This section provides a comprehensive description of the 1553 protocol timing sequences for BC, RT, Message Monitor (MMT), and Word Monitor modes (WMT). This includes RAM transfer timing, and Message Sequence timing. All RAM transfer timing is shown for the transparent mode of operation (transfers are all internal for the buffered mode of operation and hence are not visible). The 1553 message sequence diagrams are shown as a top level summary of timing. These diagrams cross-reference detailed timing diagrams (such as Start Of Message sequence).

## 10.2 Single Word Read and Write Cycles

These transfer cycles are applicable to BC, RT, and MMT modes for the transfer of Command Words, Status Words, Data words, and Loopback words to the RAM and Data Words from the RAM.

The DMA control signal $\overline{\text{DTREQ}}$ is asserted by the Enhanced Mini-ACE to request access to the host CPU RAM bus. The CPU responds with $\overline{\text{DTGRT}}$ indicating that the interface bus is available for the Enhanced Mini-ACE to read from RAM. The Enhanced Mini-ACE in turn responds with a DMA acknowledge ($\overline{\text{DTACK}}$) and proceeds with the transfer cycle. The $\overline{\text{MEMENA\_OUT}}$ along with the Address lines are used to decode between external RAM (if applicable) and internal RAM through the use of the $\overline{\text{MEMENA\_IN}}$ input signal. (Note that for Enhanced Mini-ACE series terminals, the $\overline{\text{MEMENA\_OUT}}$ signal is not available but can be replaced by logically AND'ing $\overline{\text{DTACK}}$ and $\overline{\text{IOEN}}$).

## 10.3 SOM/EOM Burst Read/Write Timing

The Start Of Message (SOM) and End Of Message (EOM) timing sequences for BC, RT, and MMT modes consist of a multi-word read/modify/write cycle. Figure 48 illustrates a general multiword burst showing two read transfers followed by 2 write transfers. Note that the actual SOM and EOM transfers may consist of more than 2 read transfers and 2 write transfers. The timing for additional transfers remains the same. Each transfer (both read and write) consists of four clock cycles, with the exception being the first transfer which takes five clock cycles.

| Table 17. Enhanced Mini-ACE Single Word DMA Read (Transparent Mode) | | | | | |
|---|---|---|---|---|---|
| REF | DESCRIPTION | Enhanced Mini-ACE | | | UNITS |
| | | MIN | TYP | MAX | |
| t1 | CLOCK IN rising delay to $\overline{\text{DTREQ}}$ low | | | 40 | ns |
| t2 | $\overline{\text{DTREQ}}$ falling to $\overline{\text{DTGRT}}$ low (@20 MHz - 8 Bit Buffered Memory) | | N/A | | µs |
| | $\overline{\text{DTREQ}}$ falling to $\overline{\text{DTGRT}}$ low (@20 MHz - 16 Bit Buffered Memory) | | | 4.5 | µs |
| | $\overline{\text{DTREQ}}$ falling to $\overline{\text{DTGRT}}$ low (@16 MHz - 8 Bit Buffered Memory) | | N/A | | µs |
| | $\overline{\text{DTREQ}}$ falling to $\overline{\text{DTGRT}}$ low (@16 MHz - 16 Bit Buffered Memory) | | | 4 | µs |
| | $\overline{\text{DTREQ}}$ falling to $\overline{\text{DTGRT}}$ low (@12 MHz - 8 Bit Buffered Memory) | | N/A | | µs |
| | $\overline{\text{DTREQ}}$ falling to $\overline{\text{DTGRT}}$ low (@12 MHz - 16 Bit Buffered Memory) | | | 3.5 | µs |
| | $\overline{\text{DTREQ}}$ falling to $\overline{\text{DTGRT}}$ low (@10 MHz - 8 Bit Buffered Memory) | | N/A | | µs |
| | $\overline{\text{DTREQ}}$ falling to $\overline{\text{DTGRT}}$ low (@10 MHz - 16 Bit Buffered Memory) | | | 3.1 | µs |
| t3 | $\overline{\text{DTGRT}}$ low setup prior to CLOCK IN rising | 10 | | | ns |
| t4 | $\overline{\text{DTGRT}}$ falling to $\overline{\text{DTACK}}$ low (@20 MHz ) | | | 103 | ns |
| | $\overline{\text{DTGRT}}$ falling to $\overline{\text{DTACK}}$ low (@16 MHz ) | | | 115 | ns |
| | $\overline{\text{DTGRT}}$ falling to $\overline{\text{DTACK}}$ low (@12 MHz) | | | 135 | ns |
| | $\overline{\text{DTGRT}}$ falling to $\overline{\text{DTACK}}$ low (@10 MHz ) | | | 153 | ns |
| t5 | CLOCK IN rising to $\overline{\text{DTACK}}$ low | | | 40 | ns |
| t6 | $\overline{\text{DTGRT}}$ hold time following $\overline{\text{DTACK}}$ falling | 0 | | | ns |
| t7 | CLOCK IN rising to $\overline{\text{MEMENA\_OUT}}$ low | | | 40 | ns |
| t8 | CLOCK IN rising to Address outputs valid | | | 40 | ns |
| t9 | CLOCK IN rising to $\overline{\text{MEMOE}}$ low | | | 40 | ns |
| t10 | $\overline{\text{MEMENA\_IN}}$ setup delay following CLOCK IN rising (@20 MHz) | | | 20 | ns |
| | $\overline{\text{MEMENA\_IN}}$ setup delay following CLOCK IN rising (@16 MHz) | | | 30 | ns |
| | $\overline{\text{MEMENA\_IN}}$ setup delay following CLOCK IN rising (@12 MHz) | | | 50 | ns |
| | $\overline{\text{MEMENA\_IN}}$ setup delay following CLOCK IN rising (@10 MHz) | | | 70 | ns |
| t11 | $\overline{\text{DTACK}}$ low pulse width (@20 MHz – 8 Bit Memory Access) | | N/A | | ns |
| | $\overline{\text{DTACK}}$ low pulse width (@20 MHz – 16 Bit Memory Access) | | 250 | | ns |
| | $\overline{\text{DTACK}}$ low pulse width (@16 MHz – 8 Bit Memory Access) | | N/A | | ns |

| Table 17. Enhanced Mini-ACE Single Word DMA Read (Transparent Mode) | | | | | |
|---|---|---|---|---|---|
| REF | DESCRIPTION | Enhanced Mini-ACE | | | UNITS |
| | | MIN | TYP | MAX | |
| | $\overline{\text{DTACK}}$ low pulse width (@16 MHz – 16 Bit Memory Access) | 300 | 312.5 | 330 | ns |
| | $\overline{\text{DTACK}}$ low pulse width (@12 MHz – 8 Bit Memory Access) | | N/A | | ns |
| | $\overline{\text{DTACK}}$ low pulse width (@12 MHz – 16 Bit Memory Access) | 400 | 416.6 | 430 | ns |
| | $\overline{\text{DTACK}}$ low pulse width (@10 MHz – 8 Bit Memory Access) | | N/A | | ns |
| | $\overline{\text{DTACK}}$ low pulse width (@120 MHz – 16 Bit Memory Access) | | 500 | | ns |
| t12 | CLOCK IN rising to Output Data valid (Note: Asserted for reads from internal RAM only | | | 60 | ns |
| t13 | Input Data setup time prior to CLOCK IN rising (Note: Valid for reads from external RAM only) | 30 | | | ns |
| t14 | $\overline{\text{MEMOE}}$ low pulse width (@20 MHz – 8 but Memory) | | N/A | | ns |
| | $\overline{\text{MEMOE}}$ low pulse width (@20 MHz – 16 but Memory) | 135 | 150 | 165 | ns |
| | $\overline{\text{MEMOE}}$ low pulse width (@16 MHz – 8 but Memory) | | N/A | | ns |
| | $\overline{\text{MEMOE}}$ low pulse width (@16 MHz – 16 but Memory) | 170 | 187.5 | 200 | ns |
| | $\overline{\text{MEMOE}}$ low pulse width (@12 MHz – 8 but Memory) | | N/A | | ns |
| | $\overline{\text{MEMOE}}$ low pulse width (@12 MHz – 16 but Memory) | 235 | 250 | 265 | ns |
| | $\overline{\text{MEMOE}}$ low pulse width (@10 MHz – 8 but Memory) | | N/A | | ns |
| | $\overline{\text{MEMOE}}$ low pulse width (@10 MHz – 16 but Memory) | 285 | 300 | 315 | ns |
| t15 | Input Data hold time following CLOCK IN rising | 30 | | | ns |
| t16 | CLOCK IN rising to $\overline{\text{DTREQ}}$ high, $\overline{\text{DTACK}}$ high, $\overline{\text{MEMENA\_OUT}}$ high, $\overline{\text{MEMOE}}$ high | | | 40 | ns |
| t17 | Output Address and Output Data hold time following CLOCK IN rising | 0 | | | ns |
| t18 | CLOCK IN rising to Output Address and Output Data tri-state | | | 45 | ns |
| t19 | $\overline{\text{MEMENA\_IN}}$ low hold time following CLOCK IN rising edge | 0 | | | ns |

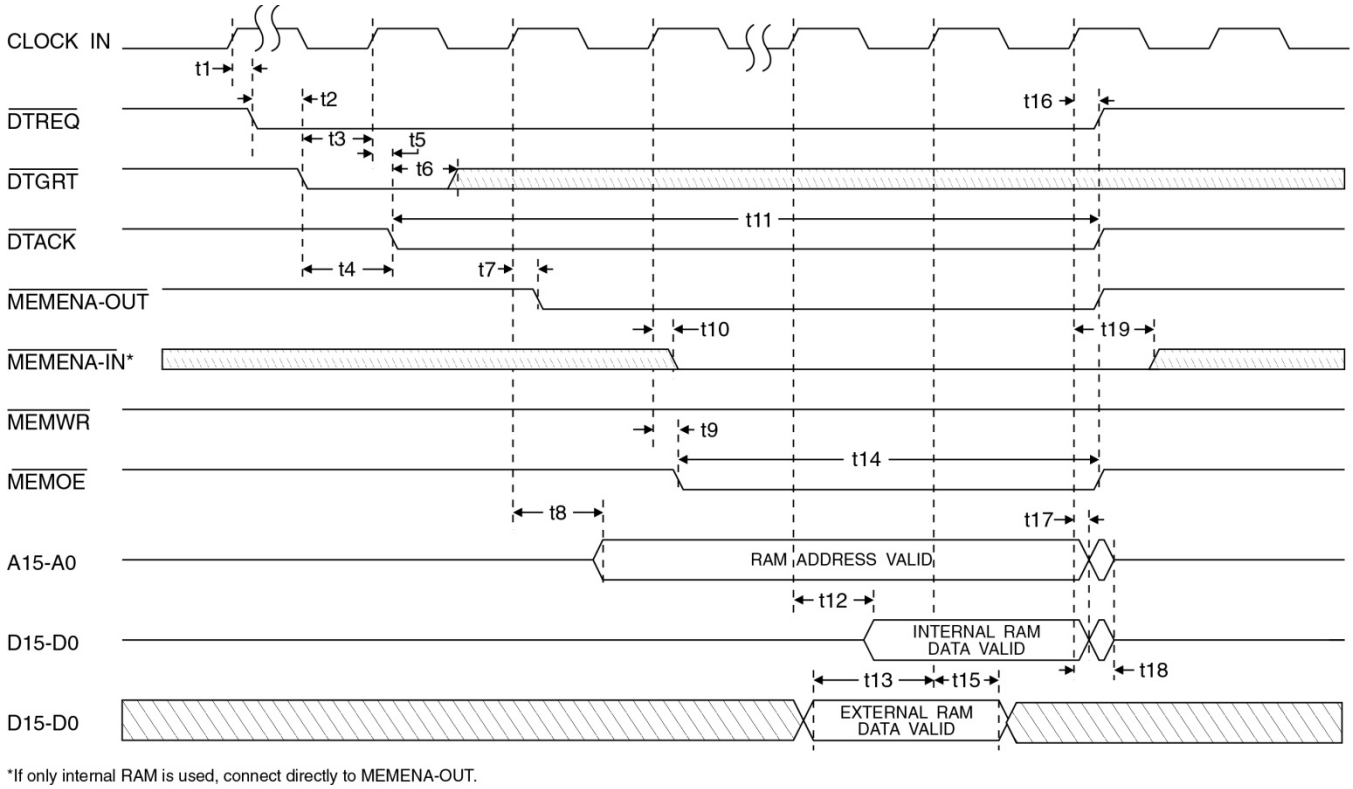



**Figure 46. Enhanced Mini-ACE Single Word DMA Read (Transparent Mode)**

| Table 18. Enhanced Mini-ACE Single Word DMA Write (Transparent Mode) | | | | | |
|---|---|---|---|---|---|
| REF | DESCRIPTION | Enhanced Mini-ACE | | | UNITS |
| | | MIN | TYP | MAX | |
| t1 | CLOCK IN rising delay to $\overline{\text{DTREQ}}$ low | | | 40 | ns |
| t2 | $\overline{\text{DTREQ}}$ falling to $\overline{\text{DTGRT}}$ low (@20 MHz - 8 Bit buffered Memory) | | N/A | | µs |
| | $\overline{\text{DTREQ}}$ falling to $\overline{\text{DTGRT}}$ low (@20 MHz - 16 Bit buffered Memory) | | | 4.5 | µs |
| | $\overline{\text{DTREQ}}$ falling to $\overline{\text{DTGRT}}$ low (@16 MHz - 8 Bit buffered Memory) | | N/A | | µs |
| | $\overline{\text{DTREQ}}$ falling to $\overline{\text{DTGRT}}$ low (@16 MHz - 16 Bit buffered Memory) | | | 4 | µs |
| | $\overline{\text{DTREQ}}$ falling to $\overline{\text{DTGRT}}$ low (@12 MHz - 8 Bit buffered Memory) | | N/A | | µs |
| | $\overline{\text{DTREQ}}$ falling to $\overline{\text{DTGRT}}$ low (@12 MHz - 16 Bit buffered Memory) | | | 3.5 | µs |
| | $\overline{\text{DTREQ}}$ falling to $\overline{\text{DTGRT}}$ low (@10 MHz - 8 Bit buffered Memory) | | N/A | | µs |
| | $\overline{\text{DTREQ}}$ falling to $\overline{\text{DTGRT}}$ low (@10 MHz - 16 Bit buffered Memory) | | | 3.1 | µs |
| t3 | $\overline{\text{DTGRT}}$ low setup prior to CLOCK IN rising | 10 | | | ns |
| t4 | $\overline{\text{DTGRT}}$ falling to $\overline{\text{DTACK}}$ low (@16 MHz) | | | 115 | ns |
| t4 | $\overline{\text{DTGRT}}$ falling to $\overline{\text{DTACK}}$ low (@12 MHz) | | | 135 | ns |
| t5 | CLOCK IN rising to $\overline{\text{DTACK}}$ low | | | 40 | ns |
| t6 | $\overline{\text{DTGRT}}$ hold time following $\overline{\text{DTACK}}$ falling | 0 | | | ns |
| t7 | CLOCK IN rising to $\overline{\text{MEMENA\_OUT}}$ low | | | 40 | ns |
| t8 | CLOCK IN rising to Address outputs valid | | | 40 | ns |
| t9 | CLOCK IN rising to Output Data valid | | | 40 | ns |
| t10 | $\overline{\text{DTACK}}$ low pulse width (@20 MHz - 8 Bit Memory Access) | | N/A | | ns |
| | $\overline{\text{DTACK}}$ low pulse width (@20 MHz - 16 Bit Memory Access) | 235 | 250 | 265 | ns |
| | $\overline{\text{DTACK}}$ low pulse width (@16 MHz - 8 Bit Memory Access) | | N/A | | ns |
| | $\overline{\text{DTACK}}$ low pulse width (@16 MHz - 16 Bit Memory Access) | 300 | 312.5 | 330 | ns |
| | $\overline{\text{DTACK}}$ low pulse width (@12 MHz - 8 Bit Memory Access) | | N/A | | ns |
| | $\overline{\text{DTACK}}$ low pulse width (@12 MHz - 16 Bit Memory Access) | 400 | 416.6 | 430 | ns |
| | $\overline{\text{DTACK}}$ low pulse width (@10 MHz - 8 Bit Memory Access) | | N/A | | ns |
| | $\overline{\text{DTACK}}$ low pulse width (@10 MHz - 16 Bit Memory Access) | 485 | 500 | 515 | ns |

| Table 18. Enhanced Mini-ACE Single Word DMA Write (Transparent Mode) | | | | | |
|---|---|---|---|---|---|
| REF | DESCRIPTION | Enhanced Mini-ACE | | | UNITS |
| | | MIN | TYP | MAX | |
| t11 | $\overline{\text{MEMENA\_IN}}$ setup delay following CLOCK IN rising (@16 MHz) | | | 40 | ns |
| t11 | $\overline{\text{MEMENA\_IN}}$ setup delay following CLOCK IN rising (@12 MHz) | | | 60 | ns |
| t12 | CLOCK IN rising to $\overline{\text{MEMWR}}$ low | | | 40 | ns |
| t13 | $\overline{\text{MEMWR}}$ low pulse width (@20 MHz) | 35 | 50 | 65 | ns |
| | $\overline{\text{MEMWR}}$ low pulse width (@16 MHz) | 50 | 62.5 | 80 | ns |
| | $\overline{\text{MEMWR}}$ low pulse width (@12 MHz) | 70 | 83.3 | 100 | ns |
| | $\overline{\text{MEMWR}}$ low pulse width (@10 MHz) | 85 | 100 | 115 | ns |
| t14 | CLOCK IN rising to $\overline{\text{MEMWR}}$ high | | | 40 | ns |
| t15 | $\overline{\text{MEMENA\_IN}}$ hold time following CLOCK IN rising | 0 | | | ns |
| t16 | CLOCK IN rising to $\overline{\text{DTREQ}}$ high, $\overline{\text{DTACK}}$ high, $\overline{\text{MEMENA\_OUT}}$ high | | | 40 | ns |
| t17 | Output Address and Output Data hold time following CLOCK IN rising | 0 | | | ns |
| t18 | CLOCK IN rising to Output Address and Output Data tri-state | | | 45 | ns |

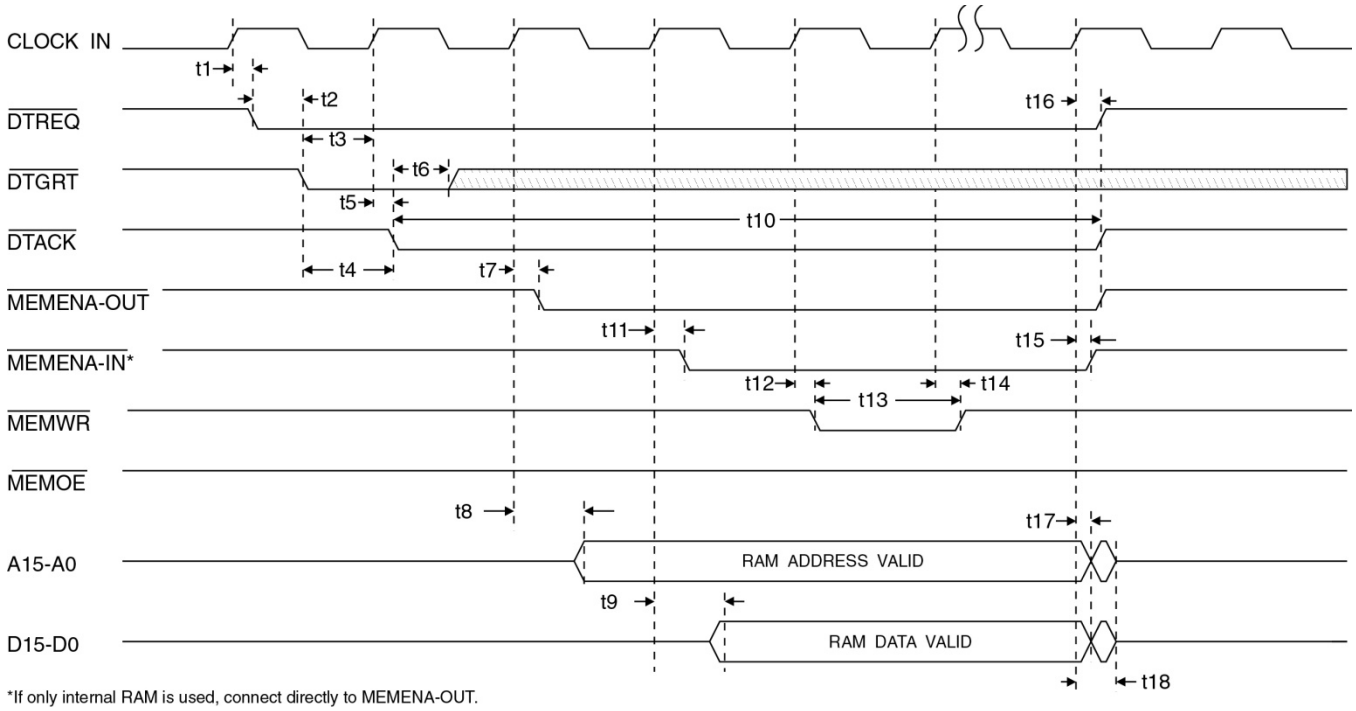



**Figure 47. Enhanced Mini-ACE Single Word DMA Write (Transparent Mode)**

| Table 19. BC/RT/MT SOM/EOM Burst Read/Write Timing | | | | | |
|---|---|---|---|---|---|
| REF | DESCRIPTION | Enhanced Mini-ACE | | | UNITS |
| | | MIN | TYP | MAX | |
| t1 | CLOCK IN rising delay to $\overline{\text{DTREQ}}$ low | | | 40 | ns |
| t2 | $\overline{\text{DTREQ}}$ falling to $\overline{\text{DTGRT}}$ low (@20 MHz - 8 Bit Buffered Memory) | | N/A | | µs |
| | $\overline{\text{DTREQ}}$ falling to $\overline{\text{DTGRT}}$ low (@20 MHz -16 Bit Buffered Memory) | | | 4.5 | µs |
| | $\overline{\text{DTREQ}}$ falling to $\overline{\text{DTGRT}}$ low (@16 MHz - 8 Bit Buffered Memory) | | N/A | | µs |
| | $\overline{\text{DTREQ}}$ falling to $\overline{\text{DTGRT}}$ low (@16 MHz -16 Bit Buffered Memory) | | | 4 | µs |
| | $\overline{\text{DTREQ}}$ falling to $\overline{\text{DTGRT}}$ low (@12 MHz - 8 Bit Buffered Memory) | | N/A | | µs |
| | $\overline{\text{DTREQ}}$ falling to $\overline{\text{DTGRT}}$ low (@12 MHz -16 Bit Buffered Memory) | | | 3.5 | µs |
| | $\overline{\text{DTREQ}}$ falling to $\overline{\text{DTGRT}}$ low (@10 MHz - 8 Bit Buffered Memory) | | N/A | | µs |
| | $\overline{\text{DTREQ}}$ falling to $\overline{\text{DTGRT}}$ low (@10 MHz -16 Bit Buffered Memory) | | | 3.1 | µs |
| t3 | $\overline{\text{DTGRT}}$ falling edge delay to $\overline{\text{DTACK}}$ falling edge (@20 MHz) | | | 107 | ns |
| | $\overline{\text{DTGRT}}$ falling edge delay to $\overline{\text{DTACK}}$ falling edge (@16 MHz) | | | 115 | ns |
| | $\overline{\text{DTGRT}}$ falling edge delay to $\overline{\text{DTACK}}$ falling edge (@12 MHz) | | | 135 | ns |
| | $\overline{\text{DTGRT}}$ falling edge delay to $\overline{\text{DTACK}}$ falling edge (@10 MHz) | | | 158 | ns |
| t4 | $\overline{\text{DTGRT}}$ low hold time following $\overline{\text{DTACK}}$ falling edge. | 0 | | | ns |
| t5 | CLOCK IN rising to $\overline{\text{DTACK}}$ low | | | 40 | ns |
| t6 | CLOCK IN rising to $\overline{\text{MEMENA\_OUT}}$ low | | | 40 | ns |
| t7 | CLOCK IN rising to Address outputs valid | | | 40 | ns |
| t8 | CLOCK IN rising to $\overline{\text{MEMOE}}$ low | | | 40 | ns |
| t9 | $\overline{\text{MEMENA\_IN}}$ setup delay following to CLOCK IN rising | | | 30 | ns |
| t10 | CLOCK IN rising to Output Data valid (Note: asserted for reads from internal RAM only) | | | 60 | ns |
| t11 | Input Data setup time prior to CLOCK IN rising (Note: valid for reads from external RAM only) | 30 | | | ns |
| t12 | Input Data hold time following CLOCK IN rising | 30 | | | ns |
| t13 | $\overline{\text{MEMENA\_IN}}$ valid hold time following CLOCK IN rising edge. | 0 | | | ns |
| t14 | CLOCK IN rising edge delay to $\overline{\text{MEMOE}}$ rising edge. | | | 40 | ns |
| t15 | Output Address and Output Data valid hold time following CLOCK IN rising edge. | 0 | | | ns |

| Table 19. BC/RT/MT SOM/EOM Burst Read/Write Timing | | | | | |
|---|---|---|---|---|---|
| REF | DESCRIPTION | Enhanced Mini-ACE | | | UNITS |
| | | MIN | TYP | MAX | |
| t16 | CLOCK IN rising edge delay to Output Address valid for next address. | | | 50 | ns |
| t17 | CLOCK IN rising edge delay to Output Data tri-state. | | | 45 | ns |
| t18 | CLOCK IN rising edge delay to Output Data valid. | | | 40 | ns |
| t19 | CLOCK IN rising edge delay to $\overline{\text{MEMWR}}$ falling edge. | | | 40 | ns |
| t20 | CLOCK IN rising edge delay to $\overline{\text{MEMWR}}$ rising edge. | | | 40 | ns |
| t22 | CLOCK IN rising edge delay to $\overline{\text{DTREQ}}$ rising edge. | | | 35 | ns |
| t23 | CLOCK IN rising edge delay to $\overline{\text{DTACK}}$ rising edge. | | | 35 | ns |
| t24 | CLOCK IN rising edge delay to $\overline{\text{MEMENA\_OUT}}$ rising edge. | | | 40 | ns |
| t25 | CLOCK IN rising edge delay to Output Address tri-state. | | | 45 | ns |

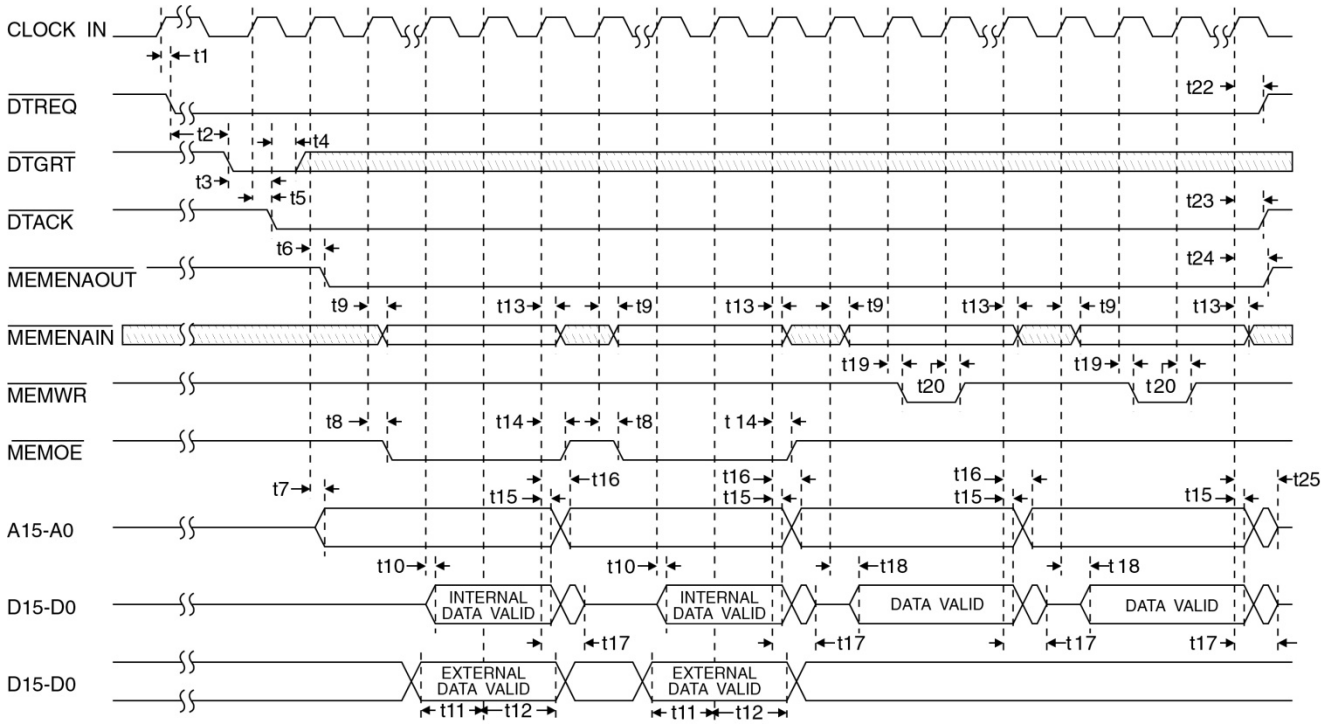



**Figure 48. BC/RT/MT SOM/EOM Burst Read/Write Timing**

## 10.4 BC Operation

FIGURES 44 thru 53 illustrate the overall BC message sequence timing for receive, transmit, and broadcast message formats. Each message sequence shows an SOM and EOM sequence as well as single word DMA read cycles and/or DMA write cycles. One of the DMA write cycles shown in the sequence is a command word or data word "looped back." Each word transmitted by the Enhanced Mini-ACE is also decoded by the Enhanced Mini-ACE's receiver section. The transmitter and receiver sections are independent within the Enhanced Mini-ACE and operate independently. Upon completion of the last word transmitted by the Enhanced Mini-ACE (Command word in a transmit message or a data word in a receive message), assuming that there are no errors detected by the receiver, the received copy of the word is written into the Enhanced Mini-ACE's RAM in a location referred to as the loopback word. The loopback word is stored in RAM to provide a simple mechanism for self testing the Enhanced Mini-ACE.

Figure 52 illustrates BC start timing for messages in a frame. The first message in a frame may be started by either an external trigger input, an internal trigger (internal frame timer), or a software start (start bit in start/reset register). Subsequent message in a frame will start based on the minimum intermessage gap time, as illustrated in Figure 52, unless the Message Gap time feature is used to increase this time. Figure 53 and Figure 54 illustrate the BC Start Of Message (SOM) and End Of Message (EOM) sequences. Figure 55 illustrates the timing of automatic retries.

| Table 20. BC Mode Receive Message Timing Sequence | | | | | |
|---|---|---|---|---|---|
| REF | DESCRIPTION | Enhanced Mini-ACE | | | UNITS |
| | | MIN | TYP | MAX | |
| t1 | Mid-sync crossing of current word delay to $\overline{\text{DTREQ}}$ falling (requesting next data word read access) (@20 MHz) | 1.0 | 1.12 | 1.2 | µs |
| | Mid-sync crossing of current word delay to $\overline{\text{DTREQ}}$ falling (requesting next data word read access) (@16 MHz) | 1.2 | 1.35 | 1.45 | µs |
| | Mid-sync crossing of current word delay to $\overline{\text{DTREQ}}$ falling (requesting next data word read access) (@12 MHz) | 1.36 | 1.52 | 1.6 | µs |
| | Mid-sync crossing of current word delay to $\overline{\text{DTREQ}}$ falling (requesting next data word read access) (@10 MHz) | 1.5 | 1.65 | 1.8 | µs |
| t2 | RT Response timeout (note 1). | | | 18.5 | µs |
| t3 | Mid-parity crossing of status word to $\overline{\text{DTREQ}}$ falling (requesting status word write access) (@20 MHz) | 1.04 | 1.32 | 1.60 | µs |
| | Mid-parity crossing of status word to $\overline{\text{DTREQ}}$ falling (requesting status word write access) (@16 MHz) | 1.2 | 1.41 | 1.77 | µs |
| | Mid-parity crossing of status word to $\overline{\text{DTREQ}}$ falling (requesting status word write access) (@12 MHz) | 1.36 | 1.6 | 1.98 | µs |
| | Mid-parity crossing of status word to $\overline{\text{DTREQ}}$ falling (requesting status word write access) (@10 MHz) | 1.45 | 1.75 | 2.1 | µs |
| t4 | Mid-parity crossing of status word to $\overline{\text{DTREQ}}$ falling (requesting BC end of message access) (@20 MHz) | 6.58 | 6.8 | 7.16 | µs |
| | Mid-parity crossing of status word to $\overline{\text{DTREQ}}$ falling (requesting BC end of message access) (@16 MHz) | 6.70 | 6.91 | 7.27 | µs |
| | Mid-parity crossing of status word to $\overline{\text{DTREQ}}$ falling (requesting BC end of message access) (@12 MHz) | 6.78 | 7.02 | 7.39 | µs |
| | Mid-parity crossing of status word to $\overline{\text{DTREQ}}$ falling (requesting BC end of message access) (@10 MHz) | 6.85 | 7.1 | 7.47 | µs |
| t5 | Mid-parity crossing of last transmitted word to $\overline{\text{DTREQ}}$ falling (requesting loopback word write access) (@20 MHz) | 2.92 | 3.15 | 3.25 | µs |
| | Mid-parity crossing of last transmitted word to $\overline{\text{DTREQ}}$ falling (requesting loopback word write access) (@16 MHz) | 3.06 | 3.29 | 3.37 | µs |
| | Mid-parity crossing of last transmitted word to $\overline{\text{DTREQ}}$ falling (requesting loopback word write access) (@12 MHz) | 3.20 | 3.43 | 3.51 | µs |
| | Mid-parity crossing of last transmitted word to $\overline{\text{DTREQ}}$ falling (requesting loopback word write access) (@10 MHz) | 3.50 | 3.75 | 3.83 | µs |

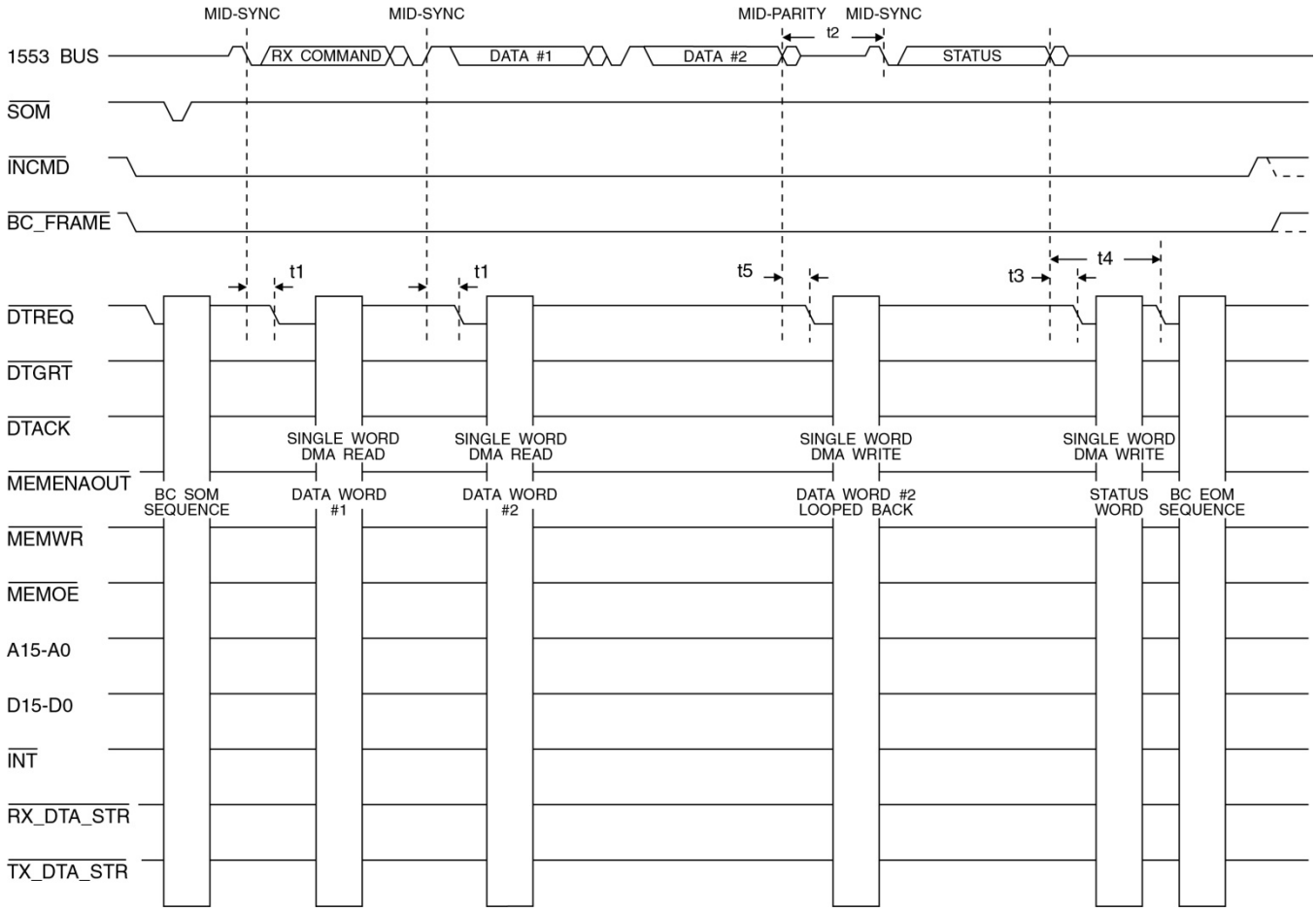



**Figure 49. BC Mode Receive Message Timing Sequence**

| Table 21. BC Mode Transmit Message Timing Sequence | | | | | |
|---|---|---|---|---|---|
| REF | DESCRIPTION | Enhanced Mini-ACE | | | UNITS |
| | | MIN | TYP | MAX | |
| t1 | RT Response timeout (note 1). | | | 18.5 | µs |
| t2 | Mid-parity crossing delay to $\overline{\text{DTREQ}}$ falling (requesting loopback write access) (@20 MHz) | 2.92 | 3.15 | 3.25 | µs |
| | Mid-parity crossing delay to $\overline{\text{DTREQ}}$ falling (requesting loopback write access) (@16 MHz) | 3.06 | 3.29 | 3.37 | µs |
| | Mid-parity crossing delay to $\overline{\text{DTREQ}}$ falling (requesting loopback write access) (@12 MHz) | 3.20 | 3.43 | 3.51 | µs |
| | Mid-parity crossing delay to $\overline{\text{DTREQ}}$ falling (requesting loopback write access) (@10 MHz) | 3.50 | 3.75 | 3.83 | µs |
| t3 | Mid-parity crossing delay to $\overline{\text{DTREQ}}$ falling (requesting BC end of message access) (@20 MHz) | 6.58 | 6.8 | 7.16 | µs |
| | Mid-parity crossing delay to $\overline{\text{DTREQ}}$ falling (requesting BC end of message access) (@16 MHz) | 6.70 | 6.91 | 7.27 | µs |
| | Mid-parity crossing delay to $\overline{\text{DTREQ}}$ falling (requesting BC end of message access) (@12 MHz) | 6.78 | 7.02 | 7.39 | µs |
| | Mid-parity crossing delay to $\overline{\text{DTREQ}}$ falling (requesting BC end of message access) (@10 MHz) | 6.85 | 7.1 | 7.47 | µs |
| t4 | Mid-parity crossing delay to $\overline{\text{DTREQ}}$ falling (requesting Status and Data Word write access) (@20 MHz) | 1.04 | 1.32 | 1.60 | µs |
| | Mid-parity crossing delay to $\overline{\text{DTREQ}}$ falling (requesting Status and Data Word write access) (@16 MHz) | 1.20 | 1.41 | 1.77 | µs |
| | Mid-parity crossing delay to $\overline{\text{DTREQ}}$ falling (requesting Status and Data Word write access) (@12 MHz) | 1.36 | 1.60 | 1.98 | µs |
| | Mid-parity crossing delay to $\overline{\text{DTREQ}}$ falling (requesting Status and Data Word write access) (@10 MHz) | 1.45 | 1.75 | 2.1 | µs |

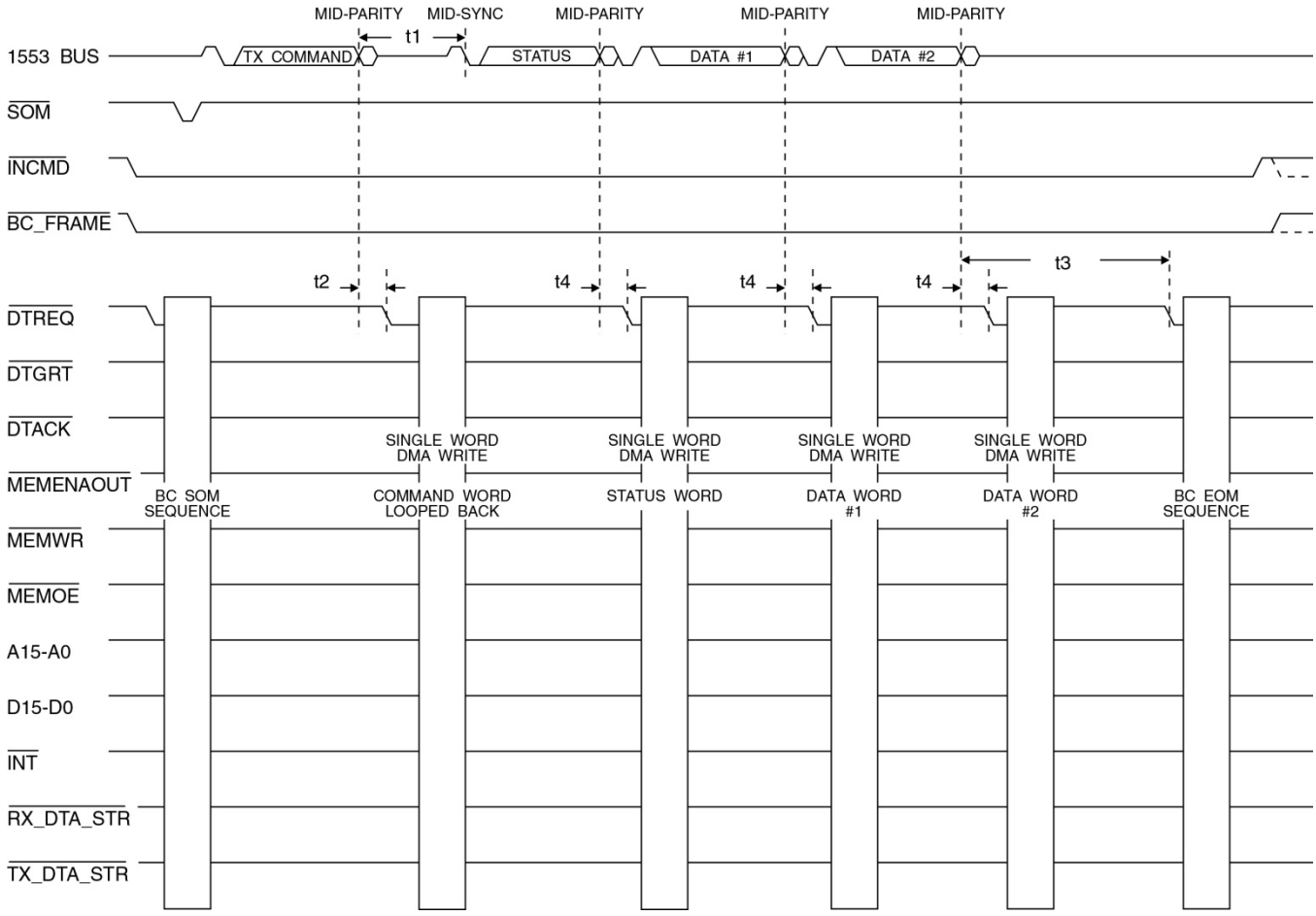



**Figure 50. BC Mode Transmit Message Timing Sequence**

NOTES For Table 20 and Table 21 and Figure 49 and Figure 50
Intermessage gap may be extended under software control. The message gap timer is assumed to be disabled.
Assumed $\overline{\text{DTREQ}}$ is connected to $\overline{\text{DTGRT}}$, there is no CPU contention, and all transfers are to memory.

| Table 22. BC Mode Broadcast Message Timing Sequence | | | | | |
|---|---|---|---|---|---|
| REF | DESCRIPTION | Enhanced Mini-ACE | | | UNITS |
| | | MIN | TYP | MAX | |
| t1 | Mid-sync crossing of current word delay to $\overline{\text{DTREQ}}$ falling (requesting next data word read access) (@20 MHz) | 1.0 | 1.12 | 1.2 | µs |
| | Mid-sync crossing of current word delay to $\overline{\text{DTREQ}}$ falling (requesting next data word read access) (@16 MHz) | 1.20 | 1.35 | 1.45 | µs |
| | Mid-sync crossing of current word delay to $\overline{\text{DTREQ}}$ falling (requesting next data word read access) (@12 MHz) | 1.36 | 1.52 | 1.60 | µs |
| | Mid-sync crossing of current word delay to $\overline{\text{DTREQ}}$ falling (requesting next data word read access) (@10 MHz) | 1.5 | 1.65 | 1.8 | µs |
| t2 | Mid-parity crossing of last data word to $\overline{\text{DTREQ}}$ falling (loopback word write access request) (@20 MHz) | 2.92 | 3.15 | 3.25 | µs |
| | Mid-parity crossing of last data word to $\overline{\text{DTREQ}}$ falling (loopback word write access request) (@16 MHz) | 3.06 | 3.29 | 3.37 | µs |
| | Mid-parity crossing of last data word to $\overline{\text{DTREQ}}$ falling (loopback word write access request) (@12 MHz) | 3.20 | 3.43 | 3.51 | µs |
| | Mid-parity crossing of last data word to $\overline{\text{DTREQ}}$ falling (loopback word write access request) (@10 MHz) | 3.50 | 3.75 | 3.83 | µs |
| t3 | $\overline{\text{DTREQ}}$ rising to $\overline{\text{DTREQ}}$ falling (@20 MHz) | 75 | 100 | 125 | ns |
| | $\overline{\text{DTREQ}}$ rising to $\overline{\text{DTREQ}}$ falling (@16 MHz) | 100 | 125 | 150 | ns |
| | $\overline{\text{DTREQ}}$ rising to $\overline{\text{DTREQ}}$ falling (@12 MHz) | 140 | 166 | 190 | ns |
| | $\overline{\text{DTREQ}}$ rising to $\overline{\text{DTREQ}}$ falling (@10 MHz) | 175 | 200 | 225 | ns |

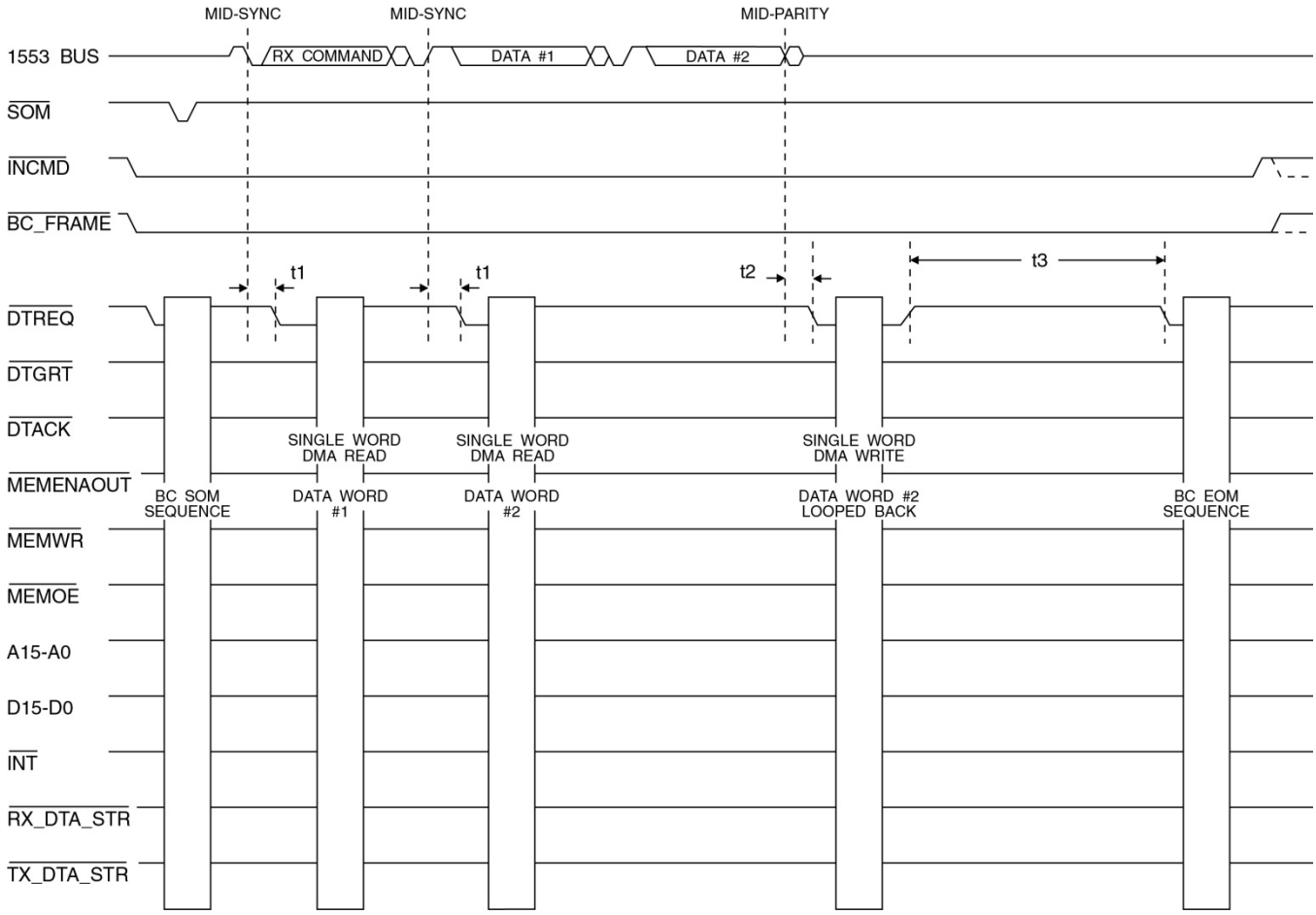



**Figure 51. BC Mode Broadcast Message Timing Sequence**

| Table 23. BC Mode Start Timing | | | | | |
|---|---|---|---|---|---|
| REF | DESCRIPTION | ENHANCED Mini-ACE | | | UNITS |
| | | MIN | TYP | MAX | |
| t1 | $\overline{\text{READYD}}$ falling (write access to start register bit) delay to $\overline{\text{DTREQ}}$ falling (BC SOM) (@20 MHz) | 120 | 150 | 180 | ns |
| | **Error! Objects cannot be created from editing field codes.** falling (write access to start register bit) delay to $\overline{\text{DTREQ}}$ falling (BC SOM) (@16 MHz) | 160 | 188 | 220 | ns |
| | $\overline{\text{READYD}}$ falling (write access to start register bit) delay to $\overline{\text{DTREQ}}$ falling (BC SOM) (@12 MHz) | 220 | 250 | 280 | ns |
| | $\overline{\text{READYD}}$ falling (write access to start register bit) delay to $\overline{\text{DTREQ}}$ falling (BC SOM) (@10 MHz) | 270 | 300 | 330 | ns |
| t2 | $\overline{\text{EXT\_TRIG}}$ rising delay to $\overline{\text{DTREQ}}$ falling (BC SOM) (@20 MHz) | 145 | 175 | 225 | ns |
| | $\overline{\text{EXT\_TRIG}}$ rising delay to $\overline{\text{DTREQ}}$ falling (BC SOM) (@16 MHz) | 160 | 220 | 280 | ns |
| | $\overline{\text{EXT\_TRIG}}$ rising delay to $\overline{\text{DTREQ}}$ falling (BC SOM) (@12 MHz) | 220 | 290 | 360 | ns |
| | $\overline{\text{EXT\_TRIG}}$ rising delay to $\overline{\text{DTREQ}}$ falling (BC SOM) (@10 MHz) | 287 | 350 | 445 | ns |
| t3 | BC Intermessage GAP (Note 1,2) (@20 MHz - first Broadcast message) | 8.4 | 8.5 | 8.7 | µs |
| | BC Intermessage GAP (Note 1,2) (@20 MHz - non-Broadcast message) | 10.7 | 10.8 | 11.0 | µs |
| | BC Intermessage GAP (Note 1,2) (@16 MHz - first Broadcast message) | 9.0 | 9.1 | 9.2 | µs |
| | BC Intermessage GAP (Note 1,2) (@16 MHz - non-Broadcast message) | 11.9 | 12.2 | 12.7 | µs |
| | BC Intermessage GAP (Note 1,2) (@12 MHz - first Broadcast message) | 10.6 | 10.7 | 10.8 | µs |
| | BC Intermessage GAP (Note 1,2) (@12 MHz - non-Broadcast message) | 13.2 | 13.6 | 14.1 | µs |
| | BC Intermessage GAP (Note 1,2) (@10 MHz - first Broadcast message) | 14.6 | 14.8 | 15.1 | µs |
| | BC Intermessage GAP (Note 1,2) (@10 MHz - non-Broadcast message) | 15.8 | 16.0 | 16.3 | µs |
| t4 | $\overline{\text{INCMD}}$ rising delay to $\overline{\text{INCMD}}$ falling (Note 1) (@20 MHz) | 35 | 50 | 65 | ns |
| | $\overline{\text{INCMD}}$ rising delay to $\overline{\text{INCMD}}$ falling (Note 1) (@16 MHz) | 40 | 62.5 | 85 | ns |
| | $\overline{\text{INCMD}}$ rising delay to $\overline{\text{INCMD}}$ falling (Note 1) (@12 MHz) | 60 | 83.3 | 105 | ns |
| | $\overline{\text{INCMD}}$ rising delay to $\overline{\text{INCMD}}$ falling (Note 1) (@10 MHz) | 85 | 100 | 115 | ns |
| t5 | $\overline{\text{INCMD}}$ falling delay to $\overline{\text{DTREQ}}$ falling (BC SOM) (@20 MHz) | 35 | 50 | 65 | ns |
| | $\overline{\text{INCMD}}$ falling delay to $\overline{\text{DTREQ}}$ falling (BC SOM) (@16 MHz) | 40 | 62.5 | 85 | ns |
| | $\overline{\text{INCMD}}$ falling delay to $\overline{\text{DTREQ}}$ falling (BC SOM) (@12 MHz) | 60 | 83.3 | 105 | ns |

| Table 23. BC Mode Start Timing | | | | | |
|---|---|---|---|---|---|
| REF | DESCRIPTION | ENHANCED Mini-ACE | | | UNITS |
| | | MIN | TYP | MAX | |
| | $\overline{\text{INCMD}}$ falling delay to $\overline{\text{DTREQ}}$ falling (BC SOM) (@10 MHz) | 85 | 100 | 115 | ns |
| t6 | $\overline{\text{DTACK}}$ falling delay to $\overline{\text{DTACK}}$ rising (@20 MHz) | 1.15 | 1.20 | 1.25 | µs |
| | $\overline{\text{DTACK}}$ falling delay to $\overline{\text{DTACK}}$ rising (@16 MHz) | 1.77 | 1.81 | 1.85 | µs |
| | $\overline{\text{DTACK}}$ falling delay to $\overline{\text{DTACK}}$ rising (@12 MHz) | 2.37 | 2.42 | 2.46 | µs |
| | $\overline{\text{DTACK}}$ falling delay to $\overline{\text{DTACK}}$ rising (@10 MHz) | 2.75 | 2.85 | 2.95 | µs |
| t7 | $\overline{\text{DTACK}}$ rising delay to mid-sync crossing of command word (@20 MHz) | 1.70 | 1.80 | 2.0 | µs |
| | $\overline{\text{DTACK}}$ rising delay to mid-sync crossing of command word (@16 MHz) | 1.82 | 1.90 | 2.05 | µs |
| | $\overline{\text{DTACK}}$ rising delay to mid-sync crossing of command word (@12 MHz) | 1.90 | 1.98 | 2.14 | µs |
| | $\overline{\text{DTACK}}$ rising delay to mid-sync crossing of command word (@10 MHz) | 1.95 | 2.05 | 2.25 | µs |

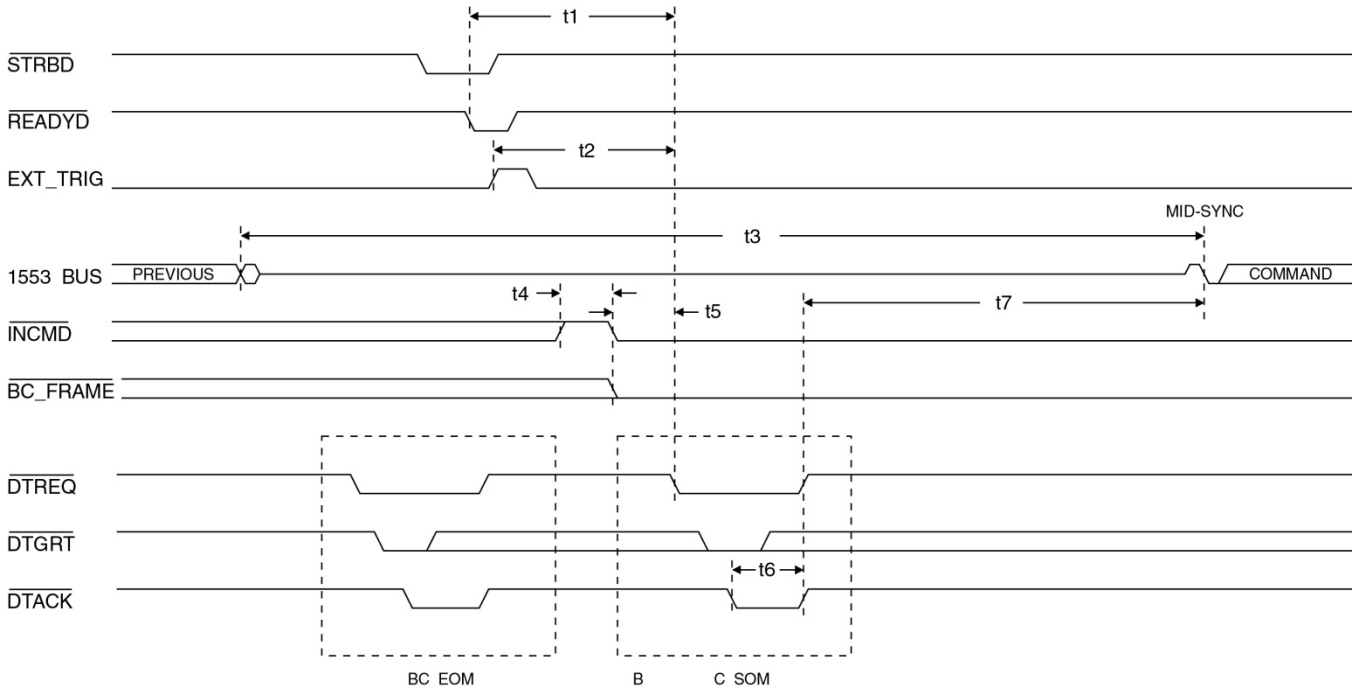



**Figure 52. BC Mode Start Timing**

| Table 24. BC Start of Message (SOM) Sequence Timing | | | | | |
|---|---|---|---|---|---|
| REF | DESCRIPTION | Enhanced Mini-ACE | | | UNITS |
| | | MIN | TYP | MAX | |
| t1 | $\overline{\text{DTREQ}}$ falling delay $\overline{\text{DTGRT}}$ low. | | | ∞ | µs |
| t2 | $\overline{\text{DTGRT}}$ falling delay to $\overline{\text{DTACK}}$ falling (@20 MHz). | | | 102 | ns |
| | $\overline{\text{DTGRT}}$ falling delay to $\overline{\text{DTACK}}$ falling (@16 MHz). | | | 115 | ns |
| | $\overline{\text{DTGRT}}$ falling delay to $\overline{\text{DTACK}}$ falling (@12 MHz). | | | 135 | ns |
| | $\overline{\text{DTGRT}}$ falling delay to $\overline{\text{DTACK}}$ falling (@10 MHz). | | | 152 | ns |
| t3 | $\overline{\text{DTGRT}}$ low hold time following $\overline{\text{DTACK}}$ falling. | 0 | | | ns |
| t4 | $\overline{\text{DTACK}}$ falling delay to $\overline{\text{DTREQ}}$ rising, $\overline{\text{DTACK}}$ rising, and $\overline{\text{MEMENAOUT}}$ rising (@20 MHz). | | 1.45 | | µs |
| | $\overline{\text{DTACK}}$ falling delay to $\overline{\text{DTREQ}}$ rising, $\overline{\text{DTACK}}$ rising, and $\overline{\text{MEMENAOUT}}$ rising (@16 MHz). | | 1.82 | | µs |
| | $\overline{\text{DTACK}}$ falling delay to $\overline{\text{DTREQ}}$ rising, $\overline{\text{DTACK}}$ rising, and $\overline{\text{MEMENAOUT}}$ rising (@12 MHz). | | 2.42 | | µs |
| | $\overline{\text{DTACK}}$ falling delay to $\overline{\text{DTREQ}}$ rising, $\overline{\text{DTACK}}$ rising, and $\overline{\text{MEMENAOUT}}$ rising (@10 MHz). | | 2.90 | | µs |
| t5 | $\overline{\text{SOM}}$ active low pulse width (@20 MHz). | | 50 | | ns |
| | $\overline{\text{SOM}}$ active low pulse width (@16 MHz). | | 62.5 | | ns |
| | $\overline{\text{SOM}}$ active low pulse width (@12 MHz). | | 83.3 | | ns |
| | $\overline{\text{SOM}}$ active low pulse width (@10 MHz). | | 100 | | ns |
| t6 | Data Bus (D15-D0) valid setup prior to $\overline{\text{SOM}}$ rising. | 60 | | | ns |
| t7 | Data Bus (D15-D0) valid hold time following $\overline{\text{SOM}}$ rising. | 60 | | | ns |
| t8 | $\overline{\text{DTACK}}$ rising delay to mid-sync crossing of command word (@20 MHz) | 1.70 | 1.80 | 2.0 | µs |
| | $\overline{\text{DTACK}}$ rising delay to mid-sync crossing of command word (@16 MHz) | 1.82 | 1.9 | 2.05 | µs |
| | $\overline{\text{DTACK}}$ rising delay to mid-sync crossing of command word (@12 MHz) | 1.90 | 1.98 | 2.14 | µs |
| | $\overline{\text{DTACK}}$ rising delay to mid-sync crossing of command word (@10 MHz) | 1.95 | 2.05 | 2.25 | µs |

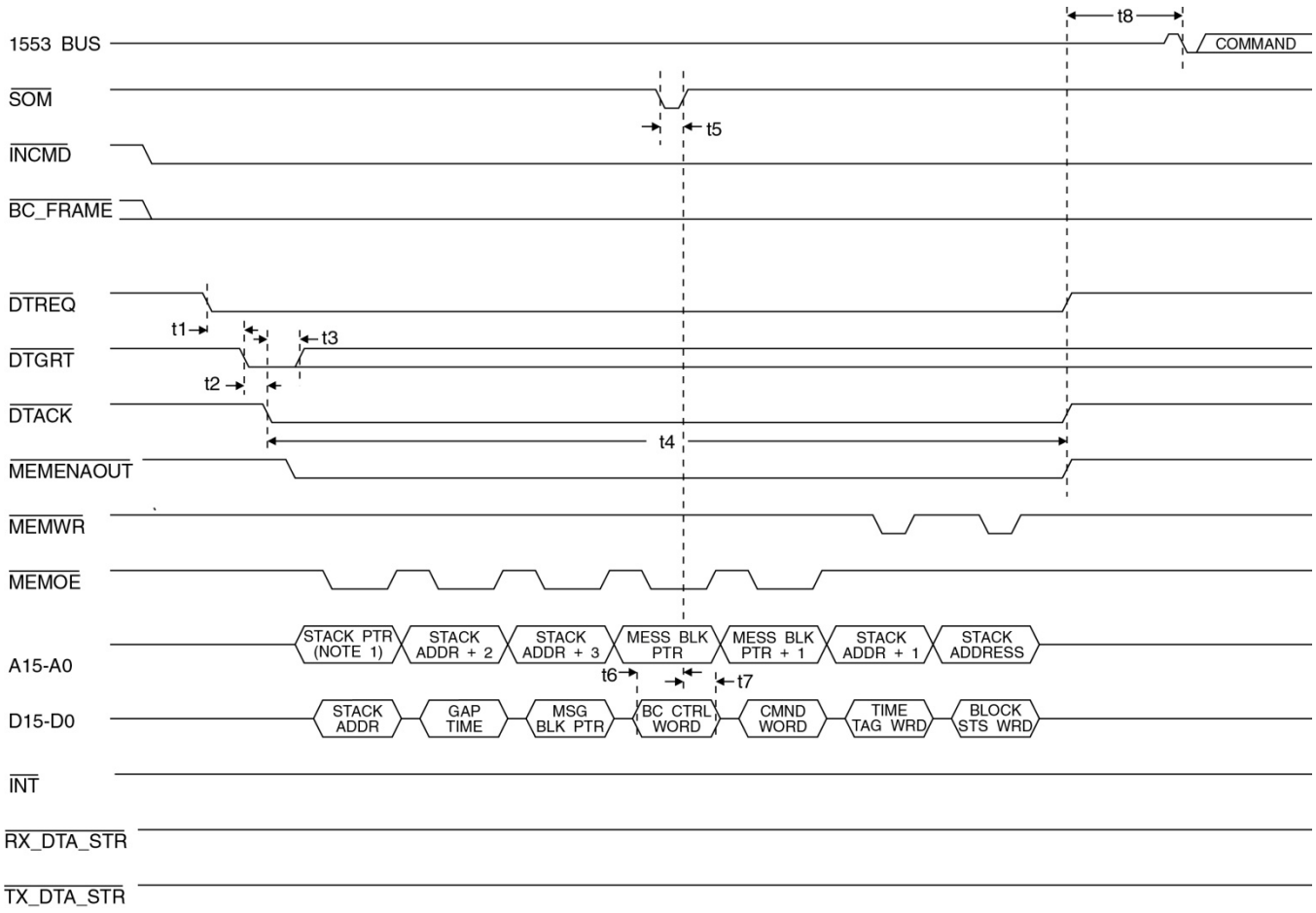



**Figure 53. BC Start of Message (SOM) Sequence Timing**

| Table 25. BC End of (EOM) Sequence Timing | | | | | |
|---|---|---|---|---|---|
| REF | DESCRIPTION | Enhanced Mini-ACE | | | UNITS |
| | | MIN | TYP | MAX | |
| t1 | Mid-parity crossing of last word delay to $\overline{\text{DTREQ}}$ falling (@20 MHz) | 6.58 | 6.8 | 7.16 | µs |
| | Mid-parity crossing of last word delay to $\overline{\text{DTREQ}}$ falling (@16 MHz) | 6.70 | 6.91 | 7.27 | µs |
| | Mid-parity crossing of last word delay to $\overline{\text{DTREQ}}$ falling (@12 MHz) | 6.78 | 7.02 | 7.39 | µs |
| | Mid-parity crossing of last word delay to $\overline{\text{DTREQ}}$ falling (@10 MHz) | 6.85 | 7.1 | 7.47 | µs |
| t2 | $\overline{\text{DTREQ}}$ falling delay to $\overline{\text{DTGRT}}$ falling | | | | µs |
| t3 | $\overline{\text{DTGRT}}$ falling delay to $\overline{\text{DTACK}}$ falling (@20 MHz) | | | 102 | ns |
| | $\overline{\text{DTGRT}}$ falling delay to $\overline{\text{DTACK}}$ falling (@16 MHz) | | | 115 | ns |
| | $\overline{\text{DTGRT}}$ falling delay to $\overline{\text{DTACK}}$ falling (@12 MHz) | | | 135 | ns |
| | $\overline{\text{DTGRT}}$ falling delay to $\overline{\text{DTACK}}$ falling (@10 MHz) | | | 152 | ns |
| t4 | $\overline{\text{DTGRT}}$ low hold time following $\overline{\text{DTACK}}$ falling. | 0 | | | ns |
| t5 | $\overline{\text{DTACK}}$ falling delay to $\overline{\text{DTREQ}}$ rising, $\overline{\text{DTACK}}$ rising, and $\overline{\text{MEMENAOUT}}$ rising (@20 MHz) | | 1.05 | | µs |
| | $\overline{\text{DTACK}}$ falling delay to $\overline{\text{DTREQ}}$ rising, $\overline{\text{DTACK}}$ rising, and $\overline{\text{MEMENAOUT}}$ rising (@16 MHz) | | 1.3125 | | µs |
| | $\overline{\text{DTACK}}$ falling delay to $\overline{\text{DTREQ}}$ rising, $\overline{\text{DTACK}}$ rising, and $\overline{\text{MEMENAOUT}}$ rising (@12 MHz) | | 1.75 | | µs |
| | $\overline{\text{DTACK}}$ falling delay to $\overline{\text{DTREQ}}$ rising, $\overline{\text{DTACK}}$ rising, and $\overline{\text{MEMENAOUT}}$ rising (@10 MHz) | | 2.10 | | µs |
| t6 | $\overline{\text{DTACK}}$ falling delay to $\overline{\text{INT}}$ falling (@20 MHz) (Note 1) | | 1.00 | | µs |
| | $\overline{\text{DTACK}}$ falling delay to $\overline{\text{INT}}$ falling (@16 MHz) (Note 1) | | 1.25 | | µs |
| | $\overline{\text{DTACK}}$ falling delay to $\overline{\text{INT}}$ falling (@12 MHz) (Note 1) | | 1.66 | | µs |
| | $\overline{\text{DTACK}}$ falling delay to $\overline{\text{INT}}$ falling (@10 MHz) (Note 1) | | 2.00 | | µs |
| t7 | $\overline{\text{INT}}$ active low pulse width (Notes 1,2). | | 500 | | ns |
| t8 | $\overline{\text{DTACK}}$ rising delay to $\overline{\text{INCMD}}$ rising (@20 MHz) | | 50.0 | | ns |
| | $\overline{\text{DTACK}}$ rising delay to $\overline{\text{INCMD}}$ rising (@16 MHz) | | 62.5 | | ns |
| | $\overline{\text{DTACK}}$ rising delay to $\overline{\text{INCMD}}$ rising (@12 MHz) | | 83.3 | | ns |
| | $\overline{\text{DTACK}}$ rising delay to $\overline{\text{INCMD}}$ rising (@10 MHz) | | 100.0 | | ns |

| Table 25. BC End of (EOM) Sequence Timing | | | | | |
|---|---|---|---|---|---|
| **REF** | **DESCRIPTION** | **Enhanced Mini-ACE** | | | **UNITS** |
| t9 | $\overline{\text{DTACK}}$ rising delay to $\overline{\text{BC\_FRAME}}$ rising (@20 MHz) | | 100 | | ns |
| | $\overline{\text{DTACK}}$ rising delay to $\overline{\text{BC\_FRAME}}$ rising (@16 MHz) | | 125 | | ns |
| | $\overline{\text{DTACK}}$ rising delay to $\overline{\text{BC\_FRAME}}$ rising (@12 MHz) | | 166 | | ns |
| | $\overline{\text{DTACK}}$ rising delay to $\overline{\text{BC\_FRAME}}$ rising (@10 MHz) | | 200 | | ns |

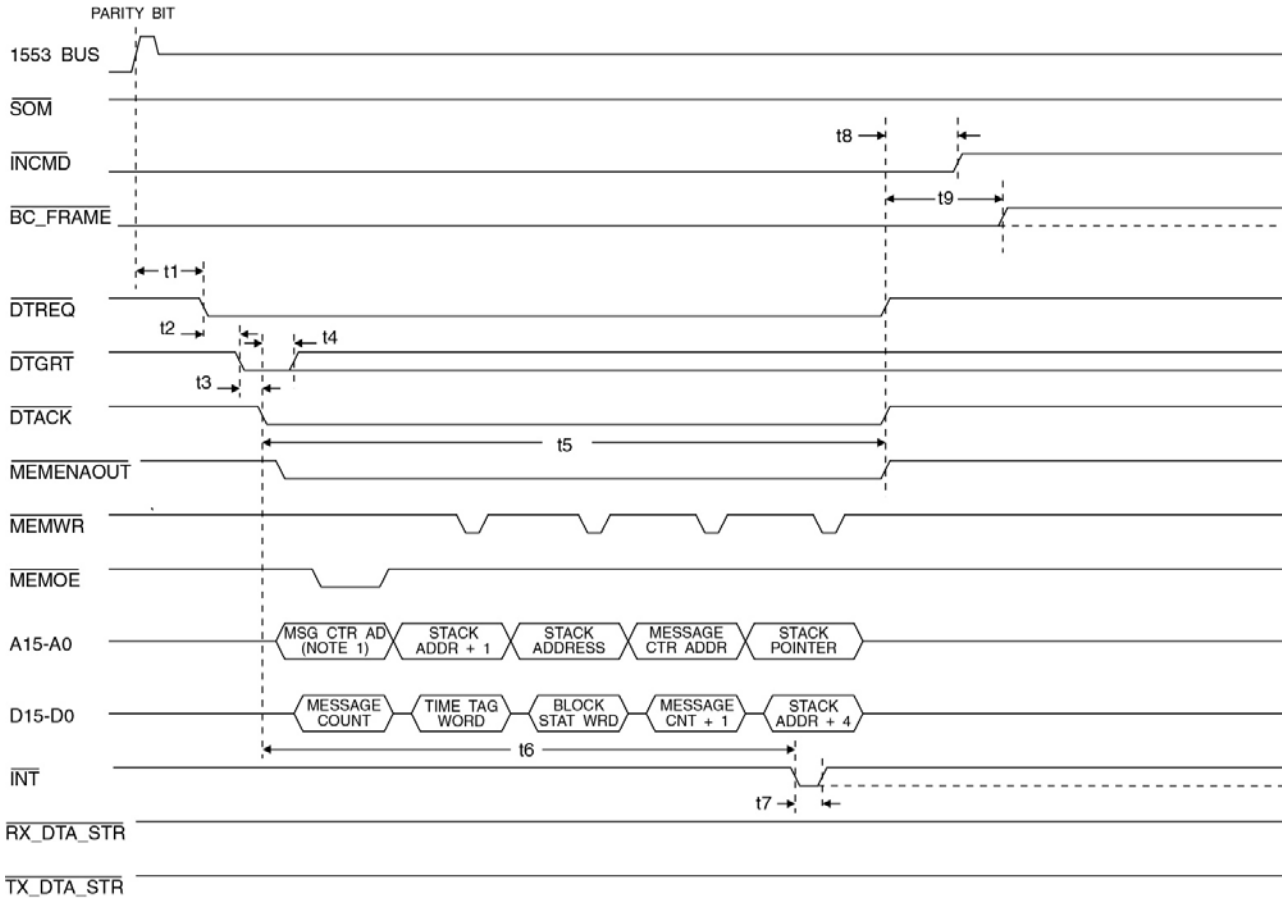



**Figure 54. BC End of Message (EOM) Sequence Timing**

NOTES For Table 25 and Figure 54
1. Assumes that the interrupt is enabled. Applies to all interrupts which occur with the end of a message.
2. Interrupt output is software programmable for a pulse or level output. Pulse mode of operation is assumed.

| Table 26. BC Retry Timing | | | | | |
|---|---|---|---|---|---|
| REF | DESCRIPTION | Enhanced Mini-ACE | | | UNITS |
| | | MIN | TYP | MAX | |
| t1a | Mid-parity crossing delay to $\overline{\text{DTREQ}}$ falling (Retry due to invalid word, incorrect sync, high word count or status address mismatch) | 6.7 | 6.9 | 7.5 | µs |
| t1b | Mid-parity crossing delay to $\overline{\text{DTREQ}}$ falling (Retry due to no response or low word count) (programmable) | 23 | | 23.7 | µs |
| t1c | $\overline{\text{DTREQ}}$ rising to $\overline{\text{DTREQ}}$ falling (Retry due to loop test fail on broadcast command) | | 2 | | clk |
| t2 | $\overline{\text{DTREQ}}$ falling delay to $\overline{\text{DTGRT}}$ falling. | | | ∞ | ns |
| t3 | $\overline{\text{DTGRT}}$ falling delay to $\overline{\text{DTACK}}$ falling (@20 MHz) | | | 102 | ns |
| | $\overline{\text{DTGRT}}$ falling delay to $\overline{\text{DTACK}}$ falling (@16 MHz) | | | 115 | ns |
| | $\overline{\text{DTGRT}}$ falling delay to $\overline{\text{DTACK}}$ falling (@12 MHz) | | | 135 | ns |
| | $\overline{\text{DTGRT}}$ falling delay to $\overline{\text{DTACK}}$ falling (@10 MHz) | | | 152 | ns |
| t4 | $\overline{\text{DTGRT}}$ low hold time following $\overline{\text{DTACK}}$ falling. | 0 | | | ns |
| t5 | $\overline{\text{DTACK}}$ falling delay to $\overline{\text{DTREQ}}$ rising, $\overline{\text{DTACK}}$ rising, and $\overline{\text{MEMENAOUT}}$ rising (@20 MHz) | | 0.650 | | µs |
| | $\overline{\text{DTACK}}$ falling delay to $\overline{\text{DTREQ}}$ rising, $\overline{\text{DTACK}}$ rising, and $\overline{\text{MEMENAOUT}}$ rising (@16 MHz) | | 0.812 | | µs |
| | $\overline{\text{DTACK}}$ falling delay to $\overline{\text{DTREQ}}$ rising, $\overline{\text{DTACK}}$ rising, and $\overline{\text{MEMENAOUT}}$ rising (@12 MHz) | | 1.083 | | µs |
| | $\overline{\text{DTACK}}$ falling delay to $\overline{\text{DTREQ}}$ rising, $\overline{\text{DTACK}}$ rising, and $\overline{\text{MEMENAOUT}}$ rising (@10 MHz) | | 1.300 | | µs |
| t6 | $\overline{\text{DTACK}}$ rising delay to mid-sync crossing of command word (@20 MHz) | 1.70 | 1.80 | 2.0 | µs |
| | $\overline{\text{DTACK}}$ rising delay to mid-sync crossing of command word (@16 MHz) | 1.82 | 1.9 | 2.05 | µs |
| | $\overline{\text{DTACK}}$ rising delay to mid-sync crossing of command word (@12 MHz) | 1.90 | 1.98 | 2.14 | µs |
| | $\overline{\text{DTACK}}$ rising delay to mid-sync crossing of command word (@10 MHz) | 1.95 | 2.05 | 2.25 | µs |

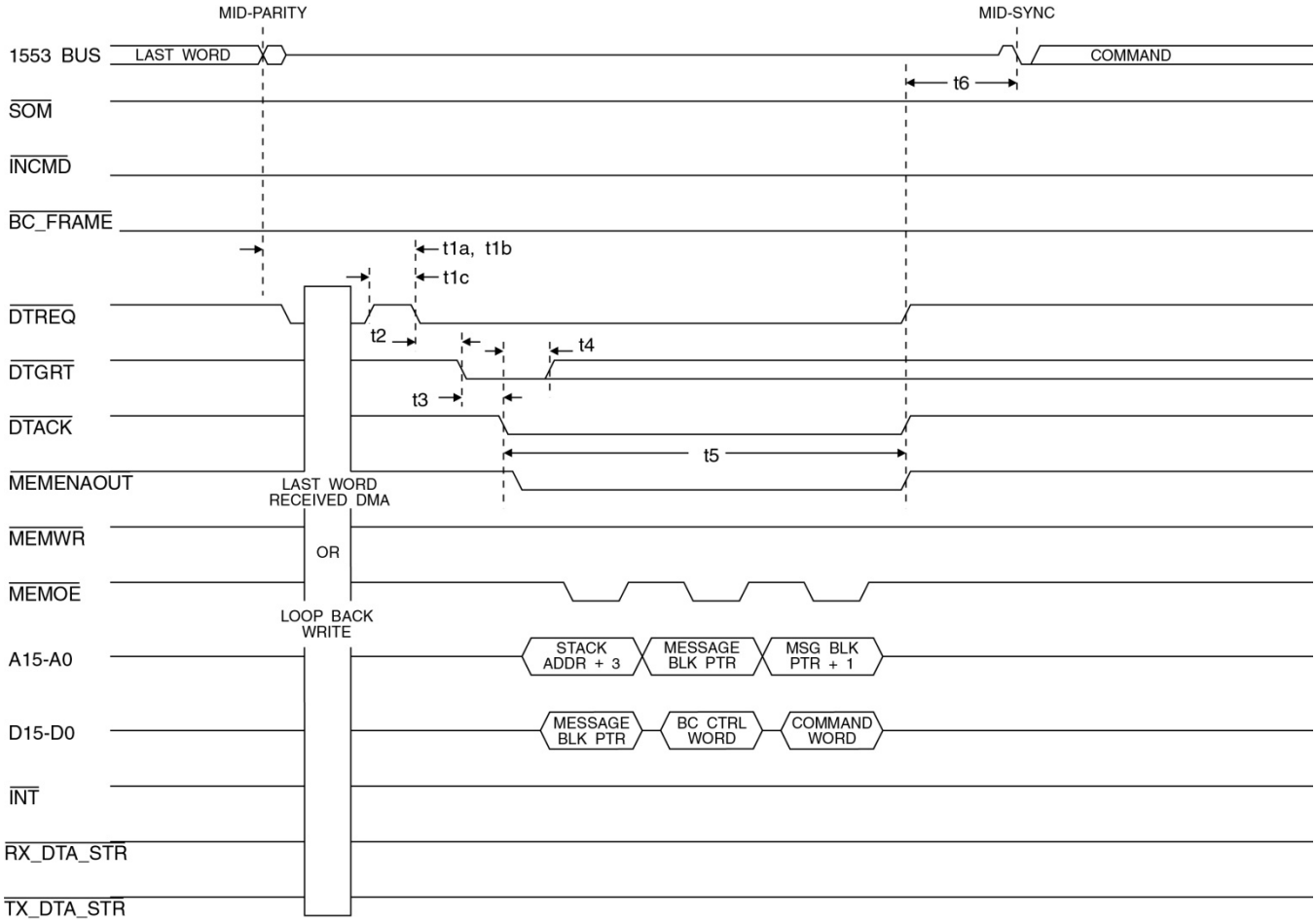



**Figure 55. BC Retry Timing**

NOTES for Table 26 and Figure 55

1. Time based on default no response timeout program (18.5 µs typ.). For Enhanced Mini-ACE products, add 5.3 µs to typical value.
2. Last word received applicable to t1A timings and loop back write applicable to t1B and t1C timings.

## 10.5 RT Operation

Figure 56 thru Figure 60 illustrate the overall RT message sequence timing for receive, transmit, and broadcast message formats. Figure 59 and Figure 60 illustrate the RT Start Of Message Sequence and the End Of Message Sequence. The Start Of Message output signal ($\overline{SOM}$) is driven low during the SOM sequence at the time when the received command word is driven onto the data bus (D15-D0). The timing of the $\overline{SOM}$ signal matches the timing of the write strobe ($\overline{MEMWR}$) and such can be used to externally latch the command word. Note also the that 1553 status bits are latched internally on the rising edge of the $\overline{SOM}$ pulse ($\overline{SSFLAG}$ is the only status bit which is driven from an external source).

During the RT SOM sequence several optional transfers are shown as dashed lines. The illegalization table is only accessed if command illegalization is enabled (bit 7 in configuration register #3 set to logic 0). A read of the busy bit table (transfer #3 in the SOM) only occurs if the busy bit lookup feature is enabled (bit 13 in configuration register #2 set to logic 1). The subaddress control word (SOM transfer #4) will only occur if enhanced RT memory management is enabled (bit 1 in configuration register #2 is set to logic 1) and the command is not a mode code or enhanced mode code handling is not enabled (bit 0 of configuration register #3 set to logic 0). The data block pointer is read (SOM transfer #5) for all commands except any mode code if enhanced mode code handling is enabled (bit 0 of configuration register #3 set to logic 1). If such is the case, the mode code interrupt look-up table will be read.

The RT EOM sequence also contains several optional transfers. The subaddress control word is re-read if enhanced RT memory management is enabled (bit 1 in configuration register #2 is set to logic 1) and the command is to receive data to a block address and the double buffering feature is enabled (bit 12 of configuration register #2 is set to logic 1). The data block address is re-read from the lookup table (EOM transfer #2) if subaddress double buffering is enabled and the command is to receive data to a block address. A write of a single data word to the third location on the descriptor stack (EOM transfer #2) will occur if the current message is a mode code with data and enhanced mode code handling is enabled (bit 0 of configuration register #3 set to logic 1). A write to the subaddress data pointer will occur if the data pointer has to be updated either because double-buffering was enabled or the stack address must be updated.

**Table 27. RT Receive Message Timing**

| REF | DESCRIPTION | Enhanced Mini-ACE | | | UNITS |
|---|---|---|---|---|---|
| | | MIN | TYP | MAX | |
| t1 | Mid-parity crossing of received command word to RT Address and RT Address Parity sampled. | 500 | 800 | 1100 | ns |
| t2 | RT Address and RT Address Parity setup prior to sampling. | 500 | | | ns |
| t3 | RT Address and RT Address Parity hold time following sampling. | 500 | | | ns |
| t4 | Mid-parity crossing of received command word to $\overline{\text{DTREQ}}$ falling edge (requesting RT Start Of Message transfer) (@20 MHz) (Note 1) | 1.10 | 1.39 | 1.75 | µs |
| | Mid-parity crossing of received command word to $\overline{\text{DTREQ}}$ falling edge (requesting RT Start Of Message transfer) (@16 MHz) (Note 1) | 1.26 | 1.49 | 1.83 | µs |
| | Mid-parity crossing of received command word to $\overline{\text{DTREQ}}$ falling edge (requesting RT Start Of Message transfer) (@12 MHz) (Note 1) | 1.44 | 1.60 | 2.06 | µs |
| | Mid-parity crossing of received command word to $\overline{\text{DTREQ}}$ falling edge (requesting RT Start Of Message transfer) (@10 MHz) (Note 1) | 1.49 | 1.69 | 2.15 | µs |
| t5 | Mid-parity crossing of received data word to $\overline{\text{DTREQ}}$ falling edge (requesting data word write transfer) (@20 MHz) | 1.12 | 1.35 | 1.68 | µs |
| | Mid-parity crossing of received data word to $\overline{\text{DTREQ}}$ falling edge (requesting data word write transfer) (@16 MHz) | 1.20 | 1.43 | 1.77 | µs |
| | Mid-parity crossing of received data word to $\overline{\text{DTREQ}}$ falling edge (requesting data word write transfer) (@12 MHz) | 1.36 | 1.52 | 1.98 | µs |
| | Mid-parity crossing of received data word to $\overline{\text{DTREQ}}$ falling edge (requesting data word write transfer) (@10 MHz) | 1.42 | 1.60 | 2.05 | µs |
| t6 | RT response time (6.9 µs max if buffered or $\overline{\text{DTGRT}}$ applied with 2 µsec for Enhanced Mini-ACE) | 5.9 | 6.3 | 9.4 | µs |
| t7 | Mid-parity crossing of RT status word to $\overline{\text{DTREQ}}$ falling edge (requesting RT End Of Message transfer). | 2.8 | | 3.2 | µs |

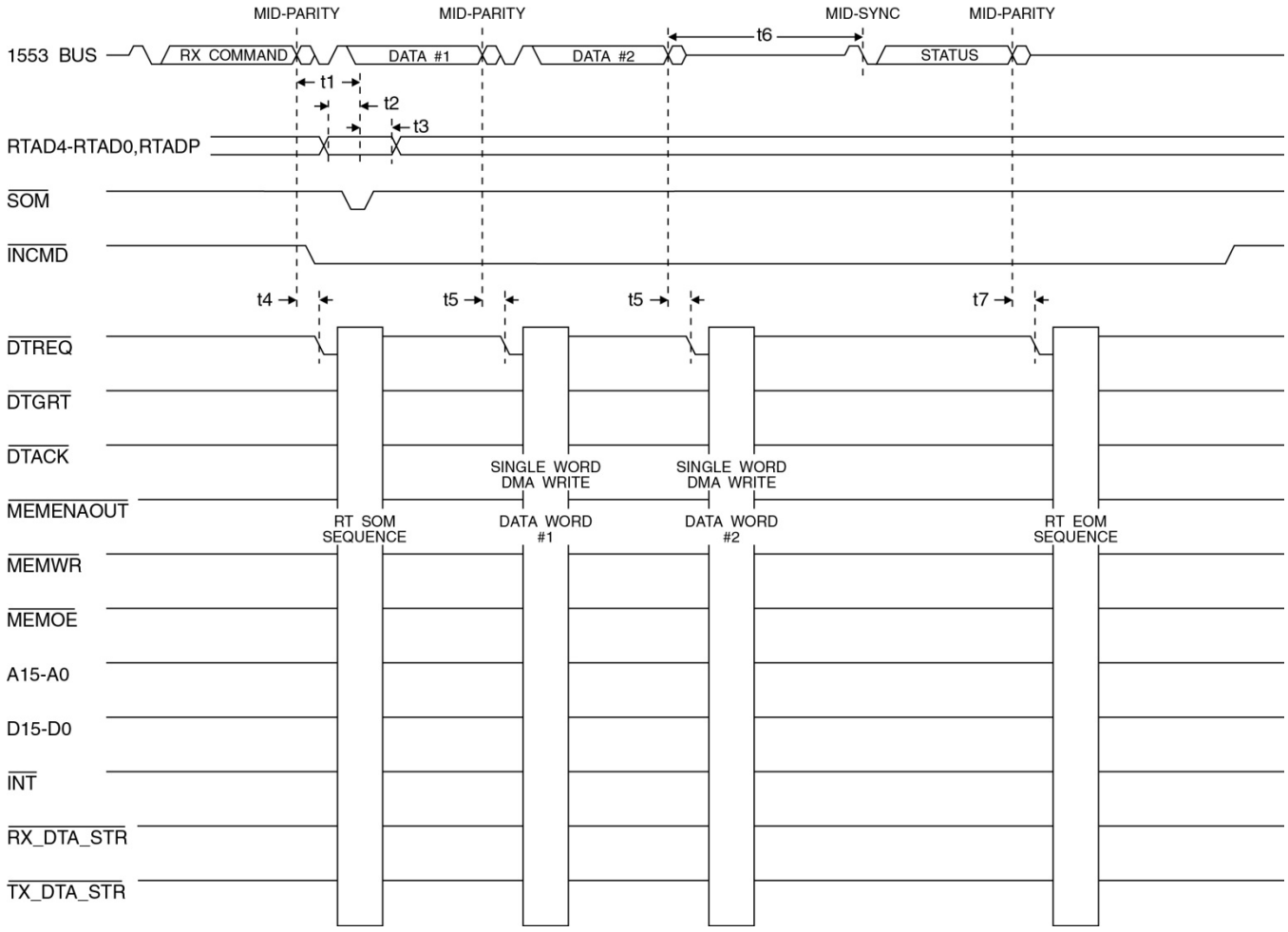



**Figure 56. RT Receive Message Timing**

NOTES For Table 27 and Figure 56
1. If superseding command, max time can increase by 5 clk cycles.

| Table 28. RT Transit Message Timing | | | | | |
|---|---|---|---|---|---|
| REF | DESCRIPTION | Enhanced Mini-ACE | | | UNITS |
| | | MIN | TYP | MAX | |
| t1 | RT Response time (6.9 s max if buffered or $\overline{\text{DTGRT}}$ applied within 2 sec for Enhanced Mini-ACE) | 5.9 | 6.3 | 9.4 | µs |
| t2 | Mid-parity crossing of received command word to RT Address and RT Address Parity sampled. | 500 | 800 | 1100 | ns |
| t3 | RT Address and RT Address Parity setup prior to sampling. | 500 | | | ns |
| t4 | RT Address and RT Address Parity hold time following sampling. | 500 | | | ns |
| t5 | Mid-parity crossing of received command word to $\overline{\text{DTREQ}}$ falling edge (requesting RT Start Of Message transfer). | 1.25 | | 2.1 | µs |
| t6 | Mid-sync crossing of current transmitting word to $\overline{\text{DTREQ}}$ falling edge (requesting data word read transfer of next word to be transmitted). | 1.2 | | 1.6 | µs |
| t7 | Mid-parity crossing of last transmitted word to $\overline{\text{DTREQ}}$ falling edge (requesting RT End Of Message transfer). | 2.8 | | 3.2 | µs |

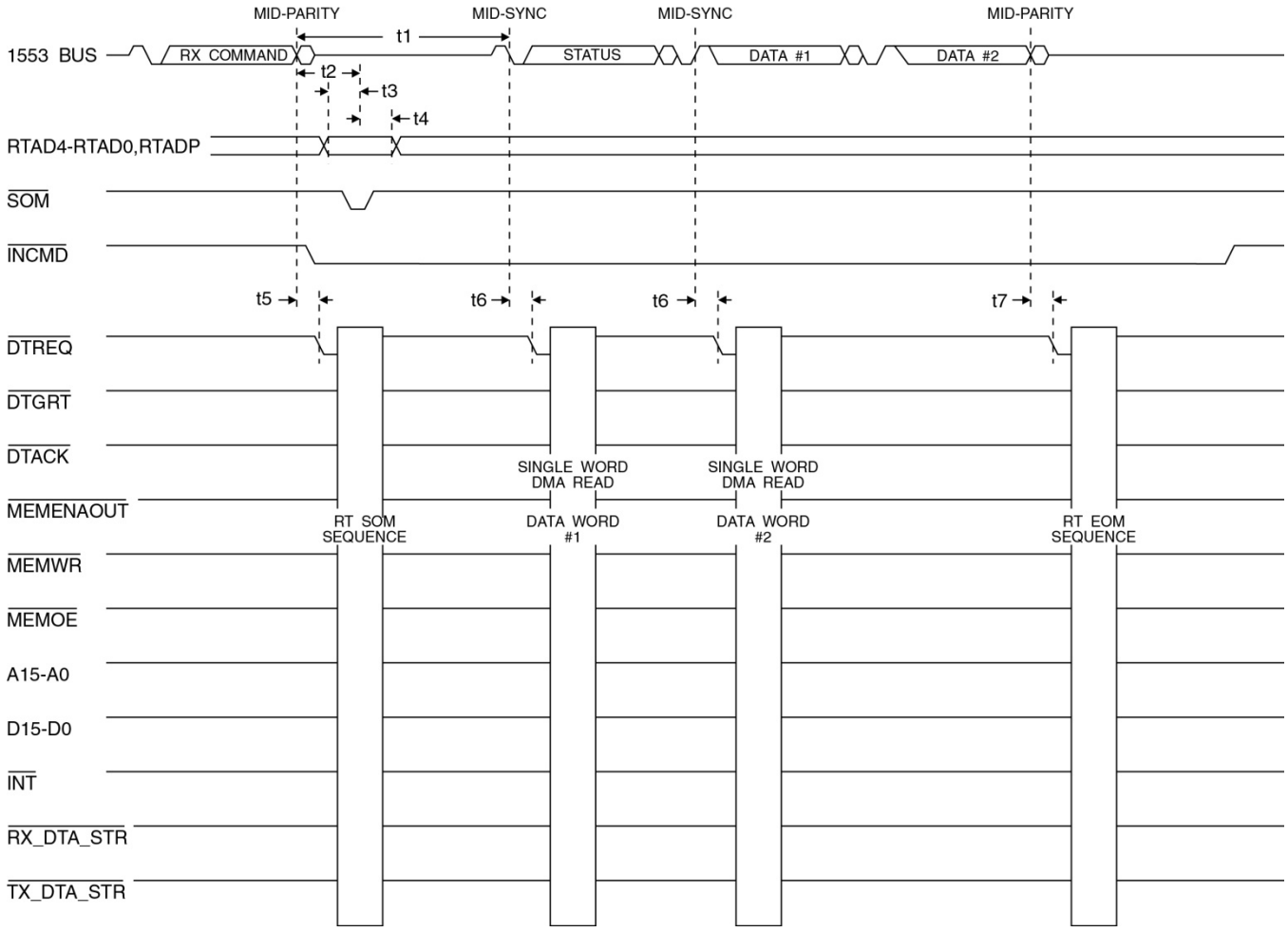



**Figure 57. RT Transmit Message Timing**

NOTES For Table 28 and Figure 57

1. In the event SOM sequence stretches into first DMA read cycle, $\overline{\text{DTREQ}}$ will fall 1 clk cycle after $\overline{\text{DTREQ}}$ rises.

| Table 29. RT Broadcast Receive Message Timing | | | | | |
|---|---|---|---|---|---|
| REF | DESCRIPTION | Enhanced Mini-ACE | | | UNITS |
| | | MIN | TYP | MAX | |
| t1 | Mid-parity crossing of received command word to RT Address and RT Address Parity sampled. | 500 | 800 | 1100 | ns |
| t2 | RT Address and RT Address Parity setup prior to sampling. | 500 | | | ns |
| t3 | RT Address and RT Address Parity hold time following sampling. | 500 | | | ns |
| t4 | Mid-parity crossing of received command word to $\overline{\text{DTREQ}}$ falling edge (requesting RT Start Of Message transfer). | 1.25 | | 2.1 | µs |
| t5 | Mid-parity crossing of received data word to $\overline{\text{DTREQ}}$ falling edge (requesting data word write transfer). | 1.2 | | 2.0 | µs |
| t6 | Mid-parity crossing of last received data word to $\overline{\text{DTREQ}}$ falling edge (requesting RT End Of Message transfer). | 6.7 | | 7.4 | µs |

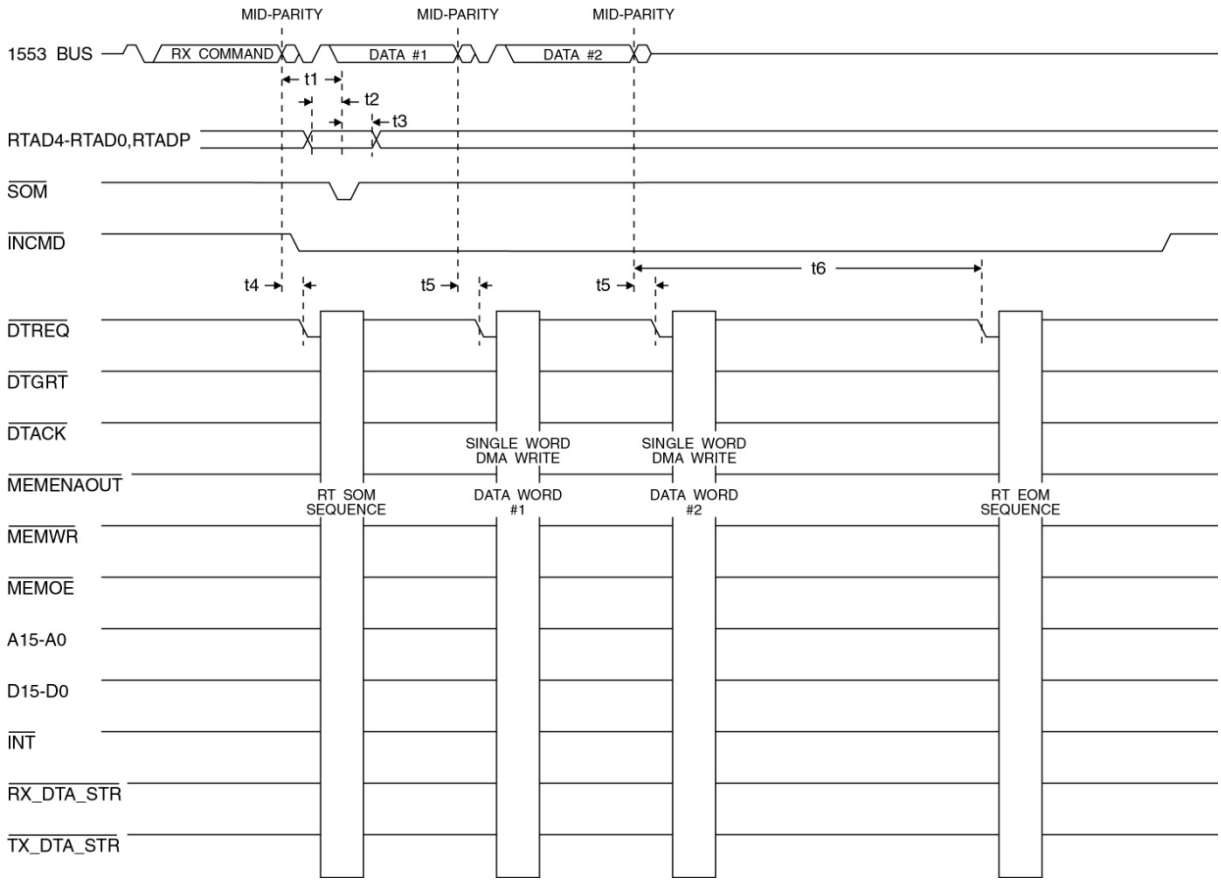



**Figure 58. RT Broadcast Receive Message Timing**

| Table 30. RT Start of Message Timing | | | | | |
|---|---|---|---|---|---|
| REF | DESCRIPTION | Enhanced Mini-ACE | | | UNITS |
| | | MIN | TYP | MAX | |
| t1 | Mid-parity crossing of received command word delay to $\overline{\text{INCMD}}$ falling edge. | 1.2 | | 2.0 | µs |
| t2 | Mid-parity crossing of received command word delay to $\overline{\text{DTREQ}}$ falling edge (requesting RT Start Of Message transfer sequence). | 1.25 | | 2.1 | µs |
| t3 | $\overline{\text{DTREQ}}$ falling edge delay to $\overline{\text{DTGRT}}$ falling edge (@20 MHz) (Note 1) | | | 4.5 | µs |
| | $\overline{\text{DTREQ}}$ falling edge delay to $\overline{\text{DTGRT}}$ falling edge (@16 MHz) (Note 1) | | | 4.0 | µs |
| | $\overline{\text{DTREQ}}$ falling edge delay to $\overline{\text{DTGRT}}$ falling edge (@12 MHz) (Note 1) | | | 3.5 | µs |
| | $\overline{\text{DTREQ}}$ falling edge delay to $\overline{\text{DTGRT}}$ falling edge (@10 MHz) (Note 1) | | | 3.1 | µs |
| t4 | $\overline{\text{DTGRT}}$ falling edge delay to $\overline{\text{DTACK}}$ falling edge (@20 MHz) | | | 102 | ns |
| | $\overline{\text{DTGRT}}$ falling edge delay to $\overline{\text{DTACK}}$ falling edge (@16 MHz) | | | 115 | ns |
| | $\overline{\text{DTGRT}}$ falling edge delay to $\overline{\text{DTACK}}$ falling edge (@12 MHz) | | | 135 | ns |
| | $\overline{\text{DTGRT}}$ falling edge delay to $\overline{\text{DTACK}}$ falling edge (@10 MHz) | | | 152 | ns |
| t5 | $\overline{\text{DTGRT}}$ low hold time following $\overline{\text{DTACK}}$ falling edge. | 0 | | | ns |
| t6 | $\overline{\text{DTACK}}$ falling edge delay to $\overline{\text{MEMENAOUT}}$ rising edge, $\overline{\text{DTREQ}}$ rising edge, and $\overline{\text{DTACK}}$ rising edge (@20 MHz) | 1.42 | | 2.08 | µs |
| | $\overline{\text{DTACK}}$ falling edge delay to $\overline{\text{MEMENAOUT}}$ rising edge, $\overline{\text{DTREQ}}$ rising edge, and $\overline{\text{DTACK}}$ rising edge (@16 MHz) | 1.78 | | 2.59 | µs |
| | $\overline{\text{DTACK}}$ falling edge delay to $\overline{\text{MEMENAOUT}}$ rising edge, $\overline{\text{DTREQ}}$ rising edge, and $\overline{\text{DTACK}}$ rising edge (@12 MHz) | 2.38 | | 3.45 | µs |
| | $\overline{\text{DTACK}}$ falling edge delay to $\overline{\text{MEMENAOUT}}$ rising edge, $\overline{\text{DTREQ}}$ rising edge, and $\overline{\text{DTACK}}$ rising edge (@10 MHz) | 2.85 | | 4.15 | µs |
| t7 | Status word inputs ($\overline{\text{SSFLAG}}$) valid setup time prior to $\overline{\text{SOM}}$ rising edge. | 40 | | | ns |
| t8 | Status word inputs ($\overline{\text{SSFLAG}}$) valid hold time following $\overline{\text{SOM}}$ rising edge. | 10 | | | ns |

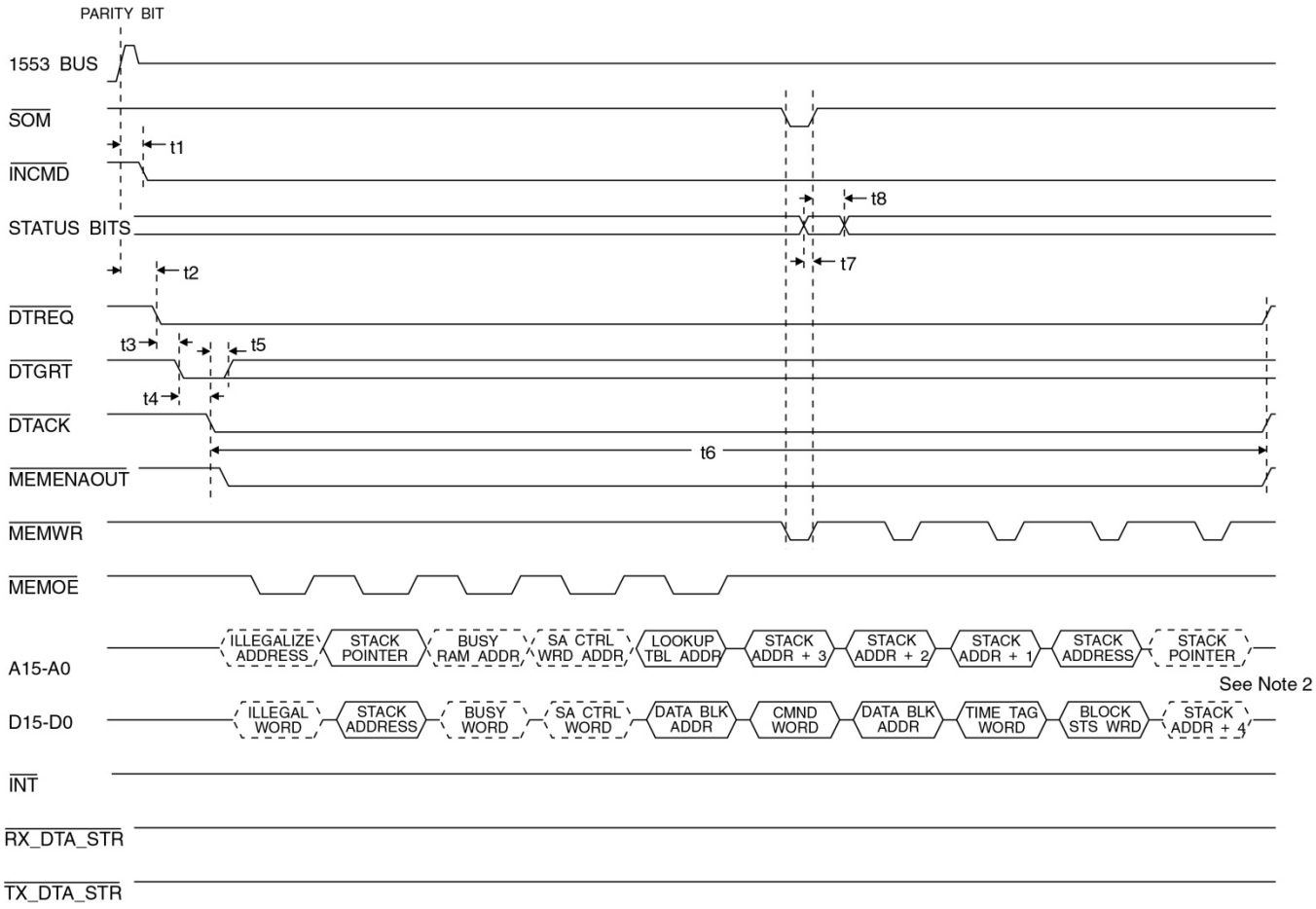



**Figure 59. RT Start of Message (SOM) Timing**

NOTES for Table 30 and Figure 59

1. If maximum allowable request to grant time is exceeded, a handshake fail condition will occur. A handshake fail on the RT Start of Message sequence will cause the Enhanced Mini-ACE to not respond to the current command.
2. The stack pointer is only written during the sum sequence if command stack pointer increment on EOM, bit 13 of configuration register #6, is logic '0.'

**Table 31. RT End of Message Timing**

| REF | DESCRIPTION | Enhanced Mini-ACE | | | UNITS |
|---|---|---|---|---|---|
| | | MIN | TYP | MAX | |
| t1 | Mid-parity crossing of last transmitted word delay to $\overline{\text{DTREQ}}$ falling edge (requesting RT End Of Message transfer sequence). | 2.8 | | 3.2 | µs |
| t2 | $\overline{\text{DTREQ}}$ falling edge delay to $\overline{\text{DTGRT}}$ falling edge (Note 1). | | | | ns |
| t3 | $\overline{\text{DTGRT}}$ falling edge delay to $\overline{\text{DTACK}}$ falling edge (@20 MHz) | | | 102 | ns |
| | $\overline{\text{DTGRT}}$ falling edge delay to $\overline{\text{DTACK}}$ falling edge (@16 MHz) | | | 115 | ns |
| | $\overline{\text{DTGRT}}$ falling edge delay to $\overline{\text{DTACK}}$ falling edge (@12 MHz) | | | 135 | ns |
| | $\overline{\text{DTGRT}}$ falling edge delay to $\overline{\text{DTACK}}$ falling edge (@10 MHz) | | | 152 | ns |
| t4 | $\overline{\text{DTGRT}}$ low hold time following $\overline{\text{DTACK}}$ falling edge. | 0 | | | ns |
| t5 | $\overline{\text{DTACK}}$ falling edge delay to $\overline{\text{MEMENAOUT}}$ rising edge, $\overline{\text{DTREQ}}$ rising edge, and $\overline{\text{DTACK}}$ rising edge (@20 MHz) | 0.43 | | 1.07 | µs |
| | $\overline{\text{DTACK}}$ falling edge delay to $\overline{\text{MEMENAOUT}}$ rising edge, $\overline{\text{DTREQ}}$ rising edge, and $\overline{\text{DTACK}}$ rising edge (@16 MHz) | 0.53 | | 1.34 | µs |
| | $\overline{\text{DTACK}}$ falling edge delay to $\overline{\text{MEMENAOUT}}$ rising edge, $\overline{\text{DTREQ}}$ rising edge, and $\overline{\text{DTACK}}$ rising edge (@12 MHz) | 0.72 | | 1.78 | µs |
| | $\overline{\text{DTACK}}$ falling edge delay to $\overline{\text{MEMENAOUT}}$ rising edge, $\overline{\text{DTREQ}}$ rising edge, and $\overline{\text{DTACK}}$ rising edge (@10 MHz) | 0.96 | | 2.03 | µs |
| t6 | $\overline{\text{INT}}$ falling prior to $\overline{\text{DTACK}}$ rising | | 1 | | clk |
| t7 | $\overline{\text{INT}}$ low pulse width (note 2). | | 500 | | ns |
| t8 | $\overline{\text{MEMENAOUT}}$ rising edge, $\overline{\text{DTREQ}}$ rising edge, and $\overline{\text{DTACK}}$ rising edge delay to INCMD rising edge. | | 2 | | clk |

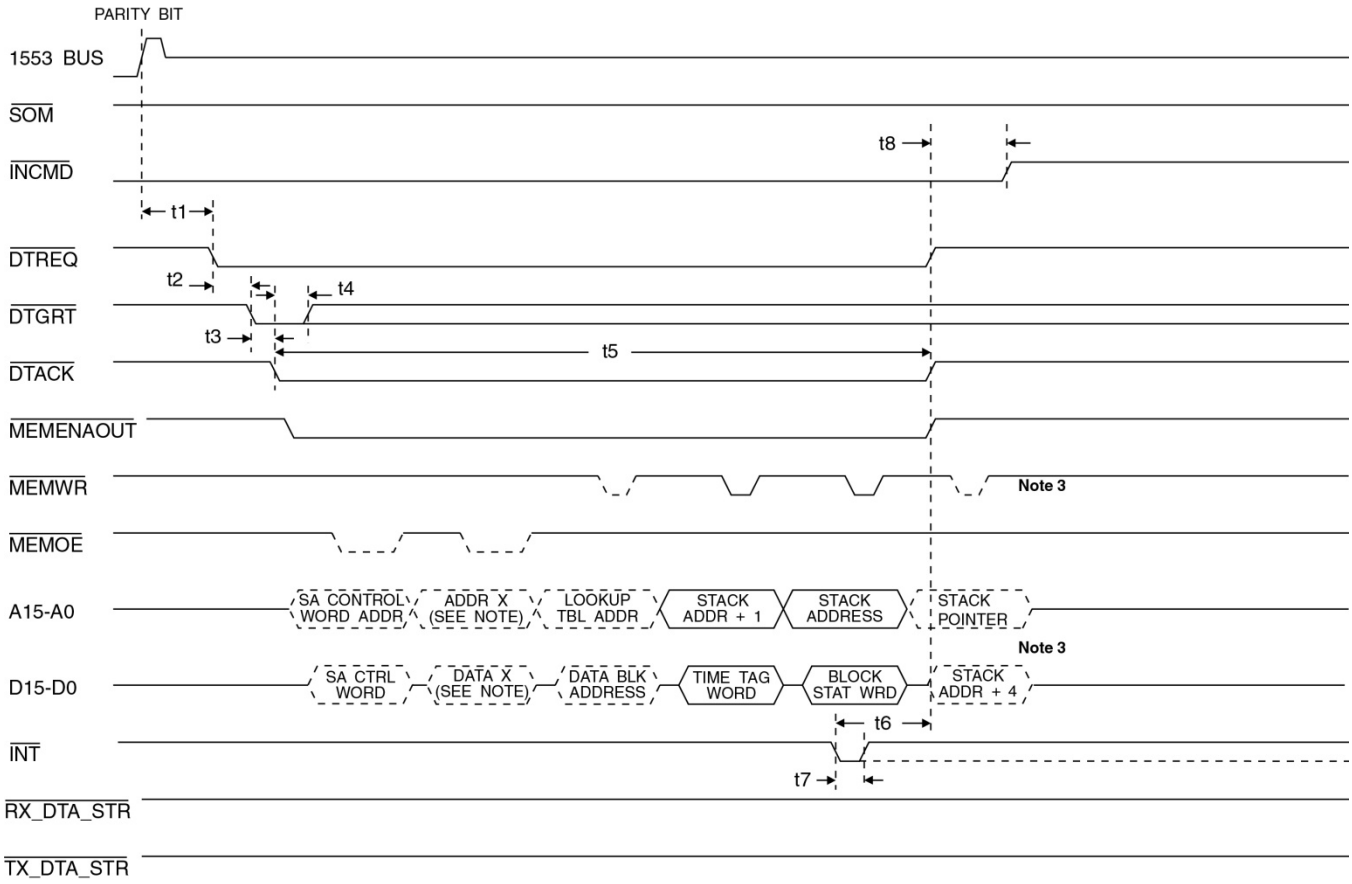



**Figure 60. RT End of Message (EOM) Timing**

NOTES For Table 31 and Figure 60

1. If maximum allowable request to grant time is exceeded, a handshake fail condition will occur. A handshake fail on the RT End of Message sequence will have no effect on 1553 message transfers.
2. Assumes that the interrupt request mode is set to pulse mode (bit 3 of configuration register #2 is set to logic "1").
3. The stack pointer is only written during the EOM sequence if command stack pointer increment on EOM, bit 13 of configuration register #6, is logic '1.'

## 10.6 Message MT Operation

Figure 61 thru Figure 66 illustrate the overall MT message sequence timing for receive, transmit, and broadcast message formats. Figure 63 illustrates the timing sequence for a message in which the command word is not enabled in the Enhanced Mini-ACE's monitor selection lookup table. The Enhanced Mini-ACE will begin a normal Start Of Message, beginning with a read of the monitor lookup table, if the command is not selected in the lookup table, the Enhanced Mini-ACE will abort the SOM sequence. By the time the Enhanced Mini-ACE aborts the sequence, a read of the monitor command stack pointer has begun, so the Enhanced Mini-ACE will finish the read cycle and abort immediately there after.

Figure 65 illustrates the Message Monitor Start Of Message (SOM) sequence. Figure 66 illustrates the Message Monitor End Of Message (EOM) sequence.

**Table 32. Message MT Receive Message Timing**

| REF | DESCRIPTION | Enhanced Mini-ACE | | | UNITS |
|---|---|---|---|---|---|
| | | MIN | TYP | MAX | |
| t1 | Mid-parity crossing of received command word to DTREQ* falling edge (requesting Message MT Start Of Message transfer). | 1.25 | | 2.10 | µs |
| t2 | Mid-parity crossing of received data word to DTREQ* falling edge (requesting data word write transfer). | 1.2 | | 2.0 | µs |
| t3 | RT no response timeout (note 1). | | | 18.5 | µs |
| t4 | Mid-parity crossing of received status word to DTREQ* falling edge (requesting status word write transfer). | 1.2 | | 2.0 | µs |
| t5 | Mid-parity crossing of RT status word to DTREQ* falling edge (requesting Message MT End Of Message transfer). | 6.7 | | 7.4 | µs |

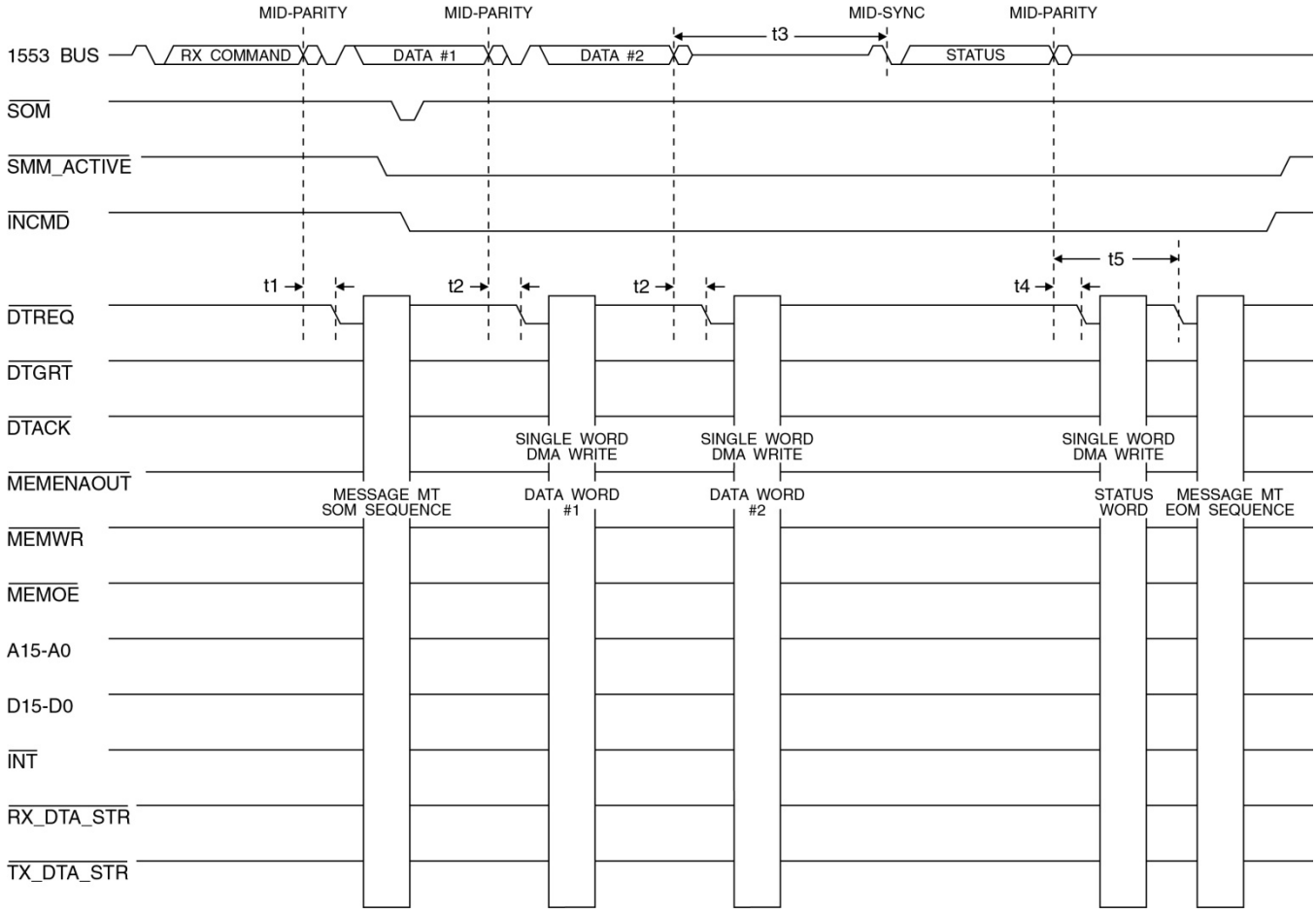



**Figure 61. Message MT Receive Message Timing**

NOTES For Table 32 and Figure 61

1. Response timeout is programmable. Assumes default response timeout value is programmed. If a status response is not received with the response time period, a response timeout condition will be flagged and the Enhanced Mini-ACE will begin looking for new command words.

| Table 33. Message MT Transmit Message Timing | | | | | |
|---|---|---|---|---|---|
| REF | DESCRIPTION | Enhanced Mini-ACE | | | UNITS |
| | | MIN | TYP | MAX | |
| t1 | RT no response timeout (Note 1). | | | 18.5 | µs |
| t2 | Mid-parity crossing of transmit command word to $\overline{\text{DTREQ}}$ falling edge (requesting Message MT Start Of Message transfer). | 1.25 | | 2.10 | µs |
| t3 | Mid-parity crossing of received status word to $\overline{\text{DTREQ}}$ falling edge (requesting status word write transfer). | 1.2 | | 2.0 | µs |
| t4 | Mid-parity crossing of received data word to $\overline{\text{DTREQ}}$ falling edge (requesting data word write transfer). | 1.2 | | 2.0 | µs |
| t5 | Mid-parity crossing of last transmitted data word to $\overline{\text{DTREQ}}$ falling edge (requesting Message MT End Of Message transfer). | 6.7 | | 7.4 | µs |

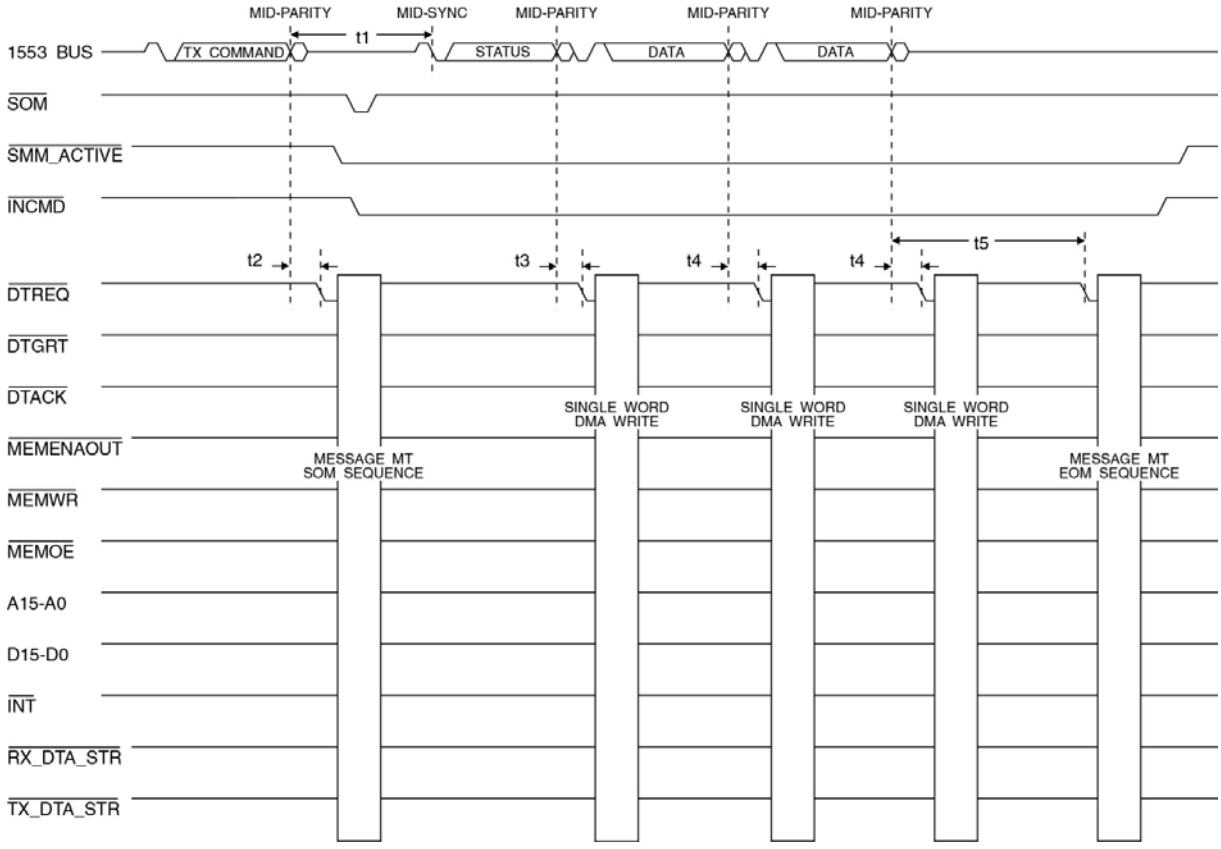



**Figure 62. Message MT Transmit Message Timing**

| Table 34. Message MT Broadcast Receive Message Timing | | | | | |
|---|---|---|---|---|---|
| REF | DESCRIPTION | Enhanced Mini-ACE | | | UNITS |
| | | MIN | TYP | MAX | |
| t1 | Mid-parity crossing of received command word to $\overline{\text{DTREQ}}$ falling edge (requesting Message MT Start Of Message transfer). | 1.25 | | 2.10 | µs |
| t2 | Mid-parity crossing of received data word to $\overline{\text{DTREQ}}$ falling edge (requesting data word write transfer). | 1.2 | | 2.0 | µs |
| t3 | Mid-parity crossing of last data word to $\overline{\text{DTREQ}}$ falling edge (requesting Message MT End Of Message transfer). | 6.7 | | 7.4 | µs |

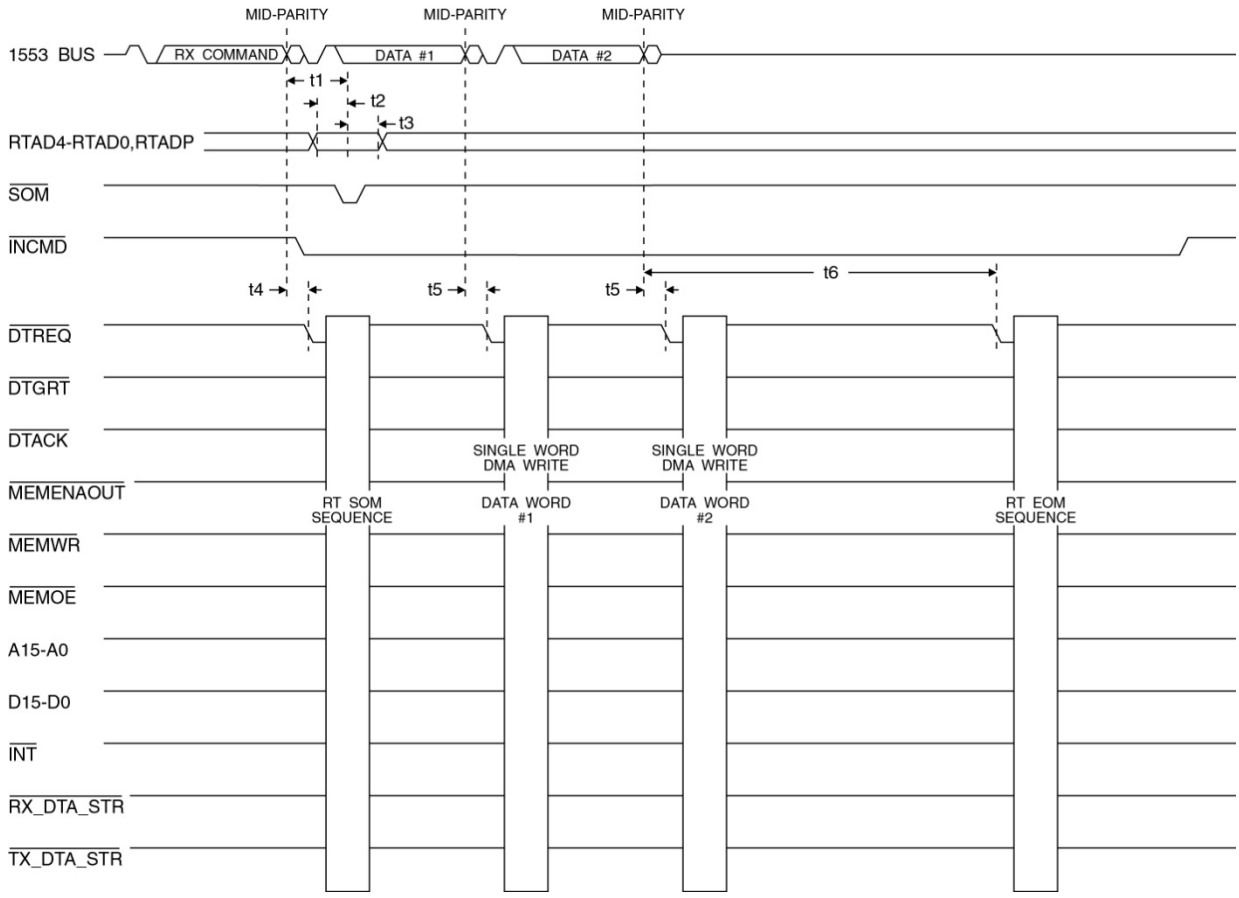


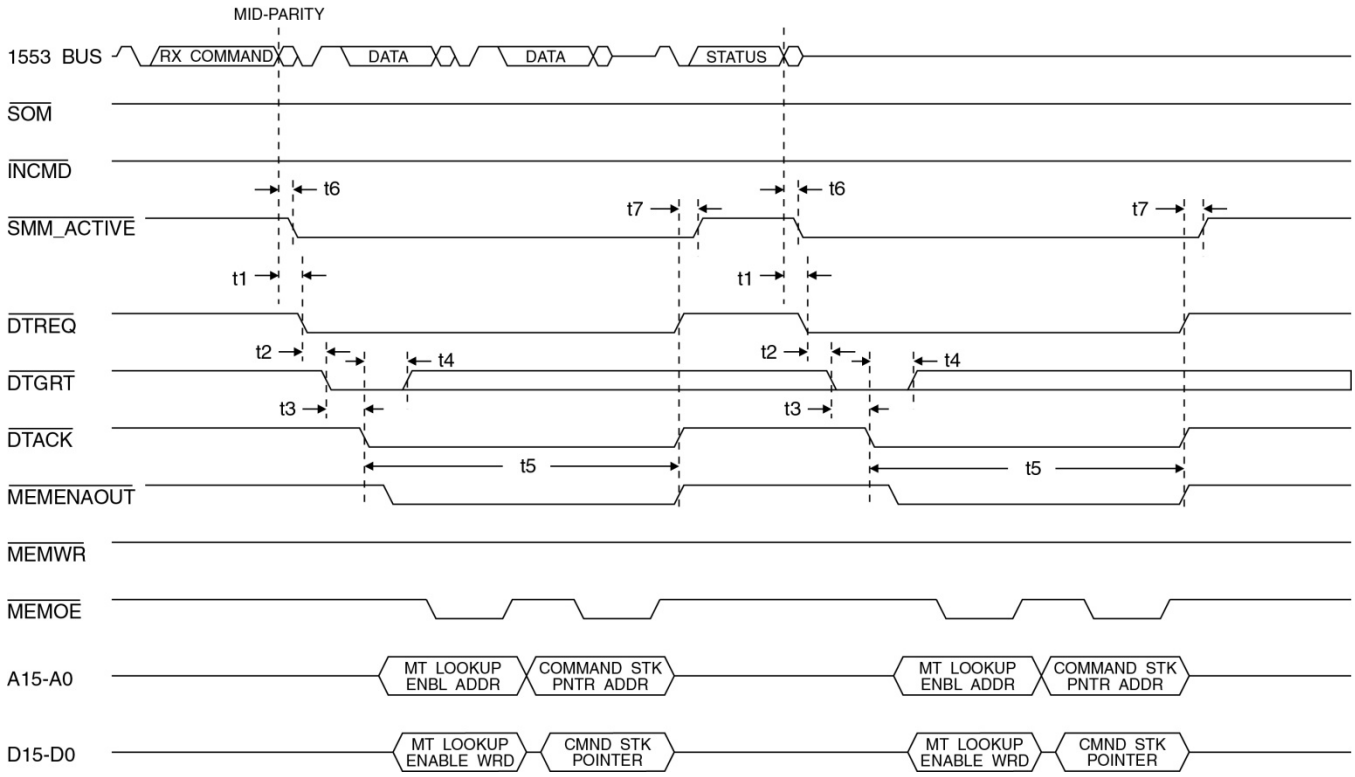

**Figure 63. Message MT Broadcast Receive Message Timing**

Notes for Table 34 and Figure 63

1. Response timeout is programmable. Assumes default response timeout value is programmed. If a status response is not received with the response time period, a response timeout condition will be flagged and the Enhanced Mini-ACE will begin looking for new command words.

| Table 35. Message MT Command Not Selected Timing | | | | | |
|---|---|---|---|---|---|
| REF | DESCRIPTION | Enhanced Mini-ACE | | | UNITS |
| | | MIN | TYP | MAX | |
| t1 | Mid-parity crossing of received command word delay to $\overline{\text{DTREQ}}$ falling edge (requesting Message MT Start Of Message transfer sequence). | 1.25 | | 2.10 | µs |
| t2 | $\overline{\text{DTREQ}}$ falling edge delay to $\overline{\text{DTGRT}}$ falling edge (@20 MHz) (Note 1) | | | 4.5 | µs |
| | $\overline{\text{DTREQ}}$ falling edge delay to $\overline{\text{DTGRT}}$ falling edge (@16 MHz) (Note 1) | | | 4.0 | µs |
| | $\overline{\text{DTREQ}}$ falling edge delay to $\overline{\text{DTGRT}}$ falling edge (@12 MHz) (Note 1) | | | 3.5 | µs |
| | $\overline{\text{DTREQ}}$ falling edge delay to $\overline{\text{DTGRT}}$ falling edge (@10 MHz) (Note 1) | | | 3.1 | µs |
| t3 | $\overline{\text{DTGRT}}$ falling edge delay to $\overline{\text{DTACK}}$ falling edge (@20 MHz) | | | 102 | ns |
| | $\overline{\text{DTGRT}}$ falling edge delay to $\overline{\text{DTACK}}$ falling edge (@16 MHz) | | | 115 | ns |
| | $\overline{\text{DTGRT}}$ falling edge delay to $\overline{\text{DTACK}}$ falling edge (@12 MHz) | | | 135 | ns |
| | $\overline{\text{DTGRT}}$ falling edge delay to $\overline{\text{DTACK}}$ falling edge (@10 MHz) | | | 152 | ns |
| t4 | $\overline{\text{DTGRT}}$ low hold time following $\overline{\text{DTACK}}$ falling edge. | 0 | | | ns |
| t5 | $\overline{\text{DTACK}}$ falling edge delay to $\overline{\text{DTREQ}}$ rising edge, $\overline{\text{DTACK}}$ rising edge, and $\overline{\text{MEMENAOUT}}$ rising edge (@20 MHz) | 0.42 | 0.45 | 0.48 | µs |
| | $\overline{\text{DTACK}}$ falling edge delay to $\overline{\text{DTREQ}}$ rising edge, $\overline{\text{DTACK}}$ rising edge, and $\overline{\text{MEMENAOUT}}$ rising edge (@16 MHz) | 0.53 | 0.56 | 0.59 | µs |
| | $\overline{\text{DTACK}}$ falling edge delay to $\overline{\text{DTREQ}}$ rising edge, $\overline{\text{DTACK}}$ rising edge, and $\overline{\text{MEMENAOUT}}$ rising edge (@12 MHz) | 0.72 | 0.75 | 0.78 | µs |
| | $\overline{\text{DTACK}}$ falling edge delay to $\overline{\text{DTREQ}}$ rising edge, $\overline{\text{DTACK}}$ rising edge, and $\overline{\text{MEMENAOUT}}$ rising edge (@10 MHz) | 0.87 | 0.90 | 0.93 | µs |
| t6 | Mid-parity crossing of receive command word to $\overline{\text{SMM\_ACTIVE}}$ falling edge (@20 MHz) | 0.82 | 1.000 | 1.450 | µs |
| | Mid-parity crossing of receive command word to $\overline{\text{SMM\_ACTIVE}}$ falling edge (@16 MHz) | 1.01 | 1.140 | 1.580 | µs |
| | Mid-parity crossing of receive command word to $\overline{\text{SMM\_ACTIVE}}$ falling edge (@12 MHz) | 1.11 | 1.370 | 1.720 | µs |
| | Mid-parity crossing of receive command word to $\overline{\text{SMM\_ACTIVE}}$ falling edge (@10 MHz) | 1.27 | 1.550 | 1.830 | µs |

| Table 35. Message MT Command Not Selected Timing | | | | | |
|---|---|---|---|---|---|
| REF | DESCRIPTION | Enhanced Mini-ACE | | | UNITS |
| t7 | $\overline{\text{DTACK}}$ rising edge delay to $\overline{\text{SMM\_ACTIVE}}$ rising edge | | 2 | | clk |




## Figure 64. Message MT Command Not Selected Timing

**NOTES For Table 35 and Figure 64**

1. If maximum allowable request to grant time is exceeded, a handshake fail condition will occur. A handshake fail on the MT Start of Message sequence will cause the Enhanced Mini-ACE to ignore the current command.

| Table 36. Message MT Start of Message Timing | | | | | |
|---|---|---|---|---|---|
| REF | DESCRIPTION | Enhanced Mini-ACE | | | UNITS |
| | | MIN | TYP | MAX | |
| t1 | Mid-parity crossing of received command word delay to $\overline{\text{DTREQ}}$ falling edge (requesting Message MT Start Of Message transfer sequence). | 1.25 | | 2.10 | µs |
| t2 | $\overline{\text{DTREQ}}$ falling edge delay to $\overline{\text{DTGRT}}$ falling edge (@20 MHz) (Note 1) | | | 4.5 | µs |
| | $\overline{\text{DTREQ}}$ falling edge delay to $\overline{\text{DTGRT}}$ falling edge (@16 MHz) (Note 1) | | | 4.0 | µs |
| | $\overline{\text{DTREQ}}$ falling edge delay to $\overline{\text{DTGRT}}$ falling edge (@12 MHz) (Note 1) | | | 3.5 | µs |
| | $\overline{\text{DTREQ}}$ falling edge delay to $\overline{\text{DTGRT}}$ falling edge (@10 MHz) (Note 1) | | | 3.1 | µs |
| t3 | $\overline{\text{DTGRT}}$ falling edge delay to $\overline{\text{DTACK}}$ falling edge (@20 MHz) | | | 102 | ns |
| | $\overline{\text{DTGRT}}$ falling edge delay to $\overline{\text{DTACK}}$ falling edge (@16 MHz) | | | 115 | ns |
| | $\overline{\text{DTGRT}}$ falling edge delay to $\overline{\text{DTACK}}$ falling edge (@12 MHz) | | | 135 | ns |
| | $\overline{\text{DTGRT}}$ falling edge delay to $\overline{\text{DTACK}}$ falling edge (@10 MHz) | | | 152 | ns |
| t4 | $\overline{\text{DTGRT}}$ low hold time following $\overline{\text{DTACK}}$ falling edge. | 0 | | | ns |
| t5 | $\overline{\text{DTACK}}$ falling edge delay to $\overline{\text{SOM}}$ falling edge (@20 MHz) | 720 | 750 | 780 | ns |
| | $\overline{\text{DTACK}}$ falling edge delay to $\overline{\text{SOM}}$ falling edge (@16 MHz) | 910 | 940 | 970 | ns |
| | $\overline{\text{DTACK}}$ falling edge delay to $\overline{\text{SOM}}$ falling edge (@12 MHz) | 1220 | 1250 | 1280 | ns |
| | $\overline{\text{DTACK}}$ falling edge delay to $\overline{\text{SOM}}$ falling edge (@10 MHz) | 1470 | 1500 | 1530 | ns |
| t6 | $\overline{\text{SOM}}$ low pulse width (@20 MHz) | 35 | 50 | 65 | ns |
| | $\overline{\text{SOM}}$ low pulse width (@16 MHz) | 45 | 62.5 | 80 | ns |
| | $\overline{\text{SOM}}$ low pulse width (@12 MHz) | 65 | 83.3 | 100 | ns |
| | $\overline{\text{SOM}}$ low pulse width (@10 MHz) | 80 | 100 | 120 | ns |
| t7 | Mid-parity crossing of receive command word to $\overline{\text{SMM\_ACTIVE}}$ falling edge (@20 MHz) | 0.82 | 1.000 | 1.450 | µs |
| | Mid-parity crossing of receive command word to $\overline{\text{SMM\_ACTIVE}}$ falling edge (@16 MHz) | 1.01 | 1.140 | 1.580 | µs |
| | Mid-parity crossing of receive command word to $\overline{\text{SMM\_ACTIVE}}$ falling edge (@12 MHz) | 1.11 | 1.370 | 1.720 | µs |
| | Mid-parity crossing of receive command word to $\overline{\text{SMM\_ACTIVE}}$ falling edge (@10 MHz) | 1.270 | 1.550 | 1.830 | µs |
| t8 | $\overline{\text{DTACK}}$ falling edge delay to $\overline{\text{INCMD}}$ falling edge (@20 MHz) | 370 | 400 | 430 | ns |
| | $\overline{\text{DTACK}}$ falling edge delay to $\overline{\text{INCMD}}$ falling edge (@16 MHz) | 470 | 500 | 530 | ns |
| | $\overline{\text{DTACK}}$ falling edge delay to $\overline{\text{INCMD}}$ falling edge (@12 MHz) | 635 | 666 | 695 | ns |

| Table 36. Message MT Start of Message Timing | | | | | |
|---|---|---|---|---|---|
| REF | DESCRIPTION | Enhanced Mini-ACE | | | UNITS |
| | | MIN | TYP | MAX | |
| | $\overline{\text{DTACK}}$ falling edge delay to $\overline{\text{INCMD}}$ falling edge (@10 MHz) | 770 | 800 | 830 | ns |
| t9 | $\overline{\text{DTACK}}$ falling edge delay to $\overline{\text{DTREQ}}$ rising edge and $\overline{\text{DTACK}}$ rising edge (@20 MHz) | 1.62 | 1.65 | 1.68 | µs |
| | $\overline{\text{DTACK}}$ falling edge delay to $\overline{\text{DTREQ}}$ rising edge and $\overline{\text{DTACK}}$ rising edge (@16 MHz) | 2.03 | 2.06 | 2.09 | µs |
| | $\overline{\text{DTACK}}$ falling edge delay to $\overline{\text{DTREQ}}$ rising edge and $\overline{\text{DTACK}}$ rising edge (@12 MHz) | 2.72 | 2.75 | 2.78 | µs |
| | $\overline{\text{DTACK}}$ falling edge delay to $\overline{\text{DTREQ}}$ rising edge and $\overline{\text{DTACK}}$ rising edge (@10 MHz) | 3.27 | 3.30 | 3.33 | µs |

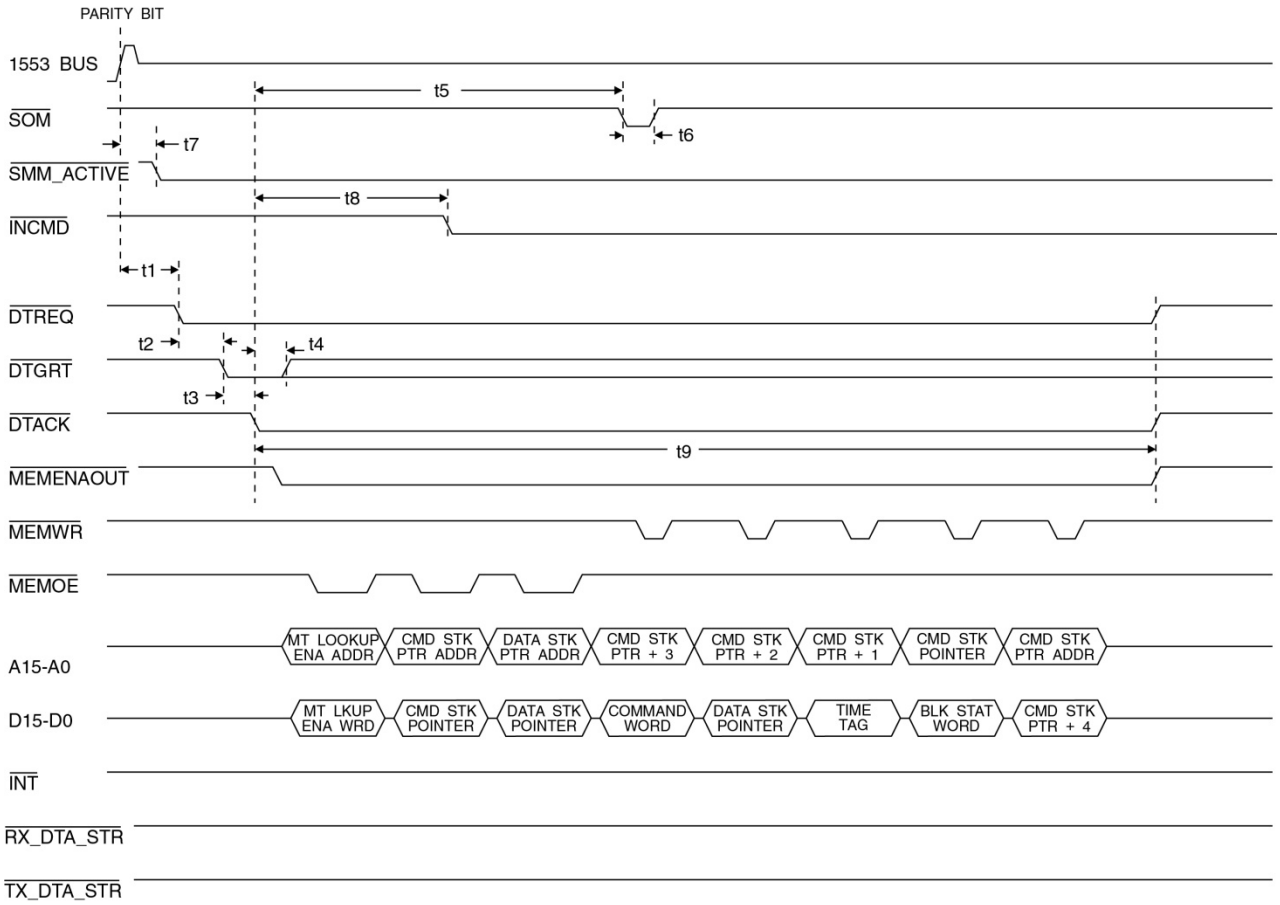
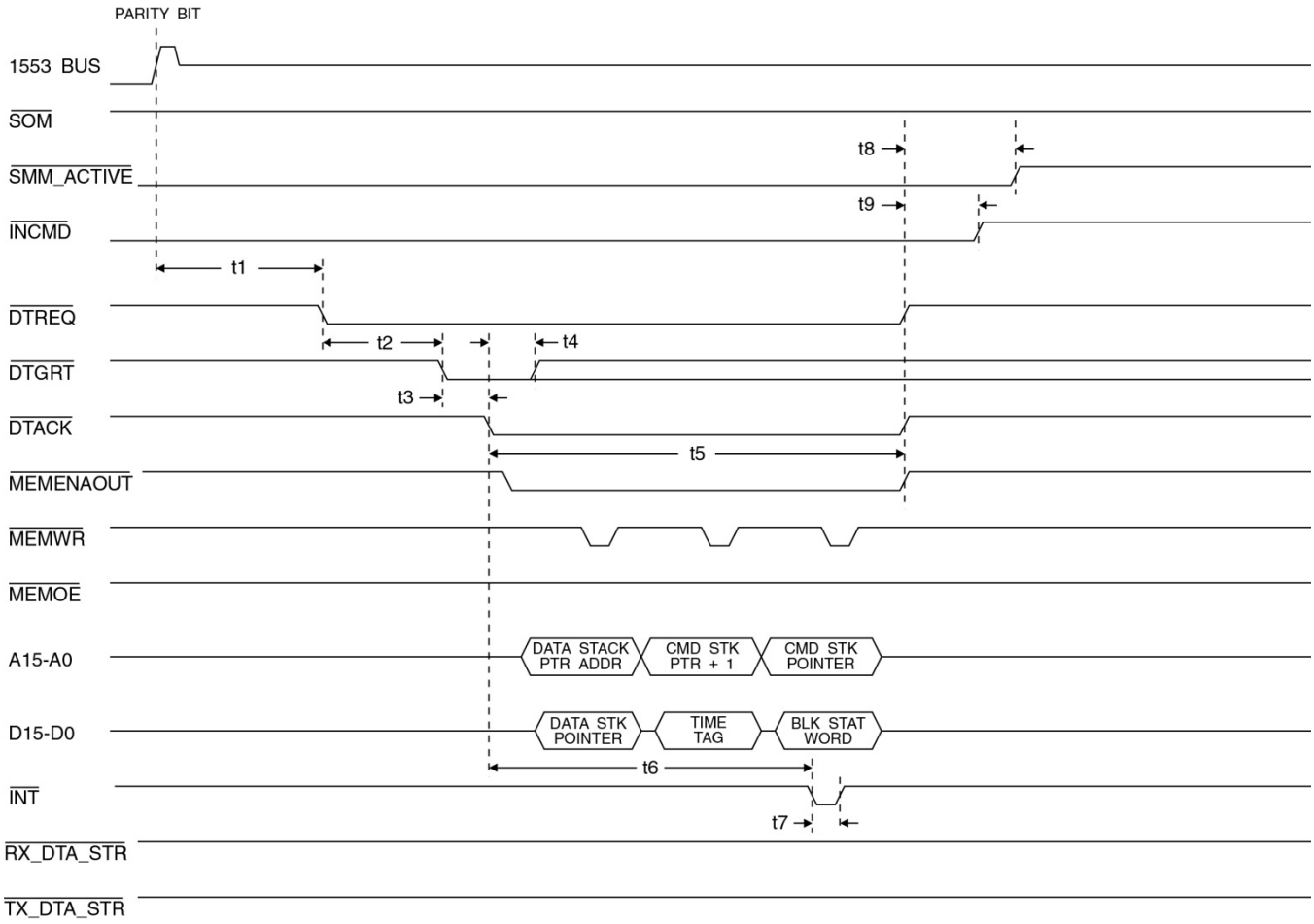



**Figure 65. Message MT Start of Message (SOM) Timing**

NOTES For Table 36 and Figure 65

1. If maximum allowable request to grant time is exceeded, a handshake fail condition will occur. A handshake fail on the MT Start of Message sequence will cause the Enhanced Mini-ACE to ignore the current command.

| Table 37. Message MT End of Message Timing | | | | | |
|---|---|---|---|---|---|
| REF | DESCRIPTION | Enhanced Mini-ACE | | | UNITS |
| | | MIN | TYP | MAX | |
| t1 | Mid-parity crossing of last word in message delay to $\overline{\text{DTREQ}}$ falling edge (requesting Message MT End Of Message transfer sequence). | 6.7 | | 7.4 | **µs** |
| t2 | $\overline{\text{DTREQ}}$ falling edge delay to $\overline{\text{DTGRT}}$ falling edge (Note 1). | | | | ns |
| t3 | $\overline{\text{DTGRT}}$ falling edge delay to $\overline{\text{DTACK}}$ falling edge (@20 MHz) | | | 102 | ns |
| | $\overline{\text{DTGRT}}$ falling edge delay to $\overline{\text{DTACK}}$ falling edge (@16 MHz) | | | 115 | ns |
| | $\overline{\text{DTGRT}}$ falling edge delay to $\overline{\text{DTACK}}$ falling edge (@12 MHz) | | | 135 | ns |
| | $\overline{\text{DTGRT}}$ falling edge delay to $\overline{\text{DTACK}}$ falling edge (@10 MHz) | | | 152 | ns |
| t4 | $\overline{\text{DTGRT}}$ low hold time following $\overline{\text{DTACK}}$ falling edge. | 0 | | | ns |
| t5 | $\overline{\text{DTACK}}$ falling edge delay to $\overline{\text{DTREQ}}$ rising edge, $\overline{\text{DTACK}}$ rising edge, and $\overline{\text{MEMENAOUT}}$ rising edge (@20 MHz) | 0.62 | 0.650 | 0.68 | µs |
| | $\overline{\text{DTACK}}$ falling edge delay to $\overline{\text{DTREQ}}$ rising edge, $\overline{\text{DTACK}}$ rising edge, and $\overline{\text{MEMENAOUT}}$ rising edge (@16 MHz) | 0.78 | 0.812 | 0.84 | µs |
| | $\overline{\text{DTACK}}$ falling edge delay to $\overline{\text{DTREQ}}$ rising edge, $\overline{\text{DTACK}}$ rising edge, and $\overline{\text{MEMENAOUT}}$ rising edge (@12 MHz) | 1.05 | 1.083 | 1.11 | µs |
| | $\overline{\text{DTACK}}$ falling edge delay to $\overline{\text{DTREQ}}$ rising edge, $\overline{\text{DTACK}}$ rising edge, and $\overline{\text{MEMENAOUT}}$ rising edge (@10 MHz) | 1.27 | 1.300 | 1.33 | µs |
| t6 | $\overline{\text{DTACK}}$ falling edge delay to $\overline{\text{INT}}$ falling edge (@20 MHz) | 0.57 | 0.60 | 0.63 | µs |
| | $\overline{\text{DTACK}}$ falling edge delay to $\overline{\text{INT}}$ falling edge (@16 MHz) | 0.72 | 0.75 | 0.78 | µs |
| | $\overline{\text{DTACK}}$ falling edge delay to $\overline{\text{INT}}$ falling edge (@12 MHz) | 0.97 | 1.00 | 1.03 | µs |
| | $\overline{\text{DTACK}}$ falling edge delay to $\overline{\text{INT}}$ falling edge (@10 MHz) | 1.17 | 1.20 | 1.23 | µs |
| t7 | $\overline{\text{INT}}$ active low pulse width (note 2). | | 500 | | ns |
| t8 | $\overline{\text{DTACK}}$ rising edge delay to $\overline{\text{SMM\_ACTIVE}}$ rising edge. | | 3 | | clk |
| t9 | $\overline{\text{DTACK}}$ rising edge delay to $\overline{\text{INCMD}}$ rising edge. | | 2 | | clk |




## Figure 66. Message MT End of Message (EOM) Timing

NOTES For Table 37 and Figure 66

1. If maximum allowable request to grant time is exceeded, a handshake fail condition will occur. A handshake fail on the MT End of Message sequence will cause the Enhanced Mini-ACE to abort processing the message. This message will appear on the communication stack as a message with the SOM bit set in the block status word.
2. Assumes that the interrupt request mode is set to pulse mode (bit 3 of configuration register #2 is set to logic "1").

## 10.7 Word MT Operation

Figure 67 illustrates the start timing for the Word Monitor mode. The word monitor may be started by either a software command (writing a start command to the start/reset register) or by an external trigger input (EXT_TRIG) if the external trigger is enabled (bit 7 of configuration register #1 set to logic 1). Upon either of the start conditions, the Enhanced Mini-ACE will perform a read operation from the stack pointer memory location (100 or 104). Once read, the stack pointer memory location (100 or 104) is not used by the Enhanced Mini-ACE monitor and may be overwritten by either the monitor stack without effecting the operation of the Enhanced Mini-ACE.

Figure 68 illustrates a word monitor received word write cycle. Once started, the Enhanced Mini-ACE Word Monitor will store all 1553 words (command, status, and data) into the RAM. Each 1553 word will be stored with a corresponding tag word.

**Table 38. Word MT Start Timing**

| REF | DESCRIPTION | Enhanced Mini-ACE | | | UNITS |
|---|---|---|---|---|---|
| | | MIN | TYP | MAX | |
| t1 | $\overline{\text{READYD}}$ falling edge (end of CPU MT start write cycle) delay to $\overline{\text{DTREQ}}$ falling edge (requesting MT start sequence) (@20 MHz) | 120 | 150 | 180 | ns |
| | $\overline{\text{READYD}}$ falling edge (end of CPU MT start write cycle) delay to $\overline{\text{DTREQ}}$ falling edge (requesting MT start sequence) (@16 MHz) | 160 | 188 | 220 | ns |
| | $\overline{\text{READYD}}$ falling edge (end of CPU MT start write cycle) delay to $\overline{\text{DTREQ}}$ falling edge (requesting MT start sequence) (@12 MHz) | 220 | 250 | 280 | ns |
| | $\overline{\text{READYD}}$ falling edge (end of CPU MT start write cycle) delay to $\overline{\text{DTREQ}}$ falling edge (requesting MT start sequence) (@10 MHz) | 270 | 300 | 330 | ns |
| t2 | $\overline{\text{EXT\_TRIG}}$ rising edge delay to $\overline{\text{DTREQ}}$ falling edge (requesting MT start sequence) (@20 MHz) (Note 1) | 100 | 170 | 240 | ns |
| | $\overline{\text{EXT\_TRIG}}$ rising edge delay to $\overline{\text{DTREQ}}$ falling edge (requesting MT start sequence) (@16 MHz) (Note 1) | 160 | 210 | 280 | ns |
| | $\overline{\text{EXT\_TRIG}}$ rising edge delay to $\overline{\text{DTREQ}}$ falling edge (requesting MT start sequence) (@12 MHz) (Note 1) | 220 | 290 | 360 | ns |
| | $\overline{\text{EXT\_TRIG}}$ rising edge delay to $\overline{\text{DTREQ}}$ falling edge (requesting MT start sequence) (@10 MHz) (Note 1) | 300 | 370 | 440 | ns |
| t3 | $\overline{\text{DTREQ}}$ falling edge delay to $\overline{\text{DTGRT}}$ falling edge (Note 2) | | | | ns |
| t4 | $\overline{\text{DTGRT}}$ falling edge delay to $\overline{\text{DTACK}}$ falling edge (@20 MHz) | | | 102 | ns |
| | $\overline{\text{DTGRT}}$ falling edge delay to $\overline{\text{DTACK}}$ falling edge (@16 MHz) | | | 115 | ns |

**Table 38. Word MT Start Timing**

| REF | DESCRIPTION | Enhanced Mini-ACE | | | UNITS |
|---|---|---|---|---|---|
| | | MIN | TYP | MAX | |
| | $\overline{\text{DTGRT}}$ falling edge delay to $\overline{\text{DTACK}}$ falling edge (@12 MHz) | | | 135 | ns |
| | $\overline{\text{DTGRT}}$ falling edge delay to $\overline{\text{DTACK}}$ falling edge (@10 MHz) | | | 152 | ns |
| t5 | $\overline{\text{DTGRT}}$ low hold time following $\overline{\text{DTACK}}$ falling edge. | 0 | | | ns |
| t6 | $\overline{\text{DTACK}}$ falling edge delay to $\overline{\text{DTREQ}}$ rising edge, $\overline{\text{DTACK}}$ rising edge, and $\overline{\text{MEMENAOUT}}$ rising edge (@20 MHz) | 220 | 250 | 280 | ns |
| | $\overline{\text{DTACK}}$ falling edge delay to $\overline{\text{DTREQ}}$ rising edge, $\overline{\text{DTACK}}$ rising edge, and $\overline{\text{MEMENAOUT}}$ rising edge (@16 MHz) | 280 | 312 | 340 | ns |
| | $\overline{\text{DTACK}}$ falling edge delay to $\overline{\text{DTREQ}}$ rising edge, $\overline{\text{DTACK}}$ rising edge, and $\overline{\text{MEMENAOUT}}$ rising edge (@12 MHz) | 390 | 417 | 450 | ns |
| | $\overline{\text{DTACK}}$ falling edge delay to $\overline{\text{DTREQ}}$ rising edge, $\overline{\text{DTACK}}$ rising edge, and $\overline{\text{MEMENAOUT}}$ rising edge (@10 MHz) | 470 | 500 | 530 | ns |

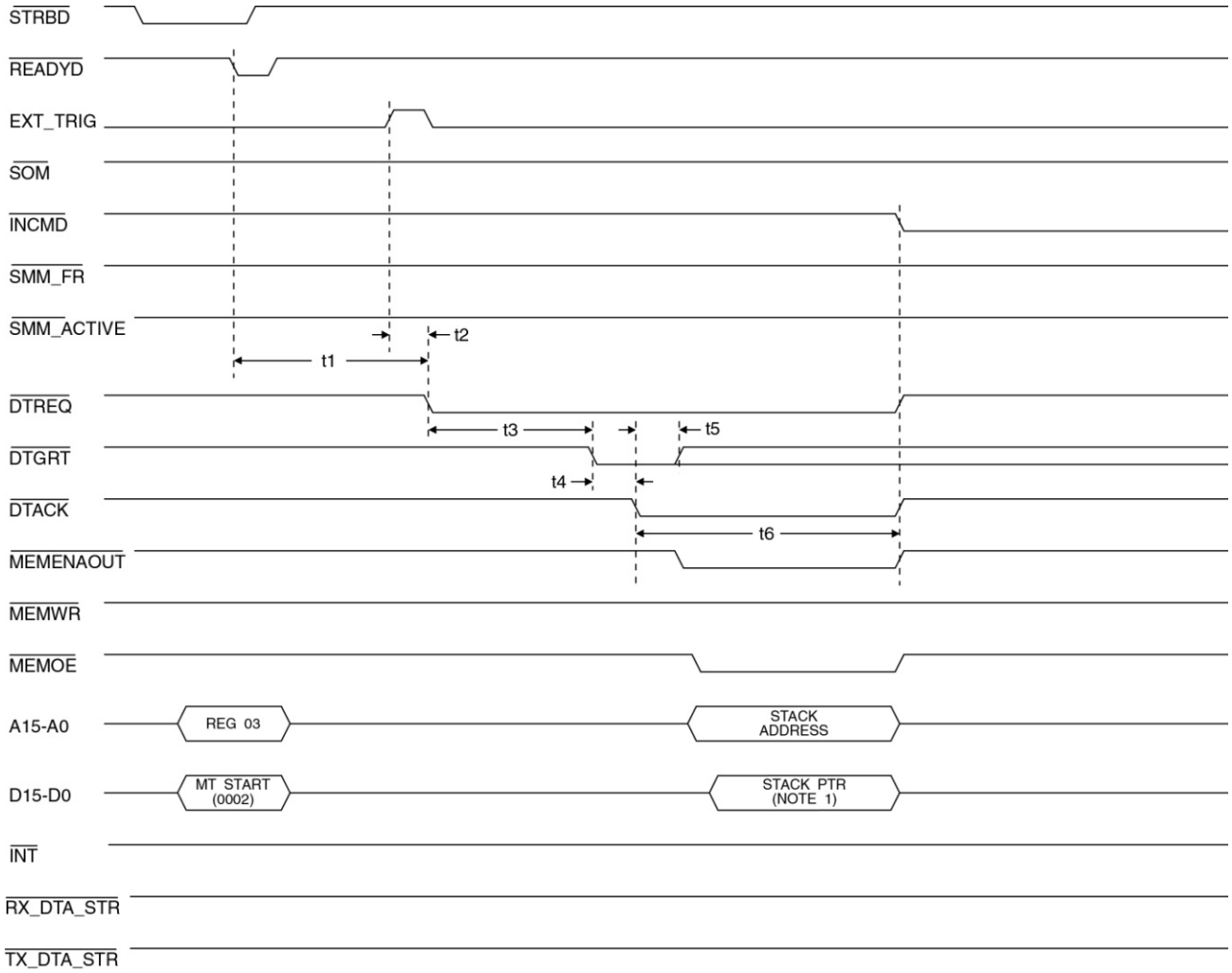



**Figure 67. Word MT Start Timing**

NOTES For Table 38 and Figure 67

1. Assumes that the external trigger is enabled in Configuration Register #1.
2. If maximum allowable request to grant time is exceeded, a handshake fail condition will occur. A handshake fail on the MT start sequence will cause the Enhanced Mini-ACE monitor to not start (i.e., the Enhanced Mini-ACE will remain in the Idle mode).

| Table 39. Word MT Received Word Write Cycle Timing | | | | | |
|---|---|---|---|---|---|
| REF | DESCRIPTION | Enhanced Mini-ACE | | | UNITS |
| | | MIN | TYP | MAX | |
| t1 | Mid-parity crossing of last word in message delay to $\overline{\text{DTREQ}}$ falling edge (requesting received word write cycle) (@ 20 MHz) | 1.04 | 1.32 | 1.60 | µs |
| | Mid-parity crossing of last word in message delay to $\overline{\text{DTREQ}}$ falling edge (requesting received word write cycle) (@16 MHz) | 1.2 | 1.41 | 1.73 | µs |
| | Mid-parity crossing of last word in message delay to $\overline{\text{DTREQ}}$ falling edge (requesting received word write cycle) (@12 MHz) | 1.36 | 1.6 | 1.94 | µs |
| | Mid-parity crossing of last word in message delay to $\overline{\text{DTREQ}}$ falling edge (requesting received word write cycle) (@10 MHz) | 1.45 | 1.75 | 2.1 | µs |
| t2 | $\overline{\text{DTREQ}}$ falling edge delay to $\overline{\text{DTGRT}}$ falling edge (@20 MHz) (Note 1) | | | 4.5 | µs |
| | $\overline{\text{DTREQ}}$ falling edge delay to $\overline{\text{DTGRT}}$ falling edge (@16 MHz) (Note 1) | | | 4.0 | µs |
| | $\overline{\text{DTREQ}}$ falling edge delay to $\overline{\text{DTGRT}}$ falling edge (@12 MHz) (Note 1) | | | 3.5 | µs |
| | $\overline{\text{DTREQ}}$ falling edge delay to $\overline{\text{DTGRT}}$ falling edge (@10 MHz) (Note 1) | | | 3.1 | µs |
| t3 | $\overline{\text{DTGRT}}$ falling edge delay to $\overline{\text{DTACK}}$ falling edge (@20 MHz) | | | 102 | ns |
| | $\overline{\text{DTGRT}}$ falling edge delay to $\overline{\text{DTACK}}$ falling edge (@16 MHz) | | | 115 | ns |
| | $\overline{\text{DTGRT}}$ falling edge delay to $\overline{\text{DTACK}}$ falling edge (@12 MHz) | | | 135 | ns |
| | $\overline{\text{DTGRT}}$ falling edge delay to $\overline{\text{DTACK}}$ falling edge (@10 MHz) | | | 152 | ns |
| t4 | $\overline{\text{DTGRT}}$ low hold time following $\overline{\text{DTACK}}$ falling edge. | 0 | | | ns |
| t5 | $\overline{\text{DTACK}}$ falling edge delay to $\overline{\text{DTREQ}}$ rising edge, $\overline{\text{DTACK}}$ rising edge, and $\overline{\text{MEMENAOUT}}$ rising edge (@20 MHz) | 0.42 | 0.450 | 0.48 | µs |
| | $\overline{\text{DTACK}}$ falling edge delay to $\overline{\text{DTREQ}}$ rising edge, $\overline{\text{DTACK}}$ rising edge, and $\overline{\text{MEMENAOUT}}$ rising edge (@16 MHz) | 0.53 | 0.560 | 0.59 | µs |
| | $\overline{\text{DTACK}}$ falling edge delay to $\overline{\text{DTREQ}}$ rising edge, $\overline{\text{DTACK}}$ rising edge, and $\overline{\text{MEMENAOUT}}$ rising edge (@12 MHz) | 0.72 | 0.750 | 0.78 | µs |
| | $\overline{\text{DTACK}}$ falling edge delay to $\overline{\text{DTREQ}}$ rising edge, $\overline{\text{DTACK}}$ rising edge, and $\overline{\text{MEMENAOUT}}$ rising edge (@10 MHz) | 0.87 | 0.900 | 0.93 | µs |

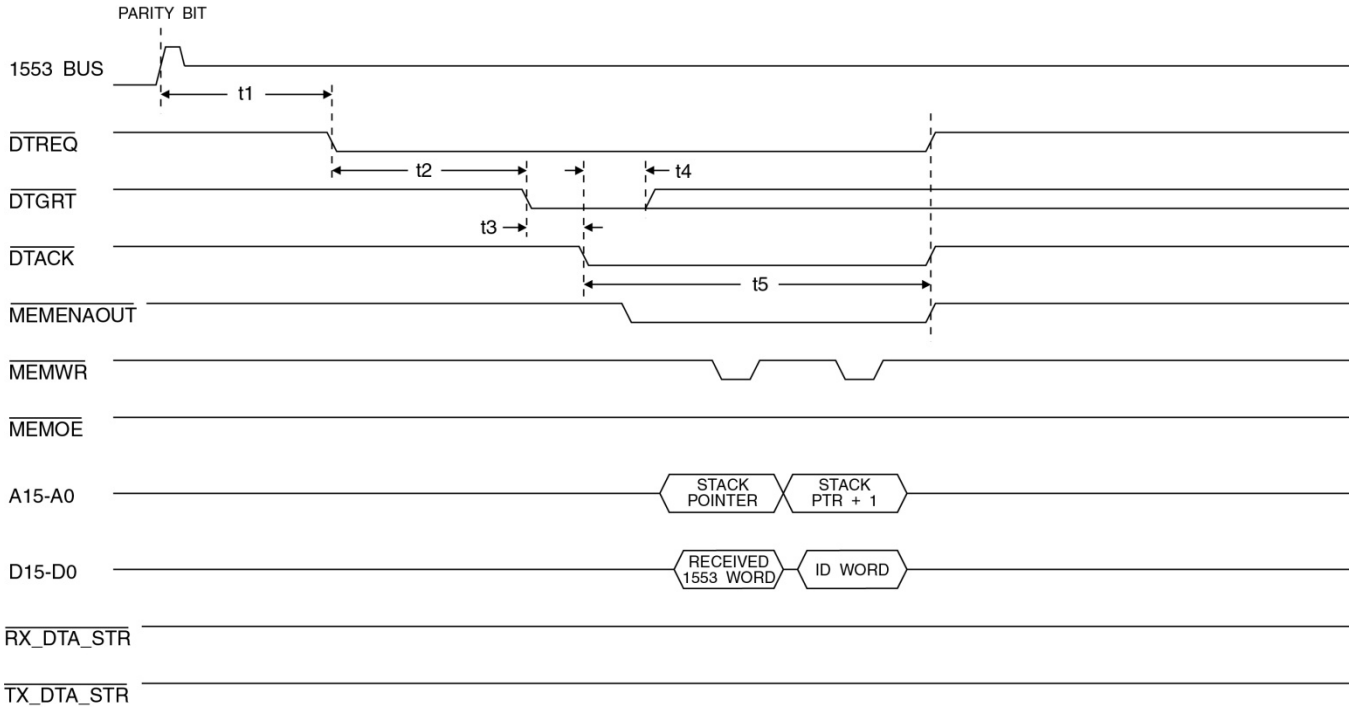



**Figure 68. Word MT Received Word Write Cycle Timing**

NOTES For Table 39 and Figure 68

1. If maximum allowable request to grant time is exceeded, a handshake fail condition will occur. A handshake fail on an MT received word write sequence will cause the Enhanced Mini-ACE monitor to ignore the received word (i.e., the word will be lost).

# 11 APPENDIX A: ISOLATION TRANSFORMERS

## 11.1 ISOLATION TRANSFORMERS FOR USE WITH DDC +5.0 VOLT MIL-STD-1553 TERMINALS

### 11.1.1 INTRODUCTION

Voltage source transmitters, such as those used in DDC's +3.3 volt terminals, are sensitive to transformer parasitic leakage inductance. Transformers with large leakage inductances (in effect, large series inductances) may result in excessively long transmitter rise and fall times which can result in a reduction in output amplitude if the slowdown becomes excessive. The higher the leakage inductance, the greater the problem.

***Note:*** *Isolation Transformer selection is not required for the Total-ACE as Isolation Transformers are an integral part of the Total-ACE plastic BGA component.*

### 11.1.2 DESIGN CONSIDERATIONS

Our voltage source design provides superior line driving capability, especially when driving a healthily loaded bus (i.e., high capacitance). This transceiver has been exhaustively tested and characterized for compliance to our published data sheets as well as to MIL-STD-1553, and has successfully passed the RT Validation Test Plan per MIL-HDBK-1553A, Section 100. In addition, for specific products, DDC has verified that it meets the transmitter amplitude requirement for MIL-STD-1760.

As mentioned, reflected leakage inductance is a parameter that must be considered when selecting isolation transformers to be used with any of these products. For transformer-coupled (stub-coupled) terminals or transceivers, the maximum allowable reflected leakage inductance is 6.0µH and a maximum reflected leakage inductance imbalance must be less than 1.0µH. For direct-coupled (stub-coupled) terminals or transceivers, the maximum allowable reflected leakage inductance is 12.0µH and the maximum reflected leakage inductance imbalance must be less than 2.0µH.

If these limits are exceeded, the transmitter rise and fall times may increase, possibly causing the bus amplitude to fall below the minimum level required by MIL-STD-1553. In addition, an excessive leakage imbalance may result in a dynamic offset (output symmetry) that exceeds 1553 specifications.

### 11.1.3 TEST METHOD

Reflected leakage inductance should be measured as follows: the side of the transformer that connects to the terminal or transceiver hybrid is defined as the

"primary" winding. If one side of the primary is shorted to the primary center-tap, the primary-to-secondary reflected inductance should be measured across the "secondary" (stub-side) winding. This inductance must be less than 6.0 µH for stub-coupled and 12.0 µH for direct coupled. Similarly, if the other side of the primary is shorted to the primary center-tap, the reflected inductance measured across the "secondary" (stub-side) winding must also be less than 6.0 µH for stub-coupled and 12.0 µH for direct coupled. The difference between these two measurements is the "differential" leakage inductance. This value must be less than 1.0 µH for stub-coupled terminals and 2.0 µH for direct-coupled terminals.

### 11.1.4 SUITABLE TRANSFORMERS FROM BETA TRANSFORMER TECHNOLOGY CORPORATION:

Beta Transformer Technology Corporation (BTTC) manufactures transformers in a variety of mechanical configurations with the required turns ratios of 1.0:2.5 direct coupled, and 1.0:1.79 transformer coupled. The table below provides a listing of many of these transformers. Except where noted, all transformers in this table meet the leakage inductance requirements described in this section and therefore may be used with DDC +5.0 Volt terminal products.

For further information, contact BTTC at 631-244-7393 or at www.bttc-beta.com.

**Table 40. BTTC +5.0 Volt Transformers for use with Enhanced Mini-ACE**

| Transformer Configuration | BTTC Part No. |
|---|---|
| Single epoxy transformer, through-hole, 0.625 X 0.625, 0.250" max height | B-3067<br>B-3226 |
| Single epoxy transformer, through-hole with stand-offs, 0.625" X 0.625", 0.275" max height | B-3225 |
| Single epoxy transformer, surface mount, 0.625" X 0.625", 0.275" max height | B-3227 |
| Single epoxy transformer, through-hole, 0.350 X 0.500, 0.250" max height | B-3229<br>B-3230 |
| Single epoxy transformer, flat pack, 0.625" X 0.625", 0.275" max height | B-3231 |
| Single epoxy transformer, through-hole, 0.625" X 0.625", 0.220" max height. | B-3818 (see NOTE 1) |
| Single epoxy transformer, surface mount, 0.625" X 0.625", 0.220" max height | B-3819 (see NOTE 1) |
| Single epoxy transformer, flat pack, 0.625" X 0.625", 0.220" max height | B-3820 (see NOTE 1) |
| Single epoxy transformer, flat pack, 0.625" X 0.625", 0.150" max height | LPB-5014 |
| Single epoxy transformer, surface mount, 0.625" X 0.625", 0.150" max height | LPB-5015 |
| Dual epoxy transformer, twin stacked, through hole, 0.625" X 0.625", 0.320" max height | TST-9107 |
| Dual epoxy transformer, twin stacked, surface mount, 0.625" X 0.625", 0.320" max height | TST-9117 |

| Table 40. BTTC +5.0 Volt Transformers for use with Enhanced Mini-ACE | |
|---|---|
| **Transformer Configuration** | **BTTC Part No.** |
| Dual epoxy transformer, twin stacked, flat pack, 0.625” X 0.625”, 0.320” max height | TST-9127 |
| Dual epoxy transformer, twin stacked, through hole, 0.625” X 0.625”, 0.280” max height | TST-9007 |
| Dual epoxy transformer, twin stacked, surface mount, 0.625” X 0.625”, 0.280” max height | TST-9017 |
| Dual epoxy transformer, twin stacked, flat pack, 0.625” X 0.625”, 0.280” max height | TST-9027 |
| Dual epoxy transformer, side-by-side, through-hole, 0.930” X 0.630”, 0.155” max height. | TLP-1205/B-3300 |
| Dual epoxy transformer, side-by-side, flat pack, 0.930” X 0.630”, 0.155” max height. | TLP-1105/B-3261 |
| Dual epoxy transformer, side-by-side, surface mount, 0.930” X 0.630”, 0.155” max height. | TLP-1005/B-3310 |
| Single epoxy transformer, flat pack, 0.750” X 0.750”, 0.130” max height | SLP-8124 (see NOTE 2) |
| Single epoxy transformer, surface mount, 0.750” X 0.750”, 0.130” max height | SLP-8107 (see NOTE 2) |
| Dual epoxy transformer, side-by-side, flat pack, 1.410” X 0.750”, 0.130” max height. | DLP-7114 (see NOTE 2) |
| Dual epoxy transformer, side-by-side, surface mount, 1.410” X 0.750”, 0.130” max height. | DLP-7115 (see NOTE 2) |
| Single nickel-plated kovar transformer, flat pack, 0.630” X 0.630”, 0.175” max height | HLP-6014 |
| Single nickel-plated kovar transformer, surface mount, 0.630” X 0.630”, 0.175” max Height | HLP-6015 |
| Single epoxy transformer, surface mount, 0.400” X 0.400”, 0.185” max height | MLP-2005 (see NOTE 2) |
| Single epoxy transformer, surface mount, 0.400” X 0.400”, 0.185” max height | MLP-2205 (see NOTE 2) |
| Single epoxy transformer, surface mount, 0.400” X 0.400”, 0.260” max height | MMT-3005 |
| Single epoxy transformer, surface mount, 0.400” X 0.400”, 0.260” max height | MMT-3205 |
| NOT RECOMMENDED | DLP-7014<br>DLP-7015<br>SLP-8007<br>SLP-8024 |

NOTES

1. Only the B-3818, B-3819 and B-3820 can be used with McAir-compatible transceivers (i.e., products with a last digit suffix of “4” rather than ”3”). All others, except for the 4 non-recommended transformers (DLP-7014, DLP-7015, SLP-8007, and SLP-8024) can be used with +5.0 Volt MIL-STD-1553 transceivers (i.e., products with a last digit suffix of “3”).
2. Operates to +105° C max. All other transformers operate to +125° C max.

## 11.2 ISOLATION TRANSFORMERS FOR USE WITH DDC +3.3 VOLT MIL-STD-1553 TERMINALS

### 11.2.1 INTRODUCTION

Voltage source transmitters, such as those used in DDC's +3.3 volt terminals, are sensitive to transformer parasitic leakage inductance. Transformers with large leakage inductances (in effect, large series inductances) may result in excessively long transmitter rise and fall times which can result in a reduction in output amplitude if the slowdown becomes excessive. The higher the leakage inductance, the greater the problem.

***Note:*** *Isolation Transformer selection is not required for the Total-ACE as Isolation Transformers are an integral part of the Total-ACE plastic BGA component.*

### 11.2.2 DESIGN CONSIDERATIONS

Our voltage source design provides superior line driving capability, especially when driving a healthily loaded bus (i.e., high capacitance). This transceiver has been exhaustively tested and characterized for compliance to our published data sheets as well as to MIL-STD-1553, and has successfully passed the RT Validation Test Plan per MIL-HDBK-1553A, Section 100. In addition, for specific products, DDC has verified that it meets the transmitter amplitude requirement for MIL-STD-1760.

As mentioned, reflected leakage inductance is a parameter that must be considered when selecting isolation transformers to be used with any of these products. For transformer-coupled (stub-coupled) terminals or transceivers, the maximum allowable reflected leakage inductance is 5.0µH and the maximum reflection leakage inductance imbalance must be less than 1.0µH. For direct-coupled (stub-coupled) terminals or transceivers, the maximum allowable reflected leakage inductance is 10.0µH and the maximum reflected leakage inductance imbalance must be less than 2.0µH.

If these limits are exceeded, the transmitter rise and fall times may increase, possibly causing the bus amplitude to fall below the minimum level required by MIL-STD-1553. In addition, an excessive leakage imbalance may result in a dynamic offset (output symmetry) that exceeds 1553 specifications.

### 11.2.3 TEST METHOD

Reflected leakage inductance should be measured as follows: the side of the transformer that connects to the terminal or transceiver hybrid is defined as the "primary" winding. If one side of the primary is shorted to the primary center-tap, the primary-to-secondary reflected inductance should be measured across the "secondary" (stub-side) winding. This inductance must be less than 5.0 µH for stub-

coupled and 10.0 µH for direct coupled. Similarly, if the other side of the primary is shorted to the primary center-tap, the reflected inductance measured across the "secondary" (stub-side) winding must also be less than 5.0 µH for stub-coupled and 10.0 µH for direct coupled. The difference between these two measurements is the "differential" leakage inductance. This value must be less than 1.0 µH for stub-coupled terminals and 2.0 µH for direct-coupled terminals.

### 11.2.4 SUITABLE TRANSFORMERS FROM BETA TRANSFORMER TECHNOLOGY CORPORATION:

Beta Transformer Technology Corporation (BTTC) manufactures transformers in a variety of mechanical configurations with the required turns ratios of 1.0:3.75 direct coupled, and 1.0:2.7 transformer coupled for the X8/9 transceiver options and 1.0:2.65 direct coupled, and 1.0:2.038 transformer coupled for the XC/D transceiver options. The table below provides a listing of many of these transformers. Except where noted, all transformers in this table meet the leakage inductance requirements described in this section and therefore may be used with DDC +3.3 Volt terminal products.

For further information, contact BTTC at 631-244-7393 or at www.bttc-beta.com.

**Table 41. BTTC +3.3 Volt Transformers for use with Enhanced Mini-ACE X8/9 Transceiver Options**

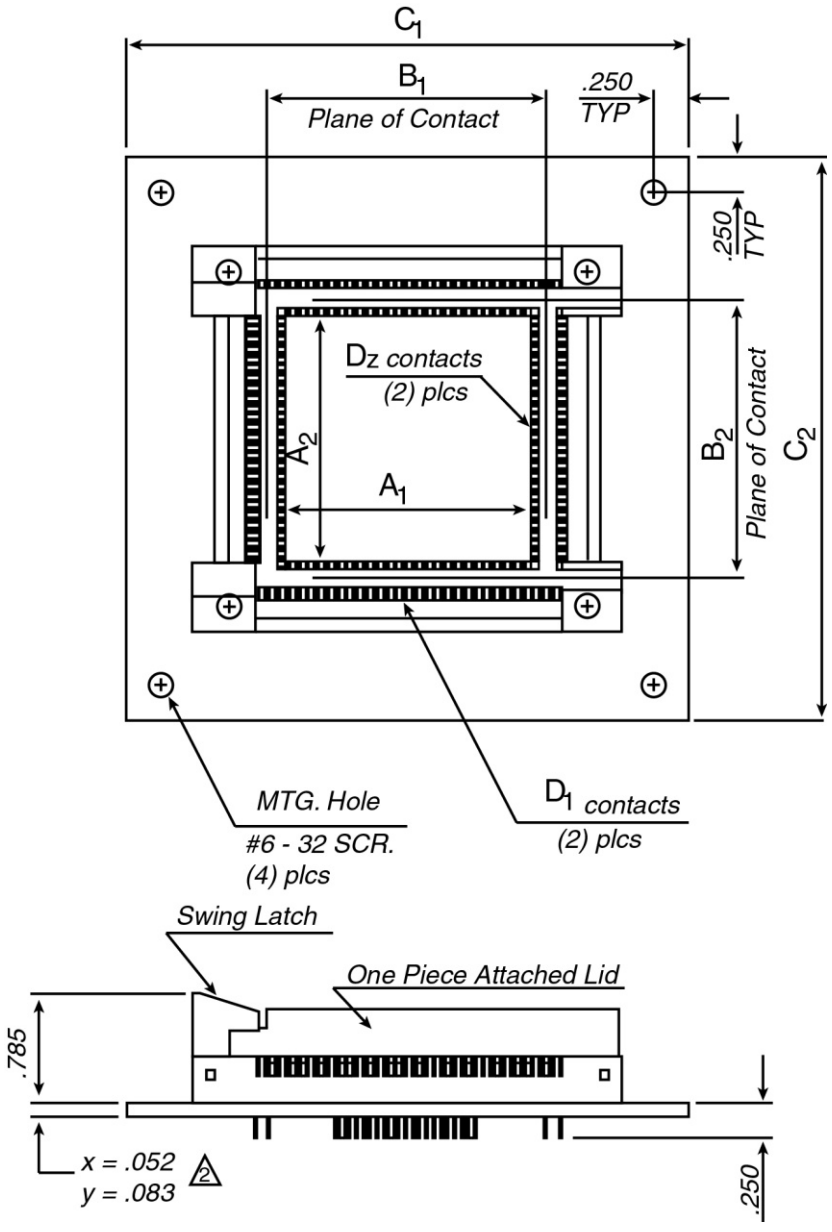
| Transceiver Option | Transformer Configuration | (BTTC Legacy Part No.) | BTTC Part No. |
|---|---|---|---|
| X8/9 | Single epoxy transformer, through-hole, transformer coupled, 0.625 X 0.630, 0.300" max height, +130° C max | (B-3372) | LVB-4203 |
| X8/9 | Single epoxy transformer, through-hole, direct coupled, 0.625" X 0.630", 0.300" max height, +130° C max | (B-3383) | LVB-4103 |
| X8/9 | Single epoxy transformer, surface mount, 0.625" X 0.625", 0.130" max height, +85° C max | (B-3389) | LVB-4213 |
| X8/9 | Single epoxy transformer, surface mount, direct coupled, 0.625 X 0.625, 0.130" max height, +85° C max | (B-3390) | LVB-4113 |
| X8/9 | Single epoxy transformer, surface mount, transformer coupled, 0.625" X 0.630", 0.300" max height, +130° C max | (B-3391) | LVB-4223 |
| X8/9 | Single epoxy transformer, surface mount, direct coupled 0.625" X 0.630", 0.300" max height, +130° C max | (B-3392) | LVB-4123 |
| X8/9 | Dual epoxy transformer, surface mount, transformer coupled, 0.960" X 0.575", 0.185" max height, +130° C max | - | DLVB-4233 |
| X8/9 | Dual epoxy transformer, surface mount, direct coupled, 0.960" X 0.575", 0.185" max height, +130° C max | - | DLVB-4133 |
| X8/9 | Dual epoxy transformer, surface mount, transformer coupled , 0.960" X 0.575", 0.155" max height, +85° C max | - | DLVB-4213 |
| X8/9 | Dual epoxy transformer, surface mount, direct coupled, 0.960" X 0.575", 0.155" max height, +85° C max | - | DLVB-4113 |

| Table 41. BTTC +3.3 Volt Transformers for use with Enhanced Mini-ACE X8/9 Transceiver Options | | | |
|---|---|---|---|
| **Transceiver Option** | **Transformer Configuration** | **(BTTC Legacy Part No.)** | **BTTC Part No.** |
| XC/D | Single epoxy transformer, surface mount, direct coupled, 0.4” X 0.52”, 0.185” max height. | - | MLP-2030 |
| XC/D | Single epoxy transformer, surface mount, transformer coupled, 0.4” X 0.52”, 0.185” max height. | - | MLP-2230 |
| XC/D | Dual epoxy transformer, surface mount, direct and transformer coupled, 0.52” X 0.675”, 0.185” max height. | - | DSS-3330 |
| XC/D | Dual epoxy transformer, surface mount, transformer coupled, 0.4” X 0.53”, 0.32” max height. | - | TSM-2230 |

NOTES
1. SMT (Surface Mount) body package size (a” x b”) does not include leads.
2. The list of approved transformers for use with +3.3V transceivers is constantly being updated. Please contact Beta Transformer Technology Corporation for the latest transformer configuration information.

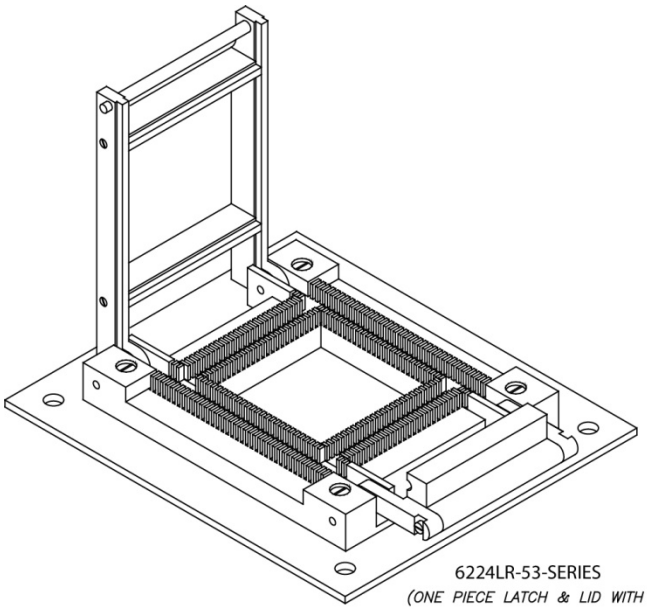
# 12 APPENDIX B: BREADBOARDING SOCKETS

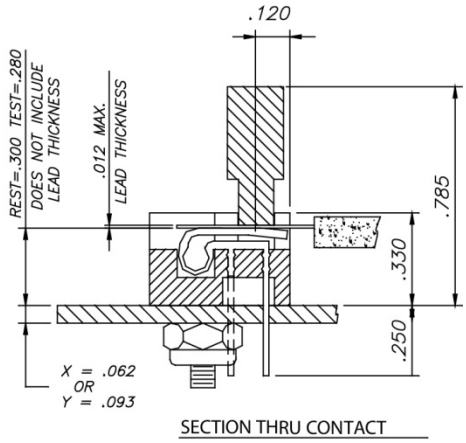
Bread Boarding Sockets
Azimuth Electronics, Inc.
2605 South El Camino Real
San Clemente, CA 92672 USA (949) 492-6481
http://www.azimuth-electronics.com




**Azimuth 72-Lead CQFP Socket Test, Flat Pack, 6224-53-21X**

Azimuth Electronics, Inc.
2605 South El Camino Real
San Clemente, CA 92672 USA (949) 492-6481
http://www.azimuth-electronics.com





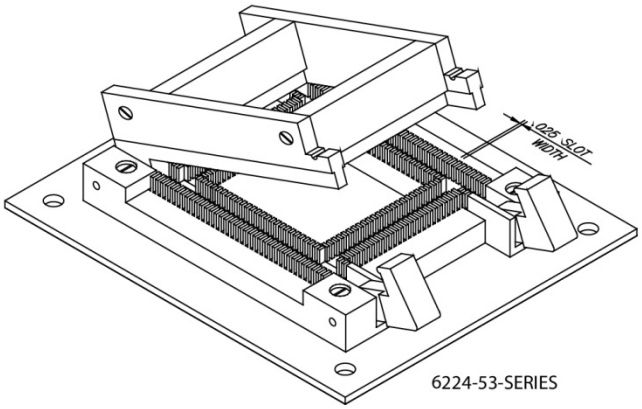

6224LR-53-SERIES
*(ONE PIECE LATCH & LID WITH ROLLER)*

SPECIFICATIONS:

*INSULATOR: PPS (POLYPHENYLENE SULFIDE).*
*CONTACTS: BeCu. SPRING TEMPERED*
*30u GOLD OVER 30u NICKEL.*
*LID & LATCH: PEI (POLYETHERIMIDE)*
*MTG. BOARD: GLASS EPOXY G-10.*
*X = .062 THICK*
*Y = .093 THICK*
*THERMAL RANGE: −65°C/+155°C.*

FEATURES:

*ACCOMMODATES MAX LEAD CROSS SECTION OF .024 WIDE X .012 THICK.*
*FLEXIBLE DESIGN TO ACCOMMODATE DIFFERENT SIZE Q.F.P.'s (QUAD FLAT PACKS).*




6224-53-SERIES

# 13 APPENDIX C: DESC DRAWING PART NUMBERS

**Table 42. Enhanced Mini-ACE BU-61743/61745 RT, and BU-61843/61845/61864/61865 BC/RT/MT DESC Drawing Part Numbers**

| Logic/RAM Voltage | SMD P/N | SMD Suffix | |
|---|---|---|---|
| | | 72-Lead [Flat Pack] | 72-Lead [Gull Wing] |
| +5V | 5962-0151401HMC | | BU-61865G3-110 |
| +5V | 5962-0151401HMC | | BU-61865G3-130 |
| +5V | 5962-0151401HMA | | BU-61865G3-140 |
| +5V | 5962-0151401HMA | | BU-61865G3-150 |
| +5V | 5962-0151401HTC | BU-61865F3-110 | |
| +5V | 5962-0151401HTC | BU-61865F3-130 | |
| +5V | 5962-0151401HTA | BU-61865F3-140 | |
| +5V | 5962-0151401HTA | BU-61865F3-150 | |
| +5V | 5962-0151402HMC | | BU-61865G4-110 |
| +5V | 5962-0151402HMC | | BU-61865G4-130 |
| +5V | 5962-0151402HMA | | BU-61865G4-140 |
| +5V | 5962-0151402HMA | | BU-61865G4-150 |
| +5V | 5962-0151402HTC | BU-61865F4-110 | |
| +5V | 5962-0151402HTC | BU-61865F4-130 | |
| +5V | 5962-0151402HTA | BU-61865F4-140 | |
| +5V | 5962-0151402HTA | BU-61865F4-150 | |
| +3.3V, +5V | 5962-0151403HMC | | BU-61864G3-110 |
| +3.3V, +5V | 5962-0151403HMC | | BU-61864G3-130 |
| +3.3V, +5V | 5962-0151403HMA | | BU-61864G3-140 |
| +3.3V, +5V | 5962-0151403HMA | | BU-61864G3-150 |
| +3.3V, +5V | 5962-0151403HTC | BU-61864F3-110 | |
| +3.3V, +5V | 5962-0151403HTC | BU-61864F3-130 | |
| +3.3V, +5V | 5962-0151403HTA | BU-61864F3-140 | |
| +3.3V, +5V | 5962-0151403HTA | BU-61864F3-150 | |
| +3.3V, +5V | 5962-0151404HMC | | BU-61864G4-110 |
| +3.3V, +5V | 5962-0151404HMC | | BU-61864G4-130 |
| +3.3V, +5V | 5962-0151404HMA | | BU-61864G4-140 |
| +3.3V, +5V | 5962-0151404HMA | | BU-61864G4-150 |
| +5V | 5962-0151404HTC | BU-61745F4-110 | |
| +5V | 5962-0151404HTC | BU-61745F4-130 | |
| +5V | 5962-0151404HTA | BU-61864F4-140 | |

| Table 42. Enhanced Mini-ACE BU-61743/61745 RT, and BU-61843/61845/61864/61865 BC/RT/MT DESC Drawing Part Numbers | | | |
|---|---|---|---|
| **Logic/RAM Voltage** | **SMD P/N** | **SMD Suffix** | |
| | | **72-Lead [Flat Pack]** | **72-Lead [Gull Wing]** |
| +5V | 5962-0151404HTA | BU-61864F4-150 | |
| +5V | 5962-0151405HMC | | BU-61745G3-110 |
| +5V | 5962-0151405HMC | | BU-61745G3-130 |
| +5V | 5962-0151405HMA | | BU-61745G3-140 |
| +5V | 5962-0151405HMA | | BU-61745G3-150 |
| +5V | 5962-0151405HTC | BU-61745F3-110 | |
| +5V | 5962-0151405HTC | BU-61745F3-130 | |
| +5V | 5962-0151405HTA | BU-61745F3-140 | |
| +5V | 5962-0151405HTA | BU-61745F3-150 | |
| +5V | 5962-0151406HMC | | BU-61745G4-110 |
| +5V | 5962-0151406HMC | | BU-61745G4-130 |
| +5V | 5962-0151406HMA | | BU-61745G4-140 |
| +5V | 5962-0151406HMA | | BU-61745G4-150 |
| +5V | 5962-0151406HTC | BU-61745F4-110 | |
| +5V | 5962-0151406HTC | BU-61745F4-130 | |
| +5V | 5962-0151406HTA | BU-61745F4-140 | |
| +5V | 5962-0151406HTA | BU-61745F4-150 | |
| +3.3V | 5962-0151407HMC | | BU-61743G3-110 |
| +3.3V | 5962-0151407HMC | | BU-61743G3-130 |
| +3.3V | 5962-0151407HMA | | BU-61743G3-140 |
| +3.3V | 5962-0151407HMA | | BU-61743G3-150 |
| +3.3V | 5962-0151407HTC | BU-61743F3-110 | |
| +3.3V | 5962-0151407HTC | BU-61743F3-130 | |
| +3.3V | 5962-0151407HTA | BU-61743F3-140 | |
| +3.3V | 5962-0151407HTA | BU-61743F3-150 | |
| +3.3V | 5962-0151408HMC | | BU-61743G4-110 |
| +3.3V | 5962-0151408HMC | | BU-61743G4-130 |
| +3.3V | 5962-0151408HMA | | BU-61743G4-140 |
| +3.3V | 5962-0151408HMA | | BU-61743G4-150 |
| +3.3V | 5962-0151408HTC | BU-61743F4-110 | |
| +3.3V | 5962-0151408HTC | BU-61743F4-130 | |
| +3.3V | 5962-0151408HTA | BU-61743F4-140 | |
| +3.3V | 5962-0151408HTA | BU-61743F4-150 | |

| Table 42. Enhanced Mini-ACE BU-61743/61745 RT, and BU-61843/61845/61864/61865 BC/RT/MT DESC Drawing Part Numbers | | | |
|---|---|---|---|
| **Logic/RAM Voltage** | **SMD P/N** | **SMD Suffix** | |
| | | **72-Lead [Flat Pack]** | **72-Lead [Gull Wing]** |
| +5V | 5962-0151409HMC | | BU-61705G3-110 |
| +5V | 5962-0151409HMC | | BU-61705G3-130 |
| +5V | 5962-0151409HMA | | BU-61705G3-140 |
| +5V | 5962-0151409HMA | | BU-61705G3-150 |
| +5V | 5962-0151409HTC | BU-61705F3-110 | |
| +5V | 5962-0151409HTC | BU-61705F3-130 | |
| +5V | 5962-0151409HTA | BU-61705F3-140 | |
| +5V | 5962-0151409HTA | BU-61705F3-150 | |
| +5V | 5962-0151410HMC | | BU-61705G4-110 |
| +5V | 5962-0151410HMC | | BU-61705G4-130 |
| +5V | 5962-0151410HMA | | BU-61705G4-140 |
| +5V | 5962-0151410HMA | | BU-61705G4-150 |
| +5V | 5962-0151410HTC | BU-61705F4-110 | |
| +5V | 5962-0151410HTC | BU-61705F4-130 | |
| +5V | 5962-0151410HTA | BU-61705F4-140 | |
| +5V | 5962-0151410HTA | BU-61705F4-150 | |
| +3.3V | 5962-0151411HMC | | BU-61703G3-110 |
| +3.3V | 5962-0151411HMC | | BU-61703G3-130 |
| +3.3V | 5962-0151411HMA | | BU-61703G3-140 |
| +3.3V | 5962-0151411HMA | | BU-61703G3-150 |
| +3.3V | 5962-0151411HTC | BU-61703F3-110 | |
| +3.3V | 5962-0151411HTC | BU-61703F3-130 | |
| +3.3V | 5962-0151411HTA | BU-61703F3-140 | |
| +3.3V | 5962-0151411HTA | BU-61703F3-150 | |
| +3.3V | 5962-0151412HMC | | BU-61703G4-110 |
| +3.3V | 5962-0151412HMC | | BU-61703G4-130 |
| +3.3V | 5962-0151412HMA | | BU-61703G4-140 |
| +3.3V | 5962-0151412HMA | | BU-61703G4-150 |
| +3.3V | 5962-0151412HTC | BU-61703F4-110 | |
| +3.3V | 5962-0151412HTC | BU-61703F4-130 | |
| +3.3V | 5962-0151412HTA | BU-61703F4-140 | |
| +3.3V | 5962-0151412HTA | BU-61703F4-150 | |
| +5V | 5962-0151413HTC | BU-61845F3-110 | |

| Table 42. Enhanced Mini-ACE BU-61743/61745 RT, and BU-61843/61845/61864/61865 BC/RT/MT DESC Drawing Part Numbers | | | |
|---|---|---|---|
| **Logic/RAM Voltage** | **SMD P/N** | **SMD Suffix** | |
| | | **72-Lead [Flat Pack]** | **72-Lead [Gull Wing]** |
| +5V | 5962-0151413HTC | BU-61845F3-130 | |
| +5V | 5962-0151413HTA | BU-61845F3-140 | |
| +5V | 5962-0151413HTA | BU-61845F3-150 | |
| +5V | 5962-0151413HMC | | BU-61845G3-110 |
| +5V | 5962-0151413HMC | | BU-61845G3-130 |
| +5V | 5962-0151413HMA | | BU-61845G3-140 |
| +5V | 5962-0151413HMA | | BU-61845G3-150 |
| +5V | 5962-0151414HTC | BU-61845F4-110 | |
| +5V | 5962-0151414HTC | BU-61845F4-130 | |
| +5V | 5962-0151414HTA | BU-61845F4-140 | |
| +5V | 5962-0151414HTA | BU-61845F4-150 | |
| +5V | 5962-0151414HMC | | BU-61845G4-110 |
| +5V | 5962-0151414HMC | | BU-61845G4-130 |
| +5V | 5962-0151414HMA | | BU-61845G4-140 |
| +5V | 5962-0151414HMA | | BU-61845G4-150 |
| +3.3V | 5962-0151415HTC | BU-61843F3-110 | |
| +3.3V | 5962-0151415HTC | BU-61843F3-130 | |
| +3.3V | 5962-0151415HTA | BU-61843F3-140 | |
| +3.3V | 5962-0151415HTA | BU-61843F3-150 | |
| +3.3V | 5962-0151415HMC | | BU-61843G3-110 |
| +3.3V | 5962-0151415HMC | | BU-61843G3-130 |
| +3.3V | 5962-0151415HMA | | BU-61843G3-140 |
| +3.3V | 5962-0151415HMA | | BU-61843G3-150 |
| +3.3V | 5962-0151416HTC | BU-61843F4-110 | |
| +3.3V | 5962-0151416HTC | BU-61843F4-130 | |
| +3.3V | 5962-0151416HTA | BU-61843F4-140 | |
| +3.3V | 5962-0151416HTA | BU-61843F4-150 | |
| +3.3V | 5962-0151416HMC | | BU-61843G4-110 |
| +3.3V | 5962-0151416HMC | | BU-61843G4-130 |
| +3.3V | 5962-0151416HMA | | BU-61843G4-140 |
| +3.3V | 5962-0151416HMA | | BU-61843G4-150 |

# 14 APPENDIX D : ISSUE INVOLVING USE OF EXECUTE AND FLIP “XGF ” BC INSTRUCTION

This information pertains only to devices operating in enhanced BC mode. It does not affect devices operating as an RT, combined RT/Monitor, Monitor, or the non-enhanced BC mode, and does not affect units operating in the transparent interface configuration (this interface configuration is **Not Applicable** to PCI Enhanced Mini-ACE). The problem will only occur in a very limited set of applications even on devices operating in Enhanced BC Mode. Errors caused by this issue are very rare and can only occur if all of a series of configurations and conditions are in effect.

The error that can occur is:

- The possibility of momentarily reading erroneous data from Enhanced Mini-ACE registers under a very limited set of circumstances. The data is only momentarily corrupted.

This error is applicable to the following products:

- BU-61743/5, BU-61843/5 and BU-61864/5 Enhanced Mini-ACE terminals
- BU-61740, BU-61840 and BU-61860 Micro-ACE
- BU-64743, BU-64843 and BU-64863 Mini-ACE Mark3
- BU-6474x, BU-6484X, BU-6486X Micro-ACE-TE
- BU-64843T Total-ACE
- BU-62743, BU-62843 and BU-62864 PCI Enhanced Mini-ACE
- BU-65743, BU-65843 and BU-65863 PCI Mini-ACE Mark3
- BU-6584X, BU-6586X PCI Micro-ACE-TE

This error can only occur if **ALL** of the following configurations and conditions are in effect:

- The 1553 terminal is in BC mode, with enhanced BC mode enabled; i.e., bit 15 of Configuration Register #7 = ‘1’.

  AND

- The Enhanced Mini-ACE is in its buffered processor interface configuration (this interface configuration is **Not Applicable** to PCI Enhanced Mini-ACE).

  AND

- ENHANCED CPU ACCESS is enabled; (i.e., bit 14 of Config Register #7 = '1'). Note that on Enhanced Mini-ACE & Micro-ACE the default condition is **disabled** and for PCI Enhanced Mini-ACE the default is **enabled.**

  AND

- The host CPU is performing a register read operation during a particular four-clock cycle time window near the end of the BC EOM (end-of-message) sequence. Register write operations, as well as memory read and write operations, are **not** affected.

  AND

- The Enhanced BC Controller performs an XQF (Execute and Flip) operation, **and** a "flip" of the instruction's parameter word, which is the pointer to the message's control/status block, occurs as a result of the executed message.

If and only if **ALL** these conditions/events occur simultaneously, then it is possible to momentarily read erroneous data from the Enhanced Mini-ACE registers.

The issue described in the following paragraph comes into play only if the host performs a register read access during a particular four-clock cycle time window near the end of the BC EOM (end-of-message) sequence. The specific time window is four clock cycles wide, and occurs just prior to the BC's internal write transfer to update the value of the XQF instruction's parameter field in the BC instruction list. This write operation, which occurs only for an XQF instruction in which a "flip" occurs, is the last word transfer of the BC EOM sequence.

Under the circumstances described above, a corrupted register read operation can occur. For an affected register read operation, the data read by the host processor will be equal to the *correct value of the register being read **OR'd** with the value of the updated control/status block pointer*.

Note that this erroneous register read access is only a temporary condition. That is, the actual value of the register is **not** affected, and that in general, for subsequent register read accesses, correct values will be read. Also, note that the operation of the XQF instruction, including processing of the specified 1553 message and the updating of the value of the instruction parameter, is **not** affected. In addition, no memory locations are corrupted as the result of this problem.

Also note that if the host reads a register (e.g., Interrupt Status Register #1 or #2) *immediately* following the occurrence of an interrupt request resulting from the end of a BC message, that the problem will **not** occur. If INTERRUPT STATUS AUTO-

CLEAR is enabled (bit 4 of Configuration Register #2 = '1'), the value of the Interrupt Status Register #1 or #2 **will** clear (internally) to '0000' following a corrupted read access of the interrupt status registers.

**There are several possible workarounds to this problem:**

1. Disable the ENHANCED CPU ACCESS feature; i.e., program bit 14 of Configuration Register #7 to logic '0'. As a compromise to minimize overall access time, disable this feature only during register read accesses. Note that for the Enhanced Mini-ACE, the power-up default condition for ENHANCED CPU ACCESS is **disabled**.
2. Eliminate use of the BC XQF (Execute and Flip) instruction. This may be done by emulating its use through other instructions, and possibly host intervention.
3. The host can avoid the complications of having to read the interrupt status registers by making use of the enhanced BC's user-defined interrupts (bits 5-2 of Interrupt Mask Register #2 and Interrupt Status Register #2) and general purpose queue features, and disabling the issuance of interrupts for other conditions defined by the two interrupt mask and status registers.

   Just prior to issuing a user-defined interrupt, the BC should post one or more words to the general purpose queue, using the PTT, PBS, PSI, and/or PSM instructions. Then, the host can issue a user-defined interrupt by means of an IRQ instruction. When an interrupt occurs, it is suggested that the host first clear the interrupt by writing logic '1' to INTERRUPT RESET, bit 2 of the Start/Reset Register, and then proceed to read all previously unread words from the general purpose queue.
4. This last method is only applicable for applications in which Interrupt Status Register #1 and Interrupt Status Register #2 are **not** read. For the case of registers other than the two interrupt status registers, reliable values may be obtained by reading the registers multiple times, until the same value is returned for two consecutive accesses.

   However, for the two interrupt status registers, this method cannot be made to work with 100% reliability. Because of the problem described above, it's not possible to eliminate the possibility of erroneous error indications, missed interrupts, and/or "ghost" interrupts.

# 15 APPENDIX E : INTENTIONALLY LEFT BLANK

# 16 APPENDIX F : SPECIAL NOTES (FOR DEVICES OPERATING ONLY IN RT AND RT/MONITOR MODE)

This information pertains only to devices that are operating in RT and RT/Monitor mode. Devices operating in either BC or MT (only) modes are not affected. Even on devices operating in RT mode, the errors caused by this issue are very rare and probabilistic in nature, and can only occur if all of a series of configurations and conditions are in effect.

The errors that can occur are:

For some of the products, it is possible for the value of the first data word transmitted by the RT to be equal to the RT status word, rather than the word read from memory. The second and subsequent data words transmitted by the RT will all have the correct values, as read from RAM.

The RT's Service Request status word bit may fail to automatically clear following receipt of a Transmit vector word mode command.

The RT's time tag register may fail to automatically clear following receipt of a Synchronize mode command (without data).

Although these issues are related, the consequences and DDC's recommended workarounds vary according to the product. Consequently Appendix "F" contains two parts describing the issue and the recommended workarounds for each of the specific products affected. As such it is only necessary that you read the section applicable to products you're using.

The remainder of this appendix is divided into two parts.

- Appendix "F" Part 1: Enhanced Mini-ACE
  - Covers the BU-61743/5, BU-61843/5 and BU-61864/5 Enhanced Mini-ACE; BU-61740, BU-61840 and BU-61860 Micro-ACE, all Mini-ACE Mark3, Micro-ACE TE, and Total-ACE products.
- Appendix "F" Part 2: PCI Enhanced Mini-ACE
  - Covers the BU-62743, BU-62843 and BU-62864 PCI Enhanced Mini-ACE, and all PCI Mini-ACE Mark3, PCI Micro-ACE TE products.

# APPENDIX "F" Part 1:

**This section applies only to the following products:**

- BU-61743/5, BU-61843/5 and BU-61864/5 Enhances Mini-ACE terminals
- BU-61740, BU-61840 and BU-61860 Micro-ACE
- BU-64743/64745, and BU-64843/64845/64863 Mini-ACE Mark3
- BU-64743B/64840B/64860B/64863B Micro-ACE-TE
- BU-64843T Total-ACE

The issues described in this appendix affect only devices that are operating in RT and RT/Monitor modes. Devices operating in either BC or Monitor (only) modes are not affected. Moreover, the errors caused by this issue are very rare and probabilistic in nature.

The first issue affects the first data word transmitted by the RT. An error can only occur if all of the following configurations and conditions are in effect:
The 1553 terminal is operating in RT mode.

**AND**

One or more of specific non-message interrupts are enabled by their respective Interrupt Mask Register bits. The Enhanced Mini-ACE's non-message interrupts that are applicable are TIME TAG ROLLOVER, RT ADDRESS PARITY ERROR, and RAM PARITY ERROR. These interrupts are enabled by bits 6, 7, and 14 respectively of Interrupt Mask Register #1.

**AND**

The interrupt status queue is enabled (i.e., bit 6 of Configuration Register #6 is set to a logic "1").

**AND**

The RT receives a non-mode code transmit command, or mode code transmit command involving a memory read operation for the transmitted data word. Receive commands to the RT are not affected.

**AND**

The internal write transfer to the interrupt status queue resulting from a non-message interrupt begins on a particular single clock cycle relative to the first data word read cycle; i.e., the read transfer from shared RAM and ensuing write to the internal manchester encoder register.

If and only if all of these conditions/events occur simultaneously, then it is possible for the value of the first data word transmitted by the RT to be equal to the RT status word, rather than the word read from memory. The second and subsequent data words transmitted by the RT will all have the correct values, as read from memory.

Note that given the conditions above, occurrences of this error condition will be probabilistic in nature, with a mean time between occurrences that's a function of clock input frequency, time tag counter resolution, and the rate of transmit messages processed. The mean time between errors is given by the following equation:

$$T_{ERR} = \frac{65{,}536 \bullet f_{CLK} \bullet R}{N}$$ , where:

$T_{ERR}$ = average time between errors, in seconds

$f_{CLK}$ = input clock frequency, in Megahertz

R = time tag resolution, in µS/LSB

N = number of *transmit* messages per second processed by the RT

For example, for an input clock frequency of 16 MHz, and a programmed time tag resolution of 64 µS/LSB, this error will occur once in every $2^{26}$ = 67,108,864 transmit messages. For an RT responding to 100 transmit messages per second, this equates to (on average) one error every 671,089 seconds, or one error every 186 hours (7.8 days).

In addition to TIME TAG ROLLOVER, the other non-message interrupts are RT ADDRESS PARITY ERROR, PROTOCOL SELF-TEST COMPLETE, and RAM PARITY ERROR. A PROTOCOL SELF-TEST COMPLETE interrupt will not result in the error described, since the Enhanced Mini-ACE will not be responding as an RT on the 1553 bus at the time that a protocol self-test completes. The occurrence of an RT ADDRESS PARITY ERROR could theoretically result in the error. However, the occurrence of this interrupt tends to be extremely rare and in any event would point to a significantly more disruptive issue for the RT than a single corrupted data word. The occurrence of a RAM PARITY ERROR at this time would point to a likely error in the data word being read from memory and transmitted on the 1553 bus, regardless of the occurrence or non-occurrence of the issue described above.

As stated, errors will not occur if either the interrupt status queue feature is disabled or non-message interrupts (principally, the TIME TAG ROLLOVER interrupt) are disabled. However, if the interrupt status queue is being used and there's a need to use the TIME TAG ROLLOVER function, we recommend using the ENHANCED INTERRUPTS feature (i.e., set bit 15 of Configuration Register #2 to logic "1"). Then, to completely eliminate the described errors and still make use of the interrupt status queue feature for interrupt events other than TIME TAG ROLLOVER, we recommend that the TIME TAG ROLLOVER interrupt be disabled (set bit 6 of Interrupt Mask Register #1, to logic "0").

In this configuration, the user can then poll the value of TIME TAG ROLLOVER bit 6 of Interrupt Status Register #1 to monitor time tag rollovers. This must be done sufficiently often such that the polling periodicity is less than the period between time tag rollover events to ensure that no time tag rollovers are missed.

There are two other issues that can affect the RT's internal operation following receipt of two specific mode code messages: Synchronize (without data) and Transmit vector word. This error will only occur if all of the following configurations and conditions are in effect:

- The 1553 terminal is operating in RT mode.

**AND**

- One or more of specific non-message interrupts are enabled by the respective Interrupt Mask Register bit. The Enhanced Mini-ACE's non-message interrupts that are applicable are TIME TAG ROLLOVER, RT ADDRESS PARITY ERROR, or RAM PARITY ERROR. These interrupts are enabled by bits 6, 7, and 14 respectively of Interrupt Mask Register #1.

**AND**

- The interrupt status queue is enabled (i.e., bit 6 of Configuration Register #6 is logic "1").

**AND**

- For the case of a Transmit vector word mode command, CLEAR SERVICE REQUEST, bit 2 of Configuration Register #2, is programmed to logic "1". For the case of a Synchronize (without data) mode command, CLEAR TIME TAG ON SYNCHRONIZE, bit 6 of Configuration Register #2, is logic"1".

**AND**

- The RT receives a Transmit vector word mode command (with CLEAR SERVICE REQUEST = logic “1”) or Synchronize (without data) mode command (with CLEAR TIME TAG ON SYNCHRONIZE = logic “1”. All other mode code commands are not affected.

**AND**

- The internal write transfer to the interrupt status queue resulting from a non-message interrupt begins within a particular five clock cycle window just prior to the start of the Enhanced Mini-ACE’s RT EOM (end of message) sequence.

If and only if all of these conditions/events occur simultaneously, then it is possible for either of the following errors to occur:

- For the case of a Transmit vector word mode command, the RT’s Service request status word bit will not clear (with CLEAR SERVICE REQUEST = “1”, it normally will clear).
- For the case of a Synchronize (without data) mode command, the RT’s internal time tag counter will not clear to 0000h (with CLEAR TIME TAG ON SYNCHRONIZE = “1”, it normally will clear to 0000h).

Note that given the conditions above, occurrences of these error conditions will be probabilistic in nature, with a mean time between occurrences that’s a function of clock input frequency, time tag counter resolution, and the frequency at which the respective mode code messages are received. The mean time between such errors is given by the following equation:

$$T_{ERR} = \frac{13107.2 \bullet f_{CLK} \bullet R}{N}$$ , where:

$T_{ERR}$ = average time between errors, in seconds

$f_{CLK}$ = input clock frequency, in Megahertz

R = time tag resolution, in µS/LSB

N = the number of Transmit vector word or Synchronize (without data) mode code messages per second received by the RT

For example, for an input clock frequency of 16 MHz, and a programmed time tag resolution of 64 µS/LSB, this error will occur once in every $2^{26}$ = 67,108,864 Transmit vector word or Synchronize (without data) mode code messages. For an RT

responding to 1 Transmit vector word or Synchronize (without data) mode code messages per second, this equates to (on average) one error every 13,421,770 seconds, or one error every 3730 hours (155 days). Note that in either case, the error is highly likely to be corrected following the RT's next reception of a Transmit vector word or Synchronize (without data) mode command.

As stated, errors will not occur if either the interrupt status queue feature is disabled or non-message interrupts (principally, the TIME TAG ROLLOVER interrupt) are disabled. Thus, the recommended workaround for this issue is the same as previously described for the issue where the first data word is equal to the status word.

# APPENDIX "F" Part 2:

**This section applies only to the following products:**

- BU-62743, BU-62843 and BU-62864 PCI Enhanced Mini-ACE
- BU-65743, BU-65843 and BU-65863 PCI-Mini-ACE Mark3
- BU-65843B, BU-65864B, BU-65863B and BU-65864B PCI Micro-ACE-TE

The issues described below affect only RT and RT/Monitor modes. BC and Monitor (only) modes are not affected. Occurrences of the errors relating to this issue are very rare and are probabilistic in nature.

There are two issues that can affect the RT's internal operation following receipt of two specific mode code messages: Synchronize (without data) and Transmit vector word. This error can only occur if all of the following configurations and conditions are in effect:

The 1553 terminal is operating in RT mode.

**AND**

One or more of certain specific non-message interrupts are enabled by the respective Interrupt Mask Register bit. The Enhanced Mini-ACE's non-message interrupts that are applicable are TIME TAG ROLLOVER, RT ADDRESS PARITY ERROR, or RAM PARITY ERROR. These interrupts are enabled by bits 6, 7, and 14 respectively of Interrupt Mask Register #1.

**AND**

The interrupt status queue is enabled (i.e., bit 6 of Configuration Register #6 is logic "1").

**AND**

For the case of a Transmit vector word mode command, CLEAR SERVICE REQUEST, bit 2 of Configuration Register #2, is programmed to logic "1". For the case of a Synchronize (without data) mode command, CLEAR TIME TAG ON SYNCHRONIZE, bit 6 of Configuration Register #2, is logic "1".

**AND**

The RT receives a Transmit vector word mode command (with CLEAR SERVICE REQUEST = logic “1”) or Synchronize (without data) mode command (with CLEAR TIME TAG ON SYNCHRONIZE = logic “1”. All other mode code commands are not affected.

**AND**

The internal write transfer to the interrupt status queue resulting from a non-message interrupt begins within a particular five clock cycle window just prior to the start of the Enhanced Mini-ACE’s RT EOM (end of message) sequence.

If and only if **all** of these conditions/events occur simultaneously, then it is possible for either of the following errors to occur:

For the case of a Transmit vector word mode command, the RT’s Service request status word bit will *not* clear (with CLEAR SERVICE REQUEST = “1”, it normally will clear).

For the case of a Synchronize (without data) mode command, the RT’s internal time tag counter will *not* clear to 0000h (with CLEAR TIME TAG ON SYNCHRONIZE = “1”, it normally will clear to 0000h).

Note that given the conditions above, occurrences of these error conditions will be probabilistic in nature, with a mean time between occurrences that’s a function of clock input frequency, time tag counter resolution, and the frequency at which the respective mode code messages are received. The mean time between such errors is given by the following equation:

$$T_{ERR} = \frac{13107.2 \bullet f_{CLK} \bullet}{R}$$ , where:

$T_{ERR}$ = average time between errors, in seconds

$f_{CLK}$ = input clock frequency, in Megahertz

R = time tag resolution, in µS/LSB

N = the number of Transmit vector word or Synchronize (without data) mode code messages per second received by the RT

For example, for an input clock frequency of 16 MHz, and a programmed time tag resolution of 64 µS/LSB, this error will occur once in every $2^{26}$ = 67,108,864 Transmit vector word or Synchronize (without data) mode code messages. For an RT

responding to 1 Transmit vector word or Synchronize (without data) mode code messages per second, this equates to (on average) one error every 13,421,770 seconds, or one error every 3730 hours (155 days). Note that in either case, the error is *highly likely* to be corrected following the RT's next reception of a Transmit vector word or Synchronize (without data) mode command.

As stated, this problem will **not** occur if ***either*** the interrupt status queues feature or non-message interrupts (principally, the TIME TAG ROLLOVER interrupt) are not used. However, if the interrupt status queue is used and there's a need to use the TIME TAG ROLLOVER function, we recommend using the ENHANCED INTERRUPTS feature (i.e., set bit 15 of Configuration Register #2 to logic "1"). Then, to completely eliminate the probability of encountering the described problems and still make use of the interrupt status queue feature for interrupt events other than TIME TAG ROLLOVER, we recommend that the TIME TAG ROLLOVER interrupt be disabled (set bit 6 of Interrupt Mask Register #1, to logic "0").

In this configuration, time tag rollovers may be monitored by polling the value of TIME TAG ROLLOVER bit 6 of Interrupt Status Register #1, sufficiently often such that the polling periodicity is less than the period between time tag rollover events.

In addition to TIME TAG ROLLOVER, the other non-message interrupts are RT ADDRESS PARITY ERROR, and RAM PARITY ERROR. The occurrence of an RT ADDRESS PARITY ERROR could theoretically result in the problems. However, the occurrence of this interrupt tends to be extremely rare and in any event would point to a significantly more disruptive problem for the RT than the failure of the Service request bit or time tag counter to clear. The occurrence of a RAM PARITY ERROR at this time would point to an error in a word being read from memory by the PCI Enhanced Mini-ACE's host processor. However, occurrences of RAM parity errors are extremely rare.

As stated, errors will **not** occur if ***either*** the interrupt status queue feature is disabled or non-message interrupts (principally, the TIME TAG ROLLOVER interrupt) are disabled. However, if the interrupt status queue is being used and there's a need to use the TIME TAG ROLLOVER function, we recommend using the ENHANCED INTERRUPTS feature (i.e., set bit 15 of Configuration Register #2 to logic "1"). Then, to completely eliminate the described errors and still make use of the interrupt status queue feature for interrupt events other than TIME TAG ROLLOVER, we recommend that the TIME TAG ROLLOVER interrupt be disabled (set bit 6 of Interrupt Mask Register #1, to logic "0").

In this configuration, the user can then poll the value of TIME TAG ROLLOVER bit 6 of Interrupt Status Register #1 to monitor time tag rollovers. This must be done sufficiently often such that the polling periodicity is less than the period between time tag rollover events to ensure that no time tag rollovers are missed.

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