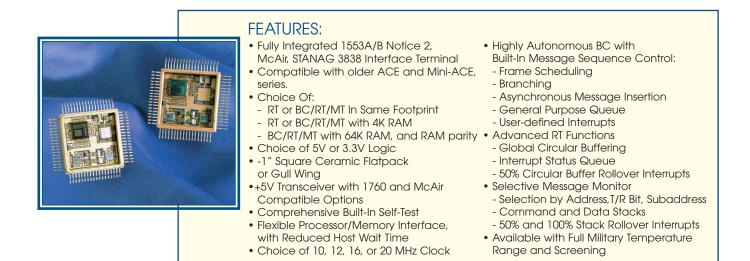


# Enhanced Mini-ACE® 1553 Terminal Model: BU-6174X/6184X/6186X



### DESCRIPTION

The Enhanced Mini-ACE family of MIL-STD-1553 terminals provides complete interfaces between a host processor and 1553 bus, integrating dual transceiver, protocol logic, and 4K or 64K words of RAM.

The terminals offer a choice of 5V or 3.3V logic, and feature multi-protocol support of MIL-STD-1553A/B and STANAG 3838, including versions incorporating McAir compatible transmitters. There is a choice of 10,12,16, or 20 MHz clocks. The BC/RT/MT versions with 64K words of RAM include built-in RAM real-time parity checking.

BC features include a built-in programmable message sequence control engine with a set of 20 instructions. This feature provides an autonomous means of implementing multi-frame message scheduling, message retry schemes, data double buffering, asynchronous message insertion, and reporting to the host CPU.

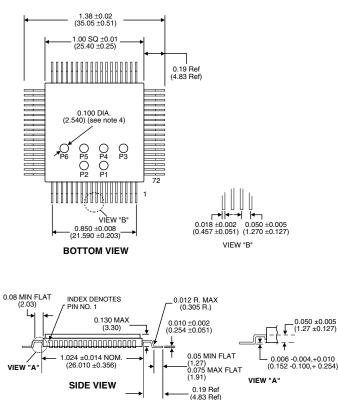
The RT offers the same choices of subaddress buffering as the ACE and Mini-ACE, along with a global circular buffering option, 50% rollover interrupt for circular buffers, an interrupt status queue, and an "Auto-boot" option to support MIL-STD-1760.

The Enhanced Mini-ACE incorporates a fully autonomous built-in self-test engine, providing comprehensive testing of the internal protocol logic and/or RAM.

The terminals provide the same flexibility in host interface configurations as the ACE and Mini-ACE, along with a reduction in the host processor's worst case hold-off time. Most software features are compatible with the previous generations of ACE and Mini-ACE series. Enhanced Mini-ACE architecture is also available in several new package styles, supply voltages and backend interfaces in the Mini-ACE Mark3, Micro-ACE TE series components. (See Separate Product Brief).



## Figure 1. Enhanced Mini-ACE 1553 Terminal Model: BU-6174X/6184X/6186X



Notes:

- 1) Dimensions are in inches(mm)
- 2) Package Material: Alumina(AL<sub>2</sub>0<sub>3</sub>)

3) Lead Material: Kovar, Plated by 50, in. minimum nickel under 60, in. minimum gold. 4) There are 6 test pads located on the bottom of the package. These pads are recessed so as not to interfere when mounting the hybrid. There are no user connections to these pads.

#### Most Autonomous BC Architecture

- Built-in Message Sequence Control Engine
- Defined Set of 20 Instructions
- Control/Status Blocks for Individual Messages
- Minor and Major Frame Scheduling
- Asynchronous Message Insertion
- Conditional Branching and Subroutines
- General Purpose Queue: Message Status, Time Tag, Immediate Data, Indirect Data
- Fully User-definable Interrupts
- Legacy Mode for Compatibility with ACE and **Mini-ACE** Applications

#### **Remote Terminal Flexibility**

- Multiprotocol: MIL-STD-1553A/B, STANAG-3838
- Choice of Subaddress Single Message, Double Buffering, Circular Buffering, or Global Circular Buffering
- 50% and 100% Circular Buffer Rollover Interrupts
- Hardware or Software-Programmable **RT** Address
- Programmable Command Illegalization
- Programmable Busy by Subaddress
- Interrupts on All Messages, or Individual Subaddresses and/or Mode Codes
- 32-Entry Interrupt Status Queue
- Option for RT AUTO-BOOT: Initialize to RT Mode with Busy bit Set Following Power-Up for MIL-STD-1760 Applications.

#### True Message Monitor

- Selective Message Monitor
- Filter Based on RT Address, T/R bit, Subaddress
- Command and Data Stacks
- 50% and 100% Rollover Interrupts
- 32-Entry Interrupt Status Queue
- Simultaneous RT/Message Monitor Option
- Autonomous Built-In Self-Test
- Protocol Self-Test
- RAM Self-Test
- Online Loopback Test
- Capability to Test Transmitter Timeout Function **Processor Interface Flexibility**
- Direct Interface to 8,16, or 32-bit Microprocessor or Microcontrollers
- Supports DMA Interface to External RAM
- Supports 3.3 Volt Logic Interface
- +5 Volt-Tolerant Loaic Sianals
- **Extensive User Configurability**
- Software programmable divider selects master 1553 clock of 10, 12, 16 or 20 MHz

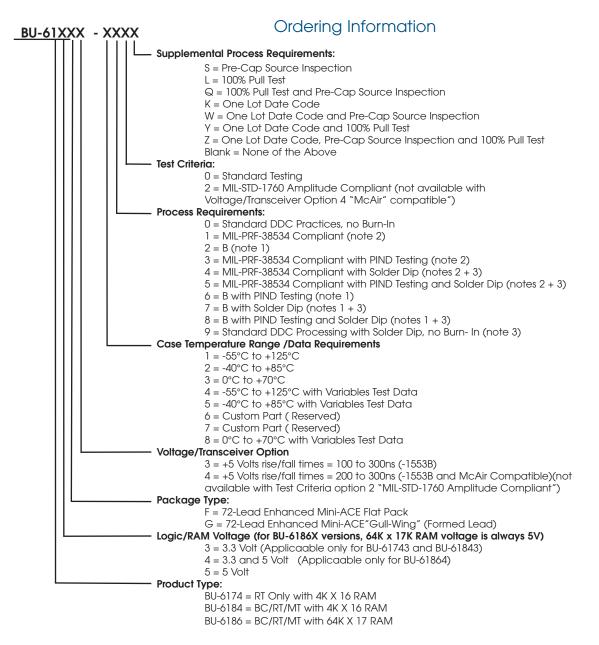
Specifications										
PARAMETER	MIN	TYP	MAX	UNITS	PARAMETER	MIN	TYP	MAX	UNITS	
POWER SUPPLY REQUIREMENTS Voltages/Tolerance +3.3V (Logic) +5.0V Transceiver (Ch. A, Ch. B) +5.0V(Logic),5 V-RAM (64K RAM for 61864/65)	3.0 4.75 4.5	3.3 5.0 5.0	3.6 5.25 5.5	V V V	BU-61745X3/4 & BU-61845X3/4-XX0 0% Transmit/Monitor 25% Duty Transmitter Cycle 50% Duty Transmitter Cycle 75% Duty Transmitter Cycle		0.64 0.93 1.22 1.52	0.88 1.11 1.33 1.65	W W W W	
CURRENT DRAIN (Total Hybrid) BU-61743X3/4-XX0 & BU-61843X3/4-XX0 +5V(Ch. A, Ch. B) 0% Transmit/Monitor 25% Duty Transmitter Cycle		65 169	100 205	mA mA	BU-61864X3/4-XX0 0% Transmit/Monitor 25% Duty Transmitter Cycle 50% Duty Transmitter Cycle 75% Duty Transmitter Cycle		0.44 0.75 1.05 1.36	0.80 1.03 1.26 1.49	W W W W	
50% Duty Transmitter Cycle 75% Duty Transmitter Cycle +3.3V (Logic) BU-61745X3/4-XX0 & BU-61845X3/4-XX0 +5V(Logic, RAM, CH A, CH B)	1	273 377 25	310 415 40	mA mA mA	BU-61865X3/4-XX0 0% Transmit/Monitor 25% Duty Transmitter Cycle 50% Duty Transmitter Cycle 75% Duty Transmitter Cycle		0.64 0.93 1.22 1.51	0.99 1.22 1.45 1.68	W W W W	
0% Transmit/Monitor 25% Duty Transmitter Cycle 50% Duty Transmitter Cycle 75% Duty Transmitter Cycle		116 222 328 434	160 265 370 475	mA mA mA	Hottest Die (Transceiver Chip) 0% Transmit/Monitor 25% Duty Transmitter Cycle 50% Duty Transmitter Cycle 75% Duty Transmitter Cycle		0.18 0.42 0.66 .90	0.28 0.51 0.75 .985	W W W W	
BU-61864X3/4-XX0 +5V (Ch. A, Ch. B) 0% Transmit/Monitor 25% Duty Transmitter Cycle 50% Duty Transmitter Cycle +75% Duty Transmitter Cycle +3.3V (Logic)		66 163 260 357 25	120 225 330 435 40	mA mA mA mA	CLOCK INPUTS Frequency: Nominal Value Default Mode Option Option Option		16.0 12.0 10.0 20.0		MHz MHz MHz MHz	
BU-61865X3/4-XX0 +5V (Logic RAM Ch. A, Ch. B) 0% Transmit/Monitor 25% Duty Transmitter Cycle 50% Duty Transmitter Cycle 75% Duty Transmitter Cycle		116 217 318 419	180 285 390 495	mA mA mA	<b>THERMAL</b> Thermal Resistance, Junction-to-Case, Hottest Die (0jc,) Operating Junction Temperature Storage Temperature	-55 -65	9	11 +150 +150	°C/W °C °C	
POWER DISSIPATION (See Note) Total Hybrid BU-61743X3/4 & BU-61843X3/4-XX0 0% Transmit/Monitorl 25% Duty Transmitter Cycle 50% Duty Transmitter Cycle 75% Duty Transmitter Cycle		0.41 0.70 0.94 1.17	0.63 0.85 1.07 1.29	W W W W	PHYSICAL CHARACTERISTICS Size Ceramic Flat Pack/ Gull Wing Weight		< 1.0 X 0 4 x 25.4 x 0.6 17		in. mm oz. g	

Note: Power dissipation specifications assume a transformer coupled configuration with external dissipation (while transmitting) of 0.14 watts for the active isolation transformer, 0.80 watts for the active bus coupling transformer, 0.45 watts for each of the two bus isolation resistors and 0.15 watts for each of the two bus termination resistors.

STANDARD DDC PROCESSING FOR HYBRID AND MONOLITHIC HERMETIC PRODUCTS							
TEST	MIL-STD-883						
1231	METHODS	CONDITION(S)					
INSPECTION	2009, 2010, 2017, and 2032	-					
SEAL	1014	A and C					
TEMPERATURE CYCLE	1010	C					
CONSTANT ACCELERATION	2001	3000g					
BURN-IN	1015 <sup>(note1)</sup> , 1030 <sup>(note2)</sup>	TABLE 1					

Notes: 1. For Process Requirement "B" (refer to ordering information), devices may be non-compliant with MIL-STD-883, Test Method 1015, Paragraph 3.2. Contact factory for details.

2.When applicable.



Notes:

 Standard DDC processing with burn-in and full temperature test. See table on preceding page.
MIL-PRF- 38534 product grading is designated with the following dash numbers: Class H is a -11X, 13X, 14X, 15X, 41X, 43X, 44X, 45X
Class G is a -21X, 23X, 24X, 25X, 51X, 53X, 54X, 55X
Class D is a -31X, 33X, 34X, 35X, 81X, 83X, 84X, 85X
The above products contain tin-lead solder finish as applicable to solder dip requirements.



The information in this **Product Brief** is believed to be accurate; however, no responsibility is assumed by Data Device Corporation for its use, and no license or rights are granted by implication or otherwise in connection therewith. Specifications are subject to change without notice.



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