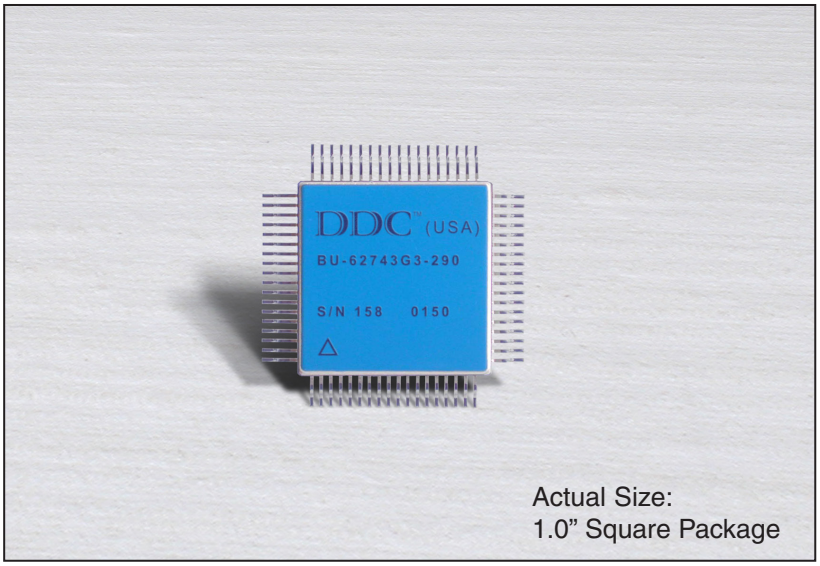
BU-62743/62843/62864

# PCI ENHANCED MINIATURE ADVANCED COMMUNICATION ENGINE (PCI ENHANCED MINI-ACE®)




Actual Size:
1.0” Square Package

## DESCRIPTION

The PCI Enhanced Mini-ACE family of MIL-STD-1553 terminals provides a complete interface between a 32-Bit / 33MHz PCI Bus and a MIL-STD-1553 bus. These terminals integrate dual transceiver, protocol logic, and 4K words or 64K words of RAM.

With a 1.0-inch square package, the PCI Enhanced Mini-ACE is nearly 100% footprint and software compatible with the Enhanced Mini-ACE, previous generation Mini-ACE (Plus) terminals, and is software compatible with the older ACE series.

The PCI portion of the PCI Enhanced Mini-ACE is powered by 3.3V. The PCI interface is NOT 5V tolerant.

Multiprotocol support of MIL-STD-1553A/B and STANAG 3838, including versions incorporating McAir compatible transmitters, is provided. There is a choice of 10, 12, 16, or 20 MHz 1553 clocks. The BC/RT/MT versions with 64K words of RAM include built-in RAM parity checking.

BC features include a built-in message sequence control engine, with a set of 20 instructions. This provides an autonomous means of implementing multi-frame message scheduling, message retry schemes, data double buffering, asynchronous message insertion, and reporting to the host CPU.

The PCI Enhanced Mini-ACE RT offers the choices of single and circular buffering, along with a global circular buffering option, 50% rollover interrupt for circular buffers, and an interrupt status queue.

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## FEATURES

- 32-Bit/33MHz, 3.3Volt, PCI Target Interface
- Fully Integrated 1553A/B Notice 2, McAir, STANAG 3838 Interface Terminal
- Compatible with Enhanced Mini-ACE, Mini-ACE (Plus) and ACE Generations
- Choice of:
  - RT only with 4K RAM (BU-62743)
  - BC/RT/MT with 4K RAM (BU-62843)
  - BC/RT/MT with 64K RAM, with RAM Parity (BU-62864)
- 3.3V Logic
- 5V Transceiver. Available with 1760 or McAir Compatible Options
- 1.0-inch square, 72-Pin Flatpack / Formed Gull Lead Ceramic Package
- Choice of 10, 12, 16, or 20MHz 1553 Clock
- Highly Autonomous BC with Built-in Message Sequence Control:
  - Frame Scheduling
  - Branching
  - Asynchronous Message Insertion
  - General Purpose Queue
  - User-defined Interrupts
- Advanced RT Functions:
  - Global Circular Buffering
  - Interrupt Status Queue
  - 50% Circular Buffer Rollover Interrupts
- Selective Message Monitor or RT/Monitor


FOR MORE INFORMATION CONTACT:

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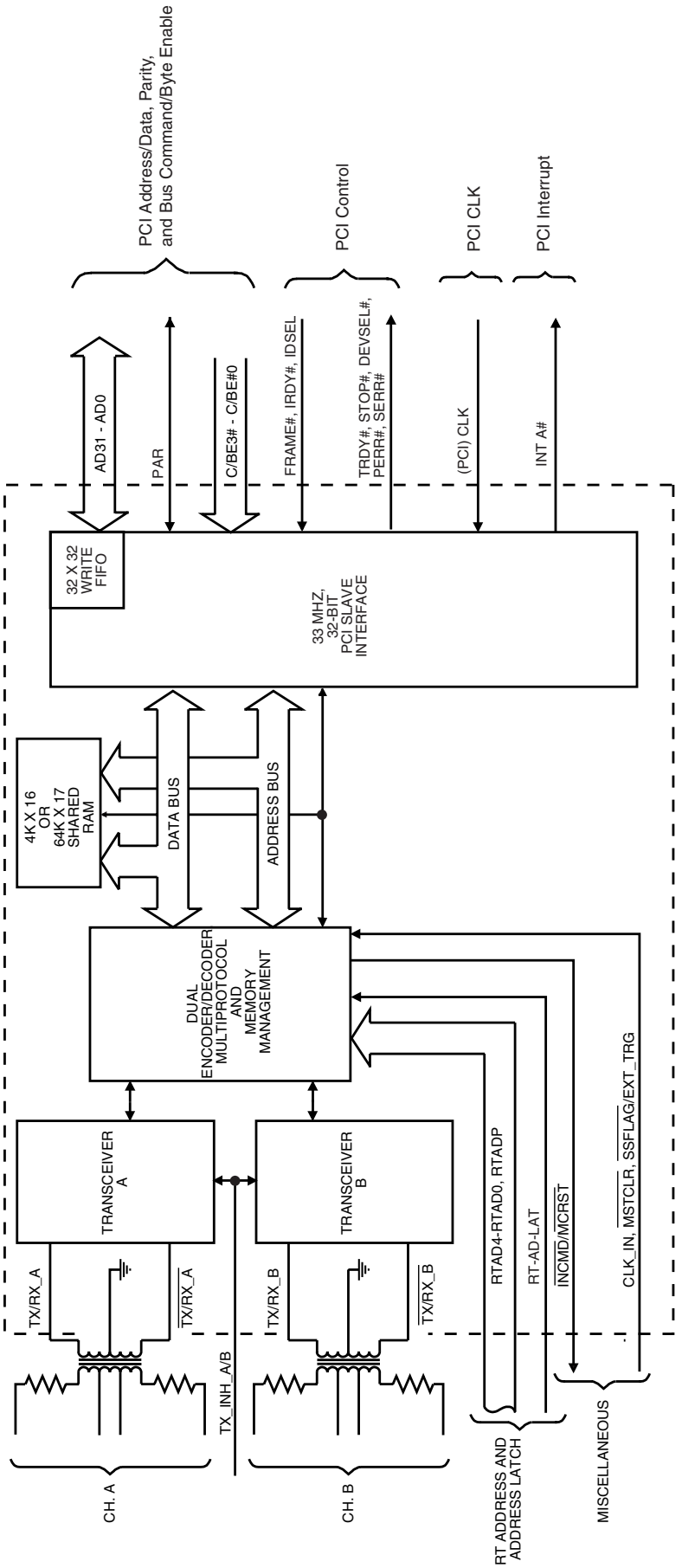



**FIGURE 1. PCI ENHANCED MINI-ACE BLOCK DIAGRAM**

## TABLE 1. PCI ENHANCED MINI-ACE SPECIFICATIONS

| PARAMETER | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|
| **ABSOLUTE MAXIMUM RATINGS** | | | | |
| Supply Voltage | | | | |
| • Logic +3.3V | -0.3 | | 4.0 | V |
| • RAM +5V | -0.3 | | 6.0 | V |
| • Transceiver +5V (Note 13) | -0.3 | | 7.0 | V |
| Logic | | | | |
| • Voltage Input Range | -0.3 | | Vdd+0.3 | V |
| • Voltage Input Range, 5v Tolerant pins (Note 16) | -0.3 | | 6.0 | V |
| **RECEIVER** | | | | |
| Differential Input Resistance (Notes 1-6) | 2.5 | | | kΩ |
| Differential Input Capacitance (Notes 1-6) | | | 5 | pF |
| Threshold Voltage, Transformer Coupled | 0.200 | | 0.860 | Vp-p |
| Common Mode Voltage (Note 7) | | | 10 | Vpeak |
| **TRANSMITTER** | | | | |
| Differential Output Voltage | | | | |
| • Direct Coupled Across 35 ohms Measured on Bus | 6 | 7 | 9 | Vp-p |
| • Transformer Coupled Across 70 ohms | | | | |
| (BU-62XXXXX-XX0, | 18 | 20 | 27 | Vp-p |
| BU-62XXXXX-XX2) (Note 14) | 20 | 22 | 27 | Vp-p |
| Output Noise, Differential (Direct Coupled) | | | 10 | mVp-p |
| Output Offset Voltage, Transformer Coupled Across 70 ohms | -250 | 150 | 250 | mVp-p |
| Rise/Fall Time | | | | |
| (BU-62XXXX3, | 100 | 150 | 300 | nsec |
| BU-62XXXX4) | 200 | 250 | 300 | nsec |
| **LOGIC** | | | | |
| $V_{IH}$ | | | | |
| All signals except PCI | 2.1 | | | V |
| $V_{IL}$ | | | | |
| All signals except PCI | | | 0.7 | V |
| Schmidt Hysteresis | | | | |
| All signals except PCI | 0.4 | | | V |
| $I_{IH}$, $I_{IL}$ | | | | |
| All signals except PCI | | | | |
| $I_{IH}$ (Vcc=3.6V, $V_{IN}$=Vcc) | -10 | | 10 | µA |
| $I_{IH}$ (Vcc=3.6V, $V_{IN}$=2.7V) | -100 | | -33 | µA |
| $I_{IL}$ (Vcc=3.6V, $V_{IN}$=0.4V) | -100 | | -33 | µA |
| $V_{OH}$ (Vcc=3.0V, $I_{OH}$=max) | 2.4 | | | V |
| $V_{OL}$ (Vcc=3.0V, $I_{OL}$=max) | | | 0.4 | V |
| $I_{OL}$ | 3.4 | | | mA |
| $I_{OH}$ | | | -3.4 | mA |
| $C_I$ (Input Capacitance) | | | 50 | pF |
| PCI LOGIC (see PCI spec 3.3V signaling environment) | | | | |
| $C_I$ (Input Capacitance) all PCI except PCI_CLK&IDSEL | | | 16 | pF |
| $C_I$ (Input Capacitance)PCI_CLK | | | 11 | pF |
| $C_I$ (Input Capacitance) IDSEL | | | 13 | pF |
| **POWER SUPPLY REQUIREMENTS** | | | | |
| Voltages/Tolerances | | | | |
| +5V (RAM for 62864), | 4.5 | 5.0 | 5.5 | V |
| +3.3V (Logic) Vcc | 3.0 | 3.3 | 3.6 | V |
| +5V (Ch. A, Ch. B) | 4.75 | 5.0 | 5.5 | V |

## TABLE 1. PCI ENHANCED MINI-ACE SPECIFICATIONS (CONT.)

| PARAMETER | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|
| Current Drain (Total Hybrid) | | | | |
| • BU-62864XX-XX0 | | | | |
| +5V (RAM, Ch. A, Ch. B) | | | | |
| • Idle | | 66 | 120 | mA |
| • 25% Transmitter Duty Cycle | | 163 | 225 | mA |
| • 50% Transmitter Duty Cycle | | 260 | 330 | mA |
| • 100% Transmitter Duty Cycle | | 454 | 540 | mA |
| • 3.3V (Logic) | | 25 | 40 | mA |
| • BU-62864XX-XX2 | | | | |
| +5V (RAM, Ch. A, Ch. B) | | | | |
| • Idle | | 66 | 120 | mA |
| • 25% Transmitter Duty Cycle | | 174 | 236 | mA |
| • 50% Transmitter Duty Cycle | | 282 | 352 | mA |
| • 100% Transmitter Duty Cycle | | 498 | 585 | mA |
| • 3.3V (Logic) | | 25 | 40 | mA |
| • BU-62743XX-XX0, BU-62843XX-XX0 | | | | |
| +5V (Ch. A, Ch. B) | | | | |
| • Idle | | 65 | 100 | mA |
| • 25% Transmitter Duty Cycle | | 169 | 205 | mA |
| • 50% Transmitter Duty Cycle | | 273 | 310 | mA |
| • 100% Transmitter Duty Cycle | | 481 | 520 | mA |
| • 3.3V Logic | | 25 | 40 | mA |
| • BU-62743XX-XX0, BU-62843XX-XX2 | | | | |
| +5V (Ch. A, Ch. B) | | | | |
| • Idle | | 65 | 100 | mA |
| • 25% Transmitter Duty Cycle | | 180 | 216 | mA |
| • 50% Transmitter Duty Cycle | | 295 | 332 | mA |
| • 100% Transmitter Duty Cycle | | 525 | 565 | mA |
| • 3.3V Logic | | 25 | 40 | mA |
| **POWER DISSIPATION** (NOTE 15) | | | | |
| Total Hybrid | | | | |
| • BU-62864XX-XX0 | | | | |
| • Idle | | 0.44 | 0.80 | W |
| • 25% Transmitter Duty Cycle | | 0.75 | 1.03 | W |
| • 50% Transmitter Duty Cycle | | 1.05 | 1.26 | W |
| • 100% Transmitter Duty Cycle | | 1.66 | 1.71 | W |
| • BU-62864XX-XX2 | | | | |
| • Idle | | 0.44 | 0.80 | W |
| • 25% Transmitter Duty Cycle | | 0.80 | 1.09 | W |
| • 50% Transmitter Duty Cycle | | 1.17 | 1.39 | W |
| • 100% Transmitter Duty Cycle | | 1.89 | 1.97 | W |
| • BU-62743XX-XX0, BU-62843XX-XX0 | | | | |
| • Idle | | 0.41 | 0.63 | W |
| • 25% Transmitter Duty Cycle | | 0.70 | 0.85 | W |
| • 50% Transmitter Duty Cycle | | 0.94 | 1.07 | W |
| • 100% Transmitter Duty Cycle | | 1.40 | 1.51 | W |
| • BU-62743XX-XX2, BU-62843XX-XX2 | | | | |
| • Idle | | 0.41 | 0.63 | W |
| • 25% Transmitter Duty Cycle | | 0.72 | 0.86 | W |
| • 50% Transmitter Duty Cycle | | 0.97 | 1.09 | W |
| • 100% Transmitter Duty Cycle | | 1.45 | 1.56 | W |
| Hottest Die | | | | |
| • BU-62XXXXX-XX0 | | | | |
| • Idle | | 0.18 | 0.28 | W |
| • 25% Transmitter Duty Cycle | | 0.42 | 0.51 | W |
| • 50% Transmitter Duty Cycle | | 0.66 | 0.75 | W |
| • 100% Transmitter Duty Cycle | | 1.14 | 1.22 | W |
| • BU-62XXXXX-XX2 | | | | |
| • Idle | | 0.18 | 0.28 | W |
| • 25% Transmitter Duty Cycle | | 0.48 | 0.58 | W |
| • 50% Transmitter Duty Cycle | | 0.78 | 0.88 | W |
| • 100% Transmitter Duty Cycle | | 1.39 | 1.48 | W |

## TABLE 1. PCI ENHANCED MINI-ACE SPECIFICATIONS (CONT.)

| PARAMETER | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|
| **CLOCK INPUTS** | | | | |
| **PCI Clock Input Frequency** | | | 33.3 | MHz |
| • 1553 Clock Frequency | | | | |
| • Default Mode | | 16.0 | | MHz |
| • Option | | 12.0 | | MHz |
| • Option | | 10.0 | | MHz |
| • Option | | 20.0 | | MHz |
| • Long Term Tolerance | | | | |
| • 1553A Compliance | -0.01 | | 0.01 | % |
| • 1553B Compliance | -0.10 | | 0.10 | % |
| • Short Term Tolerance, 1 second | | | | |
| • 1553A Compliance | -0.001 | | 0.001 | % |
| • 1553B Compliance | -0.01 | | 0.01 | % |
| **1553 MESSAGE TIMING** | | | | |
| Completion of CPU Write (BC Start)-to-Start of Next Message (for Non-enhanced BC Mode) | | 2.5 | | µs |
| BC Intermessage Gap (Note 8) | | | | |
| Non-enhanced (Mini-ACE compatible) BC mode | | 9.5 | | µs |
| Enhanced BC mode (Note 9) | | 10.0 to 10.5 | | µs |
| BC/RT/MT Response Timeout (Note 10) | | | | |
| • 18.5 nominal | 17.5 | 18.5 | 19.5 | µs |
| • 22.5 nominal | 21.5 | 22.5 | 23.5 | µs |
| • 50.5 nominal | 49.5 | 50.5 | 51.5 | µs |
| • 128.0 nominal | 127 | 129.5 | 131 | µs |
| RT Response Time (mid-parity to mid-sync) (Note 11) | 4 | | 7 | µs |
| Transmitter Watchdog Timeout | | 660.5 | | µs |
| **THERMAL** | | | | |
| 72-Pin, Ceramic Flatpack / Gull Lead Thermal Resistance, Junction-to-Case, Hottest Die ($\theta_{JC}$) (Note 12) | | 8.4 | | °C/W |
| Operating Case/Ball Temperature | | | | |
| -1XX, -4XX | -55 | | +125 | °C |
| -2XX, -5XX | -40 | | +85 | °C |
| -3XX, -8XX | 0 | | +70 | °C |
| -EXX | -40 | | +100 | °C |
| Storage Temperature | -65 | | +150 | °C |
| Lead Temperature (soldering, 10 sec.) | | | +300 | °C |
| **PHYSICAL CHARACTERISTICS** | | | | |
| 72-Pin, Ceramic Flatpack / Gull Lead Size | 1.0 X 1.0 X 0.155 (25.4 x 25.4 x 3.94) | | | in. (mm) |
| Weight | 0.6 (17) | | | oz (g) |

**TABLE 1 NOTES:**

Notes 1 through 6 are applicable to the Receiver Differential Resistance and Differential Capacitance specifications:

(1) Specifications include both transmitter and receiver (tied together internally).

(2) Impedance parameters are specified directly between pins TX/RX_A(B) and $\overline{\text{TX/RX\_A(B)}}$ of the PCI Enhanced Mini-ACE hybrid.

(3) It is assumed that all power and ground inputs to the hybrid are connected.

(4) The specifications are applicable for both unpowered and powered conditions.

(5) The specifications assume a 2 volt rms balanced, differential, sinusoidal input. The applicable frequency range is 75 kHz to 1 MHz.

(6) Minimum resistance and maximum capacitance parameters are guaranteed over the operating range, but are not tested.

(7) Assumes a common mode voltage within the frequency range of dc to 2 MHz, applied to pins of the isolation transformer on the stub side (either direct or transformer coupled), and referenced to hybrid ground. Transformer must be a DDC recommended transformer or other transformer that provides an equivalent minimum CMRR.

(8) Typical value for minimum intermessage gap time. Under software control, this may be lengthened (to 65,535 ms - message time) in increments of 1 µs. If ENHANCED CPU ACCESS, bit 14 of Configuration Register #6, is set to logic "1", then host accesses during BC Start-of-Message (SOM) and End-of-Message (EOM) transfer sequences could have the effect of lengthening the intermessage gap time. For each host access during an SOM or EOM sequence, the intermessage gap time will be lengthened by 6 clock cycles. Since there are 7 internal transfers during SOM and 5 during EOM, this could theoretically lengthen the intermessage gap by up to 72 clock cycles; i.e., up to 7.2 µs with a 10 MHz clock, 6.0 µs with a 12 MHz clock, 4.5 µs with a 16 MHz clock, or 3.6 µs with a 20 MHz clock.

(9) For Enhanced BC mode, the typical value for intermessage gap time is approximately 10 clock cycles longer than for the non-enhanced BC mode. That is, an addition of 1.0 µs at 10 MHz, 833 ns at 12 MHz, 625 ns at 16 MHz, or 500 ns at 20 MHz.

(10) Software programmable (4 options). Includes RT-to-RT Timeout (measured mid-parity of transmit Command Word to mid-sync of transmitting RT Status Word).

(11) Measured from mid-parity crossing of Command Word to mid-sync crossing of RT's Status Word.

(12) θjc is measured to the bottom of the case.

(13) External 10 µF tantalum and 0.1 µF capacitors should be located as close as possible to Pins 20 and 72, and a 0.1 µF at pin 37. The BU-62864 should also have a 0.1 µF at pin 26.

(14) MIL-STD-1760 requires that the PCI Enhanced Mini-ACE produce a 20 Vp-p minimum output on the stub connection.

(15) Power dissipation specifications assume a transformer coupled configuration with external dissipation (while transmitting) of:
0.14 watts for the active isolation transformer,
0.08 watts for the active bus coupling transformer,
0.45 watts for each of the two bus isolation resistors and
0.15 watts for each of the two bus termination resistors.

(16) The 5V tolerant pins are CLOCK_IN, RTAD0-5, RTAD_PAR, RTAD_LAT, TXINH_A/B, and $\overline{\text{SSFLAG}}$/EXT_TRIG.

## INTRODUCTION

The BU-62743 RT, and BU-62843/62864 BC/RT/MT PCI Enhanced Mini-ACE family of MIL-STD-1553 terminals comprise a complete integrated interface between a PCI host processor and a MIL-STD-1553 bus. All members of the PCI Enhanced Mini-ACE family are packaged in the same 1.0 square inch flat-pack package. The PCI Enhanced Mini-ACE hybrids provide footprint and software compatibility with the Enhanced Mini-ACE, Mini-ACE (Plus) terminals, as well as software compatibility with the older ACE series.

The PCI Enhanced Mini-ACE provides complete multiprotocol support of MIL-STD-1553A/B/McAir and STANAG 3838. All versions integrate dual transceiver; along with protocol, host interface, memory management logic; and a minimum of 4K words of RAM. In addition, the BU-62864 BC/RT/MT terminals include 64K words of internal RAM, with built-in parity checking.

The PCI Enhanced Mini-ACEs include a 5V, voltage source transceiver for improved line driving capability, with options for MIL-STD-1760 and McAir compatibility. To provide further flexibility, the PCI Enhanced Mini-ACE may operate with a choice of 10, 12, 16, or 20 MHz clock inputs.

The PCI Enhanced Mini-ACEs are fully compliant targets, as defined by the PCI Local Bus Specification Revision 2.2, using a 32 bit interface that operates at clock speeds of up to 33 MHz, from a 3.3V bus. The interface supports PCI interrupts and contains a FIFO that handles PCI burst write transfer cycles. The FIFO is deep enough to accept an entire 1553 message. The PCI interface is NOT 5V tolerant and cannot be used in a 5V PCI signaling environment. The PCI interface is powered by 3.3V.

The 64K RAM, in the 64K version, is powered by 5V.

One of the new salient features of the PCI Enhanced Mini-ACE is its Enhanced Bus Controller architecture. The Enhanced BC's highly autonomous message sequence control engine provides a means for offloading the host processor for implementing multi-frame message scheduling, message retry schemes, data double buffering, and asynchronous message insertion. For the purpose of performing messaging to the host processor, the Enhanced BC mode includes a General Purpose Queue, along with user-defined interrupts.

The PCI Enhanced Mini-ACE RT offers the choice of single and circular buffering for individual subaddresses. New enhancements to the RT architecture include a global circular buffering option for multiple (or all) receive subaddresses, a 50% rollover interrupt for circular buffers, an interrupt status queue for logging up to 32 interrupt events, and an option to automatically initialize to RT mode with the Busy bit set. The interrupt status queue and 50% rollover interrupt features are also included as improvements to the PCI Enhanced Mini-ACE's Monitor architecture.

The PCI Enhanced Mini-ACE series terminals operate over the full military temperature range of -55°C to +125°C. Available screened to MIL-PRF-38534C, the terminals are ideal for military and industrial processor-to-1553 applications.

## TRANSCEIVERS

The transceivers in the PCI Enhanced Mini-ACE series terminals are fully monolithic, requiring only a +5V power input. The transmitters are voltage sources, which provide improved line driving capability over current sources. This serves to improve performance on long buses with many taps. The transmitters also offer an option which satisfies the MIL-STD-1760 requirement for a minimum of 20 volts peak-to-peak, transformer coupled output.

Besides eliminating the demand for an additional power supply, the use of a +5V-only transceiver requires the use of a step-up, rather than a step-down, isolation transformer. This provides the advantage of higher terminal input impedance than is possible for a 15 volt or 12 volt transmitter. As a result, there is a greater margin for the input impedance test, mandated for the 1553 validation test. This characteristic allows for longer cable lengths between a system connector and the isolation transformers of an embedded 1553 terminal.

To provide compatibility to McAir specs, the PCI Enhanced Mini-ACE is available with an option for transmitters with increased rise and fall times.

Additionally, for MIL-STD-1760 applications, the PCI Enhanced Mini-ACE provides an option for a minimum stub voltage level of 20 volts peak-to-peak, transformer coupled.

The receiver sections of the PCI Enhanced Mini-ACE are fully compliant with MIL-STD-1553B Notice 2 in terms of front-end overvoltage protection, threshold, common mode rejection, and word error rate.

### PCI REGISTER AND MEMORY ADDRESSING

The PCI Interface contains a set of "Type 00h" PCI configuration registers that are used to map the device into the host system. There are two Base Address Registers that are used to implement ACE memory space (BAR0) and register space (BAR1). The PCI configuration register space is mapped in accordance with PCI revision 2.2 specifications.

The PCI Enhanced Mini-ACE acts as a target and responds to the PCI commands listed in TABLE 2.

The PCI Enhanced Mini-ACE does NOT implement the Memory Read Multiple, Memory Read Line or Memory Write and Invalidate commands. However, in accordance with PCI rules, the PCI Enhanced Mini-ACE will accept these requests and alias them to the basic memory commands. For example, Memory

| TABLE 2. PCI TARGET COMMAND CODES | |
|---|---|
| **COMMAND TYPE** | **CODE (C/BE[3:0]#)** |
| Memory Read | 0110 (6h) |
| Memory Write | 0111 (7h) |
| Configuration Read | 1010 (Ah) |
| Configuration Write | 1011 (Bh) |
| Memory Read Multiple | 1100 (Ch) |
| Memory Read Line | 1110 (Eh) |
| Memory Write and Invalidate | 1111 (Fh) |

Read Multiple and Memory Read Line commands will be accepted and treated as Memory Read commands. Similarly, the PCI Enhanced Mini-ACE will accept a memory Write and Invalidate command and treat it as a Memory Write command.

ACE memory is accessed internally in 16-bit words, but memory is accessed sequentially allowing for 32-bits of data to be read from the PCI bus. In other words, if a 32-bit PCI read is requested the first 16 bits of data would be read from the requested internal address, the next 16 bits of data would be read from the initial internal address + 1, and then the resulting 32-bit double word would be transferred to the PCI bus. The PCI Enhanced Mini-ACE supports 32-bit and 16-bit read and write operations, 8-bit reads will return 16-bit data, and 8-bit writes are illegal and will cause target-aborts.

The ACE register mapping is located in PCI memory space. Although the PCI Enhanced Mini-ACE can be accessed in 32-bit words, all ACE registers are accessed in 16 bit word reads / writes. If a 32-bit read is performed from the PCI bus in ACE register space only the first 16 bits of data are valid.

This data sheet describes the PCI registers that are specific to configuring the integrated terminal and shared RAM. For specifics or definitions on other PCI bus configuration registers, please see the PCI Local Bus specification revision 2.2.

### *VENDOR ID*

The Vendor ID field contains the vendor's ID configuration register. Data Device Corporation's ID code is 4DDCh.

### *DEVICE ID*

The Device ID field is used to indicate the device being used. This field is configured by DDC to reflect the part value of the device. TABLE 4 represents all possible combinations for the Device ID field.

### *RESERVED*

These bits are read-only and return zeroes when read.

### *SERR# ENABLE*

This is an enable bit for the SERR# driver. A value of 0b disables the driver. A value of 1b enables the driver. The value after RST# is 0b.

### *PARITY ERROR CONTROL*

This bit controls the device's response to parity errors. When the bit is 1b, the device will take its normal action when a parity error is detected. When this bit is 0b, the device will ignore any parity errors that it detects and continue normal operation. The value after RST# is 0b.

**TABLE 3. CONFIGURATION REGISTER SPACE FOR THE PCI ENHANCED MINI-ACE**

| ADDRESS | 31 24 | 23 16 | 15 8 | 7 0 |
|---|---|---|---|---|
| 00h | Device ID | | Vendor ID | |
| | 04h | 0Xh<br>(X varies with part #, see text) | DDC Manufacturer Device ID value<br>(4DDCH) | |
| 04h | Status Register | | Command Register | |
| 08h | Class Code = 078000 h | | | Rev ID = 02h |
| 0Ch | BIST<br>00h | Header Type<br>00h | Latency Timer<br>00h | Cache Line Size<br>00h |
| 10h | Base Address Register 0 (for ACE memory) | | | |
| | R/W | R/W and 0's<br>see text | 00h | 00h |
| 14h | Base Address Register 1 (for ACE Registers) | | | |
| | R/W | R/W | R/W and 0's<br>see text | 00h |
| 18h - 24h | Base Address Registers 2 through 5 (not Used) 00000000h | | | |
| 28h | Card Bus CIS pointer (Not Used) 00000000h | | | |
| 2Ch | Subsystem Device and Subsystem Vendor ID. Same as Configuration Register 0, Alias Reads to Configuration Register 00 | | | |
| 30h | Expansion ROM Base Address (Not Used, bit 0 = 0) | | | |
| 34h - 38h | Reserved | | | |
| 3Ch | Max Lat.<br>00h | Min Gnt<br>00h | Interrupt Pin<br>01h | Interrupt Line<br>R/W |

| TABLE 4. DEVICE ID FIELD MAPPING | |
|---|---|
| **DEVICE ID** | **PART VALUE** |
| 0400h | BC/RT/MT with 4K of RAM (BU-62843) |
| 0402h | BC/RT/MT with 64K of RAM (BU-62864) |
| 0404h | RT Only with 4K of RAM (BU-62743) |

*MEMORY SPACE*

This bit controls the device's response to memory space accesses. A value of 0b disables the device response. A value of 1b allows the device to respond to memory space accesses. The value after RST# is 0b.

*PCI STATUS REGISTER*

This register records status information for PCI bus related events. Reads to this register behave normally, but writes can only reset bits. A bit is reset whenever the register is written and the data in the corresponding bit location is a 1.

*DETECTED PARITY ERROR*

This bit will be set by the device whenever it detects a parity error, even if the Parity Error Control bit in the PCI Control register is 0b.

*SIGNALED SYSTEM ERROR*

This bit indicates when the device has asserted SERR#. The value after RST# is 0b.

*SIGNALED TARGET ABORT*

This bit is set whenever the device terminates a transaction with a Target-Abort. The value after RST# is 0b.

*DEVSEL# TIMING*

The PCI enhanced Mini-ACE is 01b, medium.

*FAST BACK-TO-BACK CAPABLE*

This bit is set to 1b and indicates that the device is capable of accepting fast back-to-back transactions.

*RESERVED*

These bits are read-only and return zeroes when read.

*SUBSYSTEM VENDOR ID/SUBSYSTEM DEVICE ID*

This field is an alias of the Vendor ID/Device ID fields in Configuration Register 00h.

| TABLE 5. PCI COMMAND REGISTER | |
|---|---|
| **BIT** | **DESCRIPTION** |
| 15:10 | Reserved, 0s |
| 9 | 0 |
| 8 | SERR# Enable |
| 7 | 0 |
| 6 | Parity Error Control |
| 5:2 | 0 |
| 1 | Memory Space |
| 0 (LSB) | 0 |

| TABLE 6. PCI STATUS REGISTER | |
|---|---|
| **BIT** | **DESCRIPTION** |
| 31 | Detected Parity Error |
| 30 | Signaled System Error |
| 29:28 | 0 |
| 27 | Signaled Target Abort |
| 26:25 | DEVSEL# Timing = 01 (medium) |
| 24 | 0 |
| 23 | Fast Back-to-Back Capable = 1 |
| 22:21 | 0 |
| 20:16 | Reserved, 0s |

*BASE ADDRESS REGISTERS*

Base Address Registers are used to implement ACE memory space (BAR0) and ACE register space (BAR1). Base Address Registers 2 through 5 are not used.

*BAR0*

BAR0 is used to access ACE memory space. The ACE is allotted a maximum of 64K words, 128K bytes, for its memory space. BAR0 will read back as FFFE0000 after all Fs are written to it. BAR0 will read back the same for both the 4K word ACE parts (BU-62743/843) and the 64K word ACE (BU-62864).

| TABLE 7. (BAR0) ACE MEMORY | |
|---|---|
| **ADDRESS OFFSET** | **DEFINITION** |
| 00000 - 1FFFC | PCI ENHANCED Mini-ACE Memory Space |

*PCI ENHANCED MINI-ACE MEMORY SPACE*

The least significant bit (LSB) of the PCI address is dropped to form the ACE memory address.

*BAR1*

BAR1 is used to access ACE register locations. The ACE is allotted a maximum of 4K bytes for its register space. BAR1 will read back as FFFFF000h after all Fs are written to it. All ACE register locations are accessible through the PCI host via the BAR1 offsets 000h to 0FCh. The PCI-to-ACE interface control/status registers are at 800h to 81Ch. PCI accesses outside of these specific regions (e.g., to offset 100h or 820h, etc.) will produce Target Aborts.

*PCI ENHANCED MINI-ACE REGISTER SPACE*

Register accesses are on a 32-bit boundary: the last 2 bits of the PCI address are dropped to form the ACE address. (e.g. 000 = ACE Reg 0, 004 = ACE Reg1, 008 = ACE Reg2, etc.).

*PCI_INTERRUPT ACTIVE*

When set to '1', indicates that PCI Enhanced Mini-ACE has asserted it's interrupt pin. The three possible sources (if enabled and active) are the Enhanced Mini-ACE, fail-safe timer and BAR1 DRR_DATA_DISCARD.

| TABLE 8. (BAR1) ACE / CONTROL REGISTERS - 4K BYTE TOTAL SPACE | | |
|---|---|---|
| ADDRESS OFFSET | NAME | DEFINITION / ACCESSIBILITY |
| 000-0FC | ACE | PCI ENHANCED MINI-ACE Register Space |
| 100-7FC | — | RESERVED (Target-Abort if accessed) |
| 800 | REG0 | GLOBAL ACTIVITY (RD) |
| 804 | REG1 | FAIL-SAFE OPERATION / INTERRUPT (RD/WR) |
| 808 | REG2 | FAIL-SAFE TIMER (RD) |
| 80C | REG3 | FAIL-SAFE TIMER PRELOAD (RD/WR) |
| 810 | REG4 | DISCARD TIMER (RD) |
| 814 | REG5 | DISCARD TIMER PRELOAD (RD/WR) |
| 818 | REG6 | GENERAL PURPOSE, CUSTOMER USE (RD/WR) |
| 81C | REG7 | CLEAR FAIL-SAFE INT/RESET ACE (WR) |
| 820-FFC | — | RESERVED (Target-Abort if accessed) |

*FIFO NOT EMPTY*

When set to '1', indicates that the write FIFO is not empty.

*BAR1 DRR_DATA_DISCARD*

If the data discard timer times out while waiting for a retry on a BAR1 access, this bit will be set. If BAR1 read is discarded, it may have caused an action (for example clearing an ACE interrupt) that has not been recognized by the PCI MASTER.

| TABLE 9. REG0 GLOBAL ACTIVITY REGISTER (READ 800H) | |
|---|---|
| BIT | DESCRIPTION |
| 31 (MSB) | PCI INTERRUPT ACTIVE |
| 30 | FIFO NOT EMPTY |
| 29 | 0 |
| 28 | 0 |
| 27 | 0 |
| 26 | 0 |
| 25 | 0 |
| 24 | 1 |
| 23 | BAR1 DRR_DATA_DISCARD |
| 22 | FAIL_SAFE ERROR |
| 21 | 0 |
| 20 | 0 |
| 19 | 0 |
| 18 | 0 |
| 17 | 0 |
| 16 | PCI ENHANCED MINI-ACE INTERRUPT ACTIVE |
| 15 | 0 |
| • | • |
| • | • |
| • | • |
| 0 (LSB) | 0 |

This register will be all 0s after RST#, except for bit 24.

*FAIL-SAFE ERROR*

If not in FAIL_SAFE OFF mode and fail-safe error occurs (ACE does not respond), this bit will be set. Fail-safe errors are extremely unlikely.

*DRR_HOLD*

When '0', a delayed read request is discarded if the PCI Enhanced Mini-ACE has obtained requested data and a different transaction is requested. When '1', delayed read request is held until master repeats original request or timeout occurs.

*BITS 30 - 22*

Reserved, write as 0s.

*PCI ENHANCED MINI-ACE INTERRUPT ENABLE*

Must be set to "1".

*BAR1 DRR_DATA_DISCARD INTERRUPT ENABLE*

Enables interrupt to occur on a BAR1 delayed read timeout.

*FAIL-SAFE INTERRUPT ENABLE*

When set to a "1", an interrupt is generated if not in FAILSAFE OFF mode and a fail-safe error is detected.

*FAIL-SAFE INTERRUPT AUTOCLEAR ENABLE*

If set, causes interrupt and the FAIL_SAFE ERROR bit (REG0-bit 22) to be cleared whenever upper word of REG0 is read by the PCI MASTER. If not set, bit 1 in Reg 7 must be used to clear fail-safe interrupts.

| TABLE 10. REG1 FAIL-SAFE OPERATION / INTERRUPT REGISTER (READ/WRITE 804H) | |
|---|---|
| BIT | DESCRIPTION |
| 31 (MSB) | DRR_HOLD |
| 30 | RESERVED, WRITE AS 0 |
| • | • |
| • | • |
| • | • |
| 22 | RESERVED, WRITE AS 0 |
| 21 | PCI ENHANCED MINI-ACE INTERRUPT ENABLE |
| 20 | BAR1 DRR_DATA_DISCARD INTERRUPT ENABLE |
| 19 | FAILSAFE INTERRUPT ENABLE |
| 18 | FAILSAFE INTERRUPT AUTOCLEAR ENABLE |
| 17 | FAILSAFE MODE - BIT 1 (MSB) |
| 16 | FAILSAFE MODE - BIT 0 (LSB) |
| 15 | RESERVED, WRITE AS 0 |
| • | • |
| • | • |
| • | • |
| 0 (LSB) | RESERVED, WRITE AS 0 |

This register will be all 0s after RST#, except that bit 17 will be 1 (Failsafe mode = Failsafe Halt). Note that Fail-safe errors are extremely unlikely.

| TABLE 11. FAIL-SAFE MODE | | |
|---|---|---|
| BIT 17 | BIT 16 | FAIL-SAFE MODE |
| 0 | 0 | Fail-safe Off |
| 0 | 1 | Fail-safe Retry |
| 1 | 0 | Fail-safe Halt |
| 1 | 1 | Fail-safe Skip |

NOTE: Fail-safe errors are extremely unlikely.

### *FAIL-SAFE MODE*

Fail-safe Errors occur when the internal ACE fails to assert it's hand-shake signal within 1 millisecond (programmable) of when the internal Strobe or Request signal is asserted. Four possible FAIL-SAFE Modes determine how this situation is handled:

#### *MODE 1 - FAIL-SAFE OFF*

PCI Enhanced Mini-ACE will wait indefinitely for the transaction to complete. The local bus could hang as a result. The FAILSAFE ERROR bit and interrupt will not be generated even if the enable bit is set.

#### *MODE 2 - FAIL-SAFE RETRY*

PCI Enhanced Mini-ACE will retry the transfer on the local bus when the FAIL-SAFE timer times out.

#### *MODE 3 - FAIL-SAFE HALT*

Once the FAIL-SAFE timer times out, all future transfers will be terminated with a target abort until the PCI master clears the interrupt.

#### *MODE 4 - FAIL-SAFE SKIP*

Once the FAIL-SAFE timer times out, the current transaction is discarded or skipped and the next transaction, whether a stored write in the FIFO or a new transaction, will be attempted.

| TABLE 12. REG2 FAIL-SAFE TIMER REGISTER (READ 808H) | |
|---|---|
| BIT | DESCRIPTION |
| 31 (MSB) | 0 |
| • | • |
| • | • |
| • | • |
| 16 | 0 |
| 15 | FAIL-SAFE TIMER COUNT - BIT 15 (MSB) |
| • | • |
| • | • |
| • | • |
| 0 (LSB) | FAIL-SAFE TIMER COUNT - BIT 0 (LSB) |

### *FAIL-SAFE TIMER COUNT*

Read this register to obtain the current value of the fail-safe timer. Default is 8400h.

| TABLE 13. REG3 FAIL-SAFE TIMER PRELOAD REGISTER (READ/WRITE 80CH) | |
|---|---|
| BIT | DESCRIPTION |
| 31 (MSB) | 0 |
| • | • |
| • | • |
| • | • |
| 16 | 0 |
| 15 | FAIL-SAFE TIMER VALUE - BIT 15 (MSB) |
| • | • |
| • | • |
| • | • |
| 0 (LSB) | FAIL-SAFE TIMER VALUE - BIT 0 (LSB) |

### *FAIL-SAFE TIMER VALUE*

Write to this register to set the value for the fail-safe timer. The default value is 8400h and no access to this register is needed for normal applications.

| TABLE 14. REG4 DISCARD TIMER REGISTER (READ 810H) | |
|---|---|
| BIT | DESCRIPTION |
| 31 (MSB) | 0 |
| • | • |
| • | • |
| • | • |
| 16 | 0 |
| 15 | DISCARD TIMER CURRENT - BIT 15 (MSB) |
| • | • |
| • | • |
| • | • |
| 0 (LSB) | DISCARD TIMER CURRENT - BIT 0 (LSB) |

### *DISCARD TIMER CURRENT*

Read this register to obtain the current value of the DISCARD TIMER. Default is 0000h.

| TABLE 15. REG5 DISCARD TIMER PRELOAD REGISTER (READ/WRITE 814H) | |
|---|---|
| BIT | DESCRIPTION |
| 31 (MSB) | 0 |
| • | • |
| • | • |
| • | • |
| 16 | 0 |
| 15 | DISCARD TIMER VALUE - BIT 15 (MSB) |
| • | • |
| • | • |
| • | • |
| 0 (LSB) | DISCARD TIMER VALUE - BIT 0 (LSB) |

### *DISCARD TIMER VALUE*

Write this register to set the value to be used for the discard timer. The default value is "0". The default value meets the PCI spec and no access to this register is needed for normal applications.

| TABLE 16. REG6 GENERAL PURPOSE REGISTER (READ/WRITE 818H) | |
|---|---|
| **BIT** | **DESCRIPTION** |
| 31 (MSB) | RESERVED - BIT 31 (MSB) |
| • | • |
| • | • |
| • | • |
| 0 (LSB) | RESERVED - BIT 0 (LSB) |

Note: This register will be all 0s after RST#. This read/write register is available for customer use, perhaps as a flag register for signaling between bus masters.

| TABLE 17. REG7 RESERVED REGISTER (WRITE 81CH) | |
|---|---|
| **BIT** | **DESCRIPTION** |
| 31 (MSB) | RESERVED, WRITE AS 0 - BIT 31 (MSB) |
| • | • |
| • | • |
| • | • |
| 1 | CLEAR FAILSAFE INTERRUPT |
| 0 (LSB) | ACE RESET - BIT 0 (LSB) |

Note: This register will be all 0s after RST#. No access to this register is needed for normal applications.

*BITS 15-0 ARE RESERVED*

Write these bits as 0s.

*BITS 31-2 ARE RESERVED*

Must be written as 0s.

*CLEAR FAIL-SAFE INTERRUPT*

Clears the Fail-safe Interrupt when set to "1". Fail-safe interrupts can also be cleared via the Fail-safe Interrupt Autoclear mechanism, enabled by bit 18 in Reg 1.

*ACE RESET*

Resets the ACE when set to "1".

## PCI ENHANCED MINI-ACE REGISTER AND MEMORY ADDRESSING

The software interface of the Enhanced Mini-ACE portion of the PCI EMA to the host processor consists of 24 internal operational registers for normal operation, an additional 24 test registers, plus 64K words of shared memory address space. The PCI Enhanced Mini-ACE's 4K X 16 or 64K X 17 internal RAM resides in this address space.

For normal operation, the host processor only needs to access the lower 32 register address locations (00-1Fh, PCI BAR1 offset 00-7Ch). The next 32 locations (20-3F, PCI BAR1 offset 80h-FCh) should be reserved, since many of these are used for factory test.

## INTERNAL 1553 REGISTERS

The internal address mapping for the PCI Enhanced Mini-ACE registers is illustrated in TABLE 18. Note that the address lines shown are the PCI Enhanced Mini-ACE's internal ACE register bus and are left shifted 2 bits with respect to the PCI address: A0 = PCI A2, A1 = PCI A3, etc. For example, Interrupt mask register #1 is located at PCI address BAR1 offset + 0h, Configuration Register #1 is at BAR1 offset + 4h, etc. Note that TABLE 18 does not show the internal A5 register address line, which is normally 0 and is set only for access to the reserved factory test registers.

The configuration registers will be cleared to 0000h after hardware or software reset, with the exception of the Enhanced CPU Access bit (bit 14 in Configuration register #6).

| TABLE 18. 1553 REGISTER ADDRESS MAPPING | | | | | | |
|---|---|---|---|---|---|---|
| INTERNAL ADDRESS LINES | | | | | PCI BAR1 ADDR OFFSET | REGISTER DESCRIPTION / ACCESSIBILITY |
| A4 | A3 | A2 | A1 | A0 | | |
| 0 | 0 | 0 | 0 | 0 | 00h | Interrupt Mask Register #1 (RD/WR) |
| 0 | 0 | 0 | 0 | 1 | 04h | Configuration Register #1 (RD/WR) |
| 0 | 0 | 0 | 1 | 0 | 08h | Configuration Register #2 (RD/WR) |
| 0 | 0 | 0 | 1 | 1 | 0Ch | Start/Reset Register (WR) |
| 0 | 0 | 0 | 1 | 1 | 0Ch | Non-Enhanced BC or RT Command Stack Pointer / Enhanced BC Instruction List Pointer Register (RD) |
| 0 | 0 | 1 | 0 | 0 | 10h | BC Control Word / RT Subaddress Control Word Register (RD/WR) |
| 0 | 0 | 1 | 0 | 1 | 14h | Time Tag Register (RD/WR) |
| 0 | 0 | 1 | 1 | 0 | 18h | Interrupt Status Register #1 (RD) |
| 0 | 0 | 1 | 1 | 1 | 1Ch | Configuration Register #3 (RD/WR) |
| 0 | 1 | 0 | 0 | 0 | 20h | Configuration Register #4 (RD/WR) |
| 0 | 1 | 0 | 0 | 1 | 24h | Configuration Register #5 (RD/WR) |
| 0 | 1 | 0 | 1 | 0 | 28h | RT / Monitor Data Stack Address Register (RD/WR) |
| 0 | 1 | 0 | 1 | 1 | 2Ch | BC Frame Time Remaining Register (RD) |
| 0 | 1 | 1 | 0 | 0 | 30h | BC Time Remaining to Next Message Register (RD) |
| 0 | 1 | 1 | 0 | 1 | 34h | Non-Enhanced BC Frame Time / Enhanced BC Initial Instruction Pointer / RT Last Command / MT Trigger Word Register(RD/WR) |
| 0 | 1 | 1 | 1 | 0 | 38h | RT Status Word Register (RD) |
| 0 | 1 | 1 | 1 | 1 | 3Ch | RT BIT Word Register (RD) |
| 1 | 0 | 0 | 0 | 0 | 40h | Test Mode Register 0 |
| 1 | 0 | 0 | 0 | 1 | 44h | Test Mode Register 1 |
| 1 | 0 | 0 | 1 | 0 | 48h | Test Mode Register 2 |
| 1 | 0 | 0 | 1 | 1 | 4Ch | Test Mode Register 3 |
| 1 | 0 | 1 | 0 | 0 | 50h | Test Mode Register 4 |
| 1 | 0 | 1 | 0 | 1 | 54h | Test Mode Register 5 |
| 1 | 0 | 1 | 1 | 0 | 58h | Test Mode Register 6 |
| 1 | 0 | 1 | 1 | 1 | 5Ch | Test Mode Register 7 |
| 1 | 1 | 0 | 0 | 0 | 60h | Configuration Register #6 (RD/WR) |
| 1 | 1 | 0 | 0 | 1 | 64h | Configuration Register #7 (RD/WR) |
| 1 | 1 | 0 | 1 | 0 | 68h | RESERVED |
| 1 | 1 | 0 | 1 | 1 | 6Ch | BC Condition Code Register (RD) |
| 1 | 1 | 0 | 1 | 1 | 6Ch | BC General Purpose Flag Register (WR) |
| 1 | 1 | 1 | 0 | 0 | 70h | BIT Test Status Register (RD) |
| 1 | 1 | 1 | 0 | 1 | 74h | Interrupt Mask Register #2 (RD/WR) |
| 1 | 1 | 1 | 1 | 0 | 78h | Interrupt Status Register #2 (RD) |
| 1 | 1 | 1 | 1 | 1 | 7Ch | BC General Purpose Queue Pointer / RT-MT Interrupt Status Queue Pointer Register (RD/WR) |

| TABLE 19. INTERRUPT MASK REGISTER #1 (READ/WRITE 00H, PCI 00H) | |
|---|---|
| **BIT** | **DESCRIPTION** |
| 15(MSB) | RESERVED |
| 14 | RAM PARITY ERROR |
| 13 | BC/RT TRANSMITTER TIMEOUT |
| 12 | BC/RT COMMAND STACK ROLLOVER |
| 11 | MT COMMAND STACK ROLLOVER |
| 10 | MT DATA STACK ROLLOVER |
| 9 | HANDSHAKE FAIL |
| 8 | BC RETRY |
| 7 | RT ADDRESS PARITY ERROR |
| 6 | TIME TAG ROLLOVER |
| 5 | RT CIRCULAR BUFFER ROLLOVER |
| 4 | RT SUBADDRESS CONTROL WORD EOM |
| 3 | BC END OF FRAME |
| 2 | FORMAT ERROR |
| 1 | BC STATUS SET/RT MODE CODE/MT PATTERN TRIGGER |
| 0(LSB) | END OF MESSAGE |

| TABLE 20. CONFIGURATION REGISTER #1 (READ/WRITE 01H, PCI 04H) | | | | |
|---|---|---|---|---|
| **BIT** | **BC FUNCTION (Bits 11-0 Enhanced Mode Only)** | **RT WITHOUT ALTERNATE STATUS** | **RT WITH ALTERNATE STATUS (Enhanced Only)** | **MONITOR FUNCTION (Enhanced mode only bits 12-0)** |
| 15 (MSB) | RT/$\overline{\text{BC-MT}}$ (logic 0) | (logic 1) | (logic 1) | (logic 0) |
| 14 | MT/$\overline{\text{BC-RT}}$ (logic 0) | (logic 0) | (logic 0) | (logic 1) |
| 13 | CURRENT AREA B/$\overline{\text{A}}$ | CURRENT AREA B/$\overline{\text{A}}$ | CURRENT AREA B/$\overline{\text{A}}$ | CURRENT AREA B/$\overline{\text{A}}$ |
| 12 | MESSAGE STOP-ON-ERROR | MESSAGE MONITOR ENABLED (MMT) | MESSAGE MONITOR ENABLED | MESSAGE MONITOR ENABLED |
| 11 | FRAME STOP-ON-ERROR | $\overline{\text{DYNAMIC BUS CONTROL ACCEPTANCE}}$ | S10 | TRIGGER WORD ENABLED |
| 10 | STATUS SET STOP-ON-MESSAGE | $\overline{\text{BUSY}}$ | S09 | START-ON-TRIGGER |
| 9 | STATUS SET STOP-ON-FRAME | $\overline{\text{SERVICE REQUEST}}$ | S08 | STOP-ON-TRIGGER |
| 8 | FRAME AUTO-REPEAT | $\overline{\text{SSFLAG}}$ | S07 | NOT USED |
| 7 | EXTERNAL TRIGGER ENABLED | $\overline{\text{RTFLAG}}$ (Enhanced Mode Only) | S06 | EXTERNAL TRIGGER ENABLED |
| 6 | INTERNAL TRIGGER ENABLED | NOT USED | S05 | NOT USED |
| 5 | INTERMESSAGE GAP TIMER ENABLED | NOT USED | S04 | NOT USED |
| 4 | RETRY ENABLED | NOT USED | S03 | NOT USED |
| 3 | DOUBLED/$\overline{\text{SINGLE}}$ RETRY | NOT USED | S02 | NOT USED |
| 2 | BC ENABLED (Read Only) | NOT USED | S01 | MONITOR ENABLED(Read Only) |
| 1 | BC FRAME IN PROGRESS (Read Only) | NOT USED | S00 | MONITOR TRIGGERED (Read Only) |
| 0 (LSB) | BC MESSAGE IN PROGRESS (Read Only) | RT MESSAGE IN PROGRESS (Enhanced mode only,Read Only) | RT MESSAGE IN PROGRESS (Read Only) | MONITOR ACTIVE (Read Only) |

| TABLE 21. CONFIGURATION REGISTER #2 (READ/WRITE 02H, PCI 08H) | |
|---|---|
| **BIT** | **DESCRIPTION** |
| 15(MSB) | ENHANCED INTERRUPTS |
| 14 | RAM PARITY ENABLE |
| 13 | BUSY LOOKUP TABLE ENABLE |
| 12 | RESERVED FUTURE USE, must be 0 |
| 11 | OVERWRITE INVALID DATA |
| 10 | 256-WORD BOUNDARY DISABLE |
| 9 | TIME TAG RESOLUTION 2 |
| 8 | TIME TAG RESOLUTION 1 |
| 7 | TIME TAG RESOLUTION 0 |
| 6 | CLEAR TIME TAG ON SYNCHRONIZE |
| 5 | LOAD TIME TAG ON SYNCHRONIZE |
| 4 | INTERRUPT STATUS AUTO CLEAR |
| 3 | LEVEL/$\overline{\text{PULSE}}$ INTERRUPT REQUEST |
| 2 | CLEAR SERVICE REQUEST |
| 1 | ENHANCED RT MEMORY MANAGEMENT |
| 0(LSB) | SEPARATE BROADCAST DATA |

| TABLE 22. START/RESET REGISTER (WRITE 03H, PCI 0CH) | |
|---|---|
| **BIT** | **DESCRIPTION** |
| 15(MSB) | RESERVED |
| 14 | RESERVED |
| 13 | RESERVED |
| 12 | RESERVED |
| 11 | CLEAR RT HALT |
| 10 | CLEAR SELF-TEST REGISTER |
| 9 | INITIATE RAM SELF-TEST |
| 8 | RESERVED |
| 7 | RESERVED |
| 6 | BC/MT STOP-ON-MESSAGE |
| 5 | BC STOP-ON-FRAME |
| 4 | TIME TAG TEST CLOCK |
| 3 | TIME TAG RESET |
| 2 | INTERRUPT RESET |
| 1 | BC/MT START |
| 0(LSB) | RESET |

| TABLE 23. BC/RT COMMAND STACK POINTER REG. (READ 03H, PCI 0CH) | |
|---|---|
| **BIT** | **DESCRIPTION** |
| 15(MSB) | COMMAND STACK POINTER 15 |
| • | • |
| • | • |
| • | • |
| 0(LSB) | COMMAND STACK POINTER 0 |

| TABLE 24. BC CONTROL WORD REGISTER (READ/WRITE 04H, PCI 10H) | |
|---|---|
| **BIT** | **DESCRIPTION** |
| 15(MSB) | RESERVED |
| 14 | MESSAGE ERROR MASK |
| 13 | SERVICE REQUEST BIT MASK |
| 12 | BUSY BIT MASK |
| 11 | SUBSYSTEM FLAG BIT MASK |
| 10 | TERMINAL FLAG BIT MASK |
| 9 | RESERVED BITS MASK |
| 8 | RETRY ENABLED |
| 7 | BUS CHANNEL A/$\overline{\text{B}}$ |
| 6 | OFF-LINE SELF-TEST |
| 5 | MASK BROADCAST BIT |
| 4 | EOM INTERRUPT ENABLE |
| 3 | 1553A/B SELECT |
| 2 | MODE CODE FORMAT |
| 1 | BROADCAST FORMAT |
| 0(LSB) | RT-to-RT FORMAT |

| TABLE 25. RT SUBADDRESS CONTROL WORD (READ 04H, PCI 10H) | |
|---|---|
| **BIT** | **DESCRIPTION** |
| 15(MSB) | RX: GLOBAL CIRCULAR BUFFER ENABLE |
| 14 | TX: EOM INT |
| 13 | TX: CIRC BUF INT |
| 12 | TX: MEMORY MANAGEMENT 2 (MM2) |
| 11 | TX: MEMORY MANAGEMENT 1 (MM1) |
| 10 | TX: MEMORY MANAGEMENT 0 (MM0) |
| 9 | RX: EOM INT |
| 8 | RX: CIRC BUF INT |
| 7 | RX: MEMORY MANAGEMENT 2 (MM2) |
| 6 | RX: MEMORY MANAGEMENT 1 (MM1) |
| 5 | RX: MEMORY MANAGEMENT 0 (MM0) |
| 4 | BCST: EOM INT |
| 3 | BCST: CIRC BUF INT |
| 2 | BCST: MEMORY MANAGEMENT 2 (MM2) |
| 1 | BCST: MEMORY MANAGEMENT 1 (MM1) |
| 0(LSB) | BCST: MEMORY MANAGEMENT 0 (MM0) |

| TABLE 26. TIME TAG REGISTER (READ/WRITE 05H, PCI 14H) | |
|---|---|
| **BIT** | **DESCRIPTION** |
| 15(MSB) | TIME TAG 15 |
| • | • |
| • | • |
| • | • |
| 0(LSB) | TIME TAG 0 |

| TABLE 27. INTERRUPT STATUS REGISTER #1 (READ/WRITE 06H, PCI 18H) | |
|---|---|
| **BIT** | **DESCRIPTION** |
| 15(MSB) | MASTER INTERRUPT |
| 14 | RAM PARITY ERROR |
| 13 | TRANSMITTER TIMEOUT |
| 12 | BC/RT COMMAND STACK ROLLOVER |
| 11 | MT COMMAND STACK ROLLOVER |
| 10 | MT DATA STACK ROLLOVER |
| 9 | HANDSHAKE FAILURE |
| 8 | BC RETRY |
| 7 | RT ADDRESS PARITY ERROR |
| 6 | TIME TAG ROLLOVER |
| 5 | RT CIRCULAR BUFFER ROLLOVER |
| 4 | RT SUBADDRESS CONTROL WORD EOM |
| 3 | BC END OF FRAME |
| 2 | FORMAT ERROR |
| 1 | BC STATUS SET / RT MODE CODE / MT PATTERN TRIGGER |
| 0(LSB) | END OF MESSAGE |

| TABLE 28. CONFIGURATION REGISTER #3 (READ/WRITE 07H, PCI 1CH) | |
|---|---|
| **BIT** | **DESCRIPTION** |
| 15(MSB) | ENHANCED MODE ENABLE |
| 14 | BC/RT COMMAND STACK SIZE 1 |
| 13 | BC/RT COMMAND STACK SIZE 0 |
| 12 | MT COMMAND STACK SIZE 1 |
| 11 | MT COMMAND STACK SIZE 0 |
| 10 | MT DATA STACK SIZE 2 |
| 9 | MT DATA STACK SIZE 1 |
| 8 | MT DATA STACK SIZE 0 |
| 7 | ILLEGALIZATION DISABLED |
| 6 | OVERRIDE MODE T/$\overline{R}$ ERROR |
| 5 | ALTERNATE STATUS WORD ENABLE |
| 4 | ILLEGAL RX TRANSFER DISABLE |
| 3 | RESERVED, set to zero |
| 2 | $\overline{RTFAIL}$ / $\overline{RTFLAG}$ WRAP ENABLE |
| 1 | 1553A MODE CODES ENABLE |
| 0(LSB) | ENHANCED MODE CODE HANDLING |

| TABLE 29. CONFIGURATION REGISTER #4 (READ/WRITE 08H, PCI 20H) | |
|---|---|
| **BIT** | **DESCRIPTION** |
| 15(MSB) | EXTERNAL BIT WORD ENABLE |
| 14 | INHIBIT BIT WORD IF BUSY |
| 13 | MODE COMMAND OVERRIDE BUSY |
| 12 | EXPANDED BC CONTROL WORD ENABLE |
| 11 | BROADCAST MASK ENA/$\overline{XOR}$ |
| 10 | RETRY IF -A AND M.E. |
| 9 | RETRY IF STATUS SET |
| 8 | 1ST RETRY ALT/$\overline{SAME}$ BUS |
| 7 | 2ND RETRY ALT/$\overline{SAME}$ BUS |
| 6 | VALID M.E./NO DATA |
| 5 | VALID BUSY/NO DATA |
| 4 | MT TAG GAP OPTION |
| 3 | LATCH RT ADDRESS WITH CONFIG #5 |
| 2 | TEST MODE 2 |
| 1 | TEST MODE 1 |
| 0(LSB) | TEST MODE 0 |

| TABLE 30. CONFIGURATION REGISTER #5 (READ/WRITE 09H, PCI 24H) | |
|---|---|
| **BIT** | **DESCRIPTION** |
| 15(MSB) | 12 / $\overline{16}$ MHZ CLOCK SELECT |
| 14 | SINGLE-ENDED SELECT |
| 13 | EXTERNAL TX INHIBIT A |
| 12 | EXTERNAL TX INHIBIT B |
| 11 | EXPANDED CROSSING ENABLED |
| 10 | RESPONSE TIMEOUT SELECT 1 |
| 9 | RESPONSE TIMEOUT SELECT 0 |
| 8 | GAP CHECK ENABLED |
| 7 | BROADCAST DISABLED |
| 6 | RT ADDRESS LATCH/$\overline{TRANSPARENT}$ |
| 5 | RT ADDRESS 4 |
| 4 | RT ADDRESS 3 |
| 3 | RT ADDRESS 2 |
| 2 | RT ADDRESS 1 |
| 1 | RT ADDRESS 0 |
| 0(LSB) | RT ADDRESS PARITY |

| TABLE 31. RT / MONITOR DATA STACK ADDRESS REGISTER (READ/WRITE 0AH, PCI 28H) | |
|---|---|
| **BIT** | **DESCRIPTION** |
| 15(MSB) | RT / MONITOR DATA STACK ADDRESS 15 |
| • | • |
| • | • |
| • | • |
| 0(LSB) | RT / MONITOR DATA STACK ADDRESS 0 |

| TABLE 32. BC FRAME TIME REMAINING REGISTER (READ/WRITE 0BH, PCI 2CH) | |
|---|---|
| **BIT** | **DESCRIPTION** |
| 15(MSB) | BC FRAME TIME REMAINING 15 |
| • | • |
| • | • |
| • | • |
| 0(LSB) | BC FRAME TIME REMAINING 0 |

**Note:** resolution = 100 μs per LSB

| TABLE 33. BC MESSAGE TIME REMAINING REGISTER (READ 0CH, PCI 30H) | |
|---|---|
| **BIT** | **DESCRIPTION** |
| 15(MSB) | BC MESSAGE TIME REMAINING 15 |
| • | • |
| • | • |
| • | • |
| 0(LSB) | BC MESSAGE TIME REMAINING 0 |

**Note:** resolution = 1 μs per LSB

| TABLE 34. BC FRAME TIME / RT LAST COMMAND / MT TRIGGER REGISTER (READ/WRITE 0DH, PCI 34H) | |
|---|---|
| **BIT** | **DESCRIPTION** |
| 15(MSB) | BIT 15 |
| • | • |
| • | • |
| • | • |
| 0(LSB) | BIT 0 |

| TABLE 35. RT STATUS WORD REGISTER (READ 0EH, PCI 38H) | |
|---|---|
| **BIT** | **DESCRIPTION** |
| 15(MSB) | LOGIC “0” |
| 14 | LOGIC “0” |
| 13 | LOGIC “0” |
| 12 | LOGIC “0” |
| 11 | LOGIC “0” |
| 10 | MESSAGE ERROR |
| 9 | INSTRUMENTATION |
| 8 | SERVICE REQUEST |
| 7 | RESERVED |
| 6 | RESERVED |
| 5 | RESERVED |
| 4 | BROADCAST COMMAND RECEIVED |
| 3 | BUSY |
| 2 | SSFLAG |
| 1 | DYNAMIC BUS CONTROL ACCEPT |
| 0(LSB) | TERMINAL FLAG |

| TABLE 36. RT BIT WORD REGISTER (READ 0FH, PCI 3CH) | |
|---|---|
| **BIT** | **DESCRIPTION** |
| 15(MSB) | TRANSMITTER TIMEOUT |
| 14 | LOOP TEST FAILURE B |
| 13 | LOOP TEST FAILURE A |
| 12 | HANDSHAKE FAILURE |
| 11 | TRANSMITTER SHUTDOWN B |
| 10 | TRANSMITTER SHUTDOWN A |
| 9 | TERMINAL FLAG INHIBITED |
| 8 | BIT TEST FAIL |
| 7 | HIGH WORD COUNT |
| 6 | LOW WORD COUNT |
| 5 | INCORRECT SYNC RECEIVED |
| 4 | PARITY / MANCHESTER ERROR RECEIVED |
| 3 | RT-to-RT GAP / SYNC / ADDRESS ERROR |
| 2 | RT-to-RT NO RESPONSE ERROR |
| 1 | RT-to-RT 2ND COMMAND WORD ERROR |
| 0(LSB) | COMMAND WORD CONTENTS ERROR |

| TABLE 37. CONFIGURATION REGISTER #6 (READ/WRITE 18H, PCI 60H) | |
|---|---|
| **BIT** | **DESCRIPTION** |
| 15(MSB) | ENHANCED BUS CONTROLLER |
| 14 | ENHANCED CPU ACCESS |
| 13 | COMMAND STACK POINTER INCREMENT ON EOM (RT, MT) |
| 12 | GLOBAL CIRCULAR BUFFER ENABLE |
| 11 | GLOBAL CIRCULAR BUFFER SIZE 2 |
| 10 | GLOBAL CIRCULAR BUFFER SIZE 1 |
| 9 | GLOBAL CIRCULAR BUFFER SIZE 0 |
| 8 | DISABLE INVALID MESSAGES TO INTERRUPT STATUS QUEUE |
| 7 | DISABLE VALID MESSAGES TO INTERRUPT STATUS QUEUE |
| 6 | INTERRUPT STATUS QUEUE ENABLE |
| 5 | RT ADDRESS SOURCE |
| 4 | ENHANCED MESSAGE MONITOR |
| 3 | RESERVED |
| 2 | 64-WORD REGISTER SPACE |
| 1 | CLOCK SELECT 1 |
| 0(LSB) | CLOCK SELECT 0 |

| TABLE 38. CONFIGURATION REGISTER #7 (READ/WRITE 19H, PCI 64H) | |
|---|---|
| **BIT** | **DESCRIPTION** |
| 15(MSB) | MEMORY MANAGEMENT BASE ADDRESS 15 |
| 14 | MEMORY MANAGEMENT BASE ADDRESS 14 |
| 13 | MEMORY MANAGEMENT BASE ADDRESS 13 |
| 12 | MEMORY MANAGEMENT BASE ADDRESS 12 |
| 11 | MEMORY MANAGEMENT BASE ADDRESS 11 |
| 10 | MEMORY MANAGEMENT BASE ADDRESS 10 |
| 9 | RESERVED |
| 8 | RESERVED |
| 7 | RESERVED |
| 6 | RESERVED |
| 5 | RESERVED |
| 4 | RT HALT ENABLE |
| 3 | 1553B RESPONSE TIME |
| 2 | ENHANCED TIMETAG SYNCHRONIZE |
| 1 | ENHANCED BC WATCHDOG TIMER ENABLED |
| 0(LSB) | MODE CODE RESET / $\overline{\text{INCMD}}$ SELECT |

| TABLE 39. BC CONDITION CODE REGISTER (READ 1BH, PCI 6CH) | |
|---|---|
| **BIT** | **DESCRIPTION** |
| 15(MSB) | ALWAYS |
| 14 | RETRY 1 |
| 13 | RETRY 0 |
| 12 | BAD MESSAGE |
| 11 | MESSAGE STATUS SET |
| 10 | GOOD BLOCK TRANSFER |
| 9 | FORMAT ERROR |
| 8 | NO RESPONSE |
| 7 | GENERAL PURPOSE FLAG 7 |
| 6 | GENERAL PURPOSE FLAG 6 |
| 5 | GENERAL PURPOSE FLAG 5 |
| 4 | GENERAL PURPOSE FLAG 4 |
| 3 | GENERAL PURPOSE FLAG 3 |
| 2 | GENERAL PURPOSE FLAG 2 |
| 1 | LESS THAN FLAG / GENERAL PURPOSE FLAG 1 |
| 0(LSB) | EQUAL FLAG / GENERAL PURPOSE FLAG 1 |

| TABLE 40. BC GENERAL PURPOSE FLAG REGISTER (WRITE 1BH, PCI 6CH) | |
|---|---|
| **BIT** | **DESCRIPTION** |
| 15(MSB) | CLEAR GENERAL PURPOSE FLAG 7 |
| 14 | CLEAR GENERAL PURPOSE FLAG 6 |
| 13 | CLEAR GENERAL PURPOSE FLAG 5 |
| 12 | CLEAR GENERAL PURPOSE FLAG 4 |
| 11 | CLEAR GENERAL PURPOSE FLAG 3 |
| 10 | CLEAR GENERAL PURPOSE FLAG 2 |
| 9 | CLEAR GENERAL PURPOSE FLAG 1 |
| 8 | CLEAR GENERAL PURPOSE FLAG 0 |
| 7 | SET GENERAL PURPOSE FLAG 7 |
| 6 | SET GENERAL PURPOSE FLAG 6 |
| 5 | SET GENERAL PURPOSE FLAG 5 |
| 4 | SET GENERAL PURPOSE FLAG 4 |
| 3 | SET GENERAL PURPOSE FLAG 3 |
| 2 | SET GENERAL PURPOSE FLAG 2 |
| 1 | SET GENERAL PURPOSE FLAG 1 |
| 0(LSB) | SET GENERAL PURPOSE FLAG 0 |

| TABLE 41. BIT TEST STATUS REGISTER (READ 1CH, PCI 70H) | |
|---|---|
| **BIT** | **DESCRIPTION** |
| 15(MSB) | LOGIC “0” |
| 14 | LOGIC “0” |
| 13 | LOGIC “0” |
| 12 | LOGIC “0” |
| 11 | LOGIC “0” |
| 10 | LOGIC “0” |
| 9 | LOGIC “0” |
| 8 | LOGIC “0” |
| 7 | RAM BUILT-IN TEST COMPLETE |
| 6 | RAM BUILT-IN TEST IN-PROGRESS |
| 5 | RAM BUILT-IN TEST PASSED |
| 4 | LOGIC “0” |
| 3 | LOGIC “0” |
| 2 | LOGIC “0” |
| 1 | LOGIC “0” |
| 0(LSB) | LOGIC “0” |

| TABLE 42. INTERRUPT MASK REGISTER #2 (READ/WRITE 1DH, PCI 74H) | |
|---|---|
| **BIT** | **DESCRIPTION** |
| 15(MSB) | NOT USED |
| 14 | BC OP CODE PARITY ERROR |
| 13 | ILLEGAL COMMAND |
| 12 | GENERAL PURPOSE QUEUE / INTERRUPT STATUS QUEUE ROLLOVER |
| 11 | CALL STACK POINTER REGISTER ERROR |
| 10 | BC TRAP OP CODE |
| 9 | RT COMMAND STACK 50% ROLLOVER |
| 8 | RT CIRCULAR BUFFER 50% ROLLOVER |
| 7 | MONITOR COMMAND STACK 50% ROLLOVER |
| 6 | MONITOR DATA STACK 50% ROLLOVER |
| 5 | ENHANCED BC IRQ3 |
| 4 | ENHANCED BC IRQ2 |
| 3 | ENHANCED BC IRQ1 |
| 2 | ENHANCED BC IRQ0 |
| 1 | BIT TEST COMPLETE |
| 0(LSB) | NOT USED |

| TABLE 43. INTERRUPT STATUS REGISTER #2 (READ 1EH, PCI 78H) | |
|---|---|
| **BIT** | **DESCRIPTION** |
| 15(MSB) | MASTER INTERRUPT |
| 14 | BC OP CODE PARITY ERROR |
| 13 | ILLEGAL COMMAND |
| 12 | GENERAL PURPOSE QUEUE / INTERRUPT STATUS QUEUE ROLLOVER |
| 11 | CALL STACK POINTER REGISTER ERROR |
| 10 | BC TRAP OP CODE |
| 9 | RT COMMAND STACK 50% ROLLOVER |
| 8 | RT CIRCULAR BUFFER 50% ROLLOVER |
| 7 | MONITOR COMMAND STACK 50% ROLLOVER |
| 6 | MONITOR DATA STACK 50% ROLLOVER |
| 5 | ENHANCED BC IRQ3 |
| 4 | ENHANCED BC IRQ2 |
| 3 | ENHANCED BC IRQ1 |
| 2 | ENHANCED BC IRQ0 |
| 1 | BIT TEST COMPLETE |
| 0(LSB) | INTERRUPT CHAIN BIT |

| TABLE 44. BC GENERAL PURPOSE QUEUE POINTER REGISTER RT, MT INTERRUPT STATUS QUEUE POINTER REGISTER (READ/WRITE 1FH, PCI 7CH) | |
|---|---|
| **BIT** | **DESCRIPTION** |
| 15(MSB) | QUEUE POINTER BASE ADDRESS 15 |
| 14 | QUEUE POINTER BASE ADDRESS 14 |
| 13 | QUEUE POINTER BASE ADDRESS 13 |
| 12 | QUEUE POINTER BASE ADDRESS 12 |
| 11 | QUEUE POINTER BASE ADDRESS 11 |
| 10 | QUEUE POINTER BASE ADDRESS 10 |
| 9 | QUEUE POINTER BASE ADDRESS 9 |
| 8 | QUEUE POINTER BASE ADDRESS 8 |
| 7 | QUEUE POINTER BASE ADDRESS 7 |
| 6 | QUEUE POINTER BASE ADDRESS 6 |
| 5 | QUEUE POINTER BASE ADDRESS 5 |
| 4 | QUEUE POINTER BASE ADDRESS 4 |
| 3 | QUEUE POINTER BASE ADDRESS 3 |
| 2 | QUEUE POINTER BASE ADDRESS 2 |
| 1 | QUEUE POINTER BASE ADDRESS 1 |
| 0(LSB) | QUEUE POINTER BASE ADDRESS 0 |

**NOTE: TABLES 45 TO 51 ARE NOT REGISTERS, BUT THEY ARE WORDS STORED IN RAM.**

**TABLE 45. BC MODE BLOCK STATUS WORD**

| BIT | DESCRIPTION |
|---|---|
| 15(MSB) | EOM |
| 14 | SOM |
| 13 | CHANNEL B/$\overline{A}$ |
| 12 | ERROR FLAG |
| 11 | STATUS SET |
| 10 | FORMAT ERROR |
| 9 | NO RESPONSE TIMEOUT |
| 8 | LOOP TEST FAIL |
| 7 | MASKED STATUS SET |
| 6 | RETRY COUNT 1 |
| 5 | RETRY COUNT 0 |
| 4 | GOOD DATA BLOCK TRANSFER |
| 3 | WRONG STATUS ADDRESS / NO GAP |
| 2 | WORD COUNT ERROR |
| 1 | INCORRECT SYNC TYPE |
| 0(LSB) | INVALID WORD |

**TABLE 46. RT MODE BLOCK STATUS WORD**

| BIT | DESCRIPTION |
|---|---|
| 15(MSB) | EOM |
| 14 | SOM |
| 13 | CHANNEL B/$\overline{A}$ |
| 12 | ERROR FLAG |
| 11 | RT-to-RT FORMAT |
| 10 | FORMAT ERROR |
| 9 | NO RESPONSE TIMEOUT |
| 8 | LOOP TEST FAIL |
| 7 | DATA STACK ROLLOVER |
| 6 | ILLEGAL COMMAND WORD |
| 5 | WORD COUNT ERROR |
| 4 | INCORRECT DATA SYNC |
| 3 | INVALID WORD |
| 2 | RT-to-RT GAP / SYNC / ADDRESS ERROR |
| 1 | RT-to-RT 2ND COMMAND ERROR |
| 0(LSB) | COMMAND WORD CONTENTS ERROR |

**TABLE 47. 1553 COMMAND WORD**

| BIT | DESCRIPTION |
|---|---|
| 15(MSB) | REMOTE TERMINAL ADDRESS BIT 4 |
| 14 | REMOTE TERMINAL ADDRESS BIT 3 |
| 13 | REMOTE TERMINAL ADDRESS BIT 2 |
| 12 | REMOTE TERMINAL ADDRESS BIT 1 |
| 11 | REMOTE TERMINAL ADDRESS BIT 0 |
| 10 | TRANSMIT / $\overline{\text{RECEIVE}}$ |
| 9 | SUBADDRESS / MODE CODE BIT 4 |
| 8 | SUBADDRESS / MODE CODE BIT 3 |
| 7 | SUBADDRESS / MODE CODE BIT 2 |
| 6 | SUBADDRESS / MODE CODE BIT 1 |
| 5 | SUBADDRESS / MODE CODE BIT 0 |
| 4 | DATA WORD COUNT / MODE CODE BIT 4 |
| 3 | DATA WORD COUNT / MODE CODE BIT 3 |
| 2 | DATA WORD COUNT / MODE CODE BIT 2 |
| 1 | DATA WORD COUNT / MODE CODE BIT 1 |
| 0(LSB) | DATA WORD COUNT / MODE CODE BIT 0 |

**TABLE 48. WORD MONITOR IDENTIFICATION WORD**

| BIT | DESCRIPTION |
|---|---|
| 15(MSB) | GAP TIME (MSB) |
| • | • |
| • | • |
| • | • |
| 8 | GAP TIME (LSB) |
| 7 | WORD FLAG |
| 6 | $\overline{\text{THIS RT}}$ |
| 5 | $\overline{\text{BROADCAST}}$ |
| 4 | ERROR |
| 3 | COMMAND / $\overline{\text{DATA}}$ |
| 2 | CHANNEL B/$\overline{A}$ |
| 1 | CONTIGUOUS DATA / $\overline{\text{GAP}}$ |
| 0(LSB) | $\overline{\text{MODE\_CODE}}$ |

## TABLE 49. MESSAGE MONITOR MODE BLOCK STATUS WORD

| BIT | DESCRIPTION |
|---|---|
| 15(MSB) | EOM |
| 14 | SOM |
| 13 | CHANNEL B/$\overline{A}$ |
| 12 | ERROR FLAG |
| 11 | RT-to-RT TRANSFER |
| 10 | FORMAT ERROR |
| 9 | NO RESPONSE TIMEOUT |
| 8 | GOOD DATA BLOCK TRANSFER |
| 7 | DATA STACK ROLLOVER |
| 6 | RESERVED |
| 5 | WORD COUNT ERROR |
| 4 | INCORRECT SYNC |
| 3 | INVALID WORD |
| 2 | RT-to-RT GAP / SYNC / ADDRESS ERROR |
| 1 | RT-to-RT 2ND COMMAND ERROR |
| 0(LSB) | COMMAND WORD CONTENTS ERROR |

## TABLE 50. 1553B STATUS WORD

| BIT | DESCRIPTION |
|---|---|
| 15(MSB) | REMOTE TERMINAL ADDRESS BIT 4 |
| 14 | REMOTE TERMINAL ADDRESS BIT 3 |
| 13 | REMOTE TERMINAL ADDRESS BIT 2 |
| 12 | REMOTE TERMINAL ADDRESS BIT 1 |
| 11 | REMOTE TERMINAL ADDRESS BIT 0 |
| 10 | MESSAGE ERROR |
| 9 | INSTRUMENTATION |
| 8 | SERVICE REQUEST |
| 7 | RESERVED |
| 6 | RESERVED |
| 5 | RESERVED |
| 4 | BROADCAST COMMAND RECEIVED |
| 3 | BUSY |
| 2 | SSFLAG |
| 1 | DYNAMIC BUS CONTROL ACCEPTANCE |
| 0(LSB) | TERMINAL FLAG |

## TABLE 51. RT/MONITOR INTERRUPT STATUS WORD (FOR INTERRUPT STATUS QUEUE)

| BIT | DEFINITION FOR MESSAGE INTERRUPT EVENT | DEFINITION FOR NON-MESSAGE INTERRUPT EVENT |
|---|---|---|
| 15 | TRANSMITTER TIMEOUT | NOT USED |
| 14 | ILLEGAL COMMAND | NOT USED |
| 13 | MONITOR DATA STACK 50% ROLLOVER | NOT USED |
| 12 | MONITOR DATA STACK ROLLOVER | NOT USED |
| 11 | RT CIRCULAR BUFFER 50% ROLLOVER | NOT USED |
| 10 | RT CIRCULAR BUFFER ROLLOVER | NOT USED |
| 9 | MONITOR COMMAND (DESCRIPTOR) STACK 50% ROLLOVER | NOT USED |
| 8 | MONITOR COMMAND (DESCRIPTOR) STACK ROLLOVER | NOT USED |
| 7 | RT COMMAND (DESCRIPTOR) STACK 50% ROLLOVER | NOT USED |
| 6 | RT COMMAND (DESCRIPTOR) STACK ROLLOVER | NOT USED |
| 5 | HANDSHAKE FAIL | NOT USED |
| 4 | FORMAT ERROR | TIME TAG ROLLOVER |
| 3 | MODE CODE INTERRUPT | RT ADDRESS PARITY ERROR |
| 2 | SUBADDRESS CONTROL WORD EOM | NOT USED |
| 1 | END-OF-MESSAGE (EOM) | RAM PARITY ERROR |
| 0 | “1” FOR MESSAGE INTERRUPT EVENT<br>“0” FOR NON-MESSAGE INTERRUPT EVENT | |

## NON-TEST REGISTER FUNCTION SUMMARY

A summary of the PCI Enhanced Mini-ACE's 24 non-test registers follows.

### INTERRUPT MASK REGISTERS #1 AND #2

Interrupt Mask Registers #1 and #2 are used to enable and disable interrupt requests for various events and conditions.

> NOTE: Please see Appendix "F" of the Enhanced Mini-ACE Users Guide for important information applicable only to RT MODE operation, enabling of the interrupt status queue and use of specific non-message interrupts.

### CONFIGURATION REGISTERS #1 AND #2

Configuration Registers #1 and #2 are used to select the PCI Enhanced Mini-ACE's mode of operation, and for software control of RT Status Word bits, Active Memory Area, BC Stop-On-Error, RT Memory Management mode selection, and control of the Time Tag operation. Note that the LEVEL/$\overline{\text{PULSE}}$ INTERRUPT REQUEST bit in Configuration Register #2 MUST be set to 1 for correct PCI operation.

### START/RESET REGISTER

The Start/Reset Register is used for "command" type functions such as software reset, BC/MT Start, Interrupt reset, Time Tag Reset, Time Tag Register Test, Initiate RAM self-test, Clear self-test register, and Clear RT Halt. The Start/Reset Register also includes provisions for stopping the BC in its auto-repeat mode, either at the end of the current message or at the end of the current BC frame.

### BC/RT COMMAND STACK REGISTER

The BC/RT Command Stack Register allows the host CPU to determine the pointer location for the current or most recent message.

### BC INSTRUCTION LIST POINTER REGISTER

The BC Instruction List Pointer Register may be read to determine the current location of the Instruction List Pointer for the Enhanced BC mode.

### BC CONTROL WORD/RT SUBADDRESS CONTROL WORD REGISTER

In BC mode, the BC Control Word/RT Subaddress Control Word Register allows host access to the current word or most recent BC Control Word. The BC Control Word contains bits that select the active bus and message format, enable off-line self-test, masking of Status Word bits, enable retries and interrupts, and specify MIL-STD-1553A or -1553B error handling. In RT mode, this register allows host access to the current or most recent Subaddress Control Word. The Subaddress Control Word is used to select the memory management scheme and enable interrupts for the current message.

### TIME TAG REGISTER

The Time Tag Register maintains the value of a real-time clock. The resolution of this register is programmable from among 2, 4, 8, 16, 32, and 64 µs/LSB. The Start-of-Message (SOM) and End-of-Message (EOM) sequences in BC, RT, and Message Monitor modes cause a write of the current value of the Time Tag Register to the stack area of the RAM.

### INTERRUPT STATUS REGISTERS #1 AND #2

Interrupt Status Registers #1 and #2 allow the host processor to determine the cause of an interrupt request by means of one or two read accesses. The interrupt events of the two Interrupt Status Registers are mapped to correspond to the respective bit positions in the two Interrupt Mask Registers. Interrupt Status Register #2 contains an INTERRUPT CHAIN bit, used to indicate an interrupt event from Interrupt Status Register #1.

### CONFIGURATION REGISTERS #3, #4, AND #5

Configuration Registers #3, #4, and #5 are used to enable many of the PCI Enhanced Mini-ACE's advanced features that were implemented by the prior generation products, the ACE and Mini-ACE (Plus). For BC, RT, and MT modes, use of the ENHANCED MODE enables the various read-only bits in Configuration Register #1. For BC mode, ENHANCED mode features include the expanded BC Control Word and BC Block Status Word, additional Stop-On-Error and Stop-On-Status Set functions, frame auto-repeat, programmable intermessage gap times, automatic retries, expanded Status Word Masking, and the capability to generate interrupts following the completion of any selected message. For RT mode, the enhanced mode features include the expanded RT Block Status Word, combined RT/Selective Message Monitor mode, internal wrapping of the $\overline{\text{RTFAIL}}$ output signal to the $\overline{\text{RTFLAG}}$ RT Status Word bit, and the alternate (fully software programmable) RT Status Word. For MT mode, use of the enhanced mode enables the Selective Message Monitor, the combined RT/Selective Monitor modes, and the monitor triggering capability.

### RT/MONITOR DATA STACK ADDRESS REGISTER

The RT/Monitor Data Stack Address Register provides a read/writable indication of the last data word stored for RT or Monitor modes.

### BC FRAME TIME REMAINING REGISTER

The BC Frame Time Remaining Register provides a read-only indication of the time remaining in the current BC frame. In the enhanced BC mode, this timer may be used for minor or major frame control, or as a watchdog timer for the BC message sequence control processor. The resolution of this register is 100 µs/LSB.

### BC TIME REMAINING TO NEXT MESSAGE REGISTER

The BC Time Remaining to Next Message Register provides a read-only indication of the time remaining before the start of the next message in a BC frame. In the enhanced BC mode, this timer may also be used for the BC message sequence control processor's Delay (DLY) instruction, or for minor or major frame control. The resolution of this register is 1 µs/LSB.

### BC FRAME TIME/RT LAST COMMAND/MT TRIGGER WORD REGISTER

In BC mode, this register is used to program the BC frame time, for use in the frame auto-repeat mode. The resolution of this register is 100 µs/LSB, with a range up to 6.55 seconds. In RT mode, this register stores the current (or most previous) 1553 Command Word processed by the PCI Enhanced Mini-ACE RT. In the Word Monitor mode, this register is used to specify a 16-bit Trigger (Command) Word. The Trigger Word may be used to start or stop the monitor, or to generate interrupts.

### BC INITIAL INSTRUCTION LIST POINTER REGISTER

The BC Initial Instruction List Pointer Register enables the host to assign the starting address for the enhanced BC Instruction List.

### RT STATUS WORD REGISTER AND BIT WORD REGISTERS

The RT Status Word Register and BIT Word Registers provide read-only indications of the RT Status and BIT Words.

### TEST MODE REGISTERS 0-7

These registers are included for factory test. In normal operation, these registers do not need to be accessed by the host processor.

### CONFIGURATION REGISTERS #6 AND #7

Configuration Registers #6 and #7 are used to enable the PCI Enhanced Mini-ACE features that extend beyond the architecture of the ACE/Mini-ACE (Plus). These include the Enhanced BC mode; Enhanced CPU Access (note that this bit is the only configuration bit that is SET after reset), RT Global Circular Buffer (including buffer size); the RT/MT Interrupt Status Queue, including valid/invalid message filtering; enabling a software-assigned RT address; clock frequency selection; a base address for the "non-data" portion of PCI Enhanced Mini-ACE memory; LSB filtering for the Synchronize (with data) time tag operations; and enabling a watchdog timer for the Enhanced BC message sequence control engine.

NOTE: Please see Appendix “F” of the Enhanced Mini-ACE Users Guide for important information applicable only to RT MODE operation, enabling of the interrupt status queue and use of specific non-message interrupts.

### BC CONDITION CODE REGISTER

The BC Condition Code Register is used to enable the host processor to read the current value of the Enhanced BC Message Sequence Control Engine's condition flags.

### BC GENERAL PURPOSE FLAG REGISTER

The BC General Purpose Flag Register allows the host processor to be able to set, clear, or toggle any of the Enhanced BC Message Sequence Control Engine's General Purpose condition flags.

### BIT TEST STATUS REGISTER

The BIT Test Status Register is used to provide read-only access of the status of the RAM built-in self-tests (BIT).

### BC GENERAL PURPOSE QUEUE POINTER

The BC General Purpose Queue Pointer provides a means for initializing the pointer for the General Purpose Queue, for the Enhanced BC mode. In addition, this register enables the host to determine the current location of the General Purpose Queue pointer, which is incremented internally by the Enhanced BC message sequence control engine.

### RT/MT INTERRUPT STATUS QUEUE POINTER REGISTER

The RT/MT Interrupt Status Queue Pointer Register provides a means for initializing the pointer for the Interrupt Status Queue, for RT, MT, and RT/MT modes. In addition, this register enables the host to determine the current location of the Interrupt Status Queue pointer, which is incremented internally by the RT/MT message processor.

## BUS CONTROLLER (BC) ARCHITECTURE

The BC functionality for the PCI Enhanced Mini-ACE includes two separate architectures: (1) the older, non-Enhanced mode, which provides complete compatibility with the previous ACE and Mini-ACE (Plus) generation products; and (2) the newer, Enhanced BC mode. The Enhanced BC mode offers several new powerful architectural features. These include the incorporation of a highly autonomous BC message sequence control engine, which greatly serves to offload the operation of the host CPU.

The Enhanced BC's message sequence control engine provides a high degree of flexibility for implementing major and minor frame scheduling; capabilities for inserting asynchronous messages in the middle of a frame; to separate 1553 message data from control/status data for the purpose of implementing double buffering and performing bulk data transfers; for implementing message retry schemes, including the capability for automatic bus channel switchover for failed messages; and for reporting various conditions to the host processor by means of 4 user-defined interrupts and a general purpose queue.

In both the non-Enhanced and Enhanced BC modes, the PCI Enhanced Mini-ACE BC implements all MIL-STD-1553B message formats. Message format is programmable on a message-by-message basis by means of the BC Control Word and the T/$\overline{R}$ bit of the Command Word for the respective message. The BC Control Word allows 1553 message format, 1553A/B type RT, bus channel, self-test, and Status Word masking to be specified on an individual message basis. In addition, automatic retries and/or interrupt requests may be enabled or disabled for individual messages. The BC performs all error checking required by MIL-STD-1553B. This includes validation of response time, sync type and sync encoding, Manchester II encoding, parity, bit count, word count, Status Word RT Address field, and various RT-to-RT transfer errors. The PCI Enhanced Mini-ACE BC response timeout value is programmable with choices of 18, 22, 50, and 130 µs. The longer response timeout values allow for operation over long buses and/or use of the repeaters.

In its non-Enhanced mode, the PCI Enhanced Mini-ACE may be programmed to process BC frames of up to 512 messages with no processor intervention. In the Enhanced BC mode, there is no explicit limit to the number of messages that may be processed in a frame. In both modes, it is possible to program for either single frame or frame auto-repeat operation. In the auto-repeat mode, the frame repetition rate may be controlled either internally, using a programmable BC frame timer, or from an external trigger input.

## ENHANCED BC MODE: MESSAGE SEQUENCE CONTROL

One of the major new architectural features of the PCI Enhanced Mini-ACE series is its advanced capability for BC message sequence control. The PCI Enhanced Mini-ACE supports highly autonomous BC operation, which greatly offloads the operation of the host processor.

The operation of the PCI Enhanced Mini-ACE's message sequence control engine is illustrated in FIGURE 2. The BC message sequence control involves an instruction list pointer register; an instruction list which contains multiple 2-word entries; a message control/status stack, which contains multiple 8-word or 10-word descriptors; and data blocks for individual messages.

The initial value of the instruction list pointer register is initialized by the host processor (via Register 0D), and is incremented by the BC message sequence processor (host readable via Register 03). During operation, the message sequence control processor fetches the operation referenced by the instruction list pointer register from the instruction list.

Note that the pointer parameter referencing the first word of a message's control/status block (the BC Control Word) must contain an address value that is **modulo 8**. Also, note that if the message is an RT-to-RT transfer, the pointer parameter must contain an address value that is **modulo 16**.

## OP CODES

The instruction list pointer register references a pair of words in the BC instruction list: an op code word, followed by a parameter word. The format of the op code word, which is illustrated in FIGURE 3, includes a 5-bit op code field and a 5-bit condition code field. The op code identifies the instruction to be executed by the BC message sequence controller.

Most of the operations are conditional, with execution dependent on the contents of the condition code field. Bits 3-0 of the condition code field identify the particular condition. Bit 4 of the condition code field identifies the logic sense ("1" or "0") of the selected condition code on which the conditional execution is dependent. TABLE 52 lists all the op codes, along with their

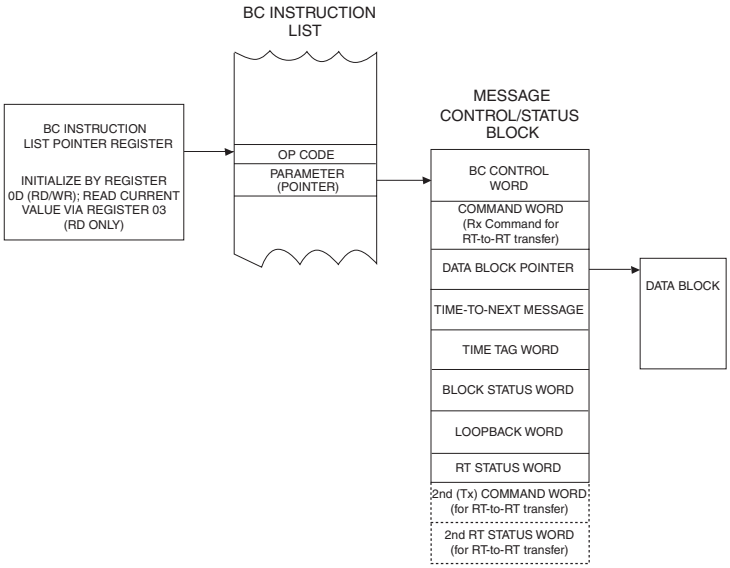



**FIGURE 2. BC MESSAGE SEQUENCE CONTROL**

respective mnemonic, code value, parameter, and description. TABLE 53 defines all the condition codes.

Eight of the condition codes (8 through F) are set or cleared as the result of the most recent message. The other eight are defined as "General Purpose" condition codes GP0 through GP7. There are three mechanisms for programming the values of the General Purpose Condition Code bits: (1) They may be set, cleared, or toggled by the host processor, by means of the BC GENERAL PURPOSE FLAG REGISTER; (2) they may be set, cleared, or toggled by the BC message sequence control processor, by means of the GP Flag Bits (FLG) instruction; and (3) GP0 and GP1 only (but none of the others) may be set or cleared by means of the BC message sequence control processor's Compare Frame Timer (CFT) or Compare Message Timer (CMT) instructions.

The host processor also has read-only access to the BC condition codes by means of the BC CONDITION CODE REGISTER.

Note that four (4) instructions are unconditional. These are Compare to Frame Timer (CFT), Compare to Message Timer (CMT), GP Flag Bits (FLG), and Execute and Flip (XQF). For these instructions, the Condition Code Field is "don't care". That is, these instructions are always executed, regardless of the result of the condition code test.

All other instructions are conditional. That is, they will only be executed if the condition code specified by the condition code field in the op code word tests true. If the condition code field tests false, the instruction list pointer will skip down to the next instruction.

As shown in TABLE 52, many of the operations include a single-word parameter. For an XEQ (execute message) operation, the parameter is a pointer to the start of the message's control/status block. For other operations, the parameter may be an address, a time value, an interrupt pattern, a mechanism to set or clear general purpose flag bits, or an immediate value. For several op codes, the parameter is "don't care" (not used).

As described above, some of the op codes will cause the message sequence control processor to execute messages. In this case, the parameter references the first word of a message control/status block. With the exception of RT-to-RT transfer messages, all message status/control blocks are eight words long: a block control word, time-to-next-message parameter, data block pointer, command word, status word, loopback word, block status word, and time tag word.

In the case of an RT-to-RT transfer message, the size of the message control/status block increases to 16 words. However, in this case, the last six words are not used; the ninth and tenth words are for the second command word and second status word.

The third word in the message control/status block is a pointer that references the first word of the message's data word block. Note that the data word block stores only data words, which are to be either transmitted or received by the BC. By segregating data words from command words, status words, and other control and "housekeeping" functions, this architecture enables the use of convenient, usable data structures, such as circular buffers and double buffers.

Other operations support program flow control; i.e., jump and call capability. The call capability includes maintenance of a call stack which supports a maximum of four (4) entries; there is also a return instruction. In the case of a call stack overrun or underrun, the BC will issue a CALL STACK POINTER REGISTER ERROR interrupt, if enabled.

Other op codes may be used to delay for a specified time; start a new BC frame; wait for an external trigger to start a new frame; do comparisons based on frame time and time-to-next message; load the time tag or frame time registers; halt; and issue host interrupts. In the case of host interrupts, the message control processor passes a 4-bit user-defined interrupt vector to the host, by means of the PCI Enhanced Mini-ACE's Interrupt Status Register.

The purpose of the FLG instruction is to enable the message sequence controller to set, clear, or toggle the value(s) of any or all of the eight general purpose condition flags.

The op code parity bit encompasses all sixteen bits of the op code word. This bit must be programmed for odd parity. If the message sequence control processor fetches an undefined op code word, an op code word with even parity, or bits 9-5 of an op code word do not have a binary pattern of 01010, the message sequence control processor will immediately halt the BC's operation. In addition, if enabled, a BC TRAP OP CODE interrupt will be issued. Also, if enabled, a parity error will result in an OP CODE PARITY ERROR interrupt. TABLE 53 describes the Condition Codes.

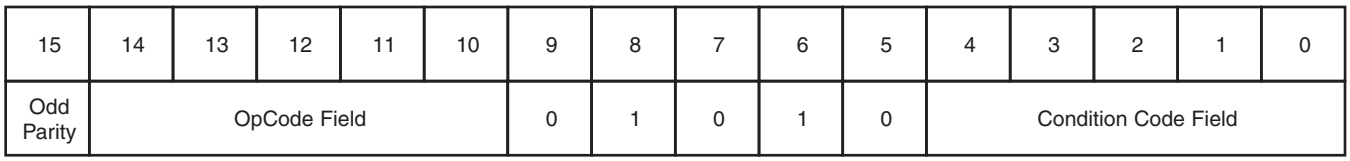



**FIGURE 3. BC OP CODE FORMAT**

| TABLE 52. BC OPERATIONS FOR MESSAGE SEQUENCE CONTROL | | | | | |
|---|---|---|---|---|---|
| **INSTRUCTION** | **MNEMONIC** | **OP CODE (HEX)** | **PARAMETER** | **CONDITIONAL OR UNCONDITIONAL** | **DESCRIPTION** |
| Execute Message | XEQ | 0001 | Message Control / Status Block Address | Conditional (See Note) | Executes the message at the specified Message Control/Status Block Address if the condition flag tests TRUE, otherwise continue execution at the next OpCode in the instruction list. |
| Jump | JMP | 0002 | Instruction List Address | Conditional | Jump to the OpCode specified in the Instruction List if the condition flag tests TRUE, otherwise continue execution at the next OpCode in the instruction list. |
| Subroutine Call | CAL | 0003 | Instruction List Address | Conditional | Jump to the OpCode specified by the Instruction List Address and push the Address of the Next OpCode on the Call Stack if the condition flag tests TRUE, otherwise continue execution at the next OpCode in the instruction list. Note that the maximum depth of the subroutine call stack is **four**. |
| Subroutine Return | RTN | 0004 | Not Used (Don't Care) | Conditional | Return to the OpCode popped off the Call Stack if the condition flag tests TRUE, otherwise continue execution at the next OpCode in the instruction list. |
| Interrupt Request | IRQ | 0006 | Interrupt Bit Pattern in 4 LS bits | Conditional | Generate an interrupt if the condition flag tests TRUE, otherwise continue execution at the next OpCode in the instruction list. The passed parameter (Interrupt Bit Pattern) specifies which of the ENHANCED BC IRQ bit(s) (bits 5-2) will be set in Interrupt Status Register #2. Only the four LSBs of the passed parameter are used. A parameter where the four LSBs are logic "0" will **not** generate an interrupt. |
| Halt | HLT | 0007 | Not Used (Don't Care) | Conditional | Stop execution of the Message Sequence Control Program until a new BC Start is issued by the host if the condition flag tests TRUE, otherwise continue execution at the next OpCode in the instruction list. |
| Delay | DLY | 0008 | Delay Time Value (Resolution = 1µS / LSB) | Conditional | Delay the time specified by the Time parameter before executing the next OpCode if the condition flag tests TRUE, otherwise continue execution at the next OpCode without delay. The delay generated will use the Time to Next Message Timer. |
| Wait Until Frame Timer = 0 | WFT | 0009 | Not Used (Don't Care) | Conditional | Wait until Frame Time counter is equal to Zero before continuing execution of the Message Sequence Control Program if the condition flag tests TRUE, otherwise continue execution at the next OpCode without delay. |
| Compare to Frame Timer | CFT | 000A | Delay Time Value (Resolution = 100µS / LSB) | Unconditional | Compare Time Value to Frame Time Counter. The LT/GP0 and EQ/GP1 flag bits are set or cleared based on the results of the compare. If the value of the CFT's parameter is less than the value of the frame time counter, then the LT/GP0 and NE/$\overline{GP1}$ flags will be set, while the GT-EQ/$\overline{GP0}$ and EQ/GP1 flags will be cleared. If the value of the CFT's parameter is equal to the value of the frame time counter, then the GT-EQ/$\overline{GP0}$ and EQ/GP1 flags will be set, while the LT/GP0 and NE/$\overline{GP1}$ flags will be cleared. If the value of the CFT's parameter is greater than the current value of the frame time counter, then the GT-EQ/$\overline{GP0}$ and NE/$\overline{GP1}$ flags will be set, while the LT/GP0 and EQ/GP1 flags will be cleared. |
| Compare to Message Timer | CMT | 000B | Delay Time Value (Resolution = 1µS / LSB) | Unconditional | Compare Time Value to Message Time Counter. The LT/GP0 and EQ/GP1 flag bits are set or cleared based on the results of the compare. If the value of the CMT's parameter is less than the value of the message time counter, then the LT/GP0 and NE/$\overline{GP1}$ flags will be set, while the GT-EQ/$\overline{GP0}$ and EQ/GP1 flags will be cleared. If the value of the CMT's parameter is equal to the value of the message time counter, then the GT-EQ/$\overline{GP0}$ and EQ/GP1 flags will be set, while the LT/GP0 and NE/$\overline{GP1}$ flags will be cleared. If the value of the CMT's parameter is greater than the current value of the message time counter, then the GT-EQ/$\overline{GP0}$ and NE/$\overline{GP1}$ flags will be set, while the LT/GP0 and EQ/GP1 flags will be cleared. |

NOTE: While the XEQ (Execute Message) instruction is conditional, not all condition codes may be used to enable its use. The ALWAYS and NEVER condition codes may be used. The eight general purpose flag bits, GP0 through GP7, may also be used. However, if GP0 through GP7 are used, it is imperative that the host processor not modify the value of the specific general purpose flag bit that enabled a particular message while that message is being processed. Similarly, the LT, GT-EQ, EQ, and NE flags, which the BC only updates by means of the CFT and CMT instructions, may also be used. However, these two flags are dual use. Therefore, if these are used, it is imperative that the host processor not modify the value of the specific flag (GP0 or GP1) that enabled a particular message while that message is being processed. The NORESP, FMT ERR, GD BLK XFER, MASKED STATUS SET, BAD MESSAGE, RETRY0, and RETRY1 condition codes are not available for use with the XEQ instruction and should not be used to enable its execution.

## TABLE 52. BC OPERATIONS FOR MESSAGE SEQUENCE CONTROL (CONT.)

| INSTRUCTION | MNEMONIC | OP CODE (HEX) | PARAMETER | CONDITIONAL OR UNCONDITIONAL | DESCRIPTION |
|---|---|---|---|---|---|
| GP Flag Bits | FLG | 000C | Used to set, clear, or toggle GP (General Purpose) Flag bits (See description) | Unconditional | Used to set, toggle, or clear any or all of the eight general purpose flags. The table below illustrates the use of the GP Flag Bits instruction for the case of GP0 (General Purpose Flag 0). Bits 1 and 9 of the parameter byte affect flag GP1, bits 2 and 10 effect GP2, etc., according to the following rules: |
| Load Time Tag Counter | LTT | 000D | Time Value. Resolution (µs/LSB) is defined by bits 9, 8, and 7 of Configuration Register #2. | Conditional | Load Time Tag Counter with Time Value if the condition flag tests TRUE, otherwise continue execution at the next OpCode in the instruction list. |
| Load Frame Timer | LFT | 000E | Time Value (resolution = 100 µs/LSB) | Conditional | Load Frame Timer Register with the Time Value parameter if the condition flag tests TRUE, otherwise continue execution at the next OpCode in the instruction list. |
| Start Frame Timer | SFT | 000F | Not Used (Don't Care) | Conditional | Start Frame Time Counter with Time Value in Time Frame register if the condition flag tests TRUE, otherwise continue execution at the next OpCode in the instruction list. |
| Push Time Tag Register | PTT | 0010 | Not Used (Don't Care) | Conditional | Push the value of the Time Tag Register on the General Purpose Queue if the condition flag tests TRUE, otherwise continue execution at the next OpCode in the instruction list. |
| Push Block Status Word | PBS | 0011 | Not Used (Don't Care) | Conditional | Push the Block Status Word for the most recent message on the General Purpose Queue if the condition flag tests TRUE, otherwise continue execution at the next OpCode in the instruction list. |
| Push Immediate Value | PSI | 0012 | Immediate Value | Conditional | Push Immediate data on the General Purpose Queue if the condition flag tests TRUE, otherwise continue execution at the next OpCode in the instruction list. |
| Push Indirect | PSM | 0013 | Memory Address | Conditional | Push the data stored at the specified memory location on the General Purpose Queue if the condition flag tests TRUE, otherwise continue execution at the next OpCode in the instruction list. |
| Wait for External Trigger | WTG | 0014 | Not Used (Don't Care) | Conditional | Wait for a logic "0"-to-logic "1" transition on the EXT_TRIG input signal before proceeding to the next OpCode in the instruction list if the condition flag tests TRUE, otherwise continue execution at the next OpCode without delay. |
| Execute and Flip | XQF | 0015 | Message Control / Status Block Address | Unconditional | Execute (unconditionally) the message referenced by the Message Control/Status Block Address. Following the processing of this message, if the condition flag tests TRUE, the BC will toggle bit 4 in the Message Control/Status Block Address, and store the new Message Block Address as the updated value of the parameter following the XQF instruction code. As a result, the **next** time that this line in the instruction list is executed, the Message Control/Status Block at the **updated** address (**old address XOR 0010h**), rather than the old address, will be processed. If the condition flag tests FALSE, the value of the Message Control/Status Block Address parameter will not change. |

| Bit 8 | Bit 0 | Effect on GP0 |
|---|---|---|
| 0 | 0 | No Change |
| 0 | 1 | Set Flag |
| 1 | 0 | Clear Flag |
| 1 | 1 | Toggle Flag |

## TABLE 53. BC CONDITION CODES

| BIT CODE | NAME (BIT 4 = 0) | INVERSE (BIT 4 = 1) | FUNCTIONAL DESCRIPTION |
|---|---|---|---|
| 0 | LT/GP0 | GT-EQ/ $\overline{\text{GP0}}$ | Less than or GP0 flag. This bit is set or cleared based on the results of the compare. If the value of the CMT's parameter is less than the value of the message time counter, then the LT/GP0 and NE/$\overline{\text{GP1}}$ flags will be set, while the GT-EQ/$\overline{\text{GP0}}$ and EQ/GP1 flags will be cleared. If the value of the CMT's parameter is equal to the value of the message time counter, then the GT-EQ/$\overline{\text{GP0}}$ and EQ/GP1 flags will be set, while the LT/GP0 and NE/$\overline{\text{GP1}}$ flags will be cleared. If the value of the CMT's parameter is greater than the current value of the message time counter, then the GT-EQ/$\overline{\text{GP0}}$ and NE/$\overline{\text{GP1}}$ flags will be set , while the LT/GP0 and EQ/GP1 flags will be cleared. Also, General Purpose Flag 1 may also be set or cleared by a FLG operation. |
| 1 | EQ/GP1 | NE/$\overline{\text{GP1}}$ | Equal Flag. This bit is set or cleared after CFT or CMT operation. If the value of the CMT's parameter is equal to the value of the message time counter, then the EQ/GP1 flag will be set and the NE/$\overline{\text{GP1}}$ bit will be cleared. If the value of the CMT's parameter is not equal to the value of the message time counter, then the NE/$\overline{\text{GP1}}$ flag will be set and the EQ/GP1 bit will be cleared. Also, General Purpose Flag 1 may also be set or cleared by a FLG operation. |
| 2<br>3<br>4<br>5<br>6<br>7 | GP2<br>GP3<br>GP4<br>GP5<br>GP6<br>GP7 | $\overline{\text{GP2}}$<br>$\overline{\text{GP3}}$<br>$\overline{\text{GP4}}$<br>$\overline{\text{GP5}}$<br>$\overline{\text{GP6}}$<br>$\overline{\text{GP7}}$ | General Purpose Flags may be set, cleared, or toggled by a FLG operation. The host processor can set, clear, or toggle these flags in the same way as the FLG instruction by means of the BC GENERAL PURPOSE FLAG REGISTER. |
| 8 | NORESP | $\overline{\text{RESP}}$ | NORESP indicates that an RT has either not responded or has responded later than the BC No Response Timeout time. The Enhanced Mini-ACE's No Response Timeout Time is defined per MIL-STD-1553B as the time from the mid-bit crossing of the parity bit of the last word transmitted by the BC to the mid-sync crossing of the RT Status Word. The value of the No Response Timeout value is programmable from among the nominal values 18.5, 22.5, 50.5, and 130 µs (±1 µs) by means of bits 10 and 9 of Configuration Register #5. |
| 9 | FMT ERR | $\overline{\text{FMT ERR}}$ | FMT ERR indicates that the received portion of the most recent message contained one or more violations of the 1553 message validation criteria (sync, encoding, parity, bit count, word count, etc.), or the RT's status word received from a responding RT contained an incorrect RT address field. |
| A | GD BLK XFER | $\overline{\text{GD BLK XFER}}$ | For the most recent message, GD BLK XFER will be set to logic "1" following completion of a valid (error-free) RT-to-BC transfer, RT-to-RT transfer, or transmit mode code with data message. This bit is set to logic "0" following an invalid message. GOOD DATA BLOCK TRANSFER is **always** logic "0" following a BC-to-RT transfer, a mode code with data, or a mode code without data. The Loop Test has **no effect** on GOOD DATA BLOCK TRANSFER. GOOD DATA BLOCK TRANSFER may be used to determine if the transmitting portion of an RT-to-RT transfer was error free. |
| B | MASKED STATUS BIT | $\overline{\text{MASKED STATUS BIT}}$ | Indicates that one or both of the following conditions have occurred for the most recent message: (1) If one (or more) of the Status Mask bits (14 through 9) in the BC Control Word is logic "0" **and** the corresponding bit(s) is (are) set (logic "1") in the received RT Status Word. In the case of the RESERVED BITS MASK (bit 9) set to logic "0," any or all of the 3 Reserved Status Word bits being set will result in a MASKED STATUS SET condition; and/or (2) If BROADCAST MASK ENABLED/$\overline{\text{XOR}}$ (bit 11 of Configuration Register #4) is logic "1" **and** the MASK BROADCAST bit of the message's BC Control Word is logic "0" and the BROADCAST COMMAND RECEIVED bit in the received RT Status Word is logic "1". |
| C | BAD MESSAGE | GOOD MESSAGE | BAD MESSAGE indicates either a format error, loop test failure, or no response error for the most recent message. Note that a "Status Set" condition has **no effect** on the "BAD MESSAGE/GOOD MESSAGE" condition code. |
| D<br><br>E | RETRY0<br><br>RETRY1 | $\overline{\text{RETRY0}}$<br><br>$\overline{\text{RETRY1}}$ | These two bits reflect the retry status of the most recent message. The number of times that the message was retried is delineated by these two bits as shown below:<br>RETRY COUNT 1 (bit 14) / RETRY COUNT 0 (bit 13) / Number of Message Retries<br>0 / 0 / 0<br>0 / 1 / 1<br>1 / 0 / N/A<br>1 / 1 / 2 |
| F | ALWAYS | NEVER | The ALWAYS bit should be asserted (bit 4 = 0) to designate an instruction as unconditional.<br>The NEVER bit (bit 4 = 1) can be used to implement an NOP instruction. |

## BC MESSAGE SEQUENCE CONTROL

The PCI Enhanced Mini-ACE BC message sequence control capability enables a high degree of offloading of the host processor. This includes using the various timing functions to enable autonomous structuring of major and minor frames. In addition, by implementing conditional jumps and subroutine calls, the message sequence control processor greatly simplifies the insertion of asynchronous, or "out-of-band" messages.

### EXECUTE AND FLIP OPERATION

The PCI Enhanced Mini-ACE BC's XQF, or "Execute and Flip" operation, provides some unique capabilities. Following execution of this unconditional instruction, if the condition code tests TRUE, the BC will modify the value of the current XQF instruction's pointer parameter by toggling bit 4 in the pointer. That is, if the selected condition flag tests true, the value of the parameter will be updated to the value = old address XOR 0010h. As a result, the next time that this line in the instruction list is executed, the Message Control/Status Block at the updated address (old address XOR 0010h), will be processed, rather than the one at the old address. The operation of the XQF instruction is illustrated in FIGURE 4.

There are multiple ways of utilizing the "execute and flip" functionality. One is to facilitate the implementation of a double buffering data scheme for individual messages. This allows the message sequence control processor to "ping-pong" between a pair of data buffers for a particular message. By so doing, the host processor can access one of the two Data Word blocks, while the BC reads or writes the alternate Data Word block.

A second application of the "execute and flip" capability is in association with message retries. This allows the BC to not only switch buses when retrying a failed message, but to automatically switch buses permanently for all future times that the same message is to be processed. This not only provides a high degree of autonomy from the host CPU, but saves BC bandwidth, by eliminating future attempts to process messages on an RT's failed channel.

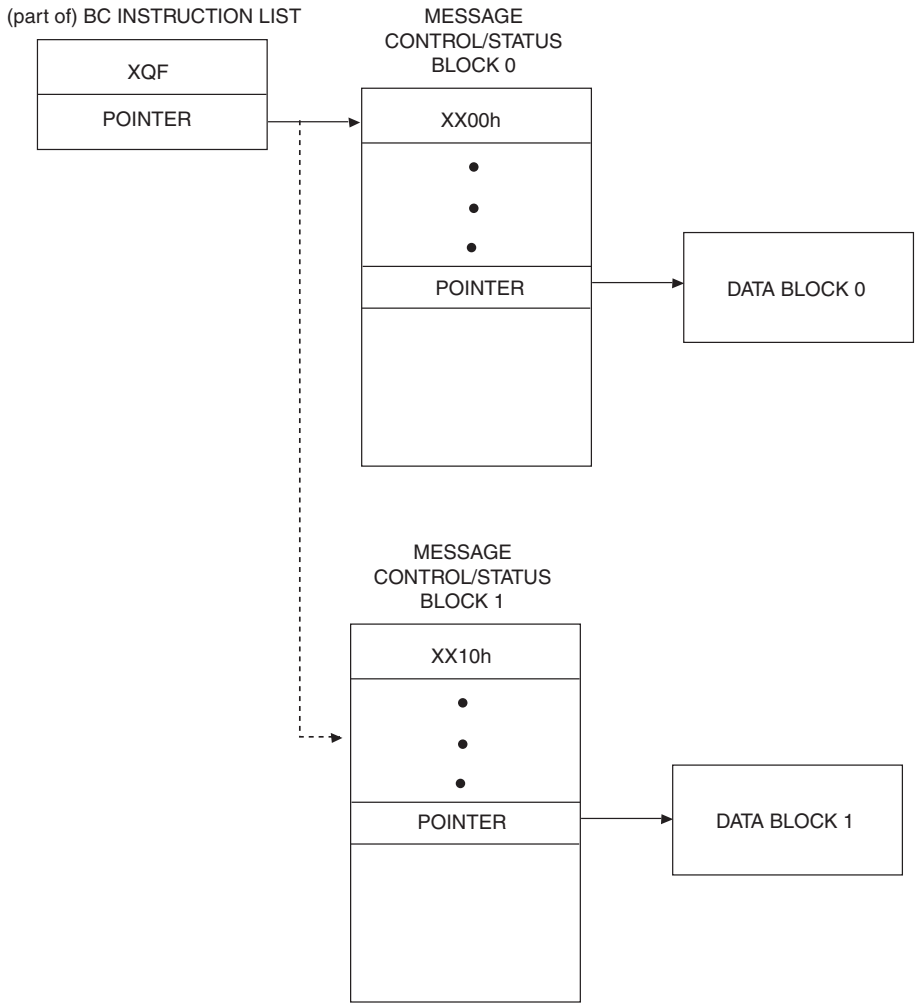



**FIGURE 4. USE OF EXECUTE AND FLIP (XQF) OPERATION**

### GENERAL PURPOSE QUEUE

The PCI Enhanced Mini-ACE BC allows for the creation of a general purpose queue. This data structure provides a means for the message sequence processor to convey information to the BC host. The BC op code repertoire provides mechanisms to push various items on this queue. These include the contents of the Time Tag Register, the Block Status Word for the most recent message, an immediate data value, or the contents of a specified memory address.

FIGURE 5 illustrates the operation of the BC General Purpose Queue. Note that the BC General Purpose Queue Pointer Register will always point to the next address location (modulo 64); that is, the location following the last location written by the BC message sequence control engine.

If enabled, a BC GENERAL PURPOSE QUEUE ROLLOVER interrupt will be issued when the value of the queue pointer address rolls over at a 64-word boundary.

## REMOTE TERMINAL (RT) ARCHITECTURE

The PCI Enhanced Mini-ACE's RT architecture builds upon that of the ACE and Mini-ACE. The PCI Enhanced Mini-ACE provides multiprotocol support, with full compliance to all of the commonly used data bus standards, including MIL-STD-1553A, MIL-STD-1553B, Notice 2, STANAG 3838, General Dynamics 16PP303, and McAirA3818, A5232, and A5690. For the PCI Enhanced Mini-ACE RT mode, there is programmable flexibility enabling the RT to be configured to fulfill any set of system requirements. This includes the capability to meet the MIL-STD-1553A response time requirement of 2 to 5 µs, and multiple options for mode code subaddresses, mode codes, RT status word, and RT BIT word.

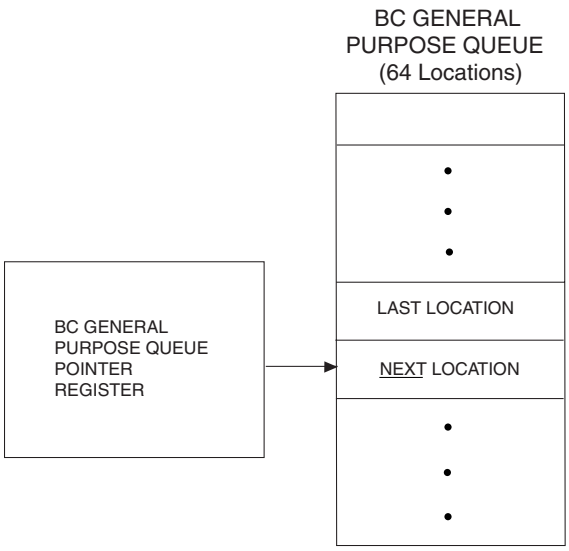



**FIGURE 5. BC GENERAL PURPOSE QUEUE**

The PCI Enhanced Mini-ACE RT protocol design implements all of the MIL-STD-1553B message formats and dual redundant mode codes. The design has passed validation testing for MIL-STD-1553B compliance. The PCI Enhanced Mini-ACE RT performs comprehensive error checking, word and format validation, and checks for various RT-to-RT transfer errors. One of the main features of the PCI Enhanced Mini-ACE RT is its choice of memory management options. These include single buffering by subaddress, circular buffering by individual subaddresses, and global circular buffering for multiple (or all) subaddresses.

Other features of the PCI Enhanced Mini-ACE RT include a set of interrupt conditions, an interrupt status queue with filtering based on valid and/or invalid messages, internal command illegalization, programmable busy by subaddress, and multiple options on time tagging.

## RT MEMORY ORGANIZATION

TABLE 54 illustrates a typical memory map for a PCI Enhanced Mini-ACE RT with 4K RAM. The two Stack Pointers reside in fixed locations in the shared RAM address space: address 0100h (PCI BAR0 + 200h) for the Area A Stack Pointer and address 0104h (PCI BAR0 + 208h) for the Area B Stack Pointer. In addition to the Stack Pointer, there are several other areas of

**TABLE 54. TYPICAL RT MEMORY MAP (SHOWN FOR 4K RAM)**

| WORD ADDRESS (HEX) | PCI BAR0 OFFSET (HEX) | DESCRIPTION |
|---|---|---|
| 0000-00FF | 0000-01FE | Stack A |
| 0100 | 0200 | **Stack Pointer A** |
| 0101 | 0202 | **Global Circular Buffer A Pointer** |
| 0102-0103 | 0204-0206 | RESERVED |
| 0104 | 0208 | **Stack Pointer B** |
| 0105 | 020A | **Global Circular Buffer B Pointer** |
| 0106-0107 | 020C-020E | RESERVED |
| 0108-010F | 0210-021E | **Mode Code Selective Interrupt Table** |
| 0110-013F | 0220-027E | **Mode Code Data** |
| 0140-01BF | 0280-037E | **Lookup Table A** |
| 01C0-023F | 0380-047E | **Lookup Table B** |
| 0240-0247 | 0480-048E | **Busy Bit Lookup Table** |
| 0248-025F | 0490-04BE | (not used) |
| 0260-027F | 04C0-04FE | Data Block 0 |
| 0280-02FF | 0500-05FE | Data Block 1-4 |
| 0300-03FF | 0600-07FE | **Command Illegalizing Table** |
| 0400-041F | 0800-083E | Data Block 5 |
| 0420-043F | 0840-087E | Data Block 6 |
| • • • | • • • | • • • |
| 0FE0-0FFF | 1FC0-1FFE | Data Block 100 |

| TABLE 55. RT LOOK-UP TABLES | | | | | |
|---|---|---|---|---|---|
| AREA A (INTERNAL MEMORY OFFSET) | AREA A (PCI BAR0 OFFSET) | AREA B (INTERNAL MEMORY OFFSET) | AREA B (PCI BAR0 OFFSET) | DESCRIPTION | COMMENT |
| 0140<br>•<br>•<br>•<br>015F | 0280<br>•<br>•<br>•<br>02BE | 01C0<br>•<br>•<br>•<br>01DF | 0380<br>•<br>•<br>•<br>03BE | Rx(/Bcst) SA0<br>•<br>•<br>•<br>Rx(/Bcst) SA31 | Receive (/Broadcast) Lookup Pointer Table |
| 0160<br>•<br>•<br>•<br>017F | 02C0<br>•<br>•<br>•<br>02FE | 01E0<br>•<br>•<br>•<br>01FF | 03C0<br>•<br>•<br>•<br>03FE | Tx SA0<br>•<br>•<br>•<br>Tx SA31 | Transmit Lookup Pointer Table |
| 0180<br>•<br>•<br>•<br>019F | 0300<br>•<br>•<br>•<br>033E | 0200<br>•<br>•<br>•<br>021F | 0400<br>•<br>•<br>•<br>043E | Bcst SA0<br>•<br>•<br>•<br>Bcst SA31 | Broadcast Lookup Pointer Table (Optional) |
| 01A0<br>•<br>•<br>•<br>01BF | 0340<br>•<br>•<br>•<br>037E | 0220<br>•<br>•<br>•<br>023F | 0440<br>•<br>•<br>•<br>047E | SACW SA0<br>•<br>•<br>•<br>SACW SA31 | Subaddress Control Word Table (Optional) |

the shared RAM address space that are designated as fixed locations (all shown in bold). These are for the Area A and Area B lookup tables, the illegalization lookup table, the busy lookup table, and the mode code data tables.

The RT lookup tables (reference TABLE 55) provide a mechanism for allocating data blocks for individual transmit, receive, or broadcast subaddresses. The RT lookup tables include subaddress control words as well as the individual data block pointers. If command illegalization is used, address range 0300-03FF (PCI BAR0 0600-07FEh) is used for command illegalizing. The descriptor stack RAM area, as well as the individual data blocks, may be located in any of the non-fixed areas in the shared RAM address space.

Note that in TABLE 54, there is no area allocated for "Stack B". This is shown for purpose of illustration. Also, note that in TABLE 54, the allocated area for the RT command stacks is 256 words. However, larger stack sizes are possible. That is, the RT command stack size may be programmed for 256 words (64 messages), 512, 1024, or 2048 words (512 messages) by means of bits 14 and 13 of Configuration Register 3.

| TABLE 56. RT SUBADDRESS CONTROL WORD - MEMORY MANAGEMENT OPTIONS | | | | | |
|---|---|---|---|---|---|
| GLOBAL CIRCULAR BUFFER (bit 15) | SUBADDRESS CONTROL WORD BITS | | | MEMORY MANAGEMENT SUBADDRESS BUFFER SCHEME DESCRIPTION | |
| | MM2 | MM1 | MM0 | | |
| 0 | 0 | 0 | 0 | Single Message | |
| 1 | 0 | 0 | 0 | Reserved for future use | |
| 0 | 0 | 0 | 1 | 128-Word | Subaddress - specific circular buffer of specified size. |
| 0 | 0 | 1 | 0 | 256-Word | |
| 0 | 0 | 1 | 1 | 512-Word | |
| 0 | 1 | 0 | 0 | 1024-Word | |
| 0 | 1 | 0 | 1 | 2048-Word | |
| 0 | 1 | 1 | 0 | 4096-Word | |
| 0 | 1 | 1 | 1 | 8192-Word | |
| 1 | 1 | 1 | 1 | (for receive and / or broadcast subaddresses only)<br><br>Global Circular Buffer: The buffer size is specified by Configuration Register #6, bits 11-9. The pointer to the global circular buffer is stored at address 0101 (BAR0 + 0202h) for Area A or address 0105 (BAR0 + 020Ah) for Area B. | |

## RT MEMORY MANAGEMENT

The PCI Enhanced Mini-ACE provides a variety of RT memory management capabilities. As with the ACE, Mini-ACE(Plus) and Enhanced Mini-ACE, the choice of memory management scheme is fully programmable on a transmit/receive/broadcast subaddress basis.

In compliance with MIL-STD-1553B Notice 2, received data from broadcast messages may be optionally separated from non-broadcast received data. For each receive or broadcast subaddress, either a single-message data block, or a variable-sized (128 to 8192 words) subaddress circular buffer may be allocated for data storage. The use of Single Buffered mode is strongly recommended for transmitted data words. The memory management scheme for individual subaddresses is designated by means of the subaddress control word (reference TABLE 56).

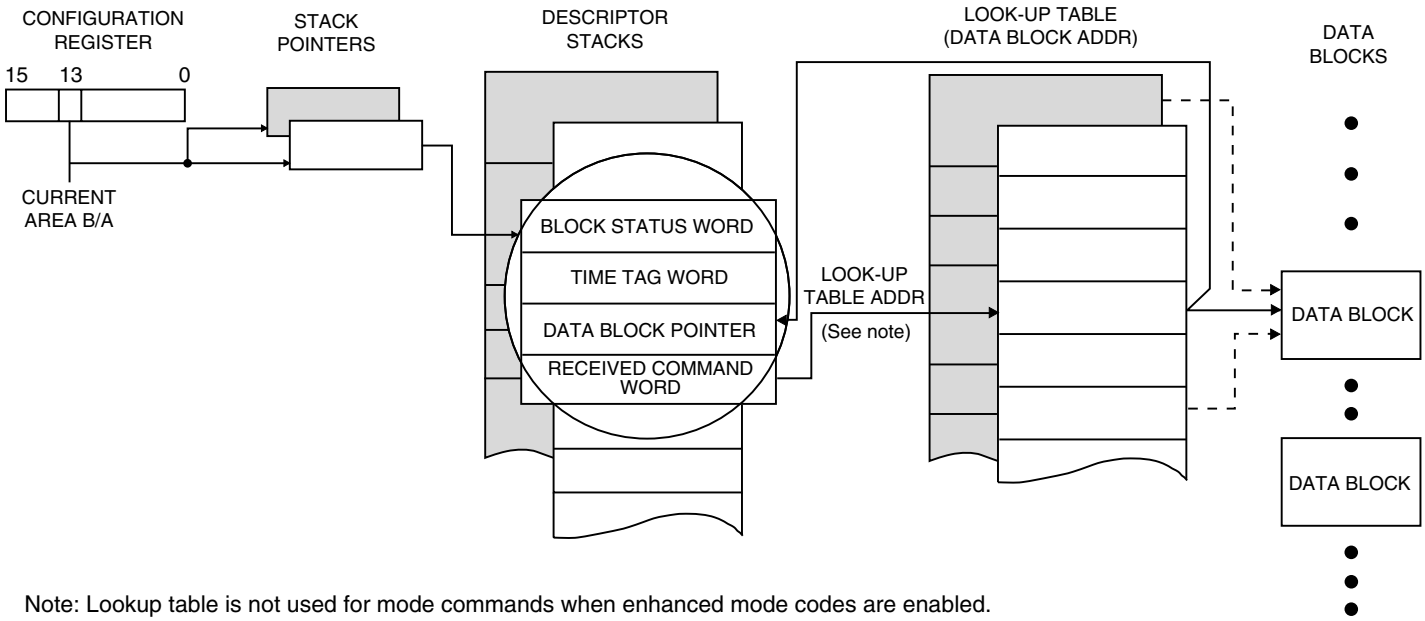
For received data, there is also a global circular buffer mode. In this configuration, the data words received from multiple (or all) subaddresses are stored in a common circular buffer structure. Like the subaddress circular buffer, the size of the global circular buffer is programmable, with a range of 128 to 8192 data words.

In addition to helping ensure data sample consistency, the circular buffer options provide a means of greatly reducing host processor overhead for multi-message bulk data transfer applications.

End-of-message interrupts may be enabled either globally (following all messages), following error messages, on a transmit/receive/broadcast subaddress or mode code basis, or when a circular buffer reaches its midpoint (50% boundary) or lower (100%) boundary. A pair of interrupt status registers allow the host processor to determine the cause of all interrupts by means of a single read operation.

### SINGLE BUFFERED MODE

The operation of the single buffered RT mode is illustrated in FIGURE 6. In the single buffered mode, the respective lookup table entry must be initialized by the host processor. Received data words are written to, or transmitted data words are read from the data word block with starting address referenced by the lookup table pointer. In the single buffered mode, the current lookup table pointer is not updated by the PCI Enhanced Mini-ACE memory management logic. Therefore, if a subsequent message is received for the same subaddress, the same Data Word block will be overwritten or overread.




Note: Lookup table is not used for mode commands when enhanced mode codes are enabled.

**FIGURE 6. RT SINGLE BUFFERED MODE**

## CIRCULAR BUFFER MODE

The operation of the PCI Enhanced Mini-ACE's circular buffer RT memory management mode is illustrated in FIGURE 7. As in the single buffered mode, the individual lookup table entries are initially loaded by the host processor. At the start of each message, the lookup table entry is stored in the third position of the respective message block descriptor in the descriptor stack area of RAM. Receive or transmit data words are transferred to (from) the circular buffer, starting at the location referenced by the lookup table pointer.

In general, the location after the last data word written or read (modulo the circular buffer size) during the message is written to the respective lookup table location during the end-of-message sequence. By so doing, data for the next message for the respective transmit, receive(/broadcast), or broadcast subaddress will be accessed from the next lower contiguous block of locations in the circular buffer.

For the case of a receive (or broadcast receive) message with a data word error, there is an option such that the lookup table pointer will only be updated following receipt of a valid message. That is, the pointer will not be updated following receipt of a message with an error in a data word. This allows failed messages in a bulk data transfer to be retried without disrupting the circular buffer data structure, and without intervention by the RT's host processor.

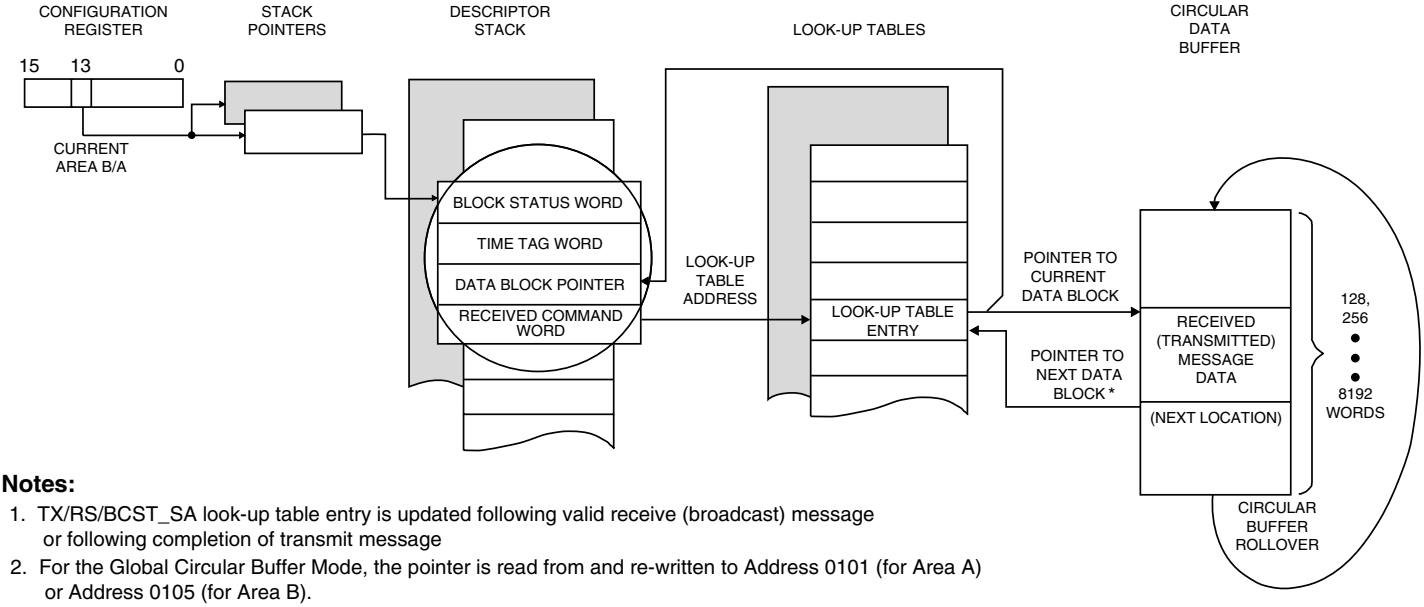
## GLOBAL CIRCULAR BUFFER

Beyond the programmable choice of single buffer mode or circular buffer mode, programmable on an individual subaddress basis, the PCI Enhanced Mini-ACE RT architecture provides an additional option, a variable sized global circular buffer.

In the global circular buffer mode, the data for multiple receive subaddresses is stored in the same circular buffer data structure. The size of the global circular buffer may be programmed for 128, 256, 512, 1024, 2048, 4096, or 8192 words, by means of bits 11, 10, and 9 of Configuration Register #6. As shown in TABLE 56, individual subaddresses may be mapped to the global circular buffer by means of their respective subaddress control words.

The pointer to the Global Circular Buffer will be stored in location 0101 (for Area A), or location 0105 (for Area B).

The global circular buffer option provides a highly efficient method for storing received message data. It allows for frequently used subaddresses to be mapped to individual data blocks, while also providing a method for asynchronously received messages to infrequently used subaddresses to be logged to a common area. Alternatively, the global circular buffer provides an efficient means for storing the received data words for all subaddresses. Under this method, all received data words are stored chronologically, regardless of subaddress.




**Notes:**

1. TX/RS/BCST_SA look-up table entry is updated following valid receive (broadcast) message or following completion of transmit message
2. For the Global Circular Buffer Mode, the pointer is read from and re-written to Address 0101 (for Area A) or Address 0105 (for Area B).

**FIGURE 7. RT CIRCULAR BUFFERED MODE**

## RT DESCRIPTOR STACK

The descriptor stack provides a chronology of all messages processed by the PCI Enhanced Mini-ACE RT. Reference FIGURE 6 and FIGURE 7. Similar to BC mode, there is a four-word block descriptor in the Stack for each message processed. The four entries to each block descriptor are the Block Status Word, Time Tag Word, the pointer to the start of the message's data block, and the 16-bit received Command Word.

The RT Block Status Word includes indications of whether a particular message is ongoing or has been completed, what bus channel it was received on, indications of illegal commands, and flags denoting various message error conditions. For the subaddress circular buffering, and global circular buffering modes, the data block pointer may be used for locating the data blocks for specific messages. Note that for mode code commands, there is an option to store the transmitted or received data word as the third word of the descriptor, in place of the data block pointer.

The Time Tag Word provides a 16-bit indication of relative time for individual messages. The resolution of the PCI Enhanced Mini-ACE's time tag is programmable from among 2, 4, 8, 16, 32, or 64 µs/LSB. There is also a provision for using an external clock input for the time tag (consult factory). If enabled, there is a time tag rollover interrupt, which is issued when the value of the time tag rolls over from FFFF(hex) to 0. Other time tag options include the capabilities to clear the time tag register following receipt of a Synchronize (without data) mode command and/or to set the time tag following receipt of a Synchronize (with data) mode command. For the latter, there is an added option to filter the "set" capability based on the LSB of the received data word being equal to logic "0".

## RT INTERRUPTS

The PCI Enhanced Mini-ACE offers a great deal of flexibility in terms of RT interrupt processing. By means of the PCI Enhanced Mini-ACE's two Interrupt Mask Registers, the RT may be programmed to issue interrupt requests for the following events/conditions: End-of-(every)Message, Message Error, Selected (transmit or receive) Subaddress, 100% Circular Buffer Rollover, 50% Circular Buffer Rollover, 100% Descriptor Stack Rollover, 50% Descriptor Stack Rollover, Selected Mode Code, Transmitter Timeout, Illegal Command, and Interrupt Status Queue Rollover.

### INTERRUPTS FOR 50% ROLLOVERS OF STACKS, CIRCULAR BUFFERS

The PCI Enhanced Mini-ACE RT and Monitor are capable of issuing host interrupts when a subaddress circular buffer pointer or stack pointer crosses its mid-point boundary. For RT circular buffers, this is applicable for both transmit and receive subaddresses. Reference FIGURE 8. There are four interrupt mask and interrupt status register bits associated with the 50% rollover function:

(1) RT circular buffer;

(2) RT command (descriptor) stack;

(3) Monitor command (descriptor) stack; and

(4) Monitor data stack.

The 50% rollover interrupt is beneficial for performing bulk data transfers. For example, when using circular buffering for a par-

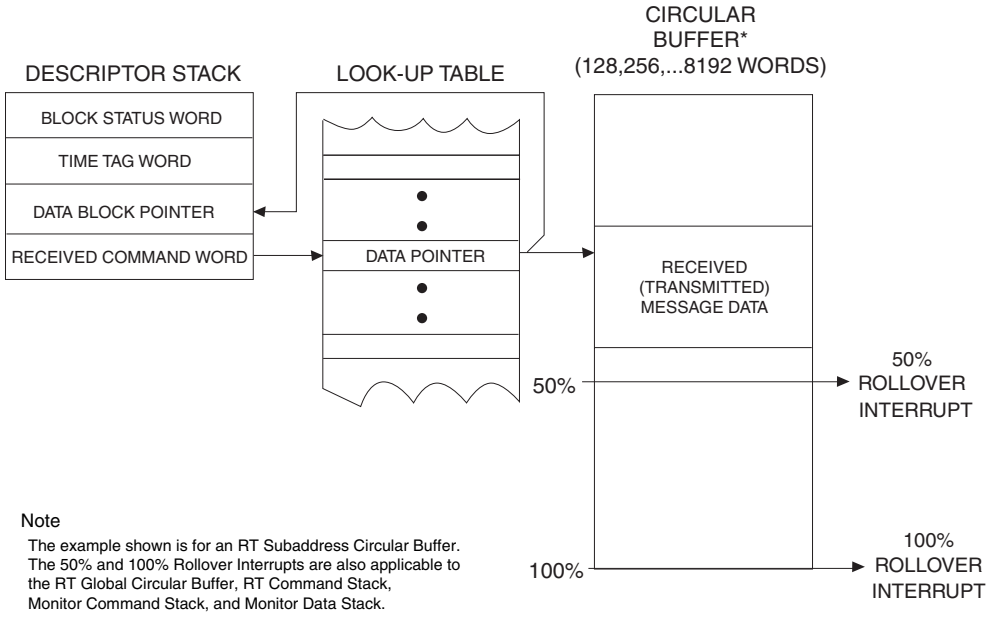



**FIGURE 8. 50% AND 100% ROLLOVER INTERRUPTS**

ticular receive subaddress, the 50% rollover interrupt will inform the host processor when the circular buffer is half full. At that time, the host may proceed to read the received data words in the upper half of the buffer, while the PCI Enhanced Mini-ACE RT writes received data words to the lower half of the circular buffer. Later, when the RT issues a 100% circular buffer rollover interrupt, the host can proceed to read the received data from the lower half of the buffer, while the PCI Enhanced Mini-ACE RT continues to write received data words to the upper half of the buffer.

## INTERRUPT STATUS QUEUE

The PCI Enhanced Mini-ACE RT, Monitor, and combined RT/Monitor modes include the capability for generating an interrupt status queue. As illustrated in FIGURE 9, this provides a chronological history of interrupt generating events and conditions. In addition to the Interrupt Mask Register, the Interrupt Status Queue provides additional filtering capability, such that only valid messages and/or only invalid messages may result in the creation of an entry to the Interrupt Status Queue. Queue entries for invalid and/or valid messages may be individually disabled by means of bits 8 and 7 of Configuration Register #6.

The pointer to the Interrupt Status Queue is stored in the INTERRUPT VECTOR QUEUE POINTER REGISTER (register address 1F). This register must be initialized by the host, and is subsequently incremented by the RT message processor. The interrupt status queue is 64 words deep, providing the capability to store entries for up to 32 messages.

The queue rolls over at addresses of modulo 64. The events that result in queue entries include both message-related and non-message related events. Note that the Interrupt Vector Queue Pointer Register will always point to the next location (modulo 64) following the last vector/pointer pair written by the PCI Enhanced Mini-ACE RT, Monitor, or RT/Monitor.

Each event that causes an interrupt results in a two-word entry to be written to the queue. The first word of the entry is the interrupt vector. The vector indicates which interrupt event(s)/condition(s) caused the interrupt.

The interrupt events are classified into two categories: message interrupt events and non-message interrupt events. Message-based interrupt events include End-of-Message, Selected mode code, Format error, Subaddress control word interrupt, RT Circular buffer rollover, Handshake failure, RT Command stack rollover, transmitter timeout, MT data stack rollover, MT command stack rollover, RT Command stack 50% rollover, MT data stack 50% rollover, MT command stack 50% rollover, and RT Circular buffer 50% rollover. Non-message interrupt events/conditions include time tag rollover, RT address parity error, RAM parity error, and BIT completed.

Bit 0 of the interrupt vector (interrupt status) word indicates whether the entry is for a message interrupt event (if bit 0 is logic "1") or a non-message interrupt event (if bit 0 is logic "0"). It is not possible for one entry on the queue to indicate both a message interrupt and a non-message interrupt.

As illustrated in FIGURE 9, for a message interrupt event, the parameter word is a pointer. The pointer will reference the first word of the RT or MT command stack descriptor (i.e., the Block Status Word).

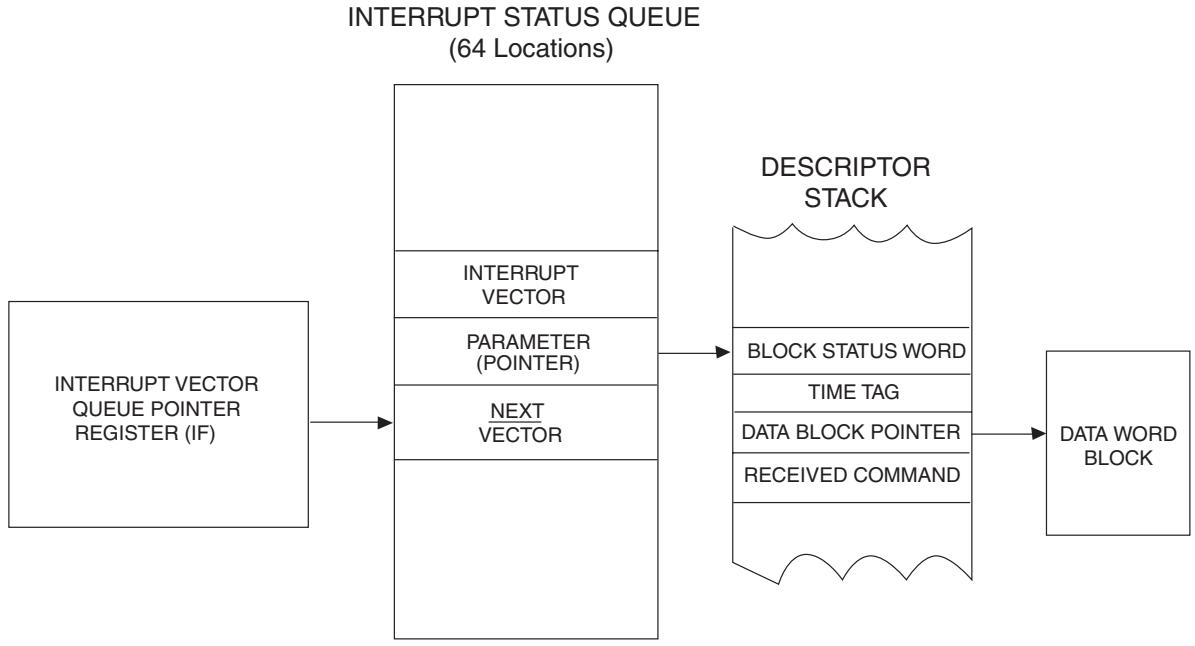



**FIGURE 9. RT (AND MONITOR) INTERRUPT STATUS QUEUE (SHOWN FOR MESSAGE INTERRUPT EVENT)**

For a RAM Parity Error non-message interrupt, the parameter will be the RAM address where the parity check failed. For the RT address Parity Error and Time Tag Rollover non-message interrupts, the parameter is not used; it will have a value of 0000.

If enabled, an INTERRUPT STATUS QUEUE ROLLOVER interrupt will be issued when the value of the queue pointer address rolls over at a 64-word address boundary.

NOTE: Please see Appendix "F" of the Enhanced Mini-ACE Users Guide for important information applicable only to RT MODE operation, enabling of the interrupt status queue and use of specific non-message interrupts.

## RT COMMAND ILLEGALIZATION

The PCI Enhanced Mini-ACE provides an internal mechanism for RT Command Word illegalizing. By means of a 256-word area in shared RAM, the host processor may designate that any message be illegalized, based on the command word T/R bit, subaddress, and word count/mode code fields. The PCI Enhanced Mini-ACE illegalization scheme provides the maximum in flexibility, allowing any subset of the 4096 possible combinations of broadcast/own address, T/$\overline{R}$ bit, subaddress, and word count/mode code to be illegalized.

The address map of the PCI Enhanced Mini-ACE's illegalizing table is illustrated in TABLE 57.

### BUSY BIT

The PCI Enhanced Mini-ACE RT provides two different methods for setting the Busy status word bit: (1) globally, by means of Configuration Register #1; or (2) on a T/R-bit/subaddress basis, by means of a RAM lookup table. If the host CPU asserts the BUSY bit low in Configuration Register #1, the PCI Enhanced Mini-ACE RT will respond to all non-broadcast commands with the Busy bit set in its RT Status Word.

Alternatively, there is a Busy lookup table in the PCI Enhanced Mini-ACE shared RAM. By means of this table, it is possible for the host processor to set the busy bit for any selectable subset of the 128 combinations of broadcast/own address, T/$\overline{R}$ bit, and subaddress.

If the busy bit is set for a transmit command, the PCI Enhanced Mini-ACE RT will respond with the busy bit set in the status word, but will not transmit any data words. If the busy bit is set for a receive command, the RT will also respond with the busy status bit set. There are two programmable options regarding the reception of data words for a non-mode code receive command for which the RT is busy: (1) to transfer the received data words to shared RAM; or (2) to not transfer the data words to shared RAM.

## RT ADDRESS

The PCI Enhanced Mini-ACE offers several different options for designating the Remote Terminal address. These include the following: (1) hardwired, by means of the 5 RT ADDRESS inputs, and the RT ADDRESS PARITY input; (2) by means of the RT ADDRESS (and PARITY) inputs, but latched via hardware, on the rising edge of the RT_AD_LAT input signal; (3) input by means of the RT ADDRESS (and PARITY) inputs, but latched via host software; and (4) fully software programmable, by means of an internal register. In all four configurations, the RT address is readable by the host processor.

## RT BUILT-IN TEST (BIT) WORD

The bit map for the PCI Enhanced Mini-ACE's internal RT Built-in-Test (BIT) Word is indicated in TABLE 58.

## OTHER RT FEATURES

The PCI Enhanced Mini-ACE includes options for the Terminal flag status word bit to be set either under software control and/or automatically following a failure of the loopback self-test. Other software programmable RT options include software programmable RT status and RT BIT words, automatic clearing of the Service Request bit following receipt of a Transmit vector word mode command, options regarding Data Word transfers for the Busy and Message error (illegal) Status word bits, and options for the handling of 1553A and reserved mode codes.

## MONITOR ARCHITECTURE

The PCI Enhanced Mini-ACE includes three monitor modes:

(1) A Word Monitor mode.

(2) A selective message monitor mode.

(3) A combined RT/message monitor mode.

For new applications, it is recommended that the selective message monitor mode be used, rather than the word monitor mode. Besides providing monitor filtering based on RT address, T/$\overline{R}$ bit, and subaddress, the message monitor eliminates the need to determine the start and end of messages by software.

| TABLE 57. ILLEGALIZATION TABLE MEMORY MAP | | |
|---|---|---|
| **INTERNAL ADDRESS** | **PCI BAR0 OFFSET** | **DESCRIPTION** |
| 300 | 600 | Brdcst / Rx, SA 0. MC15-0 |
| 301 | 602 | Brdcst / Rx, SA 0. MC31-16 |
| 302 | 604 | Brdcst / Rx, SA 1. WC15-0 |
| 303 | 606 | Brdcst / Rx, SA 1. WC31-16 |
| • • • | • • • | • • • |
| 33F | 67E | Brdcst / Rx, SA 0. MC15-0 |
| 340 | 680 | Brdcst / Tx, SA 0. MC31-16 |
| 341 | 682 | Brdcst / Tx, SA 1. WC15-0 |
| 342 | 684 | Brdcst / Tx, SA 1. MC31-16 |
| • • • | • • • | • • • |
| 37D | 6FA | Brdcst / Tx, SA 30. WC31-16 |
| 37E | 6FC | Brdcst / Tx, SA 31. MC15-0 |
| 37F | 6FE | Brdcst / Tx, SA 31. MC31-16 |
| 380 | 700 | Own Addr / Rx, SA 0. MC15-0 |
| 381 | 702 | Own Addr / Rx, SA 0. MC31-16 |
| 382 | 704 | Own Addr / Rx, SA 1. WC15-0 |
| 383 | 706 | Own Addr / Rx, SA 1. WC31-16 |
| • • • | • • • | • • • |
| 3BE | 77C | Own Addr / Rx, SA 31. MC15-0 |
| 3BF | 77E | Own Addr / Rx, SA 31. MC31-16 |
| 3C0 | 780 | Own Addr / Tx, SA 0. MC15-0 |
| 3C1 | 782 | Own Addr / Tx, SA 0. MC31-16 |
| 3C2 | 784 | Own Addr / Tx, SA 1. WC15-0 |
| 3C3 | 786 | Own Addr / Tx, SA 1. WC31-16 |
| • • • | • • • | • • • |
| 3FC | 7F8 | Own Addr / Tx, SA 30. WC15-0 |
| 3FD | 7FA | Own Addr / Tx, SA 30. WC31-16 |
| 3FE | 7FC | Own Addr / Tx, SA 31. MC15-0 |
| 3FF | 7FE | Own Addr / Tx, SA 31. MC31-16 |

## WORD MONITOR MODE

In the Word Monitor Terminal mode, the PCI Enhanced Mini-ACE monitors both 1553 buses. After the software initialization and Monitor Start sequences, the PCI Enhanced Mini-ACE stores all Command, Status, and Data Words received from both buses. For each word received from either bus, a pair of words is stored to the PCI Enhanced Mini-ACE's shared RAM. The first word is the word received from the 1553 bus. The second word is the Monitor Identification (ID), or "Tag" word. The ID word contains information relating to bus channel, word validity, and inter-word time gaps. The data and ID words are stored in a circular buffer using the whole of the shared RAM address space.

### *WORD MONITOR MEMORY MAP*

A typical word monitor memory map is illustrated in TABLE 61. TABLE 61 assumes a 64K address space for the PCI Enhanced Mini-ACE's monitor. The Active Area Stack pointer provides the address where the first monitored word is stored. In the example, it is assumed that the Active Area Stack Pointer for Area A (location 0100) is initialized to 0000. The first received data word is stored in location 0000, the ID word for the first word is stored in location 0001, etc.

The current Monitor address is maintained by means of a counter register. This value may be read by the CPU by means of the

Data Stack Address Register. It is important to note that when the counter reaches the Stack Pointer address of 0100 or 0104, the initial pointer value stored in this shared RAM location will be overwritten by the monitored data and ID Words. When the internal counter reaches an address of FFFF (or 0FFF, for a PCI Enhanced Mini-ACE with 4K RAM), the counter rolls over to 0000.

### *WORD MONITOR TRIGGER*

In the Word Monitor mode, there is a pattern recognition trigger and a pattern recognition interrupt. The 16-bit compare word for both the trigger and the interrupt is stored in the Monitor Trigger Word Register. The pattern recognition interrupt is enabled by setting the MT Pattern Trigger bit in the Interrupt Mask Register. The pattern recognition trigger is enabled by setting the Trigger Enable bit in Configuration Register #1 and selecting either the Start-on-trigger or the Stop-on-trigger bit in Configuration Register #1.

The Word Monitor may also be started by means of a low-to-high transition on the EXT_TRIG input signal.

## SELECTIVE MESSAGE MONITOR MODE

The PCI Enhanced Mini-ACE Selective Message Monitor provides monitoring of 1553 messages with filtering based on RT address, T/R bit, and subaddress with no host processor intervention. By autonomously distinguishing between 1553 command and status words, the Message Monitor determines when messages begin and end, and stores the messages into RAM, based on a programmable filter (RT address, T/R bit, and subaddress).

The selective monitor may be configured as just a monitor, or as a combined RT/Monitor. In the combined RT/Monitor mode, the PCI Enhanced Mini-ACE functions as an RT for one RT address (including broadcast messages), and as a selective message monitor for the other 30 RT addresses. The PCI Enhanced Mini-ACE Message Monitor contains two stacks, a command stack and a data stack, that are independent from the BC/RT command stack. The pointers for these stacks are located at fixed locations in the RAM.

### *MONITOR SELECTION FUNCTION*

Following receipt of a valid command word in Selective Monitor mode, the PCI Enhanced Mini-ACE will reference the selective monitor lookup table to determine if this particular command is enabled. The address for this location is determined by means of an offset based on the RT Address, T/$\overline{R}$ bit, and Subaddress bit 4 of the current command word, and concatenating it to the monitor lookup table base address of 0280 (hex). The bit location within this word is determined by subaddress bits 3-0 of the current command word.

If the specified bit in the lookup table is logic "0", the command is not enabled, and the PCI Enhanced Mini-ACE will ignore this command. If this bit is logic "1", the command is enabled and the PCI Enhanced Mini-ACE will create an entry in the monitor com-

**TABLE 58. RT BIT WORD**

| BIT | DESCRIPTION |
|---|---|
| 15(MSB) | TRANSMITTER TIMEOUT |
| 14 | LOOP TEST FAILURE B |
| 13 | LOOP TEST FAILURE A |
| 12 | HANDSHAKE FAILURE |
| 11 | TRANSMITTER SHUTDOWN B |
| 10 | TRANSMITTER SHUTDOWN A |
| 9 | TERMINAL FLAG INHIBITED |
| 8 | BIT TEST FAILURE |
| 7 | HIGH WORD COUNT |
| 6 | LOW WORD COUNT |
| 5 | INCORRECT SYNC RECEIVED |
| 4 | PARITY / MANCHESTER ERROR RECEIVED |
| 3 | RT-to-RT GAP / SYNC / ADDRESS ERROR |
| 2 | RT-to-RT NO RESPONSE ERROR |
| 1 | RT-to-RT 2ND COMMAND WORD ERROR |
| 0(LSB) | COMMAND WORD CONTENTS ERROR |

**TABLE 59. TYPICAL WORD MONITOR MEMORY MAP**

| HEX ADDRESS | FUNCTION |
|---|---|
| 0000 | First Received 1553 Word |
| 0001 | First Identification Word |
| 0002 | Second Received 1553 Word |
| 0003 | Second Identification Word |
| 0004 | Third Received 1553 Word |
| 0005 | Third Identification Word |
| • • • | • • • |
| 0100 | Stack Pointer (Fixed Location - gets overwritten) |
| • • • FFFF | • • Received 1553 Words and Identification Words • • |

| TABLE 60. MONITOR SELECTION TABLE LOOKUP ADDRESS | |
|---|---|
| **BIT** | **DESCRIPTION** |
| 15(MSB) | Logic “0” |
| 14 | Logic “0” |
| 13 | Logic “0” |
| 12 | Logic “0” |
| 11 | Logic “0” |
| 10 | Logic “0” |
| 9 | Logic “1” |
| 8 | Logic “0” |
| 7 | Logic “1” |
| 6 | RTAD_4 |
| 5 | RTAD_3 |
| 4 | RTAD_2 |
| 3 | RTAD_1 |
| 2 | RTAD_0 |
| 1 | TRANSMIT / $\overline{\text{RECEIVE}}$ |
| 0(LSB) | SUBADDRESS 4 |

mand descriptor stack (based on the monitor command stack pointer), and store the data and status words associated with the command into sequential locations in the monitor data stack. In addition, for an RT-to-RT transfer in which the receive command is selected, the second command word (the transmit command) is stored in the monitor data stack.

Note: After a command is discarded the monitor will immediately look for another "Command." Where only a subset of Subaddresses are enabled, it is possible that a succeeding Status word may be captured as a "Command". This will always be flagged as an error because the Word Count or timing will fail.

The address definition for the Selective Monitor Lookup Table is illustrated in TABLE 60.

### *SELECTIVE MESSAGE MONITOR MEMORY ORGANIZATION*

A typical memory map for the PCI Enhanced Mini-ACE, in the Selective Message Monitor mode, assuming a 4K RAM space, is illustrated in TABLE 61. This mode of operation defines several fixed locations in the RAM. These locations are allocated in a way in which none of them overlap with the fixed RT locations. This allows for the combined RT/Selective Message Monitor mode.

The fixed memory map consists of two Monitor Command Stack Pointers (locations 102 and 106 hex), two Monitor Data Stack Pointers (locations 103 and 107 hex), and a Selective Message Monitor Lookup Table (locations 0280 through 02FF hex).

For this example, the Monitor Command Stack size is assumed to be 1K words, and the Monitor Data Stack size is assumed to be 2K words.

FIGURE 10 illustrates the Selective Message Monitor operation. Upon receipt of a valid Command Word, the PCI Enhanced Mini-ACE will reference the Selective Monitor Lookup Table to determine if the current command is enabled. If the current command is disabled, the PCI Enhanced Mini-ACE monitor will ignore (and not store) the current message. If the command is enabled, the monitor will create an entry in the Monitor Command Stack at the address location referenced by the Monitor Command Stack Pointer, and an entry in the monitor data stack starting at the location referenced by the monitor data stack pointer.

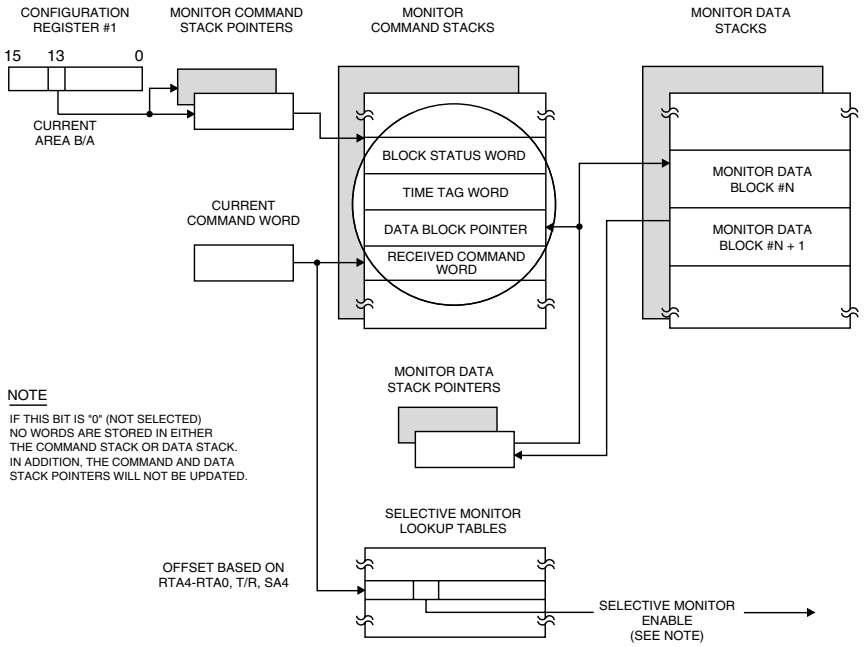



**FIGURE 10. SELECTIVE MESSAGE MONITOR MEMORY MANAGEMENT**

| TABLE 61. TYPICAL SELECTIVE MESSAGE MONITOR MEMORY MAP (shown for 4K RAM for "Monitor only" mode) | |
|---|---|
| **ADDRESS (HEX)** | **DESCRIPTION** |
| 0100-0101 | Not Used |
| 0102 | Monitor Command Stack Pointer A (fixed location) |
| 0103 | Monitor Data Stack Pointer A (fixed location) |
| 0104-0105 | Not Used |
| 0106 | Monitor Command Stack Pointer B (fixed location) |
| 0107 | Monitor Data Stack Pointer B (fixed location) |
| 0108-027F | Not Used |
| 0280-02FF | Selective Monitor Lookup Table |
| 0300-03FF | Not Used |
| 0400-07FF | Monitor Command Stack A |
| 0800-0FFF | Monitor Data Stack A |

The format of the information in the data stack depends on the format of the message that was processed. For example, for a BC-to-RT transfer (receive command), the monitor will store the command word in the monitor command descriptor stack, with the data words and the receiving RT's status word stored in the monitor data stack.

The size of the monitor command stack is programmable, with choices of 256, 1K, 4K, or 16K words. The monitor data stack size is programmable with choices of 512, 1K, 2K, 4K, 8K, 16K, 32K or 64K words.

#### *MONITOR INTERRUPTS*

Selective monitor interrupts may be issued for End-of-message and for conditions relating to the monitor command stack pointer and monitor data stack pointer. As shown in FIGURE 8, the latter includes Command Stack 50% Rollover, Command Stack 100% Rollover, Data Stack 50% Rollover, and Data Stack 100% Rollover.

The 50% rollover interrupts may be used to inform the host processor when the command stack or data stack is half full. At that time, the host may proceed to read the received messages in the upper half of the respective stack, while the PCI Enhanced Mini-ACE monitor writes messages to the lower half of the stack. Later, when the monitor issues a 100% stack rollover interrupt, the host can proceed to read the received data from the lower half of the stack, while the PCI Enhanced Mini-ACE monitor continues to write received data words to the upper half of the stack.

#### *INTERRUPT STATUS QUEUE*

Like the PCI Enhanced Mini-ACE RT, the Selective Monitor mode includes the capability for generating an interrupt status queue. As illustrated in FIGURE 9, this provides a chronological history of interrupt generating events. Besides the two Interrupt Mask Registers, the Interrupt Status Queue provides additional filtering capability, such that only valid messages and/or only invalid messages may result in entries to the Interrupt Status Queue. The interrupt status queue is 64 words deep, providing the capability to store entries for up to 32 monitored messages.

## MISCELLANEOUS

### 1553 CLOCK INPUT

The PCI Enhanced Mini-ACE decoder is capable of operating from a 10, 12, 16, or 20 MHz clock input. The clock frequency may be specified by means of the host processor writing to Configuration Register #6.

### ENCODER/DECODERS

For the selected clock frequency, there is internal logic to derive the necessary clocks for the Manchester encoder and decoders. For all clock frequencies, the decoders sample the receiver outputs on both edges of the input clock. By in effect doubling the decoders' sampling frequency, this serves to widen the tolerance to zero-crossing distortion, and reduce the bit error rate.

### TIME TAG

The PCI Enhanced Mini-ACE includes an internal read/writable Time Tag Register. This register is a CPU read/writable 16-bit counter with a programmable resolution of either 2, 4, 8, 16, 32, or 64 µs per LSB. Another option allows software controlled incrementing of the Time Tag Register. This supports self-test for the Time Tag Register. For each message processed, the value of the Time Tag Register is loaded into the second location of the respective descriptor stack entry ("TIME TAG WORD") for BC/RT/MT modes.

The functionality of the Time Tag Register is compatible with ACE/Mini-ACE (Plus) and includes: the capability to issue an interrupt request and set a bit in the Interrupt Status Register when the Time Tag Register rolls over FFFF to 0000; for RT mode, the capability to automatically clear the Time Tag Register following reception of a Synchronize (without data) mode command, or to load the Time Tag Register following a Synchronize (with data) mode command.

Additional time tag features supported by the PCI Enhanced Mini-ACE include the capability for the BC to transmit the contents of the Time Tag Register as the data word for a Synchronize (with data) mode command; the capability for the RT to "filter" the data word for the Synchronize with data mode command, by only loading the Time Tag Register if the LSB of the received data word is "0"; an instruction enabling the BC Message Sequence Control engine to autonomously load the Time Tag Register with

a specified value; and an instruction enabling the BC Message Sequence Control engine to write the value of the Time Tag Register to the General Purpose Queue.

## INTERRUPTS

The PCI Enhanced Mini-ACE series terminals provide many programmable options for interrupt generation and handling. The interrupt output pin ($\overline{INT}$) has two software programmable modes of operation: a level output cleared under software control, or a level output automatically cleared following a read of the Interrupt Status Register (#1 or #2).

Individual interrupts are enabled by the two Interrupt Mask Registers. The host processor may determine the cause of the interrupt by reading the two Interrupt Status Registers, which provide the current state of interrupt events and conditions. The Interrupt Status Registers may be updated in two ways. In one interrupt handling mode, a particular bit in Interrupt Status Register #1 or #2 will be updated only if the event occurs and the corresponding bit in Interrupt Mask Register #1 or #2 is enabled. In the enhanced interrupt handling mode, a particular bit in one of the Interrupt Status Registers will be updated if the event/condition occurs regardless of the value of the corresponding Interrupt Mask Register bit. In either case, the respective Interrupt Mask Register (#1 or #2) bit is used to enable an interrupt for a particular event/condition.

The PCI Enhanced Mini-ACE supports all the interrupt events from ACE/Mini-ACE (Plus) and Enhanced Mini-ACE including RAM Parity Error, Transmitter Timeout, BC/RT Command Stack Rollover, MT Command Stack and Data Stack Rollover, Handshake Error, BC Retry, RT Address Parity Error, Time Tag Rollover, RT Circular Buffer Rollover, BC Message, RT Subaddress, BC End-of-Frame, Format Error, BC Status Set, RT Mode Code, MT Trigger, and End-of-Message.

For the PCI Enhanced Mini-ACE's Enhanced BC mode, there are four user-defined interrupt bits. The BC Message Sequence Control Engine includes an instruction enabling it to issue these interrupts at any time.

For RT and Monitor modes, the PCI Enhanced Mini-ACE architecture includes an Interrupt Status Queue. This provides a mechanism for logging messages that result in interrupt requests. Entries to the Interrupt Status Queue may be filtered such that only valid and/or invalid messages will result in entries on the queue.

The PCI Enhanced Mini-ACE incorporates additional interrupt conditions beyond ACE/Mini-ACE (Plus), based on the addition of Interrupt Mask Register #2 and Interrupt Status Register #2. This is accomplished by chaining the two Interrupt Status Registers using the INTERRUPT CHAIN BIT (bit 0) in Interrupt Status Register #2 to indicate that an interrupt has occurred in Interrupt Status Register #1. Additional interrupts include "Self-Test Completed", masking bits for the Enhanced BC Control Interrupts, 50% Rollover interrupts for RT Command Stack, RT Circular Buffers, MT Command Stack, and MT Data Stack; BC Op Code Parity Error, (RT) Illegal Command, (BC) General Purpose Queue or (RT/MT) Interrupt Status Queue Rollover, Call Stack Pointer Register Error, BC Trap Op Code, and four User-Defined interrupts for the Enhanced BC mode.

## RAM PARITY

The BC/RT/MT version of the PCI Enhanced Mini-ACE is available with options of 4K or 64K words of internal RAM. For the 64K option, the RAM is 17 bits wide. The 64K X 17 internal RAM allows for parity generation for RAM write accesses, and parity checking for RAM read accesses. When the PCI Enhanced Mini-ACE detects a RAM parity error, it reports it to the host processor by means of an interrupt and a register bit. Also, for the RT and Selective Message Monitor modes, the RAM address(es) where a parity error(s) was detected will be stored on the Interrupt Status Queue (if enabled).

FIGURE 11 illustrates a generic connection diagram between a PCI "Initiator" and a PCI Enhanced Mini-ACE "Target."

The following timing diagrams illustrate the PCI commands that the PCI Enhanced Mini-ACE responds to. Note that these diagrams are meant to show the basic PCI bus operation of the PCI Enhanced Mini-ACE itself and do not show masters inserting wait states, masters burst reading or writing past address boundaries, masters writing into a full FIFO, etc.

To help understand the following timing diagrams an explanation of the basic architecture of the PCI Enhanced Mini-ACE is helpful. The PCI Enhanced Mini-ACE can be thought of as the very successful Enhanced Mini-ACE terminal family integrated with a 3.3V 33MHz PCI target interface. To simplify descriptions of the PCI Enhanced Mini-ACE architecture, the term ACE will be used as a substitute for "Enhanced Mini-ACE" even though the 1553 terminal function is really an Enhanced Mini-ACE. When reference is made to ACE memory (BAR0) or ACE registers (BAR1 00-FCh) these functions are part of the ACE portion of the die.

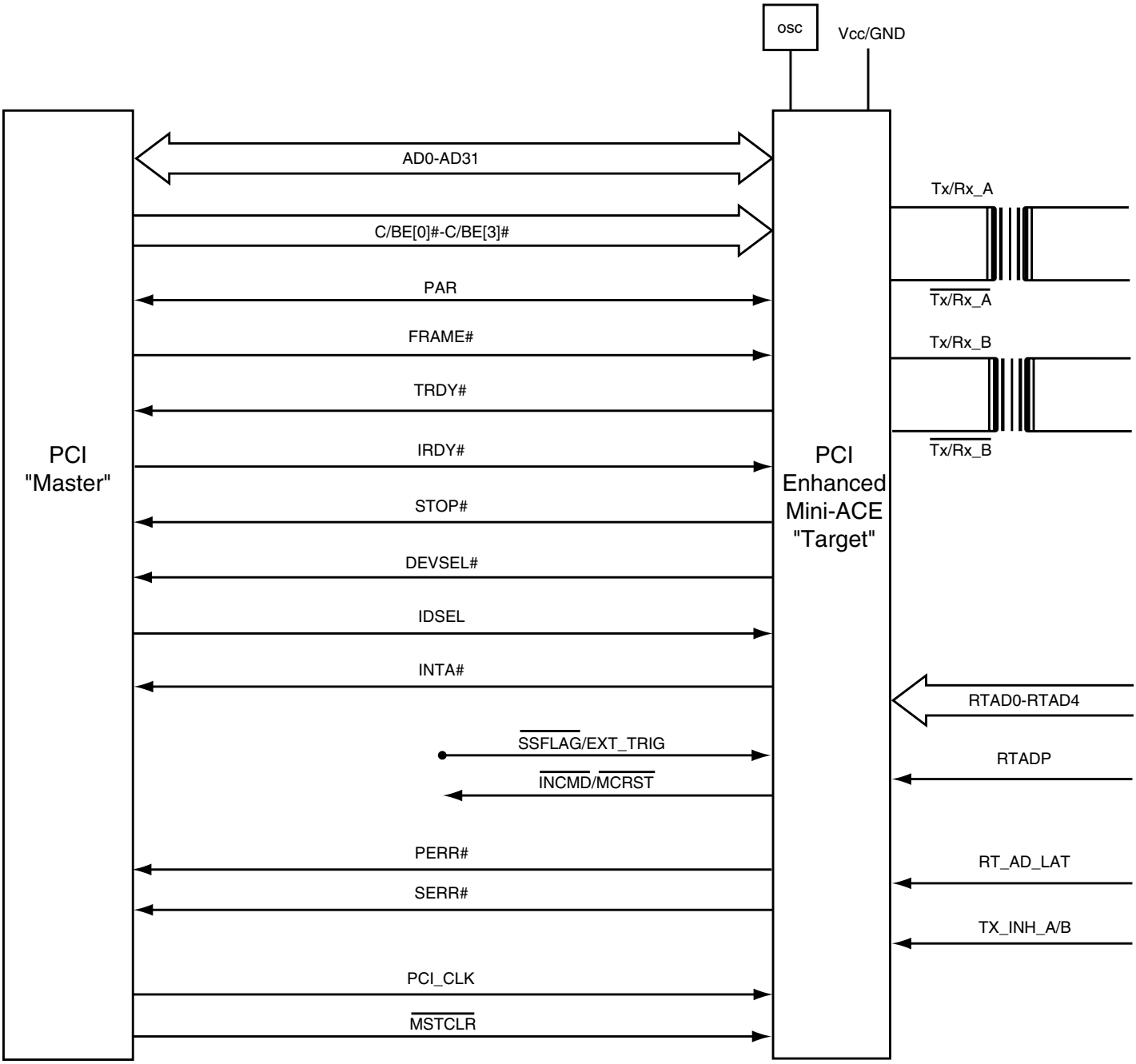
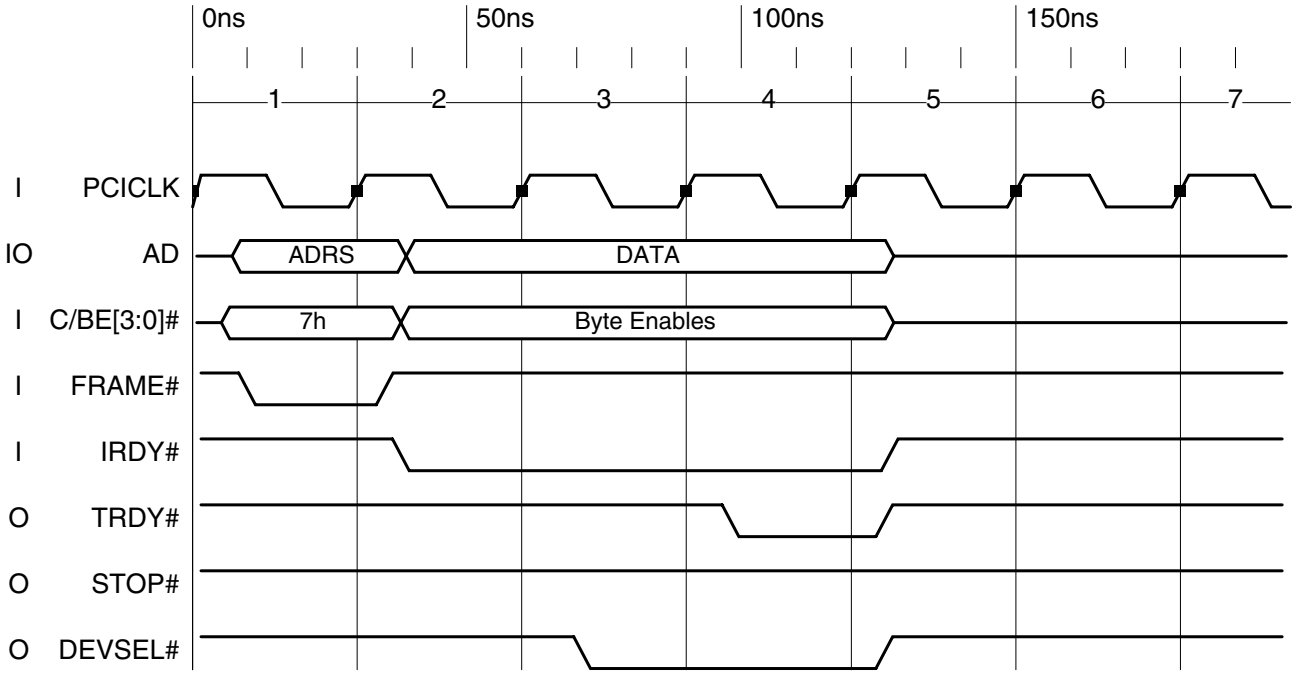



**FIGURE 11. PCI INITIATOR TO PCI ENHANCED MINI-ACE TARGET INTERFACE**

These ACE functions are accessed via the write FIFO (for writes) and delayed read request logic (for reads). The "PCI interface registers" (BAR1 800-81Ch) are part of the PCI interface portion of the die and are written and read directly from the PCI bus, without use of the write FIFO or delayed read request logic.

The PCI Enhanced Mini-ACE's basic PCI transaction takes 3 PCI clocks, on top of the command phase. For example, a single write to any location within the PCI Enhanced Mini-ACE's memory space takes 4 PCI clocks, as shown in FIGURE 12. Note that this is a single write, not an attempted burst write: FRAME# is not held asserted by the master. Also note that a write to the ACE registers or ACE memory is actually a write into the write FIFO whereas a write to the PCI interface registers (BAR1 800-81Ch) is a write to the registers themselves.




PCI single write to any legal memory location (C/BE# = 7h)

**FIGURE 12. PCI SINGLE MEMORY WRITE TO PCI ENHANCED MINI-ACE**

TABLE 62 provides the timing parameters for 3.3V PCI signaling environments applicable to the PCI Enhanced Mini-ACE, and FIGURE 13 shows the timing reference points. The timing parameters apply to the other timing diagrams, but are not illustrated. The PCI Enhanced Mini-ACE conforms to revision 2.2 of the PCI Local Bus specification. The timing parameters are provided here for ease of reference only.

**TABLE 62. PCI INTERFACE TIMINGS**

| SYMBOL | PARAMETER | MIN | MAX | UNITS |
|---|---|---|---|---|
| tv | CLK to signal valid delay | 2 | 11 | ns |
| tsu | Input setup time to CLK | 7 | | ns |
| th | Input hold time from CLK | 0 | | ns |

FIGURE 13 illustrates a PCI read from the PCI Enhanced Mini-ACE's configuration space. The PCI Enhanced Mini-ACE only responds to Type Zero configuration access: AD[1:0] must be 00 during the command phase. The PCI Enhanced Mini-ACE will drive a full Dword on the AD lines independent of which byte enables are asserted during the configuration read.

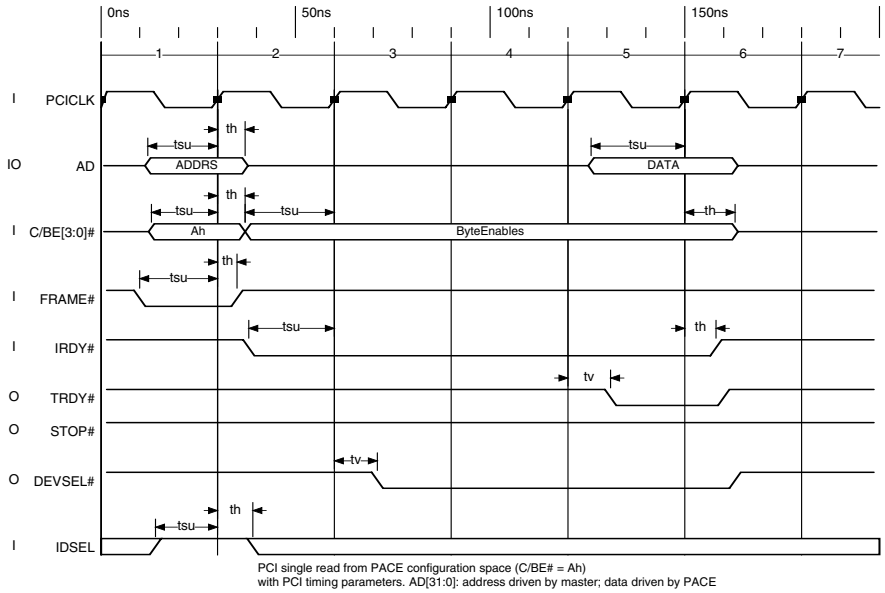



**FIGURE 13. PCI SINGLE READ OF CONFIGURATION SPACE WITH TIMING**

FIGURE 14 illustrates a PCI single write to PCI Enhanced Mini-ACE configuration space. The PCI Enhanced Mini-ACE only responds to Type Zero configuration access: AD[1:0] must be 00 during the command phase. Note that all combinations of byte enables for configuration writes are supported. If no byte enables are asserted during a burst write to configuration space no internal write will occur, but the internal address will be incremented.

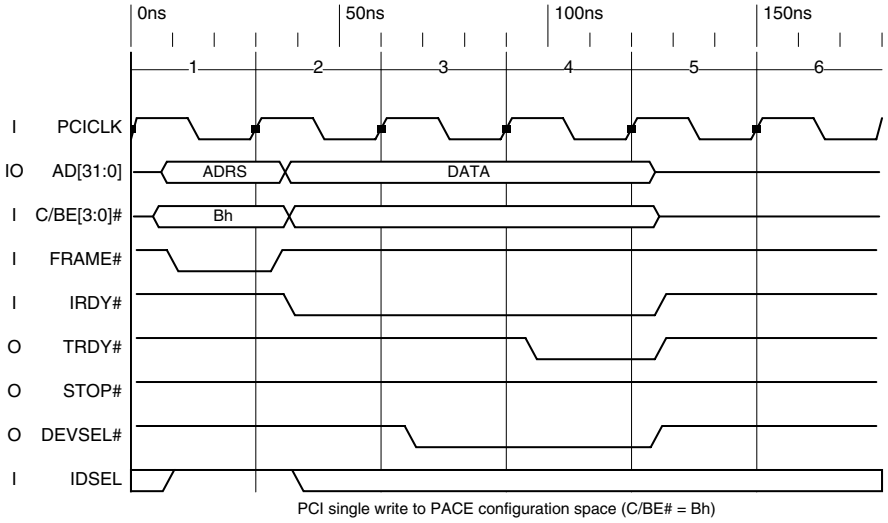
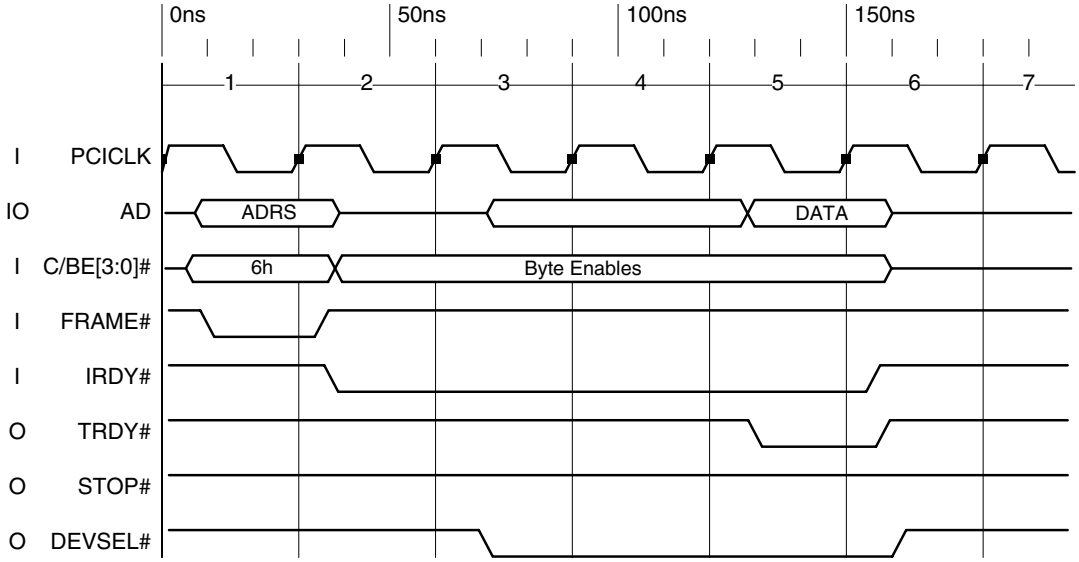



**FIGURE 14. PCI SINGLE WRITE TO CONFIGURATION SPACE**

FIGURE 15 shows the specific case of memory reads from the PCI-ACE interface registers at BAR1 800h-81Ch. Note that these registers are accessed quickly and without the Delayed Read Request (DRR) mechanism required by reads from the other memory locations (see next section).




PCI memory read from PCI-ACE interface register space (BAR1 800-81Ch)

**FIGURE 15. PCI READ OF PCI-ACE IF REGISTERS (BAR1 800-81 CH)**

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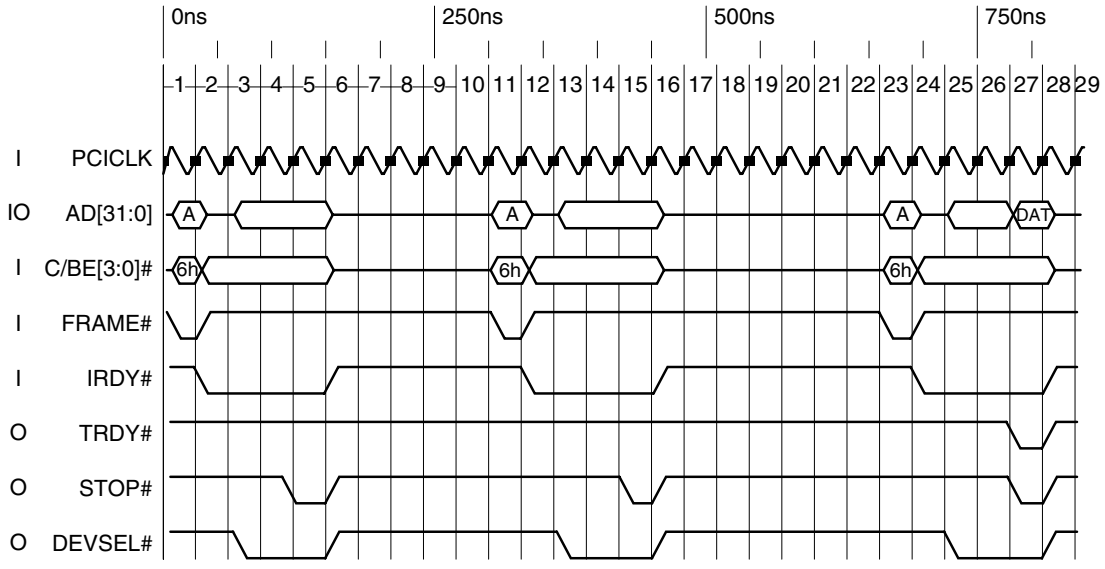
FIGURE 16 illustrates the process of reading an ACE memory (BAR0) or ACE register (BAR1 00-FCh) location. The actual read shown is that of a single word read, due to the ~600 nS response time shown, see following text and timing formula tables. If the write FIFO is empty and there isn't a previous Delayed Read Request (DRR) pending, a read from these locations enques a DRR, which is then processed by the PCI Enhanced Mini-ACE. If either of these conditions is true, the PCI Enhanced Mini-ACE will respond with a Retry, but will not enque any new DRR.




PCI memory read from ACE registers/memory with no DRR pending & FIFO empty produces Retry & enques DRR. Master should attempt read as soon as possible (preferably within 33 clocks). 3rd read produces disconnect with data, DRR complete

**FIGURE 16. PCI READ OF ACE MEMORY/REGISTER**

The PCI Enhanced Mini-ACE responds to the first read with a Retry. By PCI rules the master must repeat the same exact request until it completes. This is shown by the master's second read attempt, which also produces a Retry. Each repeated read request from the master will be target terminated with a Retry until the data from the enqued Delayed Read Request (DRR) is present in the PCI Enhanced Mini-ACE's PCI interface. The successful completion is shown at the third read request, which produces a Disconnect with Data.

This process applies to any memory read from legal address space OTHER than the PCI-ACE interface registers at BAR1 offset 800-81Ch.

Note that one of the conditions for enquing a DRR is that the write FIFO must be empty. For efficient use of PCI bus bandwidth, the driver software should be written such that it checks the FIFO condition (BAR1 800-81CH registers are directly readable, bypassing the DRR mechanism) before reading from the other PCI Enhanced Mini-ACE locations. If the FIFO is not empty (BAR1 800h bit 30 is the FIFO not empty flag) and a read is attempted, the bus master will be using PCI bandwidth repeating the read request while the FIFO empties, BEFORE the read request is actually enqued as a DRR.

When reading ACE memory (BAR0), any combination of byte enables is supported, but the PCI Enhanced Mini-ACE will drive the entire word onto the AD lines when only a single byte enable in the word is asserted.

When reading ACE registers (BAR 00-FCh), byte enable combinations where only a single byte within a word is requested will cause the PCI Enhanced Mini-ACE to terminate the transaction with a target abort. The PCI Enhanced Mini-ACE will drive all zeros onto the AD lines if only the upper word byte enables or no byte enables are asserted.

With relation to actual timing, PCI double word reads of ACE memory (BAR0) will take longer to complete than single word ACE memory reads because the internal ACE memory data path is 16 bits wide. In addition, read cycles will take longer to complete with slower ACE clocks. See TABLE 63 for min/max formulas for calculating completion time for the various types of reads.

**TABLE 63. MIN/MAX DELAYED READ FORMULAS**

| TYPE OF READ | MIN TIME FORMULA | MAX TIME FORMULA |
|---|---|---|
| ACE memory (BAR0), double word | 13 x PCI_CLKperiod + 11 x ACE_CLKperiod | 16 x PCI_CLKperiod + 14 x ACE_CLKperiod |
| ACE memory (BAR0) single word or ACE register (BAR1, double word or lower word) | 8 x PCI_CLKperiod + 5 x ACE_CLKperiod | 10 x PCI_CLKperiod + 6 x ACE_CLKperiod |
| No CBEN# asserted or ACE register (BAR1) upper word | 3 x PCI_CLKperiod | 3 x PCI_CLKperiod |

The third case returns all zeroes and is shown only for completeness.

The following examples have the same conditions: PCI clock = 33MHz, ACE clock = 16MHz, no ACE contention.

Single word read
Min time = 8 x 30 nS + 5 x 62.5 nS = 552.5 nS
Max time = 10 x 30nS + 6 x 62.5 nS = 675 nS

Double word read
Min time = 13 x 30 nS + 11 x 62.5 nS = 1077.5 nS
Max time = 16 x 30nS + 14 x 62.5 nS = 1167.5 nS

In addition, see TABLE 64 for the amount of ACE clocks that should be added for maximum time if the ACE is active.

**TABLE 64. ADDITIONAL DRR DELAY FOR CONTESTED ACE RAM ACCESS**

| ACE OPERATING MODE | MAXIMUM ADDITIONAL ACE CLOCKS |
|---|---|
| Enhanced CPU access enabled, single word xfer | 3 |
| Enhanced CPU access enabled, double word xfer | 6 |
| Enhanced CPU access disabled, single word xfer | 67 |
| Enhanced CPU access disabled, double word xfer | 74 |

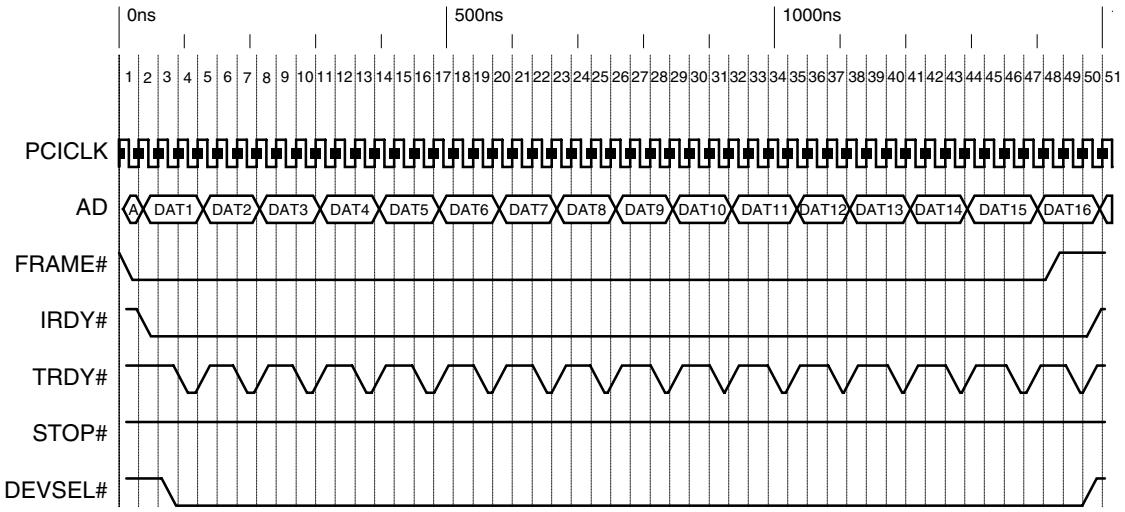
The Enhanced CPU access is controlled by bit 14 of Configuration Register #6.

FIGURE 17 illustrates a 16 Dword (32 word) PCI memory write burst, with the write FIFO empty (or with enough free space to absorb the 16 Dwords in the FIFO). The write FIFO accepts PCI memory writes to the ACE memory (BAR0) and ACE registers (BAR1 offset 00h - FCh). It does not accept writes to the PCI interface registers at BAR1 offset 800-81Ch. Writes to the BAR1 800-81Ch space go directly into the PCI interface registers. The 32 byte write shown could be an entire 1553 message being written to ACE memory.

- Writes into the BAR 0 space must be word or Dword. If only one byte enable is asserted in a word, the PCI Enhanced Mini-ACE terminates the transaction with a Target-Abort.

- Writes into the BAR 1 00-FCh space must be word or Dword. If only one byte enable is asserted in a word, the PCI Enhanced Mini-ACE terminates the transaction with a Target-Abort. Since the ACE registers in this space are really 16 bit registers packed into the lower word of a 32 bit structure, only lower word or Dword writes transfer bits into these ACE registers.

- In addition, as per PCI spec, a Memory Write and Invalidate (C/BE[3:0]# = Fh) command will be aliased to the basic Memory Write command and the timing diagram would look the same as FIGURE 17.




PCI write burst to ACE memory with FIFO empty

**FIGURE 17. PCI WRITE BURST TO ACE MEMORY WITH FIFO EMPTY**

## INTERFACE TO MIL-STD-1553 BUS

FIGURE 18 illustrates the interface between the PCI Enhanced Mini-ACE, and a MIL-STD-1553 bus. Connections for both direct (short stub) and transformer (long stub) coupling, as well as the peak-to-peak voltage levels at various points (when transmitting), are indicated in the diagram.

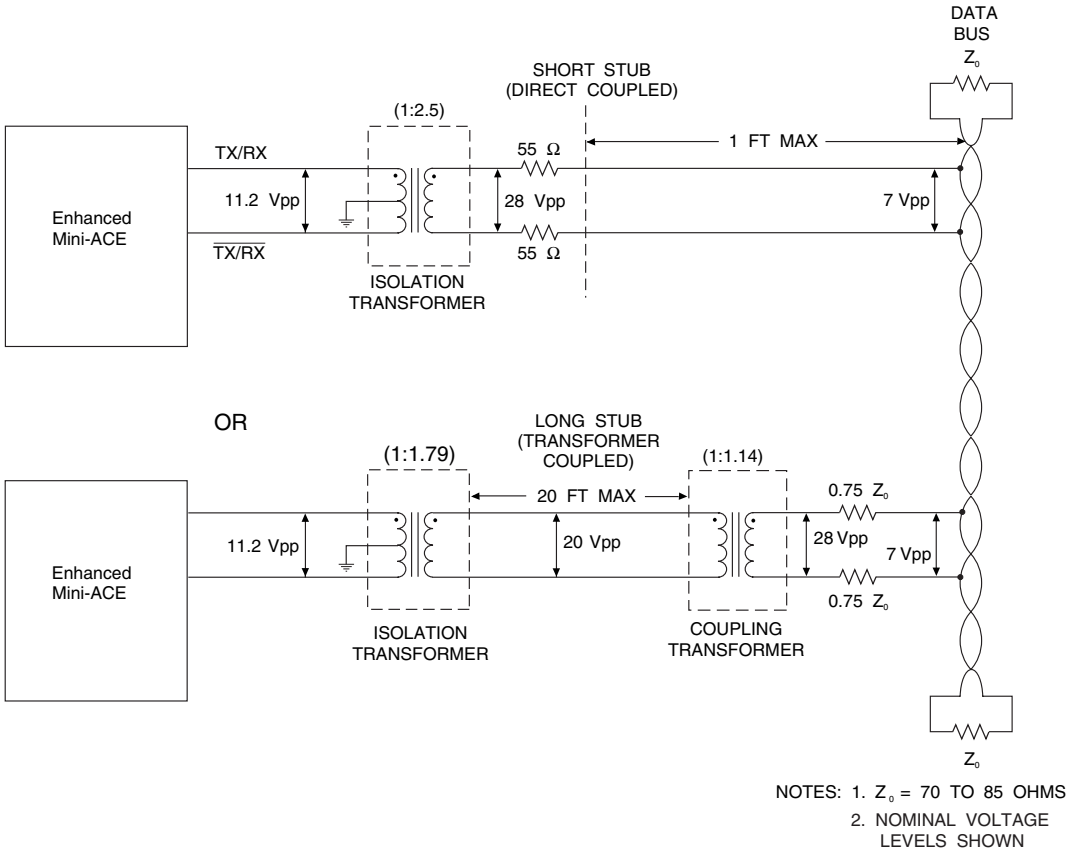



**FIGURE 18. PCI ENHANCED MINI-ACE INTERFACE TO MIL-STD-1553 BUS**

## TRANSFORMERS

In selecting isolation transformers to be used with the PCI Enhanced Mini-ACE, there is a limitation on the maximum amount of leakage inductance. If this limit is exceeded, the transmitter rise and fall times may increase, possibly causing the bus amplitude to fall below the minimum level required by MIL-STD-1553. In addition, an excessive leakage inductance imbalance may result in a transmitter dynamic offset that exceeds 1553 specifications.

The maximum allowable leakage inductance is 6.0uH. It is measured as follows:

Defining the side of the transformer that connects to the PCI Enhanced Mini-ACE as the "primary" winding, if one side of the primary is shorted to the primary center-tap, the inductance should be measured across the "secondary" (stud side) winding. This inductance must be less than 6.0µH. Similarly, if the other side of the primary is shorted to the primary center-tap, the inductance measured across the "secondary" (stub side) winding must also be less than 6.0µH.

The difference between those two measurement is the "differential" leakage inductance. This value must be less than 1.0uH.

Beta Transformer Technology Corporation (BTTC), a subsidiary of DDC, manufactures transformers in a variety of mechanical configurations with the required turns ratios of 1:2.5 direct coupled, and 1:1.79 transformer coupled. TABLE 65 provides a listing of many of these transformers.

For further information, contact BTTC at 631-244-7393 or at www.bttc-beta.com.

**TABLE 65. BTTC TRANSFORMERS FOR USE WITH ENHANCED MINI-ACE**

| BTTC PART NUMBER | # OF CHANNELS, CONFIGURATION | COUPLING RATIO DESCRIPTION | COUPLING RATIO (1:X) | MOUNTING | MAX HEIGHT | WIDTH (INCLUDING LEADS) | LENGTH (INCLUDING LEADS) |
|---|---|---|---|---|---|---|---|
| MLP-2005 | Single | Direct | (1:2.5) | SMT | 0.185" | 0.4" | 0.52" |
| MLP-3005 | Single | Direct | (1:2.5) | Through Hole | 0.185" | 0.4" | 0.4" |
| B-3230 (-30) # | Single | Direct | (1:2.5) | Through Hole | 0.25" | 0.35" | 0.5" |
| MLP-2205 | Single | Transformer | (1:1.79) | SMT | 0.185" | 0.4" | 0.52" |
| MLP-3205 | Single | Transformer | (1:1.79) | Through Hole | 0.185" | 0.4" | 0.4" |
| B-3229 (-29) # | Single | Transformer | (1:1.79) | Through Hole | 0.25" | 0.35" | 0.5" |
| HLP-6015 # | Single | Direct & Transformer | (1:2.5) & (1:1.79) | SMT | 0.19" | 0.63" | 1.13" |
| B-3227 (-27) # | Single | Direct & Transformer | (1:2.5) & (1:1.79) | SMT | 0.29" | 0.63" | 1.13" |
| MLP-3305 | Single | Direct & Transformer | (1:2.5) & (1:1.79) | Through Hole | 0.185" | 0.4" | 0.4" |
| B-3226 (-26) # | Single | Direct & Transformer | (1:2.5) & (1:1.79) | Through Hole | 0.25" | 0.625" | 0.625" |
| HLP-6014 # | Single | Direct & Transformer | (1:2.5) & (1:1.79) | Flat Pack | 0.19" | 0.63" | 1.13" |
| B-3231 (-31) # | Single | Direct & Transformer | (1:2.5) & (1:1.79) | Flat Pack | 0.29" | 0.63" | 1.13" |
| DSS-2005 | Dual (Side-by-Side) | Direct | (1:2.5) | SMT | 0.13" | 0.72" | 0.96" |
| DSS-2205 | Dual (Side-by-Side) | Transformer | (1:1.79) | SMT | 0.13" | 0.72" | 0.96" |
| DSS-1005 | Dual (Side-by-Side) | Direct & Transformer | (1:2.5) & (1:1.79) | SMT | 0.165" | 0.72" | 0.96" |
| TSM-2005 | Dual (Stacked) | Direct | (1:2.5) | SMT | 0.32" | 0.4" | 0.52" |
| TSM-2205 | Dual (Stacked) | Transformer | (1:1.79) | SMT | 0.32" | 0.4" | 0.52" |
| TST-9117 # | Dual (Stacked) | Direct & Transformer | (1:2.5) & (1:1.79) | SMT | 0.335" | 1.125" | 1.125" |
| TST-9107 # | Dual (Stacked) | Direct & Transformer | (1:2.5) & (1:1.79) | Through Hole | 0.335" | 0.625" | 0.625" |
| TST-9127 # | Dual (Stacked) | Direct & Transformer | (1:2.5) & (1:1.79) | Flat Pack | 0.335" | 0.625" | 0.625" |

Notes:
1. All Transformers in the table above can be used with BU-6XXXXX3/6 (1553B transceivers).
2. Transformers identified with "#" in the table above are not recommended for use with the BU-6XXXXX4 (McAir-Compatable transceivers)

**TABLE 66. POWER AND GROUND**

| SIGNAL NAME | PIN | | DESCRIPTION |
|---|---|---|---|
| | BU-62864 (64K RAM) | BU-62843/62743 (4K RAM) | |
| +5V Vcc CH A | 72 | 72 | Channel A transceiver power. |
| +5V Vcc CH B | 20 | 20 | Channel B transceiver power. |
| +3.3V Logic | 37 | 37 | Logic power. For BU-62864/62843/62743, this pin must be connected to **+3.3V**. |
| +5V RAM | 26 | — | For BU-62864 this pin must be connected to +5V. |
| Ground | 17 | 17 | Ground. |
| | 18 | 18 | |
| | 19 | 19 | |
| | 65 | 65 | |
| | 67 | 67 | |

**TABLE 67. 1553 ISOLATION TRANSFORMER INTERFACE (4)**

| SIGNAL NAME | PIN (F & G PACKAGE) | DESCRIPTION |
|---|---|---|
| TX/RX_A (I/O) | 5 | Analog Transmit/Receive Inputs/Outputs. Connect directly to 1553 isolation transformers. |
| $\overline{\text{TX/RX\_A}}$ (I/O) | 7 | |
| TX/RX_B (I/O) | 13 | |
| $\overline{\text{TX/RX\_B}}$ (I/O) | 16 | |

**TABLE 68. PROCESSOR INTERFACE CONTROL**

| SIGNAL NAME | PIN (F & G PACKAGE) | DESCRIPTION |
|---|---|---|
| $\overline{\text{SSFLAG}}$ (I) / EXT_TRIG(I) | 14 | Subsystem Flag (RT) or External Trigger (BC/Word Monitor) input. In RT mode, if this input is asserted low, the Subsystem Flag bit will be set in the PCI ENHANCED Mini-ACE's RT Status Word. If the $\overline{\text{SSFLAG}}$ input is logic "0" while bit 8 of Configuration Register #1 has been programmed to logic "1" (cleared), the Subsystem Flag RT Status Word bit will become logic "1," but bit 8 of Configuration Register #1, $\overline{\text{SUBSYSTEM FLAG}}$, will return logic "1" when read. That is, the sense on the $\overline{\text{SSFLAG}}$ input has no effect on the $\overline{\text{SUBSYSTEM FLAG}}$ register bit.<br><br>In the non-enhanced BC mode, this signal operates as an External Trigger input. In BC mode, if the external BC Start option is enabled (bit 7 of Configuration Register #1), a low to high transition on this input will issue a BC Start command, starting execution of the current BC frame.<br><br>In the enhanced BC mode, during the execution of a Wait for External Trigger (WTG) instruction, the PCI Enhanced Mini-ACE BC will wait for a low-to-high transition on EXT_TRIG before proceeding to the next instruction.<br><br>In the Word Monitor mode, if the external trigger is enabled (bit 7 of Configuration Register #1), a low to high transition on this input will initiate a monitor start. (RT the monitor on low).<br><br>This input has no effect in Message Monitor mode. |

| TABLE 69. RT ADDRESS | | |
|---|---|---|
| **SIGNAL NAME** | **PIN (F & G PACKAGE)** | **DESCRIPTION** |
| RTAD4 (MSB) (I) | 8 | RT Address inputs. If bit 5 of Configuration Register #6, RT ADDRESS SOURCE, is programmed to logic "0" (default), then the PCI Enhanced Mini-ACE's RT address is provided by means of these 5 input signals. In addition, if RT ADDRESS SOURCE is logic "0", the source of RT address parity is RTADP.<br><br>There are many methods for using these input signals for designating the PCI Enhanced Mini-ACE's RT address. For details, refer to the description of RT_AD_LAT.<br><br>If RT ADDRESS SOURCE is programmed to logic "1", then the PCI Enhanced Mini-ACE's source for its RT address and parity is under software control, via data lines D5-D0. In this case, the RTAD4-RTAD0 and RTADP signals are not used. |
| RTAD3 (I) | 6 | |
| RTAD2 (I) | 4 | |
| RTAD1 (I) | 3 | |
| RTAD0 (LSB) (I) | 1 | |
| RTADP | 10 | Remote Terminal Address Parity. This input signal must provide an odd parity sum with RTAD4-RTAD0 in order for the RT to respond to non-broadcast commands. That is, there must be an **odd** number of logic "1"s from among RTAD-4-RTAD0 and RTADP. |
| RT_AD_LAT (I) | 11 | RT Address Latch. Input signal used to control the PCI Enhanced Mini-ACE's internal RT address latch. If RT_AD_LAT is connected to logic "0", then the PCI Enhanced Mini-ACE RT is configured to accept a hardwired (transparent) RT address from RTAD4-RTAD and RTADP.<br><br>If RT_AD_LAT is initially logic "0", and then transitions to logic "1", the values presented on RTAD4-RTAD0 and RTADP will be latched internally on the rising edge of RT_AD_LAT.<br><br>If RT_AD_LAT is connected to logic "1", then the PCI Enhanced Mini-ACE's RT address is latchable under host processor control. In this case, there are two possibilities: (1) If bit 5 of Configuration Register #6, RT ADDRESS SOURCE, is programmed to logic "0" (default), then the source of the RT Address is the RTAD4-RTAD0 and RTADP input signals; (2) If RT ADDRESS SOURCE is programmed to logic "1", then the source of the RT Address is the lower 6 bits of the processor data bus, D5-D1 (for RTAD4-0) and D0 (for RTADP).<br><br>In **either** of these two cases (with RT_AD_LAT = "1"), the processor will cause the RT address to be latched by: (1) writing bit 15 of Configuration Register #3, ENHANCED MODE, to logic "1"; (2) writing bit 3 of Configuration Register #4, LATCH RT ADDRESS WITH CONFIGURATION REGISTER #5, to logic "1"; and (3) writing to Configuration Register #5. In the case of RT ADDRESS SOURCE = "1", then the values of RT address and RT address parity must be written to the lower 6 bits of Configuration Register #5, via D5-D0. In the case where RT ADDRESS SOURCE = "0", the bit values presented on D5-D0 become "don't care" . |

| TABLE 70. MISCELLANEOUS | | | |
|---|---|---|---|
| **SIGNAL NAME** | **PIN (F & G PACKAGE)** | | **DESCRIPTION** |
| | **BU-62864 (64K RAM)** | **BU-62843/62743 (4K RAM)** | |
| $\overline{\text{INCMD}}$ (O) / $\overline{\text{MCRST}}$ (O) | 12 | 12 | In-command or Mode Code Reset. The function of this pin is controlled by bit 0 of Configuration Register #7, MODE CODE $\overline{\text{RESET}}$/$\overline{\text{INCMD}}$ SELECT.<br><br>If this register bit is logic "0" (default), $\overline{\text{INCMD}}$ will be active on this pin. For BC, RT, or Selective Message Monitor modes, $\overline{\text{INCMD}}$ is asserted low whenever a message is being processed by the PCI Enhanced Mini-ACE. In Word Monitor mode, $\overline{\text{INCMD}}$ will be asserted low for as long as the monitor is online.<br><br>For RT mode, if MODE CODE RESET/$\overline{\text{INCMD}}$ SELECT is programmed to logic "1", $\overline{\text{MCRST}}$ will be active. In this case, $\overline{\text{MCRST}}$ will be asserted low for two clock cycles following receipt of a Reset remote terminal mode command.<br><br>In BC or Monitor modes, if MODE CODE RESET/$\overline{\text{INCMD}}$ SELECT is logic "1", this signal is inoperative; i.e., in this case, it will always output a value of logic "1". |
| CLOCK_IN (I) | 9 | 9 | 20 MHz, 16 MHz, 12 MHz, or 10 MHz clock input. |
| TX_INH_A/B (I) | 15 | 15 | Transmitter inhibit input for the Channel A and Channel B MIL-STD-1553 transmitters. For normal operation, this input should be connected to logic "0". To force a shutdown of Channel A and Channel B, a value of logic "1" should be applied to the TX_INH input. |
| $\overline{\text{MSTCLR}}$(I) | 2 | 2 | Master Clear. Negative true Reset input, normally asserted low following power turn-on. When coming out of a “reset” condition, please note that the rise time of $\overline{\text{MSTCLR}}$ must be less than 10µs. |

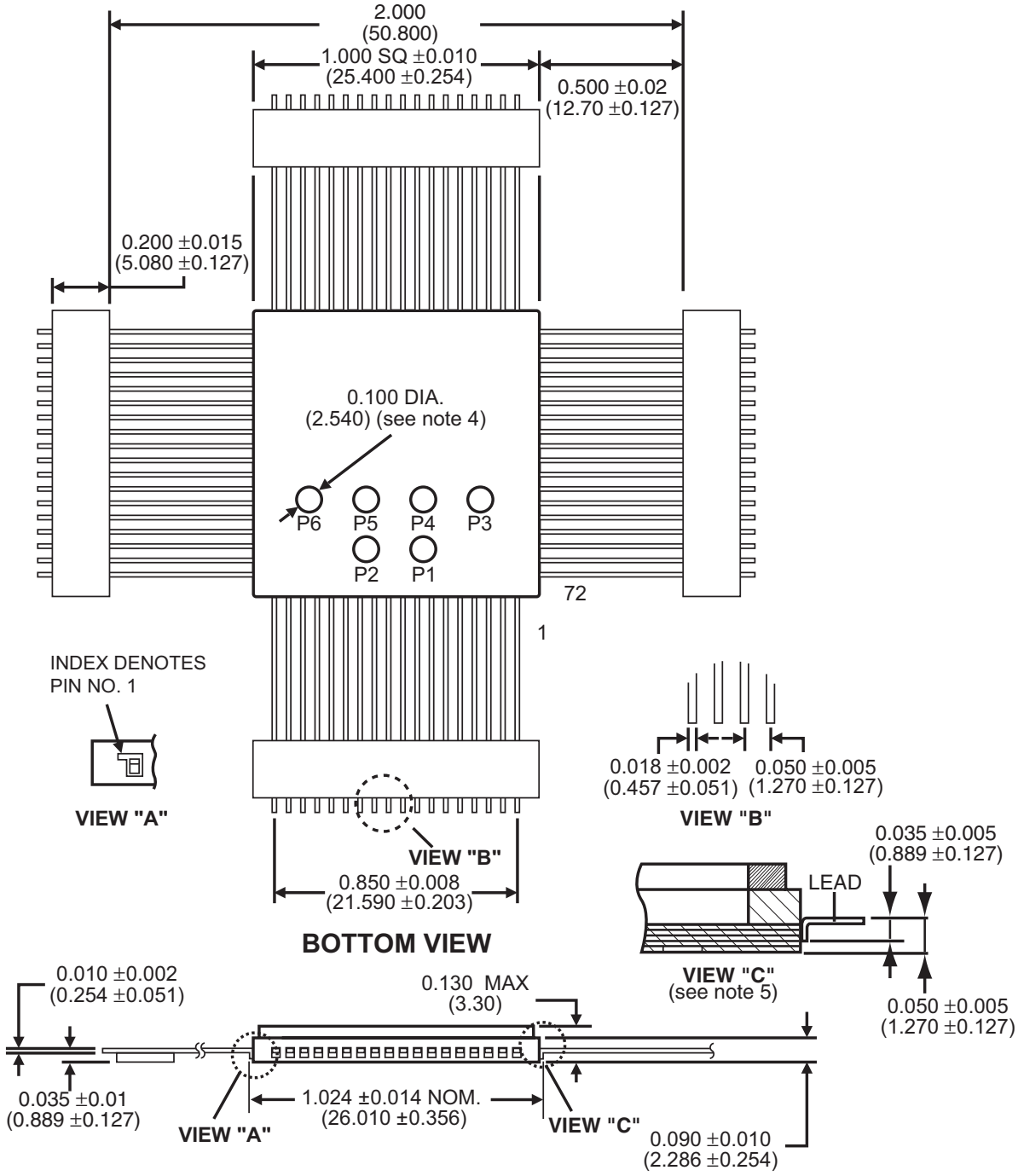
| TABLE 71. PCI BUS ADDRESS AND DATA SIGNALS | | |
|---|---|---|
| **SIGNAL NAME** | **PIN (F & G PACKAGE)** | **DESCRIPTION** |
| AD31 (I/O) (MSB) | 22 | 32-Bit PCI Bus Address / Data lines. Address and Data are multiplexed on the same pins. Each bus operation consists of an address phase followed by one or more data phases.<br><br>Address phases are identified when the control signal FRAME# is asserted. Data transfers occur during those clock cycles in which the control signals IRDY# and TRDY# are both asserted. |
| AD30 (I/O) | 23 | |
| AD29 (I/O) | 24 | |
| AD28 (I/O) | 25 | |
| AD27 (I/O) | 27 | |
| AD26 (I/O) | 28 | |
| AD25 (I/O) | 29 | |
| AD24 (I/O) | 31 | |
| AD23 (I/O) | 34 | |
| AD22(I/O) | 35 | |
| AD21 (I/O) | 36 | |
| AD20 (I/O) | 38 | |
| AD19 (I/O) | 39 | |
| AD18 (I/O) | 40 | |
| AD17 (I/O) | 41 | |
| AD16 (I/O) | 42 | |
| AD15 (I/O) | 53 | |
| AD14 (I/O) | 54 | |
| AD13 (I/O) | 55 | |
| AD12 (I/O) | 56 | |
| AD11 (I/O) | 57 | |
| AD10 (I/O) | 58 | |
| AD9 (I/O) | 59 | |
| AD8 (I/O) | 60 | |
| AD7 (I/O) | 62 | |
| AD6 (I/O) | 63 | |
| AD5 (I/O) | 64 | |
| AD4 (I/O) | 66 | |
| AD3 (I/O) | 68 | |
| AD2 (I/O) | 69 | |
| AD1 (I/O) | 70 | |
| AD0 (I/O) (LSB) | 71 | |

| TABLE 71. PCI BUS ADDRESS AND DATA SIGNALS (CONTINUED) | | |
|---|---|---|
| **SIGNAL NAME** | **PIN (F & G PACKAGE)** | **DESCRIPTION** |
| C/BE[3]# (I) | 32 | Bus Command and Byte Enables. These signals are multiplexed on the same pins. During the address phase of a bus operation, these pins identify the bus command, as shown in the table below. During the data phase of a bus operation, these pins are used as Byte Enables, with C/BE[0]# enabling byte 0 (LSB) and C/BE[3]# enabling byte 3 (MSB). The PCI Enhanced Mini-ACE responds to the following PCI commands:<br>**C/BE[3:0]#** — **DESCRIPTION (DURING ADDRESS PHASE)**<br>0 1 1 0 — Memory Read<br>0 1 1 1 — Memory Write<br>1 0 1 0 — Configuration Read<br>1 0 1 1 — Configuration Write<br>1 1 0 0 — Memory Read Multiple<br>1 1 1 0 — Memory Read Line<br>1 1 1 1 — Memory Write and Invalidate<br>Note that the last three memory commands are aliased to the basic memory commands: Memory Read and Memory Write. |
| C/BE[2]# (I) | 43 | |
| C/BE[1]# (I) | 52 | |
| C/BE[0]# (I) | 61 | |
| PAR (I/O) | 51 | Parity. This signal is even parity across the entire AD[31:0] field along with the C/BE[3:0]# field. The parity is stable in the clock following the address phase and is sourced by the Bus Master. During the data phase for write operations, the Bus Master sources this signal on the clock following IRDY# active. During the data phase for read operations, this signal is sourced by the Target and is valid on the clock following TRDY# active. The PAR signal therefore has the same timing as AD[31:0], delayed by one clock. |
| PCI_CLK (I) | 30 | Clock input. The rising edge of this signal is the reference upon which all other clock signals are based, with the exception of RST# and INTA#. The maximum frequency accepted is 33 MHz and the minimum is 0 Hz. |

| TABLE 72. PCI BUS CONTROL SIGNALS<br>(Note that all signals listed, except INTA#, are sampled on the rising edge of PCI_CLK) | | |
|---|---|---|
| **SIGNAL NAME** | **PIN (F & G PACKAGE)** | **DESCRIPTION** |
| FRAME# (I) | 44 | Frame. This signal is driven by the current bus master and identifies both the beginning and duration of a bus operation. When FRAME# is first asserted, it indicates that a bus transaction is beginning and that valid addresses and a corresponding bus command are present on the AD[31:0] and C/BE[3:0] lines, qualified by PCI_CLK. When FRAME# is deasserted the transaction is in the final data phase or has been completed. |
| IRDY# (I) | 45 | Initiator Ready. This signal is sourced by the bus master and indicates that the bus master is able to complete the current data phase of a bus transaction. For write operations, it indicates that valid data is on the AD[31:0] pins. Wait states occur until both TRDY# and IRDY# are asserted together. |
| TRDY# (O) | 46 | Target Ready. This signal is sourced by the selected target and indicates that the target is able to complete the current data phase of a bus transaction. For read operations, it indicates that the target is providing valid data on the AD[31:0] pins. Wait states occur until both TRDY# and IRDY# are asserted together. |
| STOP# (O) | 48 | Stop. The Stop signal is sourced by the selected target and conveys a request to the bus master to stop the current transaction. |
| IDSEL (I) | 33 | Initialization Device Select. This pin is used as a chip select during configuration read or write operations. |
| DEVSEL# (O) | 47 | Device Select. This signal is sourced by an active target upon decoding that its address and bus commands are valid. For bus masters, it indicates whether any device has decoded the current bus cycle. |
| PERR# (O) | 49 | Parity Error. This pin is used for reporting parity errors during the data portion of the bus transaction for all cycles except a Special Cycle. It is sourced by the agent receiving data and driven active two clocks following the detection of an error. This signal is driven inactive (high) two clocks prior to returning to the tristate condition. |
| SERR# (O) | 50 | System Error. This pin is used for reporting address parity errors, data parity errors on Special Cycle commands, or any other condition having a catastrophic system impact. |
| INTA# (O) | 21 | Interrupt A. This pin is a level sensitive, active low interrupt to the host. |

| TABLE 73. BU-62864 PCI ENHANCED MINI-ACE PINOUT | | | |
|---|---|---|---|
| (PIN) F & G PACKAGE | SIGNAL NAME | (PIN) F & G PACKAGE | SIGNAL NAME |
| 1 | RTAD0 | 43 | C/BE[2]# |
| 2 | $\overline{\text{MSTCLR}}$ | 44 | FRAME# |
| 3 | RTAD1 | 45 | IRDY# |
| 4 | RTAD2 | 46 | TRDY# |
| 5 | TX/RX_A | 47 | DEVSEL# |
| 6 | RTAD3 | 48 | STOP# |
| 7 | $\overline{\text{TX/RX\_A}}$ | 49 | PERR# |
| 8 | RTAD4 | 50 | SERR# |
| 9 | CLOCK_IN | 51 | PAR |
| 10 | RTADP | 52 | C/BE[1]# |
| 11 | RT_ADDR_LAT | 53 | AD15 |
| 12 | $\overline{\text{INCMD}}$/$\overline{\text{MCRST}}$ | 54 | AD14 |
| 13 | TX/RX_B | 55 | AD13 |
| 14 | $\overline{\text{SSFLAG}}$/EXT_TRIG | 56 | AD12 |
| 15 | TX_INH_A/B | 57 | AD11 |
| 16 | $\overline{\text{TX/RX\_B}}$ | 58 | AD10 |
| 17 | GROUND | 59 | AD9 |
| 18 | GROUND | 60 | AD8 |
| 19 | GROUND | 61 | C/BE[0]# |
| 20 | +5V Vcc CH B | 62 | AD7 |
| 21 | INTA# | 63 | AD6 |
| 22 | AD31 | 64 | AD5 |
| 23 | AD30 | 65 | GROUND |
| 24 | AD29 | 66 | AD4 |
| 25 | AD28 | 67 | GROUND |
| 26 | +5V RAM (See Note) | 68 | AD3 |
| 27 | AD27 | 69 | AD2 |
| 28 | AD26 | 70 | AD1 |
| 29 | AD25 | 71 | AD0 |
| 30 | PCI_CLOCK | 72 | +5V Vcc CH A |
| 31 | AD24 | | |
| 32 | C/BE[3]# | | |
| 33 | IDSEL | | |
| 34 | AD23 | | |
| 35 | AD22 | | |
| 36 | AD21 | | |
| 37 | +3.3V LOGIC | | |
| 38 | AD20 | | |
| 39 | AD19 | | |
| 40 | AD18 | | |
| 41 | AD17 | | |
| 42 | AD16 | | |

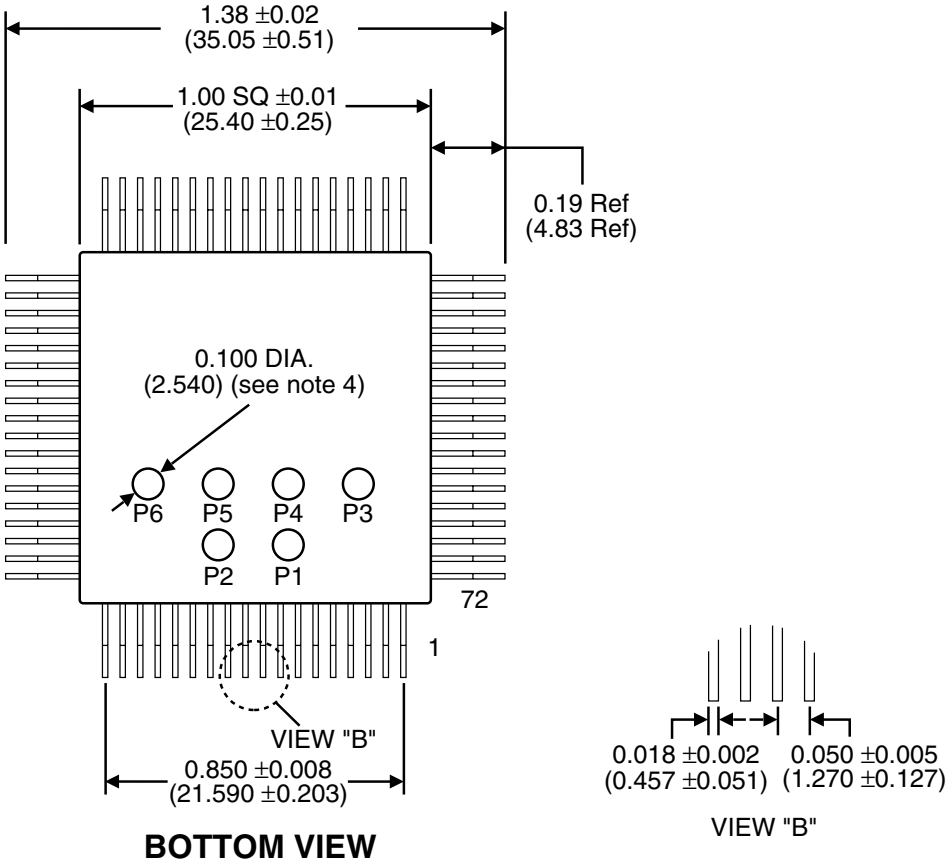
Note: Pin 26 is +5V-RAM for BU-62864. It is “N/C” for BU-62743 and BU-62843.

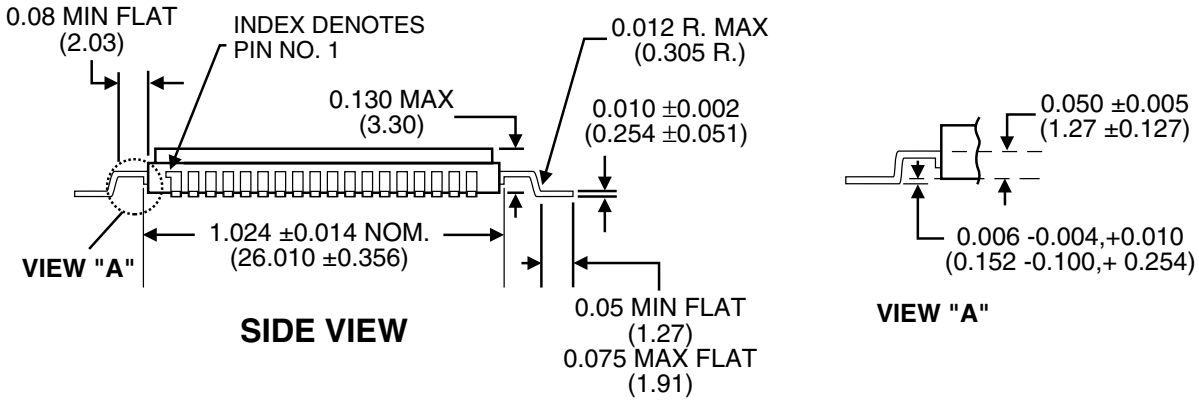



## SIDE VIEW

Notes:
1) Dimensions are in inches (mm).
2) Package Material: Alumina ($AL_2O_3$)
3) Lead Material: Kovar, Plated by 50m in. minimum nickel under 60m in. minimum gold.
4) There are 6 test pads located on the bottom of the package. These pads are recessed so as not to interfere when mounting the hybrid. There are no user connections to these pads.
5) Measurement shall be made 0.050” (1.27 mm) from the package body.

**FIGURE 19. MECHANICAL OUTLINE DRAWING FOR 72-LEAD FLATPACK**




Notes:
1) Dimensions are in inches (mm).
2) Package Material: Alumina ($AL_2O_3$)
3) Lead Material: Kovar, Plated by 50µ in. minimum nickel under 60µ in. minimum gold.
4) There are 6 test pads located on the bottom of the package. These pads are recessed so as not to interfere when mounting the hybrid. There are no user connections to these pads.

**FIGURE 20. MECHANICAL OUTLINE DRAWING FOR 72-PIN GULL LEAD PACKAGE**

## ORDERING INFORMATION

**BU-6274 3 F 3-1 2 0 X**

**Supplemental Process Requirements:**
- S = Pre-Cap Source Inspection
- L = 100% Pull Test
- Q = 100% Pull Test and Pre-Cap Source Inspection
- K = One Lot Date Code
- W = One Lot Date Code and Pre-Cap Source Inspection
- Y = One Lot Date Code and 100% Pull Test
- Z = One Lot Date Code, Pre-Cap Source Inspection, and 100% Pull test
- Blank = None of the Above

**Test Criteria:**
- 0 = Standard Testing
- 1 = X-Ray
- 2 = MIL-STD-1760 Amplitude Compliant (not available with Voltage/Transceiver Option 4 “McAir compatible”)
- 3 = MIL-STD-1760 and X-Ray

**Process Requirements:**
- 0 = Standard DDC Processing, no Burn-In (see table on next page)
- 1 = MIL-PRF-38534 Compliant (note 2)
- 2 = B
- 3 = MIL-PRF-38534 Compliant (note 2) with PIND Testing
- 4 = MIL-PRF-38534 Compliant (note 2) with Solder Dip
- 5 = MIL-PRF-38534 Compliant (note 2) with PIND Testing and Solder Dip
- 6 = B (note 1) with PIND Testing
- 7 = B (note 1) with Solder Dip
- 8 = B (note 1) with PIND Testing and Solder Dip
- 9 = Standard DDC Processing with Solder Dip, no Burn-In

**Temperature Grade/Data Requirements:**
- 1 = -55°C to +125°C
- 2 = -40°C to +85°C
- 3 = 0°C to +70°C
- 4 = -55°C to +125°C with Variables Test Data
- 5 = -40°C to +85°C with Variables Test Data
- 6 = Custom Part (Reserved)
- 7 = Custom Part (Reserved)
- 8 = 0°C to +70°C with Variables Test Data

**Voltage/Transceiver Option:**
- 3 = +5 volt, rise/fall times = 100 to 300 ns (-1553B)
- 4 = +5 volt, rise/fall times = 200 to 300 ns (-1553B and McAir compatible)

  Note: Not available with Test Criteria option “2” MIL-STD-1760 Amplitude Compliant.

**Package Type:**
- F = Flat Pack
- G = "Gull Wing" (Formed Lead)

**Logic/RAM Voltage:**
- 3 = 3.3 Volt (Applicable only for BU-62743 and BU-62843)
- 4 = 3.3 V and 5.0 V (Applicable only for BU-62864)

**Product Type:**
- BU-6274 = RT-only with 4K X 16 RAM
- BU-6284 = BC/RT/MT with 4K X 16 RAM
- BU-6286 = BC/RT/MT with 64K X 17 RAM

Notes:
1. Standard DDC processing with burn-in and full temperature test. See table on next page.
2. MIL-PRF-38534 product grading is designated with the following dash numbers:
   - Class H is a -11X, 13X, 14X, 15X, 41X, 43X, 44X, 45X
   - Class G is a -21X, 23X, 24X, 25X, 51X, 53X, 54X, 55X
   - Class D is a -31X, 33X, 34X, 35X, 81X, 83X, 84X, 85X
3. The above products contain tin-lead solder finish as applicable to solder dip requirements.

| STANDARD DDC PROCESSING FOR HYBRID AND MONOLITHIC HERMETIC PRODUCTS | | |
|---|---|---|
| TEST | MIL-STD-883 | |
| | METHOD(S) | CONDITION(S) |
| INSPECTION | 2009, 2010, 2017, and 2032 | — |
| SEAL | 1014 | A and C |
| TEMPERATURE CYCLE | 1010 | C |
| CONSTANT ACCELERATION | 2001 | 3000g |
| BURN-IN | 1015 (note 1), 1030 (note 2) | TABLE 1 |

Notes:
1. For Process Requirement "B*" (refer to ordering information), devices may be non-compliant with MIL-STD-883, Test Method 1015, Paragraph 3.2. Contact factory for details.
2. When applicable.



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REGISTERED TO AS9100:2004-01
FILE NO. A5976

# RECORD OF CHANGE

## For BU-62743 Data Sheet

| Revision | Date | Pages | Description |
|---|---|---|---|
| K | 6/09 | 46 | Replaced table 65 |
| L | 11/10 | 53 | Update to Figure 19 |
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