PRELIMINARY

This Preliminary User's Guide Supplement provides detailed functional capabilities for product currently in prototype production. These specifications are being provided to allow for electrical design, layout and operation.

BU-62743/62843/62864

PCI ENHANCED MINI-ACE SUPPLEMENT TO Enhanced Mini-ACE User Guide

FEATURES

- **32-Bit / 33Mhz, 3.3Volt, PCI Target Interface**
- **Fully Integrated 1553A/B Notice 2, McAir, STANAG 3838 Interface Terminal**
- **Compatible with Enhanced Mini-ACE, Mini-ACE (Plus) and ACE Generations**
- **Choice of:**
  - **RT only with 4K RAM (BU-62743)**
  - **BC/RT/MT with 4K RAM (BU-62843)**
  - **BC/RT/MT with 64K RAM, with RAM Parity (BU-62864)**
- **3.3V Logic**
- **5V Transceiver. Available with 1760 or McAir Compatible Options**
- **1.0-inch square, 72-Pin Flatpack / Formed Gull Lead Ceramic Package.**
- **Choice of 10, 12, 16, or 20 MHz 1553 Clock**
- **Highly Autonomous BC With Built-in Message Sequence Control:**
  - **Frame Scheduling**
  - **Branching**
  - **Asynchronous Message Insertion**
  - **General Purpose Queue**
  - **User-defined Interrupts**
- **Advanced RT Functions:**
  - **Global Circular Buffering**
  - **Interrupt Status Queue**
  - **50% Circular Buffer Rollover Interrupts**
- **Selective Message Monitor or RT/Monitor**

DESCRIPTION

This supplement is to be used in conjunction with the “Enhanced mini-ACE Users Guide”. This supplement describes the functions specific to the PCI enhanced mini-ACE and also describes the deviations from the registers/operation of the enhanced mini-ACE (non-PCI).

The PCI Enhanced Mini-ACE family of MIL-STD-1553 terminals provides a complete interface between a 32-Bit / 33Mhz PCI Bus and a MIL-STD-1553 bus. These terminals integrate dual transceiver, protocol logic, and 4K words or 64K words of RAM.

With a 1.0-inch square package, the PCI Enhanced Mini-ACE is nearly 100% software compatible with the Enhanced Mini-ACE, previous generation Mini-ACE (Plus) terminals, and is software compatible with the older ACE series.

The PCI portion of the PCI Enhanced Mini-ACE is powered by 3.3V. The PCI interface is NOT 5V tolerant.

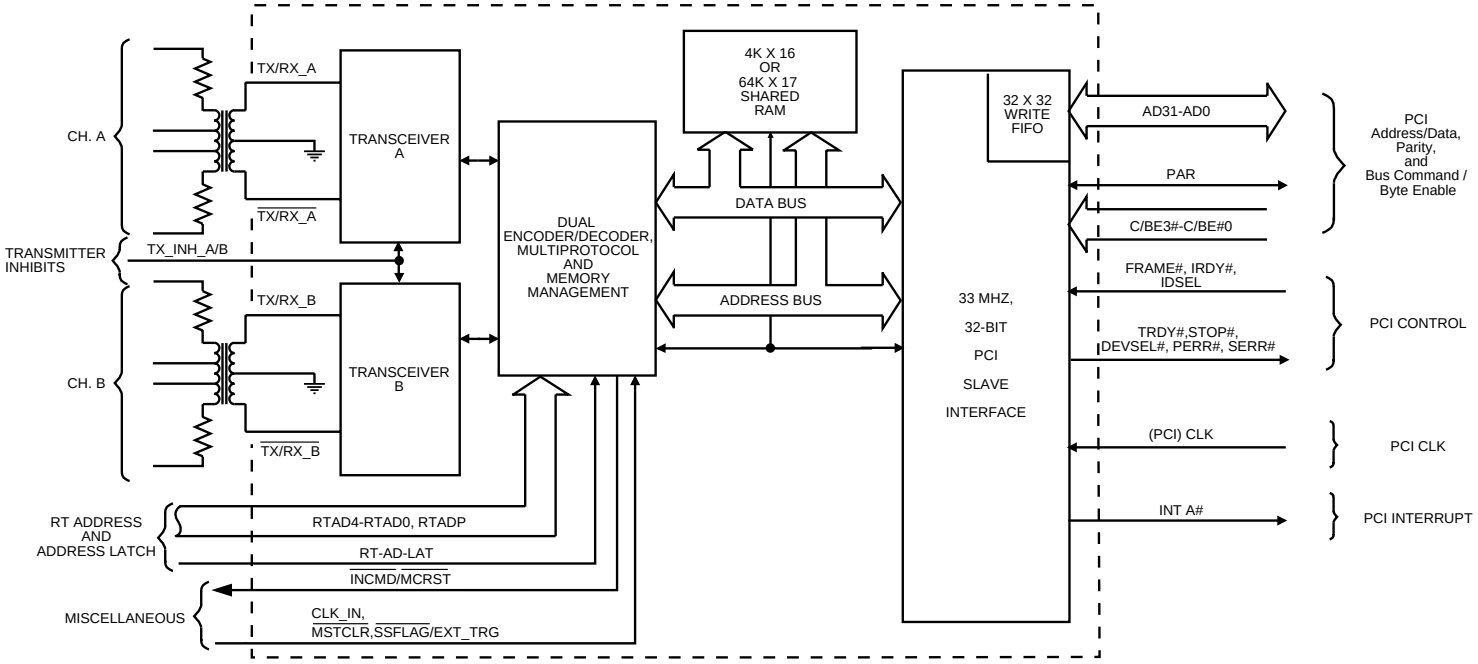


Figure 1. PCI Enhanced Mini-ACE Block Diagram

Table 1. PCI Enhanced Mini-ACE Specifications				
PARAMETER	**MIN**	**TYP**	**MAX**	**UNITS**
ABSOLUTE MAXIMUM RATINGS				
Supply Voltage				
■ Logic +3.3V	-0.3		4.0	V
■ RAM +5V	-0.3		6.0	V
■ Transceiver +5 V (Note 12)	-0.3		7.0	V
Logic				
Voltage Input Range, non-5V tolerant pins (PCI pins conform to PCI AC spec)	-0.3		Vdd+0.3	V
Voltage Input Range, 5V tolerant pins (RT address/latch, CLOCK_IN, TX_INH A/B, SSFLAG*/EXT_TRIG)	-0.3		6.0	V
RECEIVER				
Differential Input Resistance (Notes 1-6)	2.5			Kohm
Differential Input Capacitance (Notes 1-6)			5	Pf
Threshold Voltage, Transformer Coupled	0.200		0.860	VP-P
Common Mode Voltage (Note 7)			10	VPEAK
TRANSMITTER				
Differential Output Voltage				
■ Direct Coupled Across 35 ohms, Measured on Bus	6	7	9	V_{P-P}
■ Transformer Coupled Across 70 ohms				
(BU-62XXXXX-XX0,	18	20	27	V_{P-P}
BU-62XXXXX-XX2) (Note 13)	20	22	27	V_{P-P}
Output Noise, Differential (Direct Coupled)			10	mV_{P-P}
Output Offset Voltage, Transformer Coupled Across 70 ohms	-250	150	250	mV_{PEAK}
Rise/Fall Time				
(BU-62XXXX3,	100	150	300	ns
BU-62XXXX4)	200	250	300	ns
LOGIC				
V_{IH}				
All signals except PCI	2.1			V
V_{IL}				
All signals except PCI			0.7	V
Schmidt Hysteresis				
All signals except PCI	0.4			V
I_{IH}, I_{IL}				
All signals except PCI				
I_{IH} (V_{CC}=3.6V, V_{IN}=V_{CC})	-10		10	µA
I_{IH} (V_{CC}=3.6V, V_{IN}=2.7V)	-100		-33	µA
I_{IL} (V_{CC}=3.6V, V_{IN}=0.4V)	-100		-33	µA
V_{OH} (V_{CC}=3.0V, I_{OH}=max)	2.4			V
V_{OL} (V_{CC}=3.0V, I_{OL}=max)			0.4	V
I_{OL}	3.4			mA
I_{OH}			-3.4	mA

Table 1. PCI Enhanced Mini-ACE Specifications				
PARAMETER	**MIN**	**TYP**	**MAX**	**UNITS**
C_I (Input Capacitance)			50	Pf
PCI LOGIC see PCI spec 3.3V signaling environment				
C_I (Input Capacitance) all PCI except PCI_CLK & IDSEL			16	Pf
C_I (Input Capacitance) PCI_CLK			11	Pf
C_I (Input Capacitance) IDSEL			13	Pf
POWER SUPPLY REQUIREMENTS				
Voltages/Tolerance				
+5V (RAM for 62864)	4.5	5.0	5.5	V
+3.3V (Logic) V_{CC}	3.0	3.3	3.6	V
+5V (Ch. A, Ch. B)	4.75	5.0	5.5	V
Current Drain (Total Hybrid)				
BU-62864XX-XX0				
+5 V (RAM, CH A, CH B)				
• Idle			120	mA
• 25% Duty Transmitter Cycle			225	mA
• 50% Duty Transmitter Cycle			330	mA
• 100% Duty Transmitter Cycle			540	mA
+3.3 V (Logic)			40	mA
BU-62864XX-XX2				
+5 V (RAM, CH A, CH B)				
• Idle			120	mA
• 25% Duty Transmitter Cycle			236	mA
• 50% Duty Transmitter Cycle			352	mA
• 100% Duty Transmitter Cycle			585	mA
+3.3 V (Logic)			40	mA
BU-62743XX-XX0, BU-62843XX-XX0				
+5 V (CH A, CH B)				
• Idle			100	mA
• 25% Duty Transmitter Cycle			205	mA
• 50% Duty Transmitter Cycle			310	mA
• 100% Duty Transmitter Cycle			520	mA
+3.3 V (Logic)			40	mA
BU-62743XX-XX0, BU-62843XX-XX2				
+5 V (CH A, CH B)				
• Idle			100	mA
• 25% Duty Transmitter Cycle			216	mA
• 50% Duty Transmitter Cycle			332	mA
• 100% Duty Transmitter Cycle			565	mA
+3.3 V (Logic)			40	mA
POWER DISSIPATION (Note 14)				
Total Hybrid				
BU-62864XX-XX0				
Idle			0.80	W
25% Duty Transmitter Cycle			1.03	W
50% Duty Transmitter Cycle			1.26	W
100% Duty Transmitter Cycle			1.71	W
BU-62864XX-XX2				

Table 1. PCI Enhanced Mini-ACE Specifications				
PARAMETER	**MIN**	**TYP**	**MAX**	**UNITS**
Idle			0.80	W
25% Duty Transmitter Cycle			1.09	W
50% Duty Transmitter Cycle			1.39	W
100% Duty Transmitter Cycle			1.97	W
BU-62743XX-XX0, BU-62843XX-XX0				
Idle			0.69	W
25% Duty Transmitter Cycle			0.92	W
50% Duty Transmitter Cycle			1.15	W
100% Duty Transmitter Cycle			1.60	W
BU-62743XX-XX2, BU-62843XX-XX2				
Idle			0.69	W
25% Duty Transmitter Cycle			0.98	W
50% Duty Transmitter Cycle			1.28	W
100% Duty Transmitter Cycle			1.86	W
Hottest Die				
BU-62XXXXX-XX0				
Idle			0.28	W
25% Duty Transmitter Cycle			0.51	W
50% Duty Transmitter Cycle			0.75	W
100% Duty Transmitter Cycle			1.22	W
BU-62XXXXX-XX2				
Idle			0.28	W
25% Duty Transmitter Cycle			0.58	W
50% Duty Transmitter Cycle			0.88	W
100% Duty Transmitter Cycle			1.48	W
CLOCK INPUTS				
PCI Clock Input Frequency			33.3	MHz
■				
1553 Clock Frequency				
Default Mode		16.0		MHz
Option		12.0		MHz
Option		10.0		MHz
Option		20.0		MHz
■ Long Term Tolerance				
1553A Compliance	-0.01		0.01	%
1553B Compliance	-0.10		0.1	%
■ Short Term Tolerance, 1 second				
1553A Compliance	0.001		0.001	%
1553B Compliance	-0.01		0.01	%
1553 MESSAGE TIMING				
Completion of CPU Write (BC Start)-to-Start of Next Message for (Non-enhanced BC Mode)		2.5		µs
BC Intermessage Gap (Note 8)				
Non-enhanced (Mini-ACE compatible) BC mode		9.5		µs
Enhanced BC mode (Note 9)		10.0 to 10.5		µs

Table 1. PCI Enhanced Mini-ACE Specifications				
PARAMETER	**MIN**	**TYP**	**MAX**	**UNITS**
BC/RT/MT Response Timeout (Note 10)				
■ 18.5 nominal	17.5	18.5	19.5	µs
■ 22.5 nominal	21.5	22.5	23.5	µs
■ 50.5 nominal	49.5	50.5	51.5	µs
■ 128.0 nominal	127	129.5	131	µs
RT Response Time (Mid-parity to mid-sync) (Note 11)	4		7	µs
Transmitter Watchdog Timeout		660.5		µs
THERMAL				
72-Pin, Ceramic Flatpack / Gull Lead Thermal Resistance, Junction-to-Case, Hottest Die (0_{JC})			8.4	°C/W
Operating Junction Temperature	-55		150	°C
Storage Temperature	-65		150	°C
Lead Temperature (soldering, 10 sec.)			+300	°C
PHYSICAL CHARACTERISTICS				
72-Pin, Ceramic Flatpack / Gull Lead Size	1.0 X 1.0 X 0.155 (25.4 x 25.4 x 3.94)			in. (mm)
Weight	0.6 (17)			Oz. (g)

Notes:

Notes 1 through 6 are applicable to the Receiver Differential Resistance and Differential Capacitance specifications:

(1) Specifications include both transmitter and receiver (tied together internally).

(2) Impedance parameters are specified directly between pins TX/RX A(B) and TX/RX A(B) of the PCI Enhanced Mini-ACE hybrid.

(3) It is assumed that all power and ground inputs to the hybrid are connected.

(4) The specifications are applicable for both unpowered and powered conditions.

(5) The specifications assume a 2-volt rms balanced differential, sinusoidal input. The applicable frequency range is 75 kHz to 1 MHz.

(6) Minimum resistance and maximum capacitance parameters are guaranteed over the operating range, but are not tested.

(7) Assumes a common mode voltage within the frequency range of dc to 2 MHz, applied to pins of the isolation transformer on the stub side (either direct or transformer coupled), and referenced to hybrid ground. Transformer must be a DDC recommended transformer or other transformer that provides an equivalent minimum CMRR.

(8) Typical value for minimum intermessage gap time. Under software control, this may be lengthened to 65,535 ms - message time, in increments of 1 μs. If ENHANCED CPU ACCESS, bit 14 of Configuration Register #6, is set to logic "1", then host accesses during BC Start-of-Message (SOM) and End-of-Message (EOM) transfer sequences could have the effect of lengthening the intermessage gap time. For each host access during an SOM or EOM sequence, the intermessage gap time will be lengthened by 6 clock cycles. Since there are 7 internal transfers during SOM, and 5 during EOM, this could theoretically lengthen the intermessage gap by up to 72 clock cycles; i.e., up to 7.2 μs with a 10 MHz clock, 6.0 μs with a 12 MHz clock, 4.5 μs with a 16 MHz clock, or 3.6 μs with a 20 MHz clock.

(9) For Enhanced BC mode, the typical value for intermessage gap time is approximately 10 clock cycles longer than for the non-enhanced BC mode. That is, an addition of 1.0 μs at 10 MHz, 833 ns at 12 MHz, 625 ns at 16 MHz, or 500 ns at 20 MHz.

(10) Software programmable (4 options). Includes RT-to-RT Timeout (measured mid-parity of transmit Command Word to mid-sync of transmitting RT Status Word).

(11) Measured from mid-parity crossing of Command Word to mid-sync crossing of RT's Status Word.

(12) External 10 μF Tantalum and 0.1 μF capacitors should be located as close as possible to Pins 20 and 72, and a 0.1 μF at pin 37. The BU-62864 should also have a 0.1 μF at pin 26.

(13) MIL-STD-1760 requires that the PCI Enhanced Mini-ACE produce a 20 Vp-p minimum output on the stub connection.

(14) Power dissipation specifications assume a transformer coupled configuration with external dissipation (while transmitting) of 0.14 watts for the active isolation transformer, 0.80 watts for the active bus coupling transformer, 0.45 watts for each of the two bus isolation resistors and 0.15 watts for each of the two bus termination resistors.

INTRODUCTION

The BU-62743 RT, and BU-62843/62864 BC/RT/MT PCI Enhanced Mini-ACE family of MIL-STD-1553 terminals comprise a complete integrated interface between a PCI host processor and a MIL-STD-1553 bus. All members of the PCI Enhanced Mini-ACE family are packaged in the same 1.0 square inch ceramic flatpack package. The PCI Enhanced Mini-ACE hybrids provide footprint and software compatibility with the Enhanced Mini-ACE, Mini-ACE (Plus) terminals, as well as software compatibility with the older ACE series.

The PCI Enhanced Mini-ACE integrates an “enhanced mini-ACE” core with a PCI bus interface. As such, the 1553 portion functions just like the enhanced mini-ACE, with a few exceptions. The PCI-enhanced mini-ACE lacks built-in protocol self test (protocol self test requires external vectors) and it does not have a Busy Rx Transfer Disable bit. These exceptions/differences are noted in the register descriptions in this supplement. Please refer to the “Enhanced mini-ACE User Guide” for a full listing of ALL the enhanced mini-ACE registers AND an exhaustive listing of their functions and BC/RT/MT, etc. operation.

The PCI Enhanced Mini-ACEs are fully compliant targets, as defined by the PCI Local Bus Specification Revision 2.2, using a 32 bit interface that operates at clock speeds of up to 33 Mhz, from a 3.3V signaling bus. The interface supports PCI interrupts and contains a FIFO that handles PCI burst write transfer cycles. The FIFO is deep enough to accept an entire 1553 message. The PCI interface is NOT 5V tolerant and can not be used in a 5V PCI signaling environment. The PCI interface is powered by 3.3V.

The 64K RAM, in the 64K version, is powered by 5V.

The PCI Enhanced Mini-ACE series terminals operate over the full military temperature range of -55 to +125°C. Available screened to MIL-PRF-38534C, the terminals are ideal for military and industrial processor-to-1553 applications.

PCI REGISTER AND MEMORY ADDRESSING

The PCI Interface contains a set of “Type 00h” PCI configuration registers that are used to map the device into the host system. There are two Base Address Registers that are used to implement ACE memory space (BAR0) and ACE register space (BAR1). The BAR1 space also contains the PCI-to-ACE interface control/status registers. The PCI configuration register space is mapped in accordance with PCI revision 2.2 specifications.

The PCI Enhanced mini-ACE acts as a target and responds to the following PCI commands:

Table 2.PCI Target Command Codes	
Command type	**Code (C/BE[3:0]#)**
Memory Read	0110 (6h)
Memory Write	0111 (7h)
Configuration Read	1010 (Ah)
Configuration Write	1011 (Bh)
Memory Read Multiple	1100 (Ch)
Memory Read Line	1110 (Eh)
Memory Write and Invalidate	1111 (Fh)

The PCI Enhanced mini-ACE does NOT implement the Memory Read Multiple, Memory Read Line or Memory Write and Invalidate commands. However, in accordance with PCI rules, the PCI Enhanced mini-ACE will accept these requests and alias them to the basic memory commands. For example, Memory Read Multiple and Memory Read Line commands will be accepted and treated as Memory Read commands. Similarly, the PCI Enhanced mini-ACE will accept a memory Write and Invalidate command and treat it as a Memory Write command.

ACE memory (for brevity, the term “ACE” is a substitute for the Enhanced mini-ACE core) is accessed internally in 16-bit words, but memory is accessed sequentially allowing for 32-bits of data to be read from the PCI bus. In other words, if a 32-bit PCI read is requested the first 16 bits of data would be read from the requested internal address, the next 16 bits of data would be read from the initial internal address + 1, and then the resulting 32-bit double word would be transferred to the PCI bus. The PCI Enhanced Mini-ACE supports 32-bit and 16-bit read and write operations, 8 bit reads will return 16 bit data, and 8 bit writes are illegal and will cause target-aborts.

The ACE register mapping is located in PCI memory space. Although the PCI Enhanced Mini-ACE can be accessed in 32-bit words, all ACE registers are accessed internally in 16 bit word reads / writes. If a 32-bit PCI read is performed from the PCI bus in ACE register space, the lower 16 bits are the ACE register data and the upper 16 bits are all zeroes.

Table 3. Configuration Register Space for the PCI enhanced mini-ACE				
Address	**31 24**	**23 16**	**15 8**	**7 0**
00h	Device ID		Vendor ID	
	04h	0Xh (X varies with part #, see text)	DDC Manufacturer Device ID value ($4DDC_H$)	
04h	Status Register		Command Register	
08h	Class Code = 078000 h			Rev ID = 02h
0Ch	BIST 00h	Header Type 00h	Latency Timer 00h	Cache Line Size 00h
10h	Base Address Register 0 (for ACE memory)			
	R/W	R/W and 0's see text	00h	00h
14h	Base Address Register 1 (for ACE registers)			
	R/W	R/W	R/W and 0's see text	00h
18h - 24h	Base Address Registers 2 through 5 (not used) 00000000h			
28h	Card Bus CIS pointer (not used) 00000000h			
2Ch	Subsystem Device and Subsystem Vendor ID Same as Configuration Register 0, Alias Reads to Configuration Register 00			
30h	Expansion ROM Base Address (Not Used, bit 0 = 0)			
34h-38h	Reserved			
3Ch	Max Lat. 00h	Min Gnt 00h	Interrupt Pin 01h	Interrupt Line R/W

This data sheet will only describe the PCI registers that are specific to configuring the integrated terminal and shared RAM. For specifics or definitions on other PCI configuration registers, please see the PCI Local Bus specification revision 2.2. The PCI enhanced mini-Ace responds to type 00 configuration cycles and is a single function device that does NOT check the function field value in the configuration address.

Vendor ID field contains the vendor's ID configuration register. Data Device Corporation's ID code is 4DDCh.

Device ID field is used to indicate the device being used. This field is configured by DDC to reflect the part value of the device. The following Table 4 represents all possible combinations for the Device ID field:

Table 4. Device ID Field Mapping	
Device ID	**Part Value**
0400h	BC/RT/MT with 4K of RAM (BU-62843)
0402h	BC/RT/MT with 64K of RAM (BU-62864)
0404h	RT Only with 4K of RAM (BU-62743)

PCI Command register

Table 5. PCI Command Register	
BIT	**DESCRIPTION**
15:10	Reserved, 0s
9	0
8	SERR# Enable
7	0
6	Parity Error Control
5:2	0
1	Memory Space
0 (LSB)	0

Reserved: These bits are read-only and return zeroes when read.

SERR# Enable: This is an enable bit for the SERR# driver. A value of 0b disables the driver. A value of 1b enables the driver. The value after RST# is 0b.

Parity Error Control: This bit controls the device's response to parity errors. When the bit is 1b, the device will take its normal action when a parity error is detected. When this bit is 0b, the device will ignore any parity errors that it detects and continue normal operation. The value after RST# is 0b.

Memory Space: This bit controls the device's response to memory space accesses. A value of 0b disables the device response. A value of 1b allows the device to respond to memory space accesses. The value after RST# is 0b.

PCI Status register This register records status information for PCI bus related events. Reads to this register behave normally, but writes can only reset bits. A bit is reset whenever the register is written and the data in the corresponding bit location is a 1.

Table 6. PCI Status Register

BIT	DESCRIPTION
31	Detected Parity Error
30	Signaled System Error
29:28	0
27	Signaled Target Abort
26:25	DEVSEL# Timing = 01 (medium)
24	0
23	Fast Back-to-Back Capable = 1
22:21	0
20:16	Reserved, 0s

Detected Parity Error: This bit will be set by the device whenever it detects a parity error, even if the Parity Error Control bit in the PCI Control register is 0b.

Signaled System Error: This bit indicates when the device has asserted SERR#. The value after RST# is 0b.

Signaled Target Abort: This bit is set whenever the device terminates a transaction with a Target-Abort. The value after RST# is 0b.

DEVSEL# Timing: The PCI enhanced mini-ACE is 01b, medium.

Fast Back-to-Back Capable: This bit is set to 1b and indicates that the device is capable of accepting fast back-to-back transactions.

Reserved: These bits are read-only and return zeroes when read.

Subsystem Vendor ID/Subsystem Device ID field is an alias of the Vendor ID/Device ID fields in Configuration Register 00h.

Base Address Registers are used to implement ACE memory space (BAR0) and ACE register space (BAR1). Base Address Registers 2 through 5 are not used.

BAR0 is used to access ACE memory space. The ACE is allotted a maximum of 64K words, 128K bytes, for its memory space. BAR0 will read back as FFFE0000 after all Fs are written to it. The lower 4 bits being 0 indicate that BAR0 is memory space, the address decoder is 32 bits wide and the memory is non-prefetchable. BAR0 will read back the same for both the 4K word ACE parts (BU-62743/843) and the 64K word ACE (BU-62864).

Table 7. (BAR0) ACE Memory	
ADDRESS OFFSET	**DEFINITION**
00000 – 1FFFC	PCI ENHANCED MINI-ACE Memory Space

PCI ENHANCED MINI-ACE Memory Space: The least significant bit (LSB) of the PCI address is dropped to form the ACE memory address.

BAR1 is used to access ACE register locations. The ACE is allotted a maximum of 4K bytes for its register space. BAR1 will read back as FFFFF000h after all Fs are written to it. The lower 4 bits being 0 indicate that BAR0 is memory space, the address decoder is 32 bits wide and the memory is non-prefetchable. All ACE register locations are accessible through the PCI host via the BAR1 offsets 000h to 0FCh.
The PCI-to-ACE interface control/status registers are at 800h to 81Ch. PCI accesses outside of these specific regions (e.g., to offset 100h or 820h, etc.) will produce Target Aborts. The PCI-to-ACE interface control/status registers are not part of the “enhanced mini-ACE” 1553 terminal core.
For typical applications, the SW only needs to access the 800 register and the “PCI enhanced mini-ACE interrupt enable” bit in the 804 register. The registers at 808h-81Ch can be ignored by typical applications.

Table 8. (BAR1) ACE/ PCI-to-ACE interface Registers – 4K byte Total Space		
ADDRESS OFF-SET	**NAME**	**DEFINITION / ACCESSIBILITY**
000-0FC	ACE	PCI ENHANCED MINI-ACE Register Space: see **Table 8**
100-7FC	-	RESERVED (Target-Abort if accessed)
800	REG0	GLOBAL ACTIVITY (RD)
804	REG1	FAIL-SAFE OPERATION / INTERRUPT (RD/WR)
808	REG2	FAIL-SAFE TIMER (RD)
80C	REG3	FAIL SAFE TIMER PRELOAD (RD/WR)
810	REG4	DISCARD TIMER (RD)
814	REG5	DISCARD TIMER PRELOAD (RD/WR)
818	REG6	GENERAL PURPOSE, CUSTOMER USE (RD/WR)
81C	REG7	CLEAR FAILSAFE INT/RESET ACE (WR)
820-FFC	-	RESERVED (Target-Abort if accessed)

PCI ENHANCED MINI-ACE Register Space: Register accesses are on a 32-bit boundary: the last 2 bits of the PCI address are dropped to form the ACE address. The “ACE core” register PCI mapping is shown in *Table 9*. This table is

the “Register Address Mapping” table from the “Enhanced mini-ACE User Guide” with the ACTUAL PCI BAR1 offsets inserted for reference. Note that these registers are internally 16bits wide and that 32 bit PCI reads will return all zeroes in the upper PCI word. Please refer to the “Enhanced mini-ACE User Guide” for an exhaustive discussion of these registers.

Table 9.ACE core register mapping in BAR1 space

INTERNAL Address Lines					PCI BAR 1 OFFSET	Register Description/Accessibility
A4	A3	A2	A1	A0		
0	0	0	0	0	0h	Interrupt Mask Register #1 (RD/WR)
0	0	0	0	1	4h	Configuration Register #1 (RD/WR)
0	0	0	1	0	8h	Configuration Register #2 (RD/WR)
0	0	0	1	1	Ch	Start/Reset Register (WR)
0	0	0	1	1	Ch	Non-Enhanced BC or RT Command Stack Pointer/Enhanced BC Instruction List Pointer Register (RD)
0	0	1	0	0	10h	BC Control Word/ RT Subaddress Control Word Register (RD/WR)
0	0	1	0	1	14h	Time Tag Register (RD/WR)
0	0	1	1	0	18h	Interrupt Status Register #1(RD)
0	0	1	1	1	1Ch	Configuration Register #3 (RD/WR)
0	1	0	0	0	20h	Configuration Register #4 (RD/WR)
0	1	0	0	1	24h	Configuration Register #5 (RD/WR)
0	1	0	1	0	28h	RT/Monitor Data Stack Address Register (RD/WR)
0	1	0	1	1	2Ch	BC Frame Time Remaining Register (RD)
0	1	1	0	0	30h	BC Time Remaining to Next Message Register (RD)
0	1	1	0	1	34h	Non-Enhanced BC Frame Time/Enhanced BC Initial Instruction Pointer /RT Last Command/MT Trigger Word Register (RD/WR)
0	1	1	1	0	38h	RT Status Word Register (RD)
0	1	1	1	1	3Ch	RT BIT Word Register (RD)
1	0	0	0	0	40h	Test Mode Register 0
1	0	0	0	1	44h	Test Mode Register 1
1	0	0	1	0	48h	Test Mode Register 2
1	0	0	1	1	4Ch	Test Mode Register 3
1	0	1	0	0	50h	Test Mode Register 4
1	0	1	0	1	54h	Test Mode Register 5
1	0	1	1	0	58h	Test Mode Register 6
1	0	1	1	1	5Ch	Test Mode Register 7
1	1	0	0	0	60h	Configuration Register #6 (RD/WR)
1	1	0	0	1	64h	Configuration Register #7 (RD/WR)
1	1	0	1	0	68h	RESERVED
1	1	0	1	1	6Ch	BC Condition Code Register (RD)
1	1	0	1	1	6Ch	BC General Purpose Flag Register (WR)
1	1	1	0	0	70h	RESERVED
1	1	1	0	1	74h	Interrupt Mask Register #2 (RD/WR)
1	1	1	1	0	78h	Interrupt Status Register #2 (RD)
1	1	1	1	1	7Ch	BC General Purpose Queue Pointer/ RT-MT Interrupt Status Queue Pointer Register (RD/WR)

The software interface of the enhanced Mini-ACE portion of the PCI Enhanced mini-ACE to the host processor consists of 24 internal operational registers for normal operation, an additional 24 test registers, plus 64K words of shared memory address space. The PCI Enhanced Mini-ACE's 4K X 16 or 64K X 17 internal RAM resides in this address space.

For normal operation, the host processor only needs to access the lower 32 register address locations (00-1F). The next 32 locations (20-3F) should be reserved, since many of these are used for factory test.

Note that Table 9 does NOT show the internal A5 register address line, which is normally 0 and is set only for access to the reserved factory test registers.

The configuration registers will be cleared to 0000h after hardware or software reset, with the exception of the Enhanced CPU Access bit (bit 14 in Configuration register #6).

Power turn-On/Initialization State

Note that since the PCI enhanced mini-ACE does NOT have built-in protocol self test, the protocol self test will not be run following hardware reset. The protocol self-test can be run via external vectors, see external vector protocol self test vector section.

"ACE core" register differences between PCI enhanced mini-ACE and enhanced mini-ACE.

The tables below list the PCI enhanced mini-ACE registers that differ from the enhanced mini-ACE registers. Please refer to the "Enhanced mini-ACE User's Guide" for in-depth discussions on register functions, initialization, operation, etc.

In addition, some of the other bits in the registers have slightly different "operation" compared to the enhanced mini-ACE:

- The LEVEL/PULSE* INTERRUPT REQUEST bit in Configuration Register #2 MUST be set to 1 for correct PCI interrupt operation.
- The "Enhanced CPU access bit" in configuration register 6 is SET after reset. When set, this bit reduces the length of DRR cycles on the PCI bus.

Table 10. START/RESET REGISTER (WRITE 03h, PCI 0Ch)	
BIT	**DESCRIPTION**
15(MSB)	RESERVED
14	RESERVED
13	RESERVED
12	RESERVED
11	CLEAR RT HALT
10	CLEAR SELF-TEST REGISTER
9	INITIATE RAM SELF-TEST
8	RESERVED
7	RESERVED
6	BC/MT STOP-ON-MESSAGE
5	BC STOP-ON-FRAME
4	TIME TAG TEST CLOCK
3	TIME TAG RESET
2	INTERRUPT RESET
1	BC/MT START
0(LSB)	RESET

This register has eliminated the “Initiate Protocol Self-Test” bit that the Enhanced mini-ACE has in this register at the bit 7 location.

TABLE 11. CONFIGURATION REGISTER #3 (READ/WRITE 07h, PCI 1Ch)	
BIT	**DESCRIPTION**
15(MSB)	ENHANCED MODE ENABLE
14	BC/RT COMMAND STACK SIZE 1
13	BC/RT COMMAND STACK SIZE 0
12	MT COMMAND STACK SIZE 1
11	MT COMMAND STACK SIZE 0
10	MT DATA STACK SIZE 2
9	MT DATA STACK SIZE 1
8	MT DATA STACK SIZE 0
7	ILLEGALIZATION DISABLED
6	OVERRIDE MODE T/R* ERROR
5	ALTERNATE STATUS WORD ENABLE
4	ILLEGAL RX TRANSFER DISABLE
3	RESERVED, set to zero
2	RTFAIL*/RTFLAG* WRAP ENABLE
1	1553A MODE CODES ENABLE
0(LSB)	ENHANCED MODE CODE HANDLING

The only difference in this register is the elimination of the “Busy Rx transfer disable” bit (bit 3), which is a “reserved, set to 0 bit “in the PCI enhanced mini-ACE.

TABLE 12. BIT TEST STATUS REGISTER (READ 1Ch, PCI 70h)	
BIT	**DESCRIPTION**
15 (MSB)	LOGIC “0”
14	LOGIC “0”
13	LOGIC “0”
12	LOGIC “0”
11	LOGIC “0”
10	LOGIC “0”
9	LOGIC “0”
8	LOGIC “0”
7	RAM BUILT-IN TEST COMPLETE
6	RAM BUILT-IN TEST IN PROGRESS
5	RAM BUILT-IN TEST PASSED
4	LOGIC “0”
3	LOGIC “0”
2	LOGIC “0”
1	LOGIC “0”
0 (LSB)	LOGIC “0”

This register reflects the removal of the protocol built-in test bits. Bits 15-11 are protocol BIT flags in the “enhanced mini-ACE” parts.

Table 13. REG0 Global Activity Register (Read 800h)	
BIT	**DESCRIPTION**
31 (MSB)	PCI INTERRUPT ACTIVE
30	FIFO NOT EMPTY
29	0
28	0
27	0
26	0
25	0
24	1
23	BAR1 DRR_DATA_DISCARD
22	FAIL_SAFE ERROR
21	0
20	0
19	0
18	0
17	0
16	PCI ENHANCED MINI-ACE INTERRUPT ACTIVE
15	0
•	•
•	•
•	•
0 (LSB)	0

This register will be all 0s after RST#, except for bit 24. Failsafe errors are very unlikely and the "Fail_Safe Error" bit can be ignored by applications.

PCI_INTERRUPT ACTIVE: When set to '1', indicates that PCI Enhanced Mini-ACE has asserted it's interrupt pin. The three possible sources (if enabled and active) are the internal Enhanced Mini-ACE core, the FailSafe timer (very unlikely event) and BAR1 DRR_DATA_DISCARD.

FIFO NOT EMPTY: When set to '1', indicates that the write FIFO is not empty. The Write FIFO being not empty impacts the latency of PCI BAR0 and BAR1 0-FCh READ operations. See "PCI read of ACE memory/registers" section for more information.

BAR1 DRR_DATA_DISCARD: If the data discard timer times out while waiting for a retry on a BAR1 access, this bit will be set. If BAR1 read is discarded, it may have caused an action (for example clearing an ACE interrupt) that has not been recognized by the PCI MASTER.

FAIL SAFE ERROR: If not in FAIL_SAFE OFF mode and fail safe error occurs (ACE does not respond), this bit will be set. Fail safe errors are very unlikely events.

Table 14. REG1 Fail-Safe Operation / Interrupt Register (Read/Write 804h)	
BIT	**DESCRIPTION**
31 (MSB)	DRR_HOLD
30	RESERVED, WRITE AS 0
•	•
•	•
•	•
22	RESERVED, WRITE AS 0
21	PCI ENHANCED MINI-ACE INTERRUPT ENABLE
20	BAR1 DRR_DATA_DISCARD INTERRUPT ENABLE
19	FAILSAFE INTERRUPT ENABLE
18	FAILSAFE INTERRUPT AUTOCLEAR ENABLE
17	FAILSAFE MODE - BIT 1 (MSB)
16	FAILSAFE MODE - BIT 0 (LSB)
15	RESERVED, WRITE AS 0
•	•
•	•
•	•
0 (LSB)	RESERVED, WRITE AS 0

This register will be all 0s after RST#, except that bit 17 will be 1 (Failsafe mode = Failsafe Halt).

For typical applications, all bits in this register, except bit 21, can be left in their reset states. Bit 21 must be set to allow the internal ACE core to generate interrupts on the PCI bus.

DRR_HOLD: When '0', a delayed read request is discarded if the PCI Enhanced Mini-ACE has obtained the requested data and a different transaction is requested. When '1', delayed read request is held until master repeats original request or timeout occurs.

BITS 30 - 22: Reserved, write as 0s

PCI ENHANCED MINI-ACE INTERRUPT ENABLE: Must be set to "1".

BAR1 DRR_DATA_DISCARD INTERRUPT ENABLE: Enables interrupt to occur on a BAR1 delayed read timeout. Since system integrity is affected if a delayed read timeout occurs, this interrupt can be used to report this error to the device driver.

FAILSAFE INTERRUPT ENABLE: When set to a "1", an interrupt is generated if not in FAILSAFE OFF mode and a FAILSAFE error is detected. FAILSAFE errors are unlikely events.

FAILSAFE INTERRUPT AUTOCLEAR ENABLE: If set, causes interrupt and the FAIL_SAFE ERROR bit (REG0-bit 22) to be cleared whenever upper word of

REG0 is read by the PCI MASTER. If not set, bit 1 in Reg 7 must be used to clear Failsafe interrupts.

FAILSAFE MODE: Fail Safe Errors occur when the internal ACE data transfer handshake fails to complete within 1 millisecond (programmable). A failsafe error would be a very rare event. Four possible FAILSAFE Modes determine how this situation is handled:

Table 15. FAILSAFE MODE

BIT 17	BIT 16	FAILSAFE MODE
0	0	FailSafe Off
0	1	FailSafe Retry
1	0	FailSafe Halt
1	1	FailSafe Skip

MODE 1 - FAILSAFE OFF. PCI Enhanced Mini-ACE will wait indefinitely for the transaction to complete. The local bus could hang as a result. The FAILSAFE ERROR bit and interrupt will not be generated even if the enable bit is set.

MODE 2 - FAILSAFE RETRY. PCI Enhanced Mini-ACE will retry the transfer on the local bus when the FAILSAFE timer times out.

MODE 3 - FAILSAFE HALT. Once the FAILSAFE timer times out, all future transfers will be terminated with a target abort until the PCI master clears the interrupt.

MODE 4 - FAILSAFE SKIP. Once the FAILSAFE timer times out, the current transaction is discarded or skipped and the next transaction, whether a stored write in the FIFO or a new transaction, will be attempted.

BITS 15-0 ARE RESERVED: Write these bits as 0s.

Table 16. REG2 Fail-Safe Timer Register (Read 808h)

BIT	DESCRIPTION
31 (MSB)	0
•	•
•	•
•	•
16	0
15	FAIL-SAFE TIMER COUNT - BIT 15 (MSB)
•	•
•	•
•	•
0 (LSB)	FAIL-SAFE TIMER COUNT - BIT 0 (LSB)

This register does NOT have to be manipulated for typical applications.

FAIL-SAFE TIMER COUNT: Read this register to obtain the current value of the fail-safe timer. Default is 8400h.

Table 17. REG3 Fail Safe Timer Preload Register (Read/Write 80Ch)	
BIT	**DESCRIPTION**
31 (MSB)	0
•	•
•	•
•	•
16	0
15	FAIL-SAFE TIMER VALUE – BIT 15 (MSB)
•	•
•	•
•	•
0 (LSB)	FAIL-SAFE TIMER VALUE – BIT 0 (LSB)

This register does NOT have to be manipulated for typical applications.

FAIL-SAFE TIMER VALUE: Write to this register to set the value for the fail-safe timer. The default value is 8400h. The timer has a 30ns resolution (PCI clock). The timer is loaded when an access is initiated on the local bus and counts down until the access is completed. It will time out if it reaches 0.

Table 18. REG4 Discard Timer Register (Read 810h)	
BIT	**DESCRIPTION**
31 (MSB)	0
•	•
•	•
•	•
16	0
15	DISCARD TIMER CURRENT - BIT 15 (MSB)
•	•
•	•
•	•
0 (LSB)	DISCARD TIMER CURRENT- BIT 0 (LSB)

This register does NOT have to be manipulated for typical applications.

DISCARD TIMER CURRENT: Read this register to obtain the current value of the DISCARD TIMER. Default is 0000h

Table 19. REG5 Discard Timer Preload Register (Read/Write 814h)	
BIT	**DESCRIPTION**
31 (MSB)	0
•	•
•	•
•	•
16	0
15	DISCARD TIMER VALUE- BIT 15 (MSB)
•	•
•	•
•	•
0 (LSB)	DISCARD TIMER VALUE- BIT 0 (LSB)

This register does NOT have to be manipulated for typical applications.

DISCARD TIMER VALUE: Write this register to set the value to be used for the discard timer. The default value is "0". The timer has a 30ns resolution (PCI clock). The timer is loaded on the completion of a local bus read. The discard timer will then count up. If the PCI retry has not occurred by the time that bit 15 becomes a "1", the timer stops and the data is discarded.

Note that the default value of 0, in combination with the terminal count of 2 to the 15, satisfies the PCI specification Discard Timer requirement. If the discard timer times out and the BAR1 DRR_DATA_DISCARD INTERRUPT ENABLE bit is set, an interrupt will occur that can be used to signal the device driver that a system integrity error has occurred . During normal operation the discard timer should never time out, since any read request started by a master must be repeated until it completes.

Table 20. REG6 General Purpose Register (Read/Write 818h)	
BIT	**DESCRIPTION**
31 (MSB)	RESERVED - BIT 31 (MSB)
•	•
•	•
•	•
0 (LSB)	RESERVED - BIT 0 (LSB)

This register will be all 0s after RST#.

This read/write register is available for customer use, perhaps as a flag register for signaling between bus masters.

Table 21. REG7 Reserved Register (Write 81Ch)	
BIT	**DESCRIPTION**
31 (MSB)	RESERVED, WRITE AS 0 - BIT 31 (MSB)
•	•
•	•
•	•
1	CLEAR FAILSAFE INTERRUPT
0 (LSB)	ACE RESET - BIT 0 (LSB)

This register will be all 0s after RST#.
This register does NOT have to be manipulated for typical applications.

BITS 31-2 ARE RESERVED AND MUST BE WRITTEN AS 0s

CLEAR FAILSAFE INTERRUPT: Clears the Failsafe Interrupt when set to “1”. Failsafe interrupts can also be cleared via the Failsafe Interrupt Autoclear mechanism, enabled by bit 18 in Reg 1.

ACE RESET: Resets the ACE when set to “1”

Figure 2 illustrates a generic connection diagram between a PCI “Initiator” and a PCI ENHANCED mini-ACE “Target.” Refer to Table 1, Note 12, for recommended power supply capacitors.

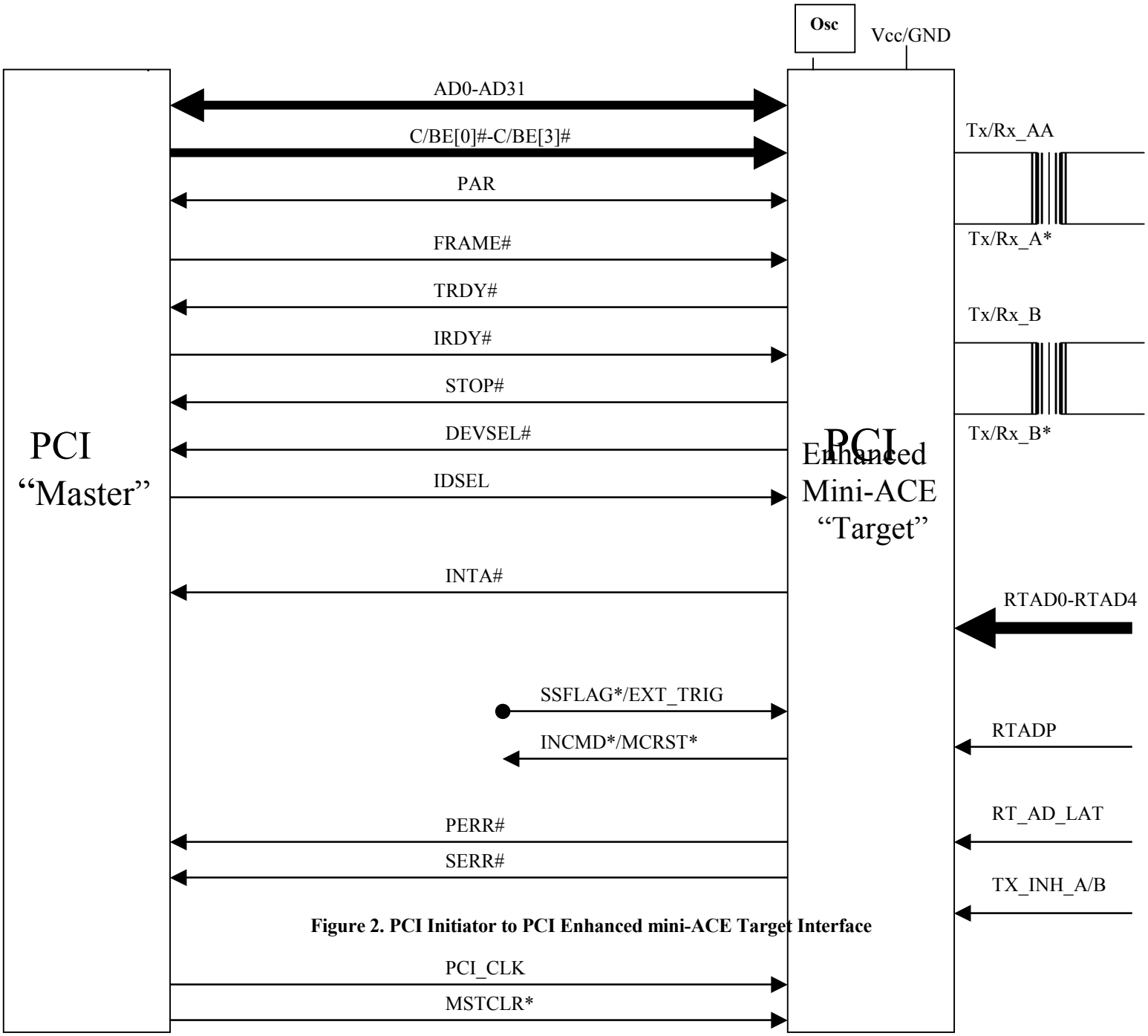
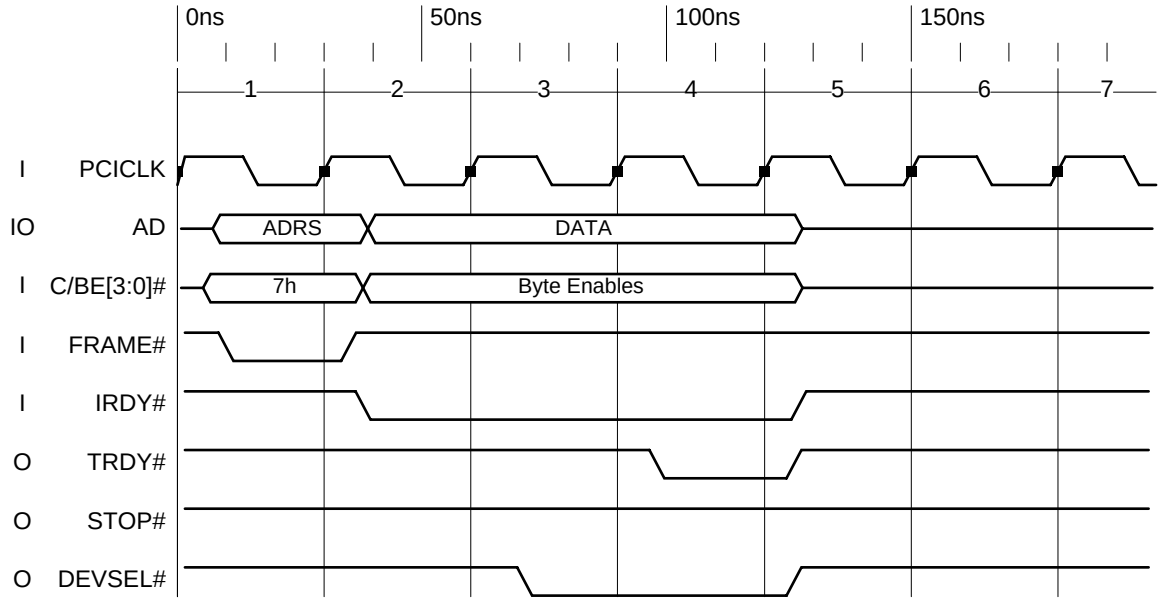


Figure 2. PCI Initiator to PCI Enhanced mini-ACE Target Interface

The following timing diagrams illustrate the PCI commands that the PCI enhanced mini-ACE responds to. Note that these diagrams are meant to show the basic PCI bus operation of the PCI enhanced mini-ACE itself and do not show masters inserting wait states, masters burst reading or writing past address boundaries, masters writing into a full FIFO, etc.
To help understand the following timing diagrams an explanation of the basic architecture of the PCI Enhance mini-ACE is helpful. The PCI enhanced mini-ACE be thought of as the very successful enhanced mini-ACE terminal family integrated with a 3.3V 33MHz PCI target interface. To simplify descriptions of the PCI enhanced mini-ACE architecture, the term ACE will be used as a substitute for "enhanced mini-ACE" even though the 1553 terminal function is really an enhanced mini-ACE. When reference is made to ACE memory (BAR0) or ACE registers (BAR1 00-FCh) these functions are part of the ACE portion of the die. These ACE functions are accessed via the write FIFO (for writes) and delayed read request logic (for reads).

The "PCI interface registers" (BAR1 800-81Ch) are part of the PCI interface portion of the die and are written and read directly from the PCI bus, without use of the write FIFO or delayed read request logic.

The PCI enhanced mini-ACE's basic PCI transaction takes 3 PCI clocks, on top of the command phase. For example, a single write to any location within the PCI Enhanced mini_ACE's memory space takes 4 PCI clocks, as shown in Figure 3. Note that this is a single write, not an attempted burst write: FRAME# is not held asserted by the master. Also note that a write to the ACE registers or ACE memory is actually a write into the write FIFO whereas a write to the PCI interface registers (BAR1 800-81Ch) is a write to the registers themselves.



PCI single write to any legal memory location (C/BE# = 7h)

Figure 3. PCI single memory write to PCI Enhanced mini-ACE

Table 22 provides the timing parameters for 3.3V PCI signaling environments applicable to the PCI enhanced mini-ACE, and Figure 4 shows the timing reference points. The timing parameters apply to the other timing diagrams, but are not illustrated. The PCI Enhanced mini-ACE conforms to revision 2.2 of the PCI Local Bus specification. The timing parameters are provided here for ease of reference only.

Table 22 PCI Interface Timings

Symbol	Parameter	Min	Max	units	
tv	CLK to signal valid delay	2	11	ns	
tsu	Input setup time to CLK	7		ns	
th	Input hold time from CLK	0		ns	

Figure 4 illustrates a PCI read from the PCI Enhanced mini-ACE's configuration space. The PCI Enhanced mini-ACE only responds to Type Zero configuration access: AD[1:0] must be 00 during the command phase. The PCI Enhanced mini-ACE will drive a full Dword on the AD lines independent of which byte enables are asserted during the configuration read.

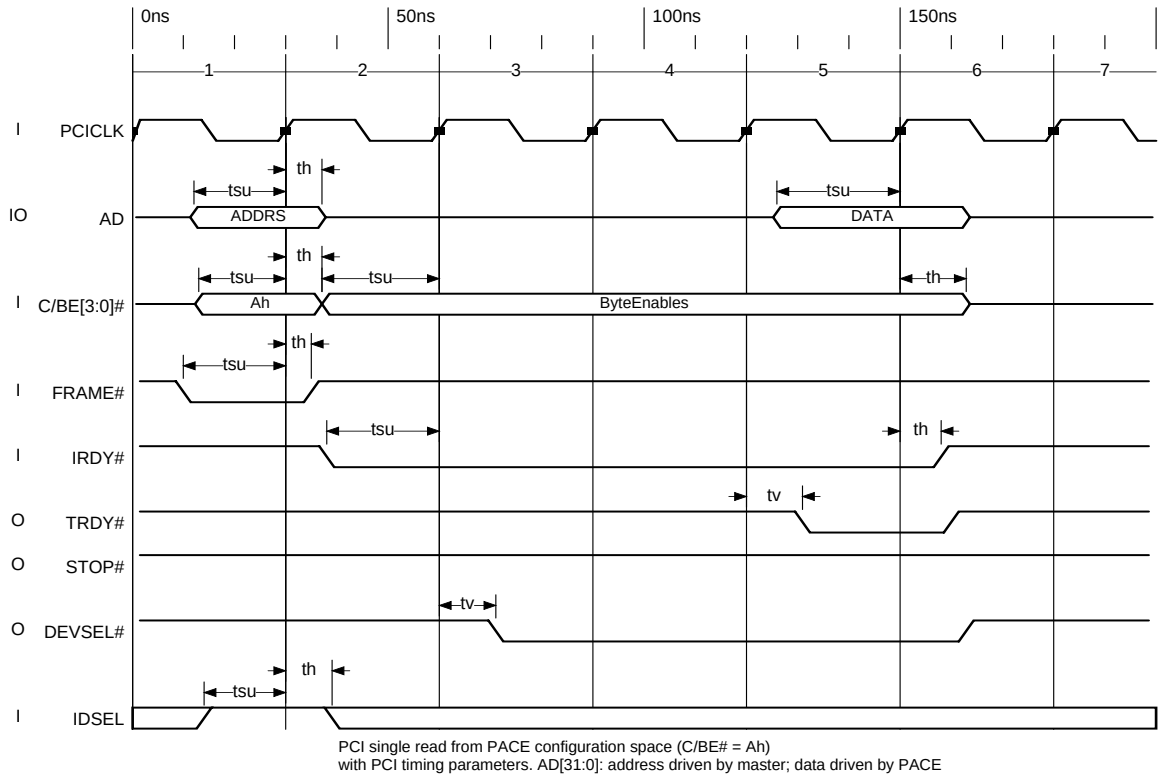


Figure 4. PCI single read of configuration space with timing

Figure 5 illustrates a PCI single write to PCI Enhanced mini-ACE configuration space. The PCI Enhanced mini-ACE only responds to Type Zero configuration access: AD[1:0] must be 00 during the command phase. Note that all combinations of byte enables for configuration writes are supported. If no byte enables are asserted during a burst write to configuration space no internal write will occur, but the internal address will be incremented.

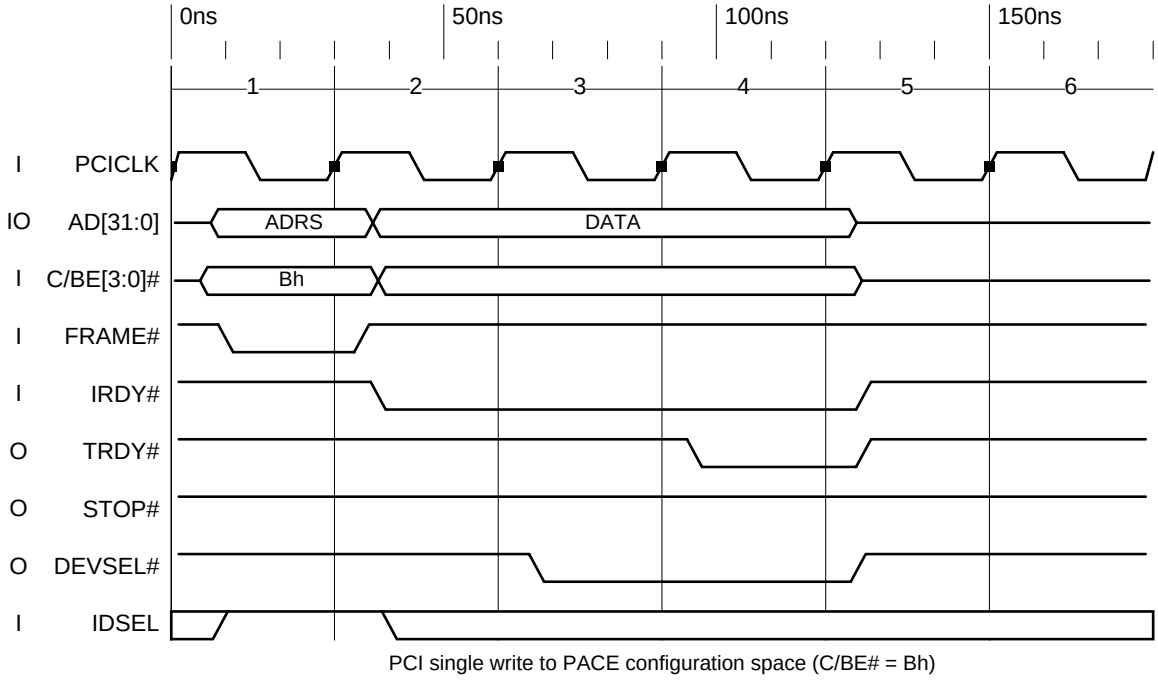
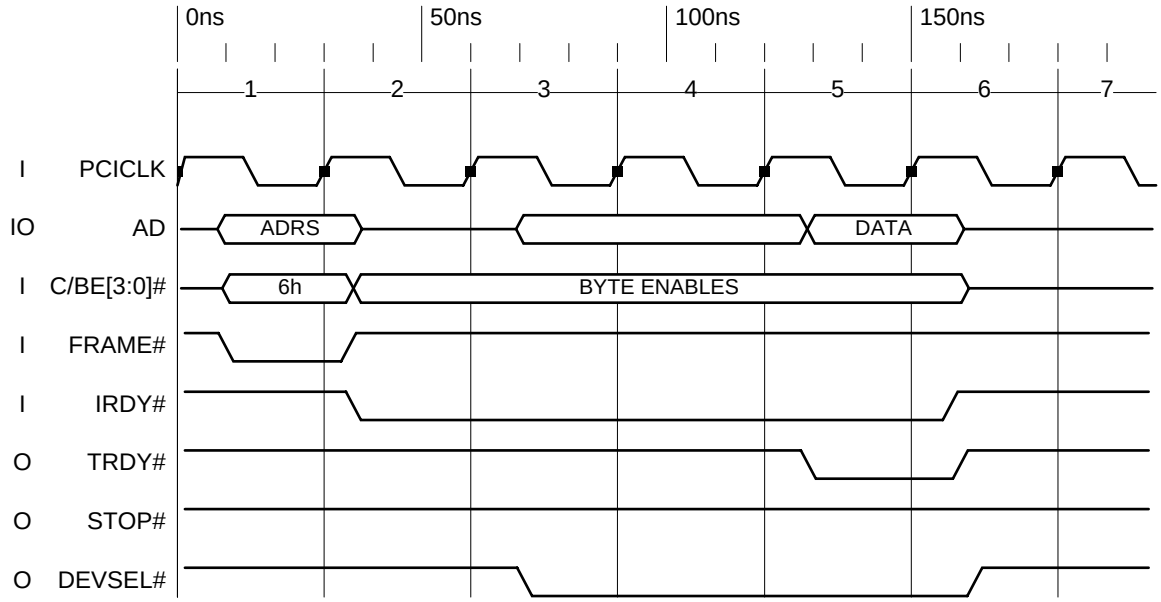


Figure 5. PCI single write to configuration space

Figure 6 shows the specific case of memory reads from the PCI-ACE interface registers at BAR1 800h-81Ch. Note that these registers are accessed quickly (they are not part of the “ACE core”) and without the Delayed Read Request mechanism required by reads from the other memory locations (see next section).



PCI memory read from PCI-ACE interface register space (BAR1 800-81Ch)

Figure 6 PCI read of PCI-ACE IF registers (BAR1 800-81Ch)

Figure *7* illustrates the process of reading an ACE memory (BAR0) or ACE register (BAR1 00-FCh) location. The actual read shown is that of a single word read, due to the ~600 nS response time shown, see following text and timing formula tables. If the write FIFO is empty and there isn't a previous Delayed Read Request (DRR) pending, a read from these locations enques a DRR, which is then processed by the PCI Enhanced mini-ACE. If either of these conditions is true, the PCI ENHANCED mini-ACE will respond with a Retry, but will not enque any new DRR. The PCI ENHANCED mini-ACE uses a DRR mechanism to respond to BA0 and BAR1 00-FCh reads because the time required to fetch these locations from the internal 16-bit shared memory is greater than the PCI data latency rules.

The PCI ENHANCED mini-ACE responds to the first read with a Retry. By PCI rules the master must repeat the same exact request until it completes. This is shown by the master's second read attempt, which also produces a Retry. Each repeated read request from the master will be target terminated with a Retry until the data from the enqued DRR is present in the PCI Enhanced mini-ACE's PCI interface. The successful completion is shown at the third read request, which produces a Disconnect with Data.

This process applies to any memory read from legal address space OTHER than the PCI-ACE interface registers at BAR1 offset 800-81Ch.

When reading ACE memory (BAR0), any combination of byte enables is supported, but the PCI Enhanced mini-ACE will drive the entire word onto the AD lines when only a single byte enable in the word is asserted.

When reading ACE registers (BAR1 00-FCh), byte enable combinations where only a single byte within a word is requested will cause the PCI Enhanced mini-ACE to terminate the transaction with a target abort. The PCI Enhanced mini-ACE will drive all zeros onto the AD lines if only the upper word byte enables or no byte enables are asserted.

With relation to actual timing, PCI double word reads of ACE memory (BAR0) will take longer to complete than single word ACE memory reads because the internal ACE memory data path is 16 bits wide. In addition, read cycles will take longer to complete with slower ACE clocks. See *Table 23* for min/max formulas for calculating completion time for the various types of reads.

Table 23 Min/Max delayed read formulas		
Type of read	**Min time formula**	**Max time formula**
ACE memory (BAR0), double word	13 x PCI_CLKperiod + 11 x ACE_CLKperiod	16 x PCI_CLKperiod + 14 x ACE_CLKperiod
ACE memory (BAR0) single word or ACE register (BAR1, double word or lower word)	8 x PCI_CLKperiod + 5 x ACE_CLKperiod	10 x PCI_CLKperiod + 6 x ACE_CLKperiod
No CBEN# asserted or ACE register (BAR1) upper word	3 x PCI_CLKperiod	3 x PCI_CLKperiod

The third case returns all zeroes and is shown only for completeness.

The following examples have the same conditions: PCI clock = 33MHz, ACE clock = 16MHz, no ACE contention.

Single word read
Min time = 8 x 30 nS + 5 x 62.5 nS = 552.5 nS
Max time = 10 x 30nS + 6 x 62.5 nS = 675 nS

Double word read
Min time = 13 x 30 nS + 11 x 62.5 nS = 1077.5 nS
Max time = 16 x 30nS + 14 x 62.5 nS = 1167.5 nS

In addition, the following amount of ACE clocks should be added for maximum time if the ACE is active.

Table 24 Additional DRR delay for contested ACE RAM access	
ACE operating mode	**Maximum additional ACE clocks**
Enhanced CPU access enabled, single word xfer	3
Enhanced CPU access enabled, double word xfer	6
Enhanced CPU access disabled, single word xfer	67
Enhanced CPU access disabled, double word xfer	74

The Enhanced CPU access is controlled by bit 14 of Configuration Register #6.

Note that one of the conditions for enquing a DRR is that the write FIFO must be empty. For efficient use of PCI bus bandwidth, the driver software should be written such that it checks the FIFO condition (BAR1 800-81CH registers are directly readable, bypassing the DRR mechanism) before reading from the other PCI Enhanced mini-ACE locations. If the FIFO is not empty (BAR1 800h bit 30 is the FIFO not empty flag) and a read is attempted, the bus master will be using PCI

bandwidth repeating the read request while the FIFO empties, BEFORE the read request is actually enqued as a DRR in the PCI Enhanced mini-ACE. The FIFO “drain” delay will increase the overall read delay further.

A typical situation where the extra FIFO “drain” delay might be encountered is during diagnostics of the internal RAM. When a RAM pattern is written to the device the FIFO can fill completely and the readback of the pattern might occur immediately after the pattern is written. In this case, the first read attempt will produce a retry which will cause the master to start repeating the read request. AFTER the FIFO drains fully the next repeated read request will actually cause the PCI Enhanced mini-ACE to enque the read request, which will start the DRR mechanism described earlier.

The FIFO drain speed is dependent upon the ACE clock and how full the FIFO is. On average, a 16MHz ACE clock can drain a Dword from the FIFO every ~600nS. For example, if the FIFO is full when a PCI read is attempted, the read will complete in ~ (32 x 0.6uS) + 1 uS = 20.2uS.

This extra delay is something to be aware of with PCI bridges/controllers that have PCI retry counters. Examples of such devices for the PPC environment are the CPC710, GT-64260, etc. If the retry counters are enabled in these parts the value should be large enough that the number of retries when reading from the PCI enhanced mini-ACE does not hit the maximum retry value. Typically, power-on default value is 0, which defeats the counter and allows infinite retries.

The minimum retry period is determined by how quickly the PCI enhanced mini-ACE terminates a transaction and the PCI rule that a master "must deassert REQ# for two consecutive clocks, one of which while the bus is Idle, before any transaction that was target terminated can be repeated". The PCI enhanced mini-ACE terminates a PCI transaction in 5 clocks, as shown in **Figure 7**. The "deassert REQ#" rule involves the bus arbiter during bus reacquisition by the master.

Actual measurements of a PCI-enhanced mini-ACE being read by the PCI motherboard host in a hi-performance X86 system (NOT the timing shown in **Figure 7**) show that a read can be retried every 8 PCI clocks. Since it is the motherboard PCI controller, the arbiter parks the PCI bus on this controller, which allows such fast retry speeds.

Therefore, in this extreme case, the motherboard host can repeat the read 84 times (20.2us/(8x30ns)) before data is presented, so the PCI retry counter should be set to a value higher than 84.

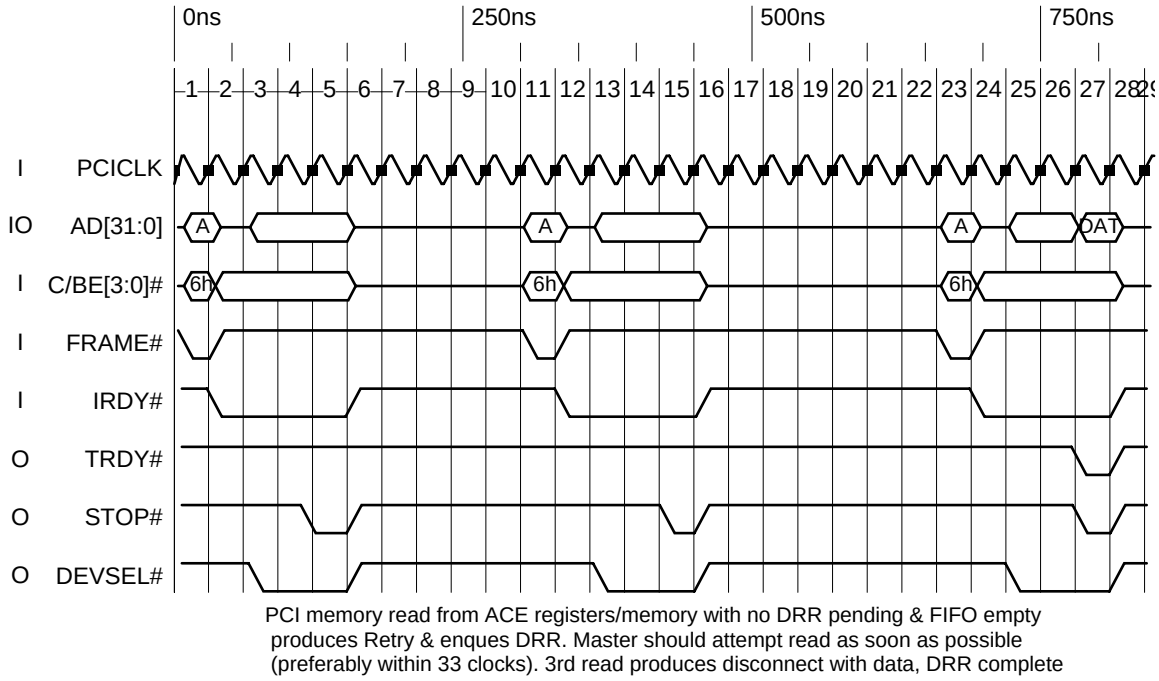


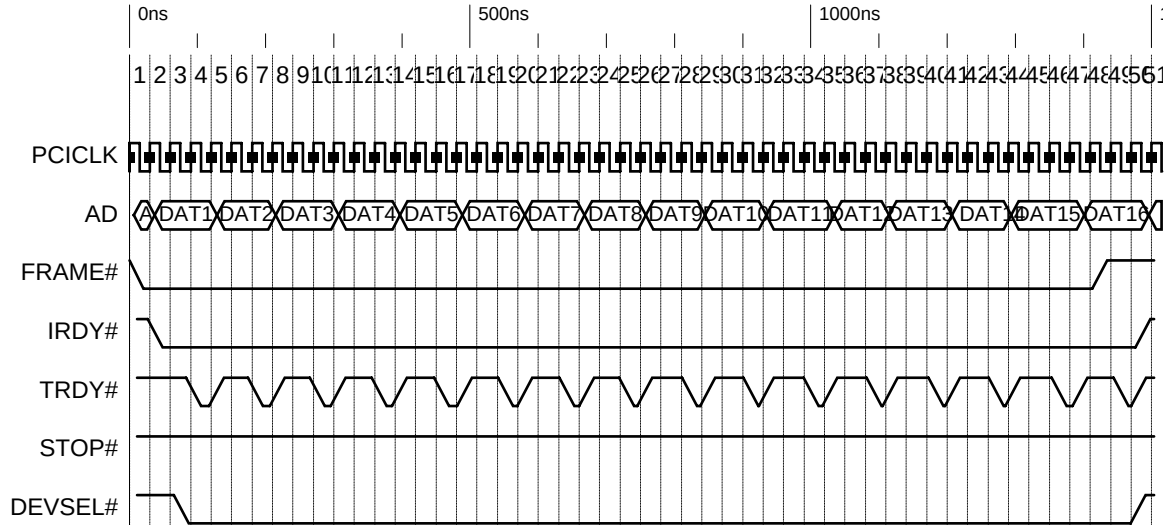
Figure 7. PCI read of ACE memory/register

Figure 8 illustrates a 16 Dword (32 word) PCI memory write burst, with the write FIFO empty (or with enough free space to absorb the 16 Dwords in the FIFO). The write FIFO accepts PCI memory writes to the ACE memory (BAR0) and ACE registers (BAR1 offset 00h – FCh). It does not accept writes to the PCI interface registers at BAR1 offset 800-81Ch. Writes to the BAR1 800-81Ch space go directly into the PCI interface registers. The 32 byte write shown could be an entire 1553 message being written to ACE memory.

Writes into the BAR 0 space must be word or Dword. If only one byte enable is asserted in a word, the PCI Enhanced mini-ACE terminates the transaction with a Target-Abort.

Writes into the BAR 1 00-FCh space must be word or Dword. If only one byte enable is asserted in a word, the PCI Enhanced mini-ACE terminates the transaction with a Target-Abort. Since the ACE registers in this space are really 16 bit registers packed into the lower word of a 32bit structure, only lower word or Dword writes transfer bits into these ACE registers.

In addition, as per PCI spec, a Memory Write and Invalidate (C/BE[3:0]# = Fh) command will be aliased to the basic Memory Write command and the timing diagram would look the same as *Figure 8*.



PCI write burst to ACE memory with FIFO empty

Figure 8 PCI write burst to ACE memory w FIFO empty

Table 25. SIGNAL DESCRIPTIONS BY FUNCTIONAL GROUPS POWER AND GROUND			
SIGNAL NAME	**PIN**		**DESCRIPTION**
	BU-62864 (64K RAM)	**BU-62843/62743 (4K RAM)**	
+5V Vcc - CH A	72	72	Channel A transceiver power.
+5V Vcc - CH B	20	20	Channel B transceiver power.
+3.3V – LOGIC	37	37	Logic power. This pin must be connected to +3.3V.
+5V - RAM	26	---	For BU-62864 this pin must be connected to +5V**.**
GROUND	17	17	Ground.
	18	18	
	19	19	
	65	65	
	67	67	

Table 26. SIGNAL DESCRIPTIONS BY FUNCTIONAL GROUPS 1553 ISOLATION TRANSFORMER INTERFACE (4)		
SIGNAL NAME	**PIN (F & G Package)**	**DESCRIPTION**
TX/RX_A (I/O)	5	Analog Transmit/Receive Inputs/Outputs. Connect directly to 1553 isolation transformers.
TX/RX_A* (I/O)	7	
TX/RX_B (I/O)	13	
TX/RX_B* (I/O)	16	

Table 27. SIGNAL DESCRIPTIONS BY FUNCTIONAL GROUPS **PROCESSOR INTERFACE CONTROL**		
SIGNAL NAME	**PIN (F & G Package)**	**DESCRIPTION**
SSFLAG* (I)/ EXT_TRIG (I)	14	Subsystem Flag (RT) or External Trigger (BC/Word Monitor) input. In RT mode, if this input is asserted low, the Subsystem Flag bit will be set in the PCI ENHANCED MINI-ACE's RT Status Word. If the SSFLAG* input is logic "0" while bit 8 of Configuration Register #1 has been programmed to logic "1" (cleared), the Subsystem Flag RT Status Word bit will become logic "1," but bit 8 of Configuration Register #1, SUBSYSTEM FLAG*, will return **logic "1"** when read. That is, the sense on the SSFLAG* input **has no effect** on the SUBSYSTEM FLAG* register bit. In the non-enhanced BC mode, this signal operates as an External Trigger input. In BC mode, if the external BC Start option is enabled (bit 7 of Configuration Register #1), a low to high transition on this input will issue a BC Start command, starting execution of the current BC frame. In the enhanced BC mode, during the execution of a Wait for External Trigger (WTG) instruction, the PCI Enhanced Mini-ACE BC will wait for a low-to-high transition on EXT_TRIG before proceeding to the next instruction. In the Word Monitor mode, if the external trigger is enabled (bit 7 of Configuration Register #1), a low to high transition on this input will initiate a monitor start. (RT the monitor on low). This input has no effect in Message Monitor mode. 5V tolerant.

Table 28. SIGNAL DESCRIPTIONS BY FUNCTIONAL GROUPS **RT ADDRESS (NOTE: ALL RT ADDRESS INPUTS ARE 5V TOLERANT)**		
SIGNAL NAME	**PIN (F & G Package)**	**DESCRIPTION**
RTAD4 (MSB) (I)	8	RT Address inputs. If bit 5 of Configuration Register #6, RT ADDRESS SOURCE, is programmed to logic "0" (default), then the PCI Enhanced Mini-ACE's RT address is provided by means of these 5 input signals. In addition, if RT ADDRESS SOURCE is logic "0", the source of RT address parity is RTADP. There are many methods for using these input signals for designating the PCI Enhanced Mini-ACE's RT address. For details, refer to the description of RT_AD_LAT. If RT ADDRESS SOURCE is programmed to logic "1", then the PCI Enhanced Mini-ACE's source for its RT address and parity is under software control, via data lines IfD5-D0. In this case, the RTAD4-RTAD0 and RTADP signals are not used.
RTAD3 (I)	6	
RTAD2 (I)	4	
RTAD1 (I)	3	
RTAD0 (LSB) (I)	1	
RTADP (I)	10	Remote Terminal Address Parity. This input signal must provide an odd parity sum with RTAD4-RTAD0 in order for the RT to respond to non-broadcast commands. That is, there must be an **odd** number of logic "1"s from among RTAD-4-RTAD0 and RTADP.
RT_AD_LAT (I)	11	RT Address Latch. Input signal used to control the PCI PCI Enhanced Mini-ACE's internal RT address latch. If RT_AD_LAT is connected to logic "0", then the PCI Enhanced Mini-ACE RT is configured to accept a hardwired (transparent) RT address from RTAD4-RTAD0 and RTADP. If RT_AD_LAT is initially logic "0", and then transitions to logic "1", the values presented on RTAD4-RTAD0 and RTADP will be latched internally on the rising edge of RT_AD_LAT. If RT_AD_LAT is connected to logic "1", then the PCI Enhanced Mini-ACE's RT address is latchable under host processor control. In this case, there are two possibilities: (1) If bit 5 of Configuration Register #6, RT ADDRESS SOURCE, is programmed to logic "0" (default), then the source of the RT Address is the RTAD4-RTAD0 and RTADP input signals; (2) If RT ADDRESS SOURCE is programmed to logic "1", then the source of the RT Address is the lower 6 bits of the processor data bus, D5-D1 (for RTAD4-0) and D0 (for RTADP). In **either** of these two cases (with RT_AD_LAT = "1"), the processor will cause the RT address to be latched by: (1) writing bit 15 of Configuration Register #3, ENHANCED MODE, to logic "1"; (2) writing bit 3 of Configuration Register #4, LATCH RT ADDRESS WITH CONFIGURATION REGISTER #5, to logic "1"; and (3) writing to Configuration Register #5. In the case of RT ADDRESS SOURCE = "1", then the values of RT address and RT address parity must be written to the lower 6 bits of Configuration Register #5, via D5-D0. In the case where RT ADDRESS SOURCE = "0", the bit values presented on D5-D0 become "don't care" .

Table 29. SIGNAL DESCRIPTIONS BY FUNCTIONAL GROUPS MISCELLANEOUS			
SIGNAL NAME	**PIN (F & G Package)**		**DESCRIPTION**
	BU-62864 (64K RAM)	**BU-62843/62743 (4K RAM)**	
INCMD* (O)/ MCRST* (O)	12	12	In-command or Mode Code Reset. The function of this pin is controlled by bit 0 of Configuration Register #7, MODE CODE RESET*/INCMD* SELECT. If this register bit is logic "0" (default), INCMD* will be active on this pin. For BC, RT, or Selective Message Monitor modes, INCMD* is asserted low whenever a message is being processed by the PCI Enhanced Mini-ACE. In Word Monitor mode, INCMD* will be asserted low for as long as the monitor is online. For RT mode, if MODE CODE RESET/INCMD* SELECT is programmed to logic "1", MCRST* will be active. In this case, MCRST* will be asserted low for two clock cycles following receipt of a Reset remote terminal mode command. In BC or Monitor modes, if MODE CODE RESET/INCMD* SELECT is logic "1", this signal is inoperative; i.e., in this case, it will always output a value of logic "1".
CLOCK_IN (I)	9	9	20 MHz, 16 MHz, 12 MHz, or 10 MHz clock input. 5V tolerant.
TX_INH A/B(I)	15	15	Transmitter inhibit input for the Channel A and Channel B MIL-STD-1553 transmitters. For normal operation, this input should be connected to logic "0". To force a shutdown of Channel A and Channel B, a value of logic "1" should be applied to the TX_INH input. 5V tolerant.
MSTCLR* (I)	2	2	Master Clear. Negative true Reset input, normally asserted low following power turn-on. When coming out of a "reset" condition, please note that the rise time of MSTCLR* must be less than 10 µs.

Table 30. SIGNAL DESCRIPTIONS BY FUNCTIONAL GROUPS PCI BUS ADDRESS AND DATA SIGNALS		
SIGNAL NAME	**PIN (F & G Package)**	**DESCRIPTION**
AD31 (I/O) (MSB)	22	32-Bit PCI Bus Address / Data lines. Address and Data are multiplexed on the same pins. Each bus operation consists of an address phase followed by one or more data phases. Address phases are identified when the control signal FRAME# is asserted. Data transfers occur during those clock cycles in which the control signals IRDY# and TRDY# are both asserted.
AD30 (I/O)	23	
AD29 (I/O)	24	
AD28 (I/O)	25	
AD27 (I/O)	27	
AD26 (I/O)	28	
AD25 (I/O)	29	
AD24 (I/O)	31	
AD23 (I/O)	34	
AD22 (I/O)	35	
AD21 (I/O)	36	
AD20 (I/O)	38	
AD19 (I/O)	39	
AD18 (I/O)	40	
AD17 (I/O)	41	
AD16 (I/O)	42	
AD15 (I/O)	53	
AD14 (I/O)	54	
AD13 (I/O)	55	
AD12 (I/O)	56	
AD11 (I/O)	57	
AD10 (I/O)	58	
AD9 (I/O)	59	
AD8 (I/O)	60	
AD7 (I/O)	62	
AD6 (I/O)	63	
AD5 (I/O)	64	
AD4 (I/O)	66	
AD3 (I/O)	68	
AD2 (I/O)	69	
AD1 (I/O)	70	
AD0 (I/O) (LSB)	71	

Table 30. SIGNAL DESCRIPTIONS BY FUNCTIONAL GROUPS
PCI BUS ADDRESS AND DATA SIGNALS

SIGNAL NAME	PIN (F & G Package)	DESCRIPTION
C/BE[3]# (I) C/BE[2]# (I) C/BE[1]# (I) C/BE[0]# (I)	32 43 52 61	Bus Command and Byte Enables. These signals are multiplexed on the same pins. During the address phase of a bus operation, these pins identify the bus command, as shown in the table below. During the data phase of a bus operation, these pins are used as Byte Enables, with C/BE[0]# enabling byte 0 (LSB) and C/BE[3]# enabling byte 3 (MSB). The PCI Enhanced mini-ACE responds to the following PCI commands **C/BE[3:0]#** — **Description (during address phase)** 0 1 1 0 — Memory Read 0 1 1 1 — Memory Write 1 0 1 0 — Configuration Read 1 0 1 1 — Configuration Write 1 1 0 0 — Memory Read Multiple 1 1 1 0 — Memory Read Line 1 1 1 1 — Memory Write and Invalidate Note that the last three memory commands are aliased to the basic memory commands: Memory Read and Memory Write
PAR (I/O)	51	Parity. This signal is even parity across the entire AD[31:0] field along with the C/BE[3:0]# field. The parity is stable in the clock following the address phase and is sourced by the Bus Master. During the data phase for write operations, the Bus Master sources this signal on the clock following IRDY# active. During the data phase for read operations, this signal is sourced by the Target and is valid on the clock following TRDY# active. The PAR signal therefore has the same timing as AD[31:0], delayed by one clock.
PCI_CLK (I)	30	Clock input. The rising edge of this signal is the reference upon which all other clock signals are based, with the exception of RST# and INTA#. The maximum frequency accepted is 33 MHz and the minimum is 0 Hz.

Table 31. SIGNAL DESCRIPTIONS BY FUNCTIONAL GROUPS PCI BUS CONTROL SIGNALS (Note that all signals listed, except INTA#, are sampled on the rising edge of PCI_CLK)		
SIGNAL NAME	PIN (F & G Package)	DESCRIPTION
FRAME# (I)	44	Frame. This signal is driven by the current bus master and identifies both the beginning and duration of a bus operation. When FRAME# is first asserted, it indicates that a bus transaction is beginning and that valid addresses and a corresponding bus command are present on the AD[31:0] and C/BE[3:0] lines, qualified by PCI _CLK. When FRAME# is deasserted the transaction is in the final data phase or has been completed.
IRDY# (I)	45	Initiator Ready. This signal is sourced by the bus master and indicates that the bus master is able to complete the current data phase of a bus transaction. For write operations, it indicates that valid data is on the AD[31:0] pins. Wait states occur until both TRDY# and IRDY# are asserted together.
TRDY# (O)	46	Target Ready. This signal is sourced by the selected target and indicates that the target is able to complete the current data phase of a bus transaction. For read operations, it indicates that the target is providing valid data on the AD[31:0] pins. Wait states occur until both TRDY# and IRDY# are asserted together.
STOP# (O)	48	Stop. The Stop signal is sourced by the selected target and conveys a request to the bus master to stop the current transaction.
IDSEL (I)	33	Initialization Device Select. This pin is used as a chip select during configuration read or write operations.
DEVSEL# (O)	47	Device Select. This signal is sourced by an active target upon decoding that its address and bus commands are valid. For bus masters, it indicates whether any device has decoded the current bus cycle.
PERR# (O)	49	Parity Error. This pin is used for reporting parity errors during the data portion of the bus transaction for all cycles except a Special Cycle. It is sourced by the agent receiving data and driven active two clocks following the detection of an error. This signal is driven inactive (high) two clocks prior to returning to the tri-state condition.
SERR# (O)	50	System Error. This pin is used for reporting address parity errors, data parity errors on Special Cycle commands, or any other condition having a catastrophic system impact.
INTA# (O)	21	Interrupt A. This pin is a level sensitive, active low interrupt to the host.

FACTORY TEST		
SIGNAL	PIN (F & G Package)	DESCRIPTION
XCVR_TP (ZAP VOLTA)	P1(*)	For factory test only. Do not connect for normal operation.
XCVR_TP (READOUTB)	P2(*)	
XCVR_TP (READOUTA)	P3(*)	
XCVR_TP (CLOCK)	P4(*)	
XCVR_TP (RESET*)	P5(*)	
XCVR_TP (ZAP VOLTB)	P6(*)	

(*) Note that the Test Output pins are pads located on the package bottom.

Table 32. BU-62864 PCI Enhanced Mini-ACE Pinout	
F & G Package	**SIGNAL NAME**
1	RTAD0
2	MSTCLR*
3	RTAD1
4	RTAD2
5	TX/RX_A
6	RTAD3
7	TX/RX_A*
8	RTAD4
9	CLOCK_IN
10	RTADP
11	RT_ADDR_LAT
12	INCMD*/MCRST*
13	TX/RX_B
14	SSFLAG*/EXT_TRIG
15	TX_INH_A/B
16	TX/RX-B*
17	GROUND
18	GROUND
19	GROUND
20	+5V Vcc CH B
21	INTA#
22	AD31
23	AD30
24	AD29
25	AD28
26	+5V RAM (See Note)
27	AD27
28	AD26
29	AD25
30	PCI_CLOCK
31	AD24
32	C/BE[3]#
33	IDSEL
34	AD23
35	AD22
36	AD21
37	+3.3V LOGIC
38	AD20
39	AD19
40	AD18
41	AD17

Table 32. BU-62864 PCI Enhanced Mini-ACE Pinout	
F & G Package	**SIGNAL NAME**
42	AD16
43	C/BE[2]#
44	FRAME#
45	IRDY#
46	TRDY#
47	DEVSEL#
48	STOP#
49	PERR#
50	SERR#
51	PAR
52	C/BE[1]#
53	AD15
54	AD14
55	AD13
56	AD12
57	AD11
58	AD10
59	AD9
60	AD8
61	C/BE[0]#
62	AD7
63	AD6
64	AD5
65	GROUND
66	AD4
67	GROUND
68	AD3
69	AD2
70	AD1
71	AD0
72	+5V Vcc CH A
P1 **	XCVR TP
P2 **	XCVR TP (READOUTB)
P3 **	XCVR TP (READOUTA)
P4 **	XCVR TP
P5 **	XCVR TP
P6 **	XCVR TP

Note: Pin 26 is +5V-RAM for BU-62864. It is “N/C” for BU-62743 and BU-62843.