WHITE PAPER

Designing A Single Board Computer For Space Using The Most Advanced Processor and Mitigation Technologies

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Abstract

As high-end computing becomes more of a necessity in space, there currently exists a large gap between what is available to satellite manufacturers and the state of the commercial processor industry. As a result, Data Device Corporation has developed a Super Computer for Space that utilizes the latest commercial Silicon-on-Insulator PowerPC processors and state-of-the-art memory modules to achieve space-qualified performance that is from 10 to 1000 times that of current technology. In addition, DDC's Super Computer for Space (SCS750) SBC is capable of executing up to 1800+ millions of instruction per second (MIPS), while guaranteeing upset rates for the entire board of less then 1 every 1000 years. Presented is a brief synopsis of DDC's design approach and radiation mitigation techniques and radiation test results employed on DDC's next generation SBC.

Introduction

A. Design Philosophy

At the beginning of 2001, DDC defined a new overall product strategy that embodied the true core competencies of the Microelectronics division. This strategy encompasses a triad of three core principles: Guaranteed Supply, Highest Performance, and Radiation Guarantee. As it applies to DDC's single board computer product line, the words have been modified slightly to: Guaranteed Upgrade Path, Space-Qualified Performance, and Radiation Guarantee.

B. Functional Description

Initially, DDC leveraged its radiation-hardened product line to build a few single board computer products based upon a set of standard processor architectures. Following a new product strategy of offering the highest performance products for space, DDC embarked on a goal of developing a "next-generation" superior single board computer. The trick was to use a processor that was not a generation behind the latest commercial processor, but rather use the latest commercial processor, while offering radiation tolerance that equaled or exceeded that of the customer's needs. A list of features that will be included in DDC's SCS750 include:

- Space-Qualified Performance of 1800+ MIPS (million of instructions per second)
- 512KB Internal L2 Cache with ECC (error-code correction)
- Software Selectable Power Consumption—5 to 20 watts

- 256Mbytes SDRAM, 64Mbytes FLASH with Reed-Solomon advanced ECC
- Based on IBM's low power, PowerPC 750FX
- Modular Design Approach
- >100 krad (Si) TID
- SEL Immune—tested to 92 LET
- 1000X improvement in SEU (1 upset in 300 years)
- TMR Processors and Advanced EDAC—transparent to application software
- Low power 5 to 20 watts depending on operation

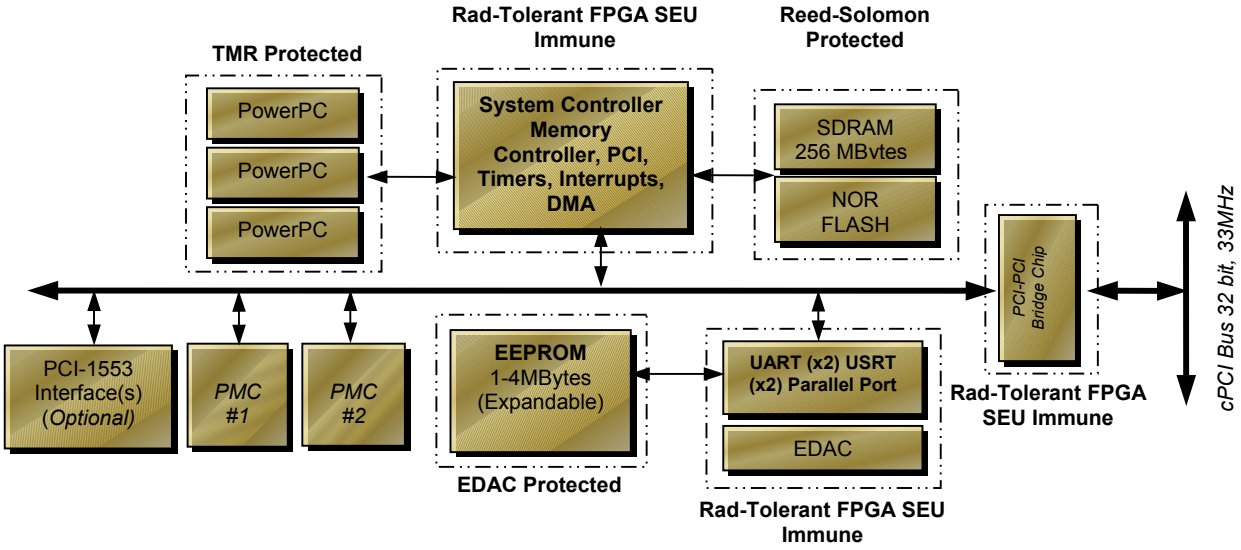
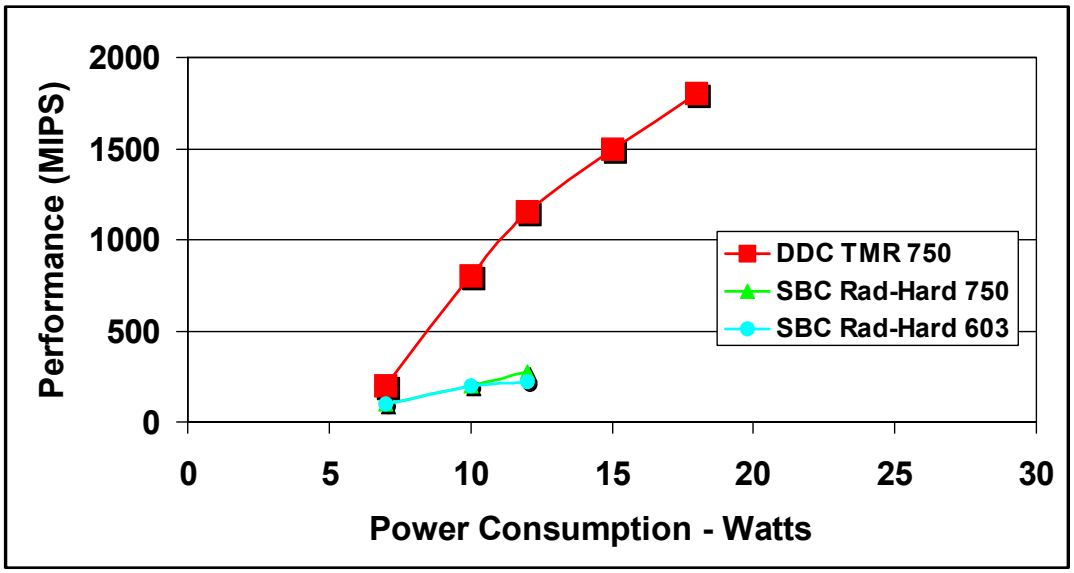


Figure 1: SCS750 Functional Block Diagram

Along with the most advanced Silicon-on-Insulator (SOI) commercial processors, DDC's SCS750 incorporates the latest radiation-tolerant FPGAs containing the core logic, along with the highest density and fastest memory (SDRAM and FLASH). With the increasing number of instruction sets and memory size, upsets and other forms of errors become a major concern in the radiation environment of space. DDC uses an advanced set of mitigation schemes such as Triple Modular Redundancy (TMR), Reed-Solomon and Bit-Scrubbing to dramatically reduce the error rates both from radiation and other sources. The combination of parts selection, testing and mitigation allows the SCS750 to achieve the highest level of performance available, while guaranteeing radiation tolerance that equals or exceeds the other computer boards currently available for the space market.

C. Processors and TMR

At the heart of DDC's SCS750 are three of the latest PowerPC750FX microprocessors from IBM, representing 800MHz of computing performance. Surprisingly, three of these processors operating in TMR mode consume less power than a single "Rad-Hard" processor. This is mostly attributable to reduced feature size and core operating voltage that is only 1.2V.



Note: Peak performance listed is based on competitors data sheets and list

Figure 2: Comparison Of Performance Versus Power Consumption For 3 Different Boards

Figure 2 shows a comparison of the performance of different radiation hardened boards versus their respective power consumption. Figure 3 shows performance versus code data/size for DDC's SCS750 as compared to a traditional rad-hard 750 board.

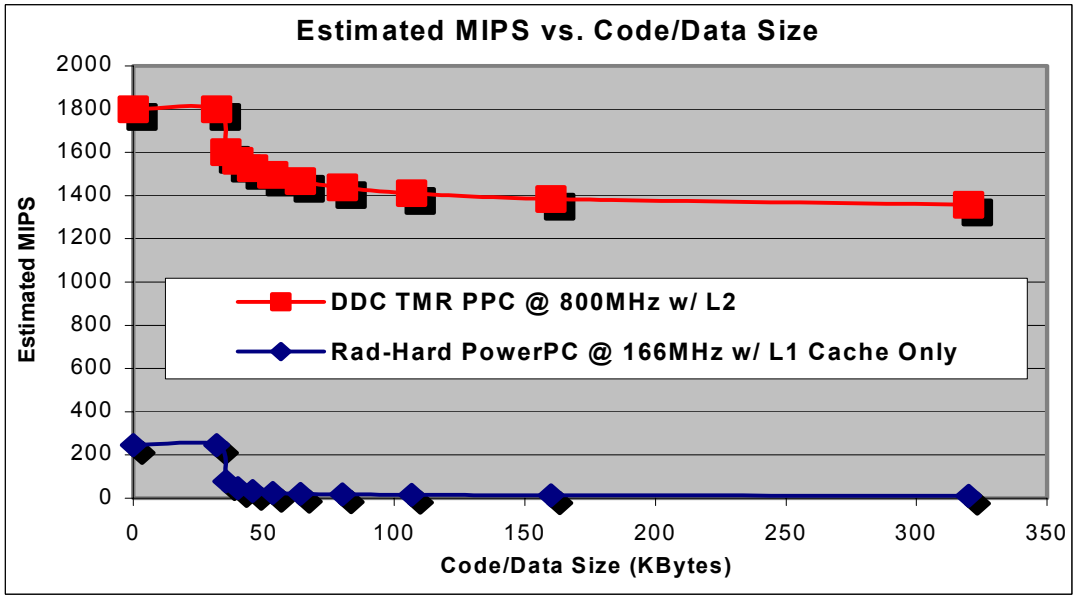


Figure 3: Performance Versus Application Code Size

SCS750 vs. Traditional RAD-HARD SBC's

Traditional Rad-Hard approaches to single board computer design revolved around fabricating custom processors and ASICs that were intended for severe radiation environments. Unfortunately, this design approach results in several undesirable effects such as long development cycles, high capital expense and often times, limited performance. Table 1 illustrates a few of the significant advantages gained by using the latest technology radiation tolerant processors in a TMR mitigation scheme. Additionally, because custom processors and ASICs often take a significant amount of time to design and develop, upgrades or redesigns may prove to be considerably more expensive.

Category	SCS750 TMR	Rad-Hard Processors
Peak Performance	>1,800 MIPS	200 to 300 MIPS
MIPS/Watt	900 MIPS / (2 wattsx3) = 150	240 MIPS / 5 watts = 48
Upgradeability	Mirrors commercial roadmap	5 to 10 years behind
Years to Upset	> 1,000 years (corrected)	273 years????

Table 1: Why Use TMR Processors?

Incorporating the latest technology Rad-Tolerant SOI processors, FPGAs, and other components takes advantage of the rapid pace of evolution that occurs in the commercial market with respect to increased speed and decreased power consumption. In addition, using an architecture that uses industry accepted development tools allows for upgrades via software and hardware drop-ins.

Table 2 shows a comparison of available processor boards—developed from a collection of public data. DDC's own data illustrates both a high performance mode (20 Watts), as well as, a configuration for low power (10 Watts). Furthermore, in the lowest performance mode, power consumption for the entire board can go down to as little as 5 watts.

Product	**Board Power (watts)**	**Memory Ram/ Nonvolatile**	**Performance**	**Time to 1st upset (years)**
DDC	20	256MB/ 64MB	1,800 MIPs @ 800 MHz	1000
DDC	10	256MB/ 64MB	900 MIPs @ 400 MHz	1000
PPC B	12	128MB/ 256KB	240 MIPs @ 133MHz	~273
PPC H	12.5	128MB/ 4MB	222 MIPs @ 133MHz	~68

Table 2: Rad-Hard Single Board Computer Comparison

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Radiation Mitigation Strategy

To facilitate the use of the highest performance commercial components, DDC has developed a comprehensive radiation mitigation strategy to provide total dose hardness, latchup immunity and unparalleled upset error rates for the SCS750. The mitigation strategy includes radiation testing both for Single Event Effects (SEE) and Total Ionizing Dose (TID), as well as, for error detection and correction. Radiation testing characterizes the radiation performance of the board allowing for verification of the total dose hardness, latchup immunity and error rate of the component parts and optimization of the error correction scheme.

A. The Processors

Single Event Upsets (SEU) and Single Event Functional Interrupts (SEFI) are mitigated using DDC's proprietary TMR approach. This TMR methodology compares all outputs of each CPU and discards the odd result. It is transparent to the application software because it is based entirely on a hardware implementation. This mitigation scheme enables errors to be detected and the upset processor to be corrected within 1 ms, thereby allowing the board to continue operating with 3 good processors without disrupting the application software. Figure 4 shows the correction and resynchronization of the processors.

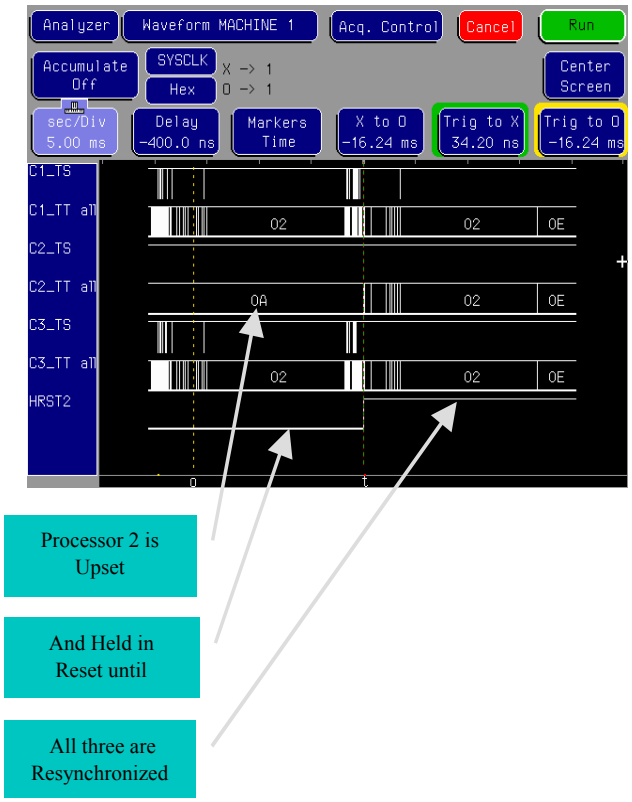

Figure 4: TMR Proof Of Design

Figure 5: Screenshot Of VxWorks On SCS750

DDC tested the TMR SCS750 board design in the laboratory utilizing the Dhrystone 1.1 benchmark in VxWorks RTOS with injected errors. A screen shot of VxWorks operating on DDC's SCS750 is shown in Figure 5.

For the actual radiation test, DDC tested three IBM 750FX PowerPC microprocessors operating with DDC's triple modular redundancy (TMR) using heavy ions at Texas A&M's cyclotron. The processors had no latchups up to the highest level tested of 92 MeV-cm^2/mg. Using DDC's TMR, all errors were detected and corrected over an LET spectrum from 2 to 92 MeV-cm^2/mg, while the beam was hitting one of the processors. As an example, in a Geosynchronous orbit using JPL 99% worst-case solar flare, the error rate for a single 750 PPC processor would be 8E-2 errors/day in the L1 data cache.

With DDC's TMR, the error rate drops to 1 E-12 errors per day (for all 3 processors) for an almost 10 order of magnitude improvement. Figure 6 depicts the test board, as well as, a close-up of the 750FX mezzanine card with the die-thinned processor. The processors had to be thinned to allow penetration of the ions during radiation testing.

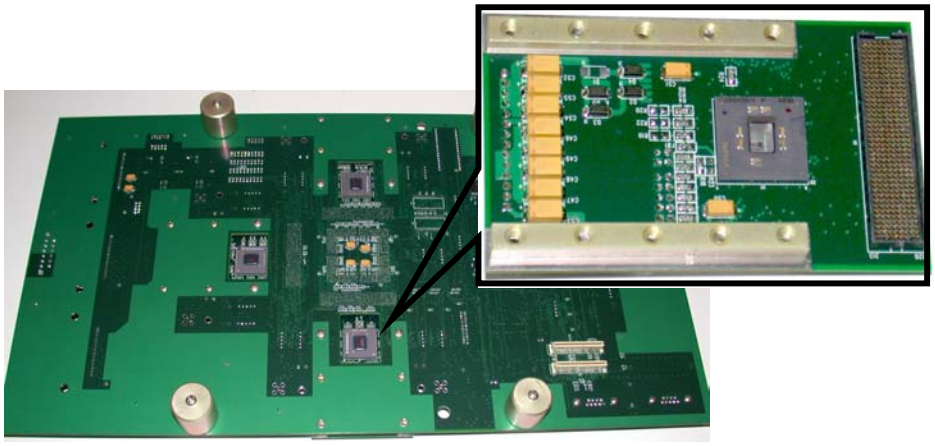

Figure 6: Backside Of Radiation Test Board

B. Memory

With respect to memory density and speed, SDRAM is required if the intent is to practically implement one gigabit memories and exploit the processing power in space. SDRAMs are a complex device because of its control structure. They are typically subject to SEL, SEU's and SEFIs (Single Event Functional Interrupt). DDC has also chosen the most sophisticated EDAC scheme of Reed-Solomon for use with the SDRAM and FLASH memory. This EDAC technique is the only solution that is capable of detecting and correcting up to two (2) nibble (4-bits wide) failures in two separate devices, while only contributing an additional 50% in overhead. This methodology utilizes 64 data bits and 32 check bits. For an error to occur, 3 out of 12 nibbles must have an error in the same row, otherwise the Reed-Solomon EDAC will correct the error.

DDC's SDRAM was tested up to 100 MeV-cm^2/mg at both room temperature (25º C) and at 100º C without latchup. The SEU rate for DDC's 256 Megabyte (2 gigabit) SDRAM configuration used on the SCS750 is 6E-18 upsets per day and 8E-14 SEFI errors per day or an error once every 12 million years for the entire memory (i.e. not a bit error rate) utilizing a Reed-Solomon EDAC scheme. Without correction the error rate would be 0.2 upsets/day and 5E-3 SEFI's/day or 73 upsets per year and a SEFI every two years in a Geosynchronous orbit.

For the remaining components, DDC has combined a proven strategy of screening commercial lots for inherent radiation hardness, including testing the SEE and TID tolerance, modeling of the intended environment and then utilizing DDC's patented Rad-Pak® shielding technology to enhance the respective part's total dose hardness.

Conclusion

To realize the highest computing performance requires the use of the latest commercial processors and components. To get the highest radiation performance requires an understanding and control of each of the individual component's radiation characteristics. This requires testing, modeling of the results in the intended environment and a robust mitigation scheme.

The Super Computer for Space—SCS750—represents a giant leap in performance of space-qualified single board computers. Using the latest commercial processors, highest density memory and standard architecture has enabled DDC to design and build a single board computer that grows with the customer's requirements, without the need for redesign, while providing unprecedented levels of radiation hardness.