SCS750

SINGLE BOARD COMPUTER FOR SPACE

- **Proven in Space**
- **Best Single Event Performance**
- **Seamless Error Correction**
- **Wide Range of Processing Power**
- **Highest Design Margin**

SCS750® FLIGHT MODULE

Overview of Specifications

- Proven in space – TRL-9
- Wide range of operating capability:
  - 200 – 1800 MIPS
  - 7 – 30 watts typical
- Speed and power settings can be managed via software in real time; no reboot required.
- Outstanding SBC radiation hardness
  - TID greater than 100 krad (Si)
  - SEU hard
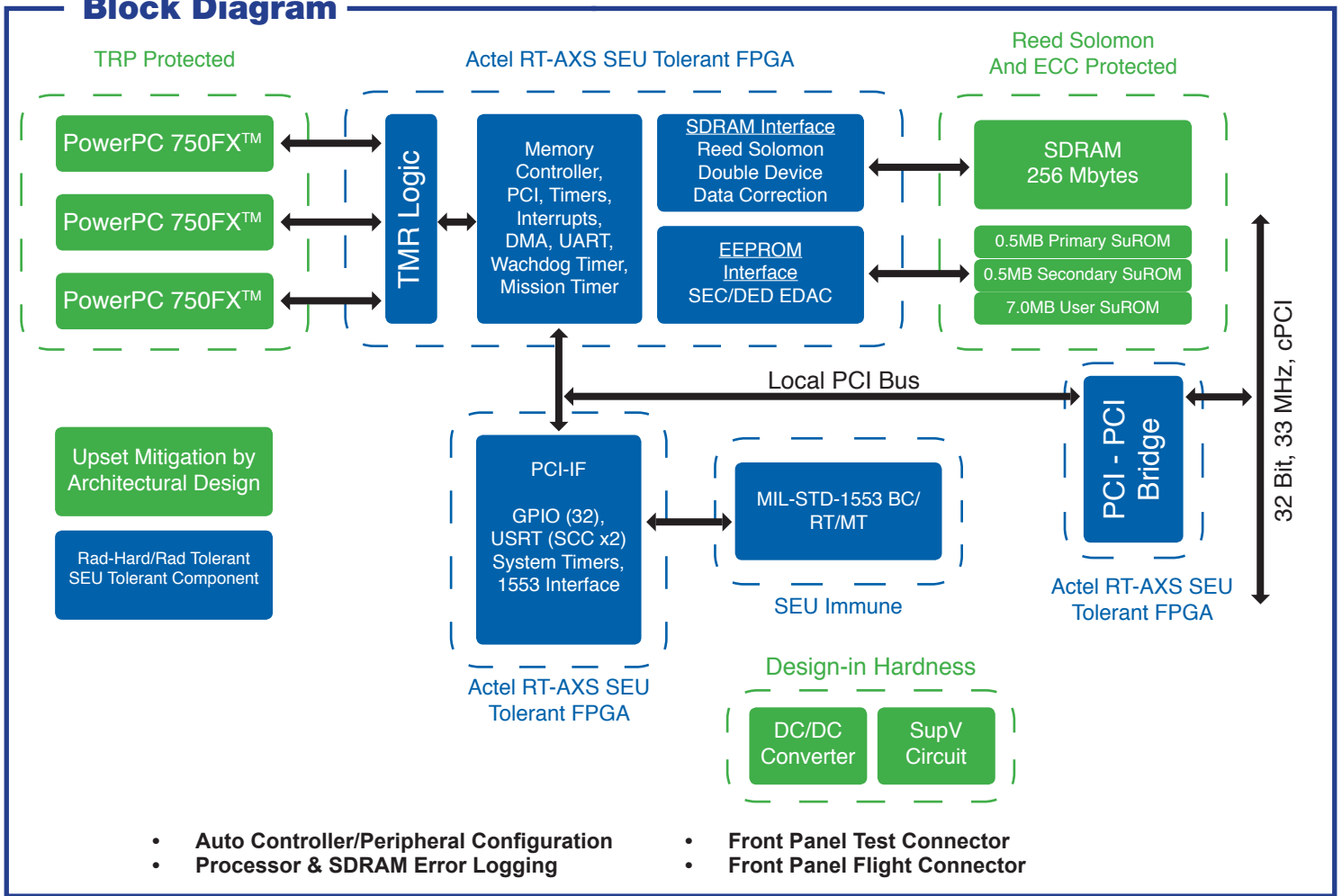 - SEL immune
- Standard development platform – VxWorks®

The **SCS750®** Single Board Computer is DDC's answer to the space industry's need for both mid- and high-performance computing, and on-board data processing requiring the upmost

data management and manipulation on the spacecraft, which requires a large amount of processing power. The **SCS750®** SBC enables satellite designs to dramatically increase error-free, on-board data processing, mission planning, and critical decision-making.
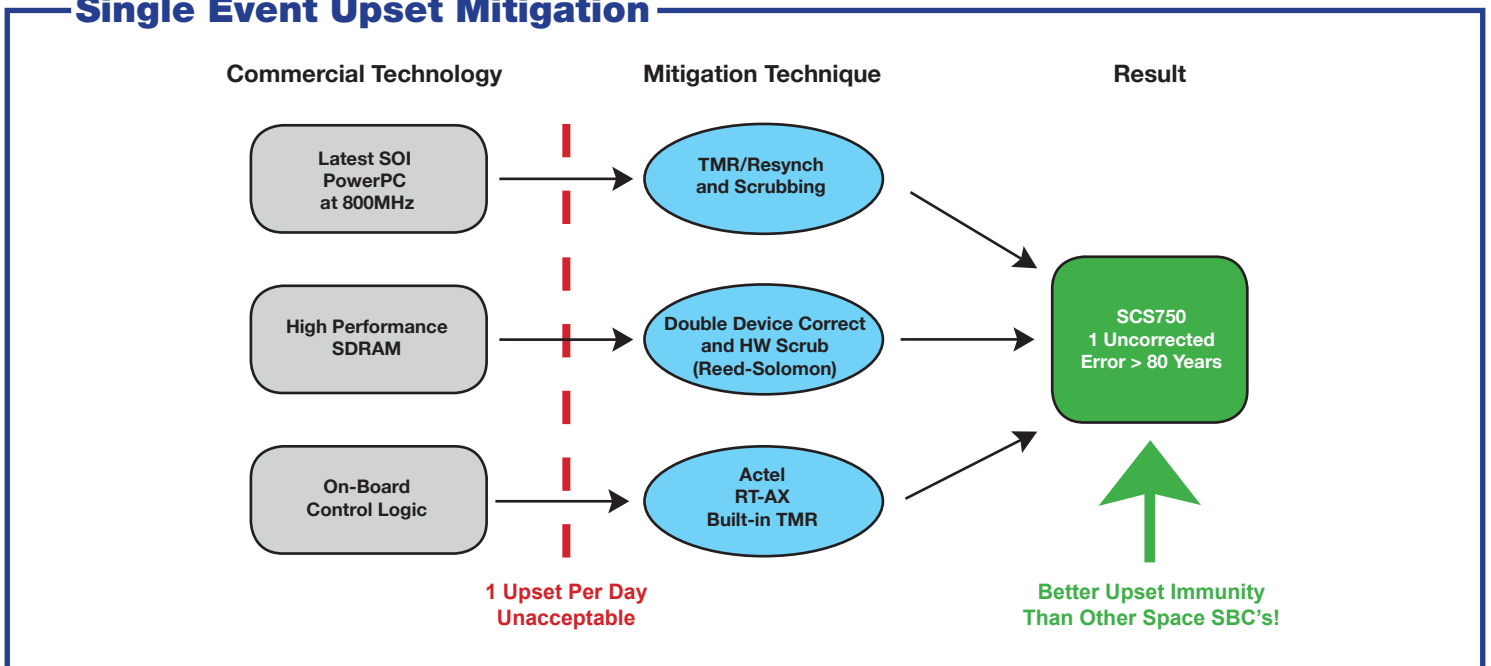
The **SCS750®** SBC has been designed to operate in a cPCI system targeting high performance computing for the most demanding space applications. Its design decisions have been driven by a guarantee of the highest reliability and performance. DDC has developed a comprehensive strategy to provide total dose, latch-up, and upset hardness for the **SCS750®** SBC.

DDC's SCS750® Single Board Computer has become the benchmark against which all space processor boards are measured.

DDC®
Connectivity Power Control

Block Diagram

TRP Protected   Actel RT-AXS SEU Tolerant FPGA   Reed Solomon
And ECC Protected

PowerPC 750FX™

PowerPC 750FX™

PowerPC 750FX™

TMR Logic

Memory
Controller,
PCI, Timers,
Interrupts,
DMA, UART,
Wachdog Timer,
Mission Timer

SDRAM Interface
Reed Solomon
Double Device
Data Correction

EEPROM
Interface
SEC/DED EDAC

SDRAM
256 Mbytes

0.5MB Primary SuROM
0.5MB Secondary SuROM
7.0MB User SuROM

32 Bit, 33 MHz, cPCI

Local PCI Bus

| Upset Mitigation by
Architectural Design |
|---|

| Rad-Hard/Rad Tolerant
SEU Tolerant Component |
|---|

PCI-IF

GPIO (32),
USRT (SCC x2)
System Timers,
1553 Interface

MIL-STD-1553 BC/
RT/MT

SEU Immune

PCI - PCI
Bridge

Actel RT-AXS SEU
Tolerant FPGA

Actel RT-AXS SEU
Tolerant FPGA

Design-in Hardness

| DC/DC
Converter | SupV
Circuit |
|---|---|

- **Auto Controller/Peripheral Configuration**
- **Processor & SDRAM Error Logging**
- **Front Panel Test Connector**
- **Front Panel Flight Connector**

Single Event Upset Mitigation

Commercial Technology   **Mitigation Technique**   **Result**

| Latest SOI
PowerPC
at 800MHz |
|---|

**TMR/Resynch
and Scrubbing**

| High Performance
SDRAM |
|---|

**Double Device Correct
and HW Scrub
(Reed-Solomon)**

| On-Board
Control Logic |
|---|

**Actel
RT-AX
Built-in TMR**

**SCS750
1 Uncorrected
Error > 80 Years**

**1 Upset Per Day
Unacceptable**

**Better Upset Immunity
Than Other Space SBC's!**
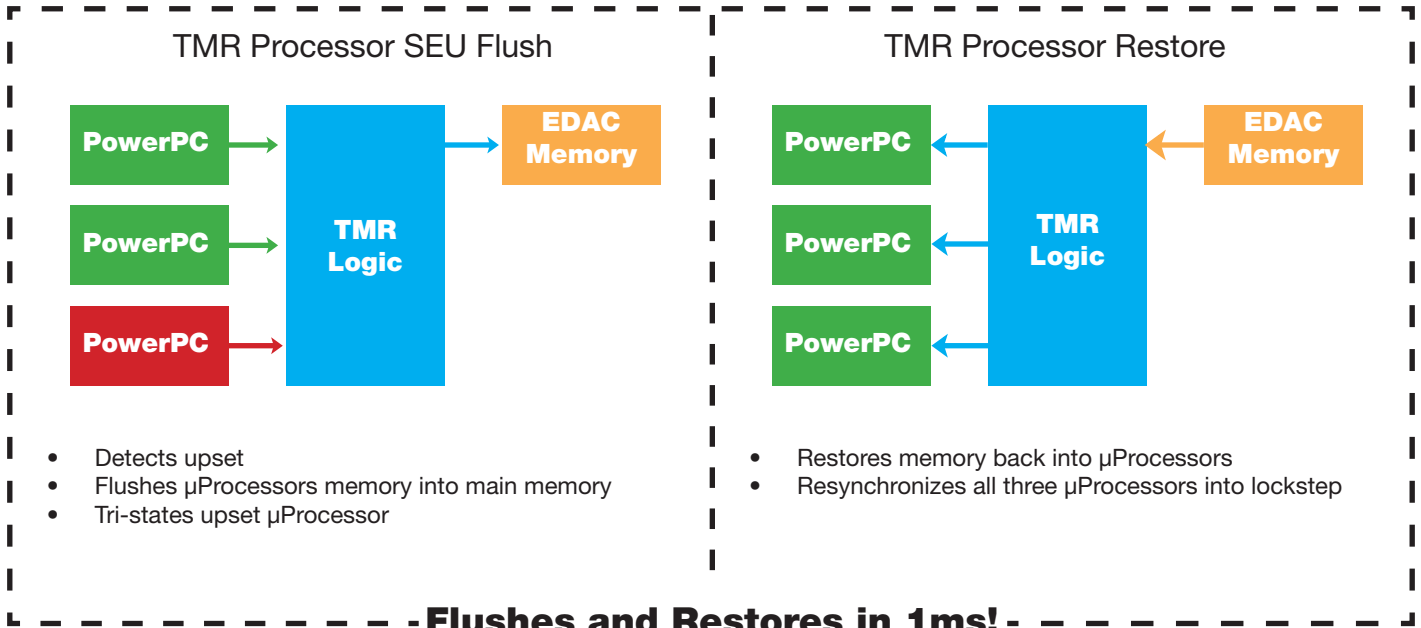
DDC®
Connectivity Power Control

Triple Redundant Processing

Resynchronization & Scrubbing
Software will reset, reload, and resynchronize
all three processors to clear errors in 1 ms.
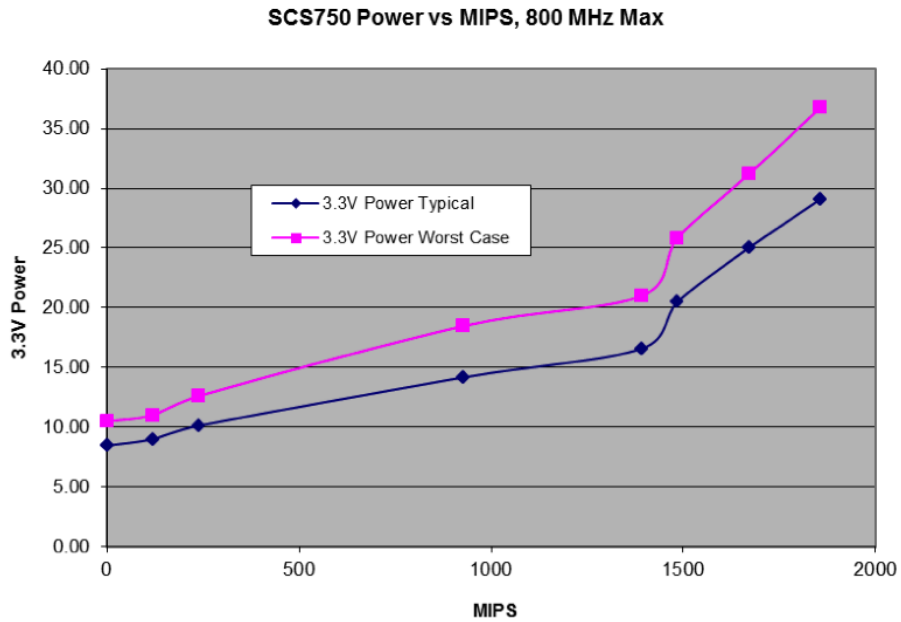
SEU Hard
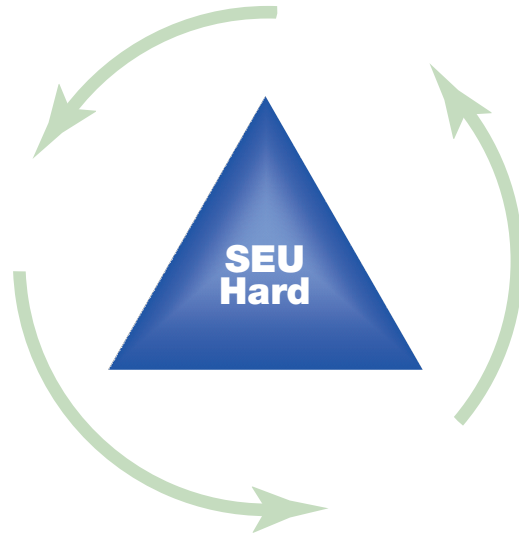
TMR Voting
Output of each clock cycle is
voted and majority is output
without delay

Error Detection
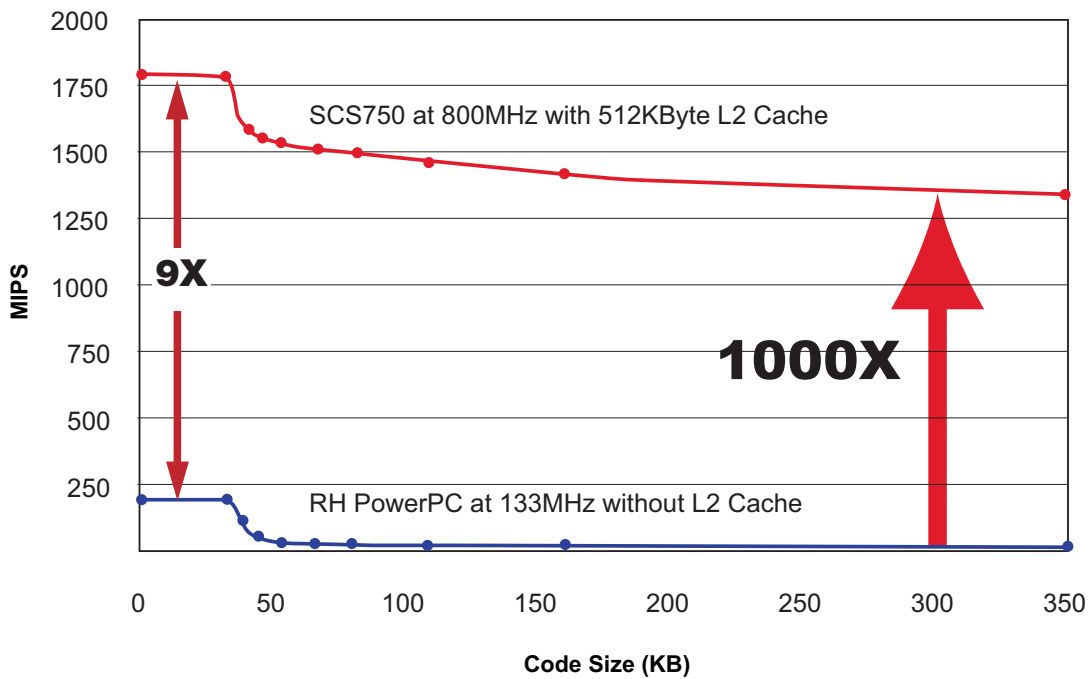Hardware isolates a disagreeing
processor and holds it in reset

Triple Modular Redundancy Protection

TMR Processor SEU Flush

PowerPC → TMR Logic → EDAC Memory
PowerPC →
PowerPC →

- Detects upset
- Flushes µProcessors memory into main memory
- Tri-states upset µProcessor

TMR Processor Restore

PowerPC ← TMR Logic ← EDAC Memory
PowerPC ←
PowerPC ←

- Restores memory back into µProcessors
- Resynchronizes all three µProcessors into lockstep

-Flushes and Restores in 1ms!-

DDC®
Connectivity Power Control

Software Selectable Power Consumption

SCS750 Power vs MIPS, 800 MHz Max

Legend:
- 3.3V Power Typical
- 3.3V Power Worst Case

X-axis: MIPS
Y-axis: 3.3V Power

Estimated MIPS vs. Code/Data Size

SCS750 at 800MHz with 512KByte L2 Cache

9X

1000X

RH PowerPC at 133MHz without L2 Cache

X-axis: Code Size (KB)
Y-axis: MIPS

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Connectivity Power Control

RADIATION TOLERANCE

- One board upset every 80 years in GEO orbit and 115 years in LEO orbit
- TID: > 100 krad (Si) - orbit dependent
- SEL (th): 84 MeV-cm^2/mg (room temperature)

(3) FULLY TMR PROTECTED PROCESSORS

- PowerPC 750FX™ on silicon on insulator (SOI), 0.13um
- 2.32 Dhrystone MIPS/MHz
- > 1800 Dhrystone MIPS @ 800MHz
- 400 to 800MHz - Software selectable core clock rate

L1 CACHE

- 32 KByte Instruction with parity
- 32 KByte Data with parity

L2 CACHE

- 512 KByte on-chip with ECC @ CPU core clock rate

MEMORY

VOLATILE

- 256 MByte SDRAM - Reed-Solomon protected - Double Device Data Correction

NON-VOLATILE

- 8 MByte EEPROM - ECC protected
  - 7.0 MByte EEPROM available to user
  - 0.5 MByte Primary SuROM
  - 0.5 MByte Secondary SuROM (autoswap on primary failure)

INTERFACES

cPCI BUS

- 6U
- 3.3V
- 32 bit, 33MHz
- Master/Target & Syscon/Peripheral

1553

- BC/RT/MT
- SEU Immune

SERIAL

- UART (Asynchronous), LVDS
- (2) USRTs (Synchronous), LVDS

PROGRAMMABLE I/O

- 32 Programmable General Purpose I/O (GPIO)

POWER

- 7 - 30 watts (typical) dependent on clock rate/MIPS requirements
- 5V for 1553 interface, 3.3V for rest of board

OPERATING SYSTEM

- VxWorks, Tornado

TEMPERATURE

- -30°C to +65°C (Acceptable levels)
- -40°C to +70°C (Qualification levels)

MECHANICAL

- 6u x 160mm
- 1.5 Kg (3.3 Lbs.) Max

MODELS

SCS750F - FLIGHT CONFIGURATION

- Rad-Tolerant, Class "S" or equivalent components
- Conduction cooled
- Flight cPCI connectors

SCS750E - ENGINEERING CONFIGURATION (EM)

- Parts identical to flight (but not screened to flight level)
- Conduction cooled
- Flight cPCI connectors

SCS750D - ENGINEERING DESIGN CONFIGURATION (EDM)

- Commercial components
- Full hardware & software compatibility w/ E & F models
- Conduction or convection cooled

SCS750P - PROTOTYPE CONFIGURATION (PEM)

- Commercial components
- Similar functionality to D, E & F models
- Convection cooled

All models are available with an optional 1553 interface

Deliverables

- Board support package
- Management documents
- Product assurance documents
- Engineering and verfication documents
- Manufacturing and test documents

DDC®
Connectivity   Power   Control