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DEI1070A-DEI1075A
ARINC 429 LINE DRIVER FAMILY

FEATURES

- TTL/CMOS to ARINC 429 Line Driver
- HI/LO Speed Control Pin for Hi (100KBS) or Lo (12.5KBS) speed slew rates
- ±9.5V to ±16.5V supplies
- Drives full ARINC load
- Output resistor options: 0, 10 or 37.5 Ohms
- Tristate Output options
- 8 lead SOICN package with exposed pad for thermal enhancement (shown actual size)
- The DEI1070A family is an improved version of the popular DEI1070 family
- Pin for pin replacements with the HI8585 and HI8586

GENERAL DESCRIPTION

The DEI107xA is a family of 8 pin bipolar integrated circuit line drivers which directly drive the ARINC 429 avionics serial digital data bus. These ARINC 429 Line Drivers convert TTL/CMOS serial input data to the "Tri-level RZ bipolar differential modulation format" of the ARINC bus. The output slew rate is selectable for HI speed (100KBS) or LOW speed (12.5KBS) operation. No external timing capacitors are required.

The DEI107xA Line Driver family is an improved version of the popular DEI107x family. It provides:

- Lower power consumption
- Excellent waveform fidelity
- Improved transient immunity. This improvement simplifies the equipment design for lightning and RF immunity requirements.

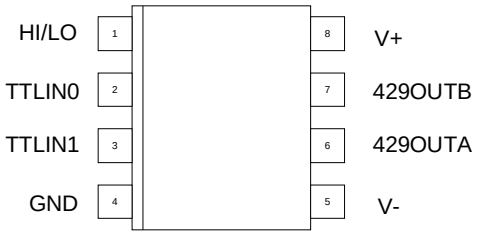
This new Line Driver family provides options for various output resistor values and output tri-state capability (see table 1). There are three output resistor options: 0Ω, 10Ω and 37Ω. The 0Ω and 10Ω versions require external resistors to achieve the 37Ω output resistance of the ARINC 429 standard. The external resistors are normally used to simplify the external transient voltage protection network. The outputs are tri-state capable on the 1073/4/5 versions. This feature is useful in non-standard applications where there are multiple drivers on a wire pair.

Table 1 Line Driver Options

	1070A	1071A	1072A	1073A	1074A	1075A
Output Resistor Value	37 Ohms	10 Ohms	0 Ohms	37 Ohms	10 Ohms	0 Ohms
Tri-state Capability	No	No	No	Yes	Yes	Yes

DS-MW-01070-02 Rev H
04/05/12

TERMINAL DESCRIPTION



Note:
Heatsink pad is electrically Isolated.

Table 2 Pin Description

PIN	NAME	DESCRIPTION
1	HI/LO	**LOGIC INPUT.** Slew rate control. 1 = Hi speed. 0 = Low speed.
2	TTLIN0	**LOGIC INPUT.** Serial digital data input 0.
3	TTLIN1	**LOGIC INPUT.** Serial digital data input 1.
4	GND	**POWER INPUT.** Ground.
5	V-	**POWER INPUT.** –9.5 to –16.5 VDC
6	429OUTA	**429 OUTPUT.** ARINC 429 format serial digital data output A.
7	429OUTB	**429 OUTPUT.** ARINC 429 format serial digital data output B.
8	V+	**POWER INPUT.** +9.5 to +16.5 VDC.

FUNCTIONAL DESCRIPTION

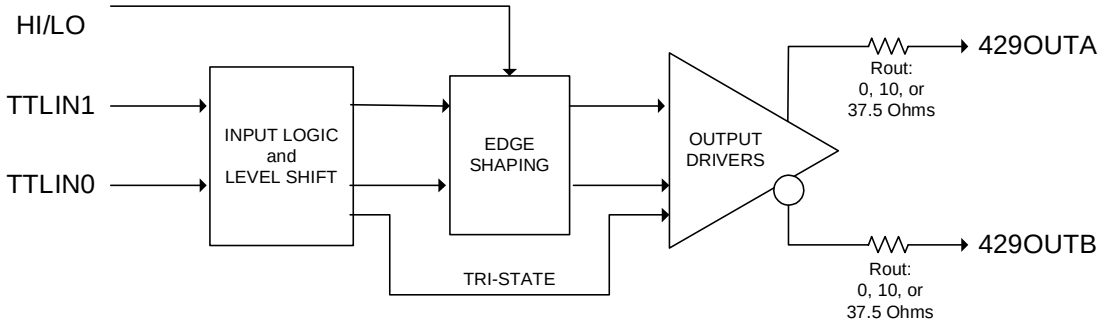


Figure 1 Block Diagram

Table 3 Speed Control Function Table

HI/LO	OUTPUT TRANSITION TIME
L	10uS (12.5KBS data)
H	1.5uS (100KBS data)

Table 4 Transmit Data Function Table

TTLIN1	TTLIN0	429OUTA	429OUTB	NOTES
L	L	0V	0V	Null output
L	H	-5V	5V	Zero output
H	L	5V	-5V	One output
H	H	0V	0V	Null output 1070A/1071A/1072A
H	H	Hi-Z	Hi-Z	Hi-Z output 1073A/1074A/1075A

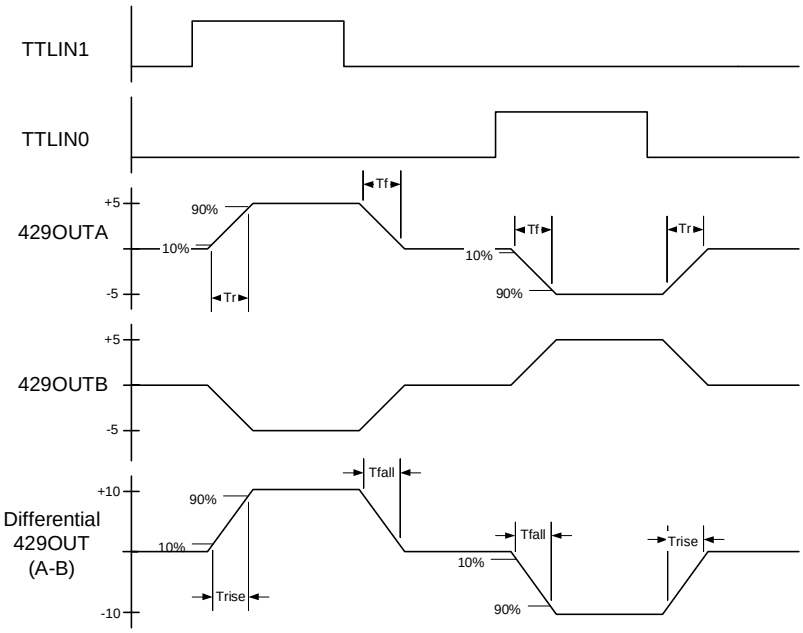


Figure 2 Line Driver Waveforms

ELECTRICAL DESCRIPTION

Table 5 Absolute Maximum Ratings

PARAMETER		MIN	MAX	UNITS
V+ Supply Voltage		-0.3	+20	V
V- Supply Voltage		0.3	-20	V
Storage Temperature		-65	+150	°C
Input Voltage				
TTLIN and HI/LO Inputs		Gnd – 0.5	'V+' + 0.5	V
429OUT Outputs (175uS surge)				
	1072A/1075A	'V-' – 1.0	'V+' + 1.0	V
	1071A/1074A	'V-' – 5.0	'V+' + 5.0	V
	1070A/1073A	'V-'– 20	'V+' + 20	V
Input Current				
429OUT Outputs (175uS surge)		-0.5	0.5	A
Power Dissipation @ 85°C				
8L EP SOIC, thermal pad soldered to heat spreader land			1.2	W
8L SB DIP			0.72	W
Junction Temperature:				
Tjmax, Plastic Packages			150	°C
Tjmax, Ceramic Packages			175	°C
ESD per JEDEC A114-A Human Body Model			2000	V
Peak body Temperature:	8L EP SOIC		260	°C

Notes:
1. Stresses above absolute maximum ratings may cause permanent damage to the device.
2. The device is tolerant of one or both outputs shorted to Ground and of both outputs shorted together.
3. Voltages referenced to Ground

Table 6 Recommended Operating Conditions

PARAMETER	SYMBOL	CONDITIONS
Supply Voltage	V+ V-	9.5 to 16.5V -9.5 to –16.5V
Operating Temperature -xEx parts -xMx parts	T_{op}	 -55 to +85 °C -55 to +125 °C

Table 7 Electrical Characteristics

PARAMETER	TEST CONDITIONS (1)	SYMBOL	MIN	NOM	MAX	UNITS
LOGIC INPUTS						
Input Voltage, Logic 1		VIH	2.0		V+	V
Input Voltage, Logic 0		VIL	-0.3		0.8	V
Input Current, Logic 1	VIN = 5.0V	IIH	0	25	100	uA
Input Current, Logic 0	VIN = 0.0V	IIL	0	-20	-100	uA
ARINC OUTPUTS						
ARINC Output Voltage HI NULL LO	Single Ended Referenced to Ground No Load.	 VoHI VoNULL VoLO	 4.5 -0.25 -5.5	 5.0 0 -5.0	 5.5 +0.25 -4.5	 V V V
Output Tristate Leakage Current 1073A/1074A/1075A	Force output to -5V and +5V	Iz	-200		+200	uA
ARINC Output Short Circuit Current 1072A/1075A	External 37.5Ω resistor to GND Output LO Output HI	 IscLO IscHI	 100 -146	 133 -133	 146 -100	 mA mA
ARINC Output Short Circuit Current 1071A/1074A	External 27.5 Ω resistor to GND Output LO Output HI	 IscLO IscHI	 67 -175	 133 -133	 175 -67	 mA mA
ARINC Output Short Circuit Current 1070A/1073A	Output shorted to GND Output LO Output HI	 IscLO IscHI	 64 -283	 133 -133	 283 -64	 mA mA
Output Resistance: 1070A/1073A 1071A/1074A 1072A/1075A	Room Temperature Calculated from delta-Vout / delta-Iload Where Iload = 0 and 20mA See Figure 3	 Rout37 Rout10 Rout0	 24 6 0	 37.5 10 0.2	 50 13.5 2	 Ohms Ohms Ohms
Output Slew Rate, Hi Speed Lo to Hi and Hi to Lo transitions	HI/LO = 1 No Load, 10% to 90% single ended output	Tr/Tf	1		2	us
Output Slew Rate, Lo Speed Lo to Hi and Hi to Lo transitions	HI/LO = 0 No Load, 10% to 90% single ended output	Tr/Tf	5		15	us
SUPPLY CURRENT						
Quiescent Operating Supply Current: IV+ IV-	V+ =15V, V- = -15V HI/LO = 0 or 1 TTLIN0=TTLIN1= 0V No Load	 IV+ IV-	 - -6.0	 3.0 -2.5	 6.0 -	 mA mA

PARAMETER	TEST CONDITIONS (1)	SYMBOL	MIN	NOM	MAX	UNITS

Notes:

1. General Conditions: Tcase = rated operating temperature, -55/+85°C or -55/+125°C. V+/- = +/-9.5 to +/-16.5V
2. Unless otherwise noted, currents flowing in to DUT are positive, currents flowing out of DUT are negative, voltages are referenced to Ground.
3. Not production tested.

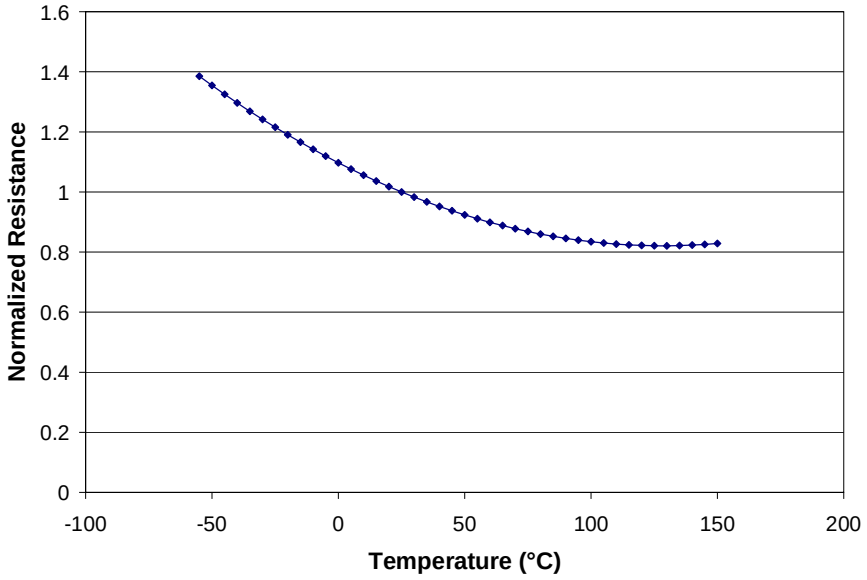


Figure 3 Normalized Output Resistance vs. Temperature

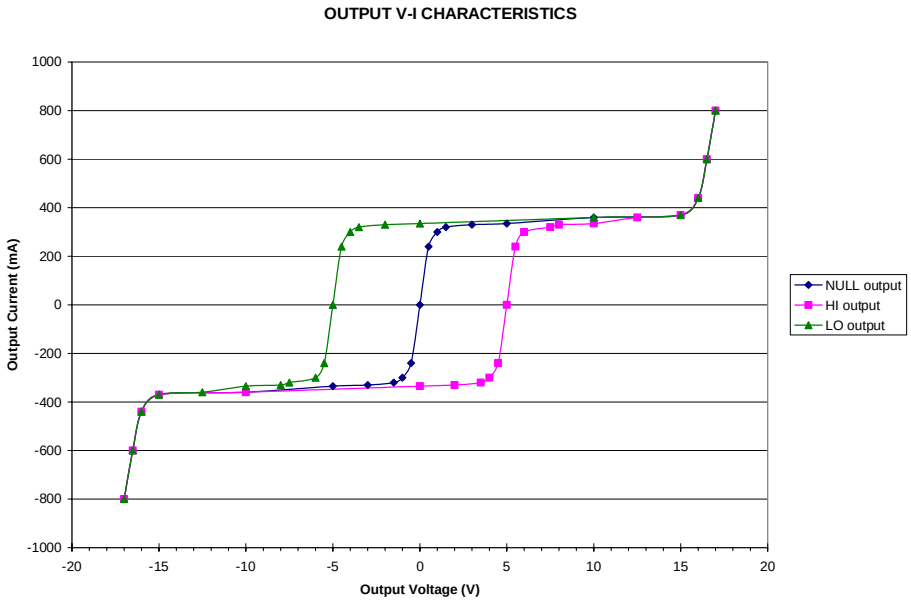


Figure 4 429OUT V-I Characteristics, ±15V supplies

DESIGN CONSIDERATIONS

Power Supplies and Bypass Capacitors

The DEI107XA Line Driver operates from ±9.5V to ±16.5V dual supplies. Proper bypassing ensures stability while driving large capacitive loads. The Line Driver requires a minimum of a 0.1uF bypass capacitor placed as close as possible to the V+ and V- pins.

Transient Voltage Protection

The DEI107xA Line Driver requires external components to achieve immunity from surges such as those defined by DO160D Section 22, "Lightning Induced Transient Susceptibility". Typical surge protection includes silicon Transient Voltage Suppressor (TVS) devices and may include all or part of the 37.5 Ohm output resistance as external resistors to limit the surge current.

The 107xA has a robust output stage which includes large driver devices and clamp diodes to the V+ and V- power rails as shown in Figure 5. It withstands surge currents of ±0.5A for 175us without damage when powered with ±15V supplies. At that surge current, the diodes clamp at ~1V above (below) the V+ (V-) supply rail. ~350mA flows to the V- (V+) supply through the output amplifier, and ~150ma flows to the V+ (V-) supply through the clamp diode. The outputs may be damaged by surges greater than 1A / 175uS. At that current, the diodes clamp at ~1.8V above (below) the supply.

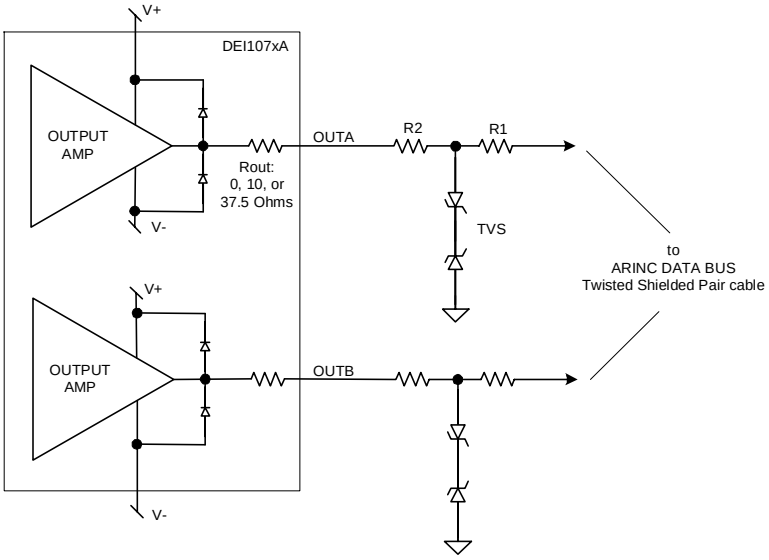


Figure 5 Surge Protection Network

The external lightning protection network should be designed to meet the specific requirements and constraints of the application equipment. The protection network should limit the OUTA/B pin surge current to the 0.5A / 175uS maximum. The generalized circuit of Figure 5 represents several TVS protection network options:

- The on-chip Rout value is 0, 10, or 37 Ohms depending on the 1070A – 1075A part number
- Select the total output resistance, Rout + R1 + R2, = 37 Ohms to meet ARINC bus requirements
  - Select R1 = 37Ω, R2 = 0Ω, Rout = 0Ω for lowest TVS surge current rating (smallest TVS devices)
  - Select R1 = 0Ω, Rout + R2 = 37Ω for highest TVS clamp voltage (20V + V+/-)
  - If the V+/V- supplies are un-powered or below operating voltage during the surge event, large currents may flow through the internal clamp diodes and damage the driver. If the application requires lightning immunity while un-powered, Select R1 = 0Ω, Rout + R2 = 37Ω, and select the TVS clamp voltage for <20V.
- Select TVS devices for the following
  - TVS Surge power/current rating must withstand the application requirements for Lightning Induced Transient Levels and Waveforms. Microsemi Corporation publishes an application note specific to the DO160 lightning requirements, available at: http://www.microsemi.com/micnotes/126.pdf
  - Select low capacitance TVS devices to minimize the load on the line driver. (Examples: Microsemi LC and HSMBJSA series TVS) This is a priority for Hi Speed ARINC applications where the low capacitance is important for optimum signal integrity and power consumption. Note that the maximum total capacitance on the ARINC bus is 30nF line to line.
  - Select the TVS clamp voltage at the lightning surge conditions such that the voltage/current into the 107XA OUT pin is within the safe region.
- If R1 is used to limit the TVS surge current, the resistor must withstand the surge current and voltage.

Alternate protection methods may be appropriate in some applications.

- External clamp diodes to the supply rails may be used to shunt surge current to the supply rails rather than to Ground.
- PTC "resetable fuses" may be used for R1 to protect the driver and TVS from shorts to 28V aircraft power.

Some general considerations related to Lightning Immunity:

- Analyze the TVS high current signal and ground return path to insure adequate surge current capability. The IR voltage and L*di/dt voltage in the ground return will add additional stress beyond the TVS clamp voltage.
- Observe suitable PCB design rules for traces subject to high voltage and high current surges.
- When possible, locate TVS devices close to the equipment connector to minimize the length of the surge voltage/current traces within the equipment.
- The shields of ARINC 429 data bus cables should be terminated to aircraft ground at all ends and at all bulkhead disconnects.

Thermal Management

Good thermal management is fundamental to Line Driver device reliability. It is particularly important in designs operating at the HI speed data rate (100KBS) with high capacitive loads as this produces maximum power dissipation. While the 107xA device will function at a junction temperature (Tj) above 190°C, it is inappropriate to continuously operate the plastic package above 150°C. Like all microcircuits, long term reliability is improved with lower operating temperatures.

The Line Driver's operating Tj is determined by internal power dissipation, package thermal resistance, and ambient temperature. The internal power dissipation (Pd) varies greatly with several variables:

- Data Rate – The Hi Speed (100kbs) rate produces maximum power dissipation
- Load – The maximum ARINC 429 load is 30nF||400 Ω line-to-line. Many applications only drive a fraction of the full load.
- Data Duty Cycle - ARINC bus activity, averaged over 10 seconds = Bits transmitted / total possible bits. Many applications are active <70%.
- Supply Voltage – V+/V- supply range is from ±9.5V to ±16.5V. Higher voltage => higher power
- Rout configuration - The power dissipated in the two 37Ω output resistors is internal to the IC for the 1070/3, and external for the 1072/5.

The internal power dissipation for 100kbs applications can be estimated from Figure 6. Pd for low speed operation (12.5kbs) is normally not an issue, so is not considered here. The curves in Figure 6 indicate Pd for various loads, supply voltage, and Rout configuration. It represents Pd for 100% Data Duty Cycle at 100KBS with no word gap null times. Thus the indicated Pd values are considered maximum values and should be reduced to account for the Data Duty Cycle as follows:

- Estimate DDC = total bits transmitted in 10 sec period / 1,000,000
  = 32 x total ARINC words transmitted in 10 sec period / 1,000,000
- Use Figure 6 to select an indicated Pd for the application supply voltage and load. This may involve estimating the Line Driver's load and interpolating between the curves.
- Calculate adjusted Pd = DDC * (Pd - 0.1) + 0.1 (W)

The operating junction temperature is calculated as follows:

$Tj = Ta + Pd*\Theta ja$

where

Tj = junction temperature (°C)

Ta = Ambient temperature (°C)

Pd = Internal power dissipation (W)

Θja = IC package thermal resistance from junction to ambient (°C/W). Refer to package details.

The ARINC 429 Line Driver outputs may be subject to short circuit conditions due to cable wiring errors or faults which typically occur during equipment test and aircraft installation environments. The common cases are one or both outputs shorted to Ground, or both outputs shorted together. These conditions may cause considerable internal power dissipation depending on the following:

- Data Duty Cycle – The line-to-line and line-to-Ground shorts cause little or no power dissipation when the outputs are in the Null state. However when the output is driving a HI/LO state, the short circuit current is limited by the 37.5Ω Rout at about ~133mA. This is modulated by the ARINC waveform, producing an effective current of ~88mA* DDC. This current causes heating in the output amplifier and Rout resistor.
- Supply Voltage – A lower supply voltage results in lower Pd during short circuit conditions. The internal Pd for both outputs shorted while operating at 100% DDC is ~2W with ±15V supplies, but is reduced to ~1.5W with ±12V supplies. This is for 0Ω Rout configurations.

- Rout configuration – Each of the two 37.5Ω Rout resistors dissipates ~0.29W when shorted at 100% DDC. This power is dissipated in the external resistors for the 1072A or 1075A parts, and internal to the IC for the 1070A or 1073A parts. Thus the 1072A or 1075A have a lower Tj and are more tolerant to short circuit conditions.

The PCB design and layout is a significant factor in determining thermal resistance (Θja) of the Line Driver IC package**.** Use maximum trace width on all power and signal connections at the IC. These traces serve as heat spreaders which improve heat flow from the IC leads**.** The exposed heat sink pad of the SOIC package should be soldered to a heat-spreader land pattern on the PCB. The IC exposed pad is electrically isolated, so the PCB land may be at any potential; typically Ground for the best heat sink. Maximize the PCB land size by extending it beyond the IC outline if possible. A grid of thermal VIAs, which drop down and connect to the buried copper plane(s), should be placed under the heat-spreader land. A typical VIA grid is 12mil holes on **a** 50mil pitch. The barrel is plated to about 1.0 ounce copper. Use as many VIAs as space allows. VIAs should be plugged to prevent voids being formed between the exposed pad and PCB heat-spreader land due to solder escaping by the capillary effect. This can be avoided by tenting the VIAs with solder mask.

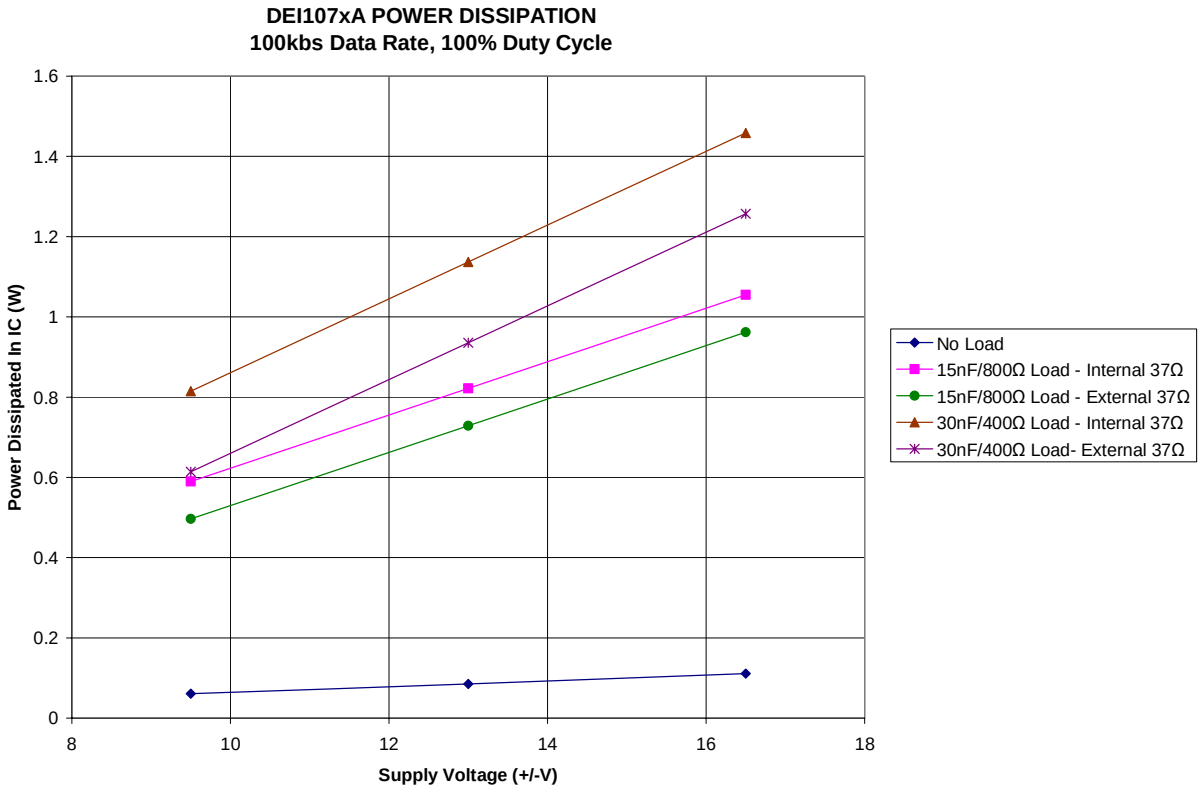


Figure 6 Internal Power Dissipation

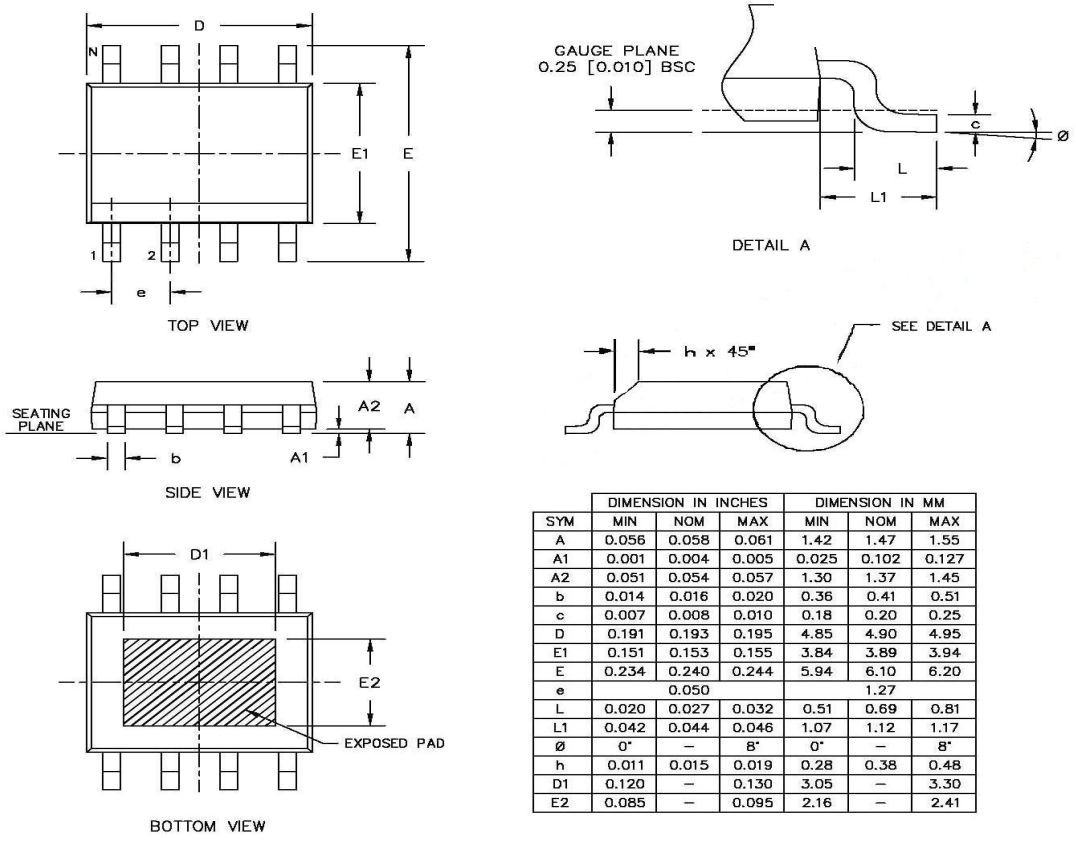
PACKAGE DESCRIPTION

Table 8 Package Characteristics

PACKAGE TYPE	PACKAGE REF	THERMAL RESIST. θJC / θJA (ºC/W)	JEDEC MOISTURE SENSITIVITY LEVEL & PEAK BODY TEMP	LEAD FINISH MATERIAL / JEDEC Pb-Free CODE	Pb Free DESIGNATON
8L SB DIP	8 SB DIP	55 / 125	HERMETIC	Au e4	Pb Free solder terminals
8L EP SOIC (Exposed Pad)	8 EP SOIC G	10 / 49 (1)	MSL 1 260ºC	NiPdAu e4	RoHS Compliant
8L ES SOIC (Exposed Slug)	8 ES SOIC G	10 / 49 (1)	MSL 1 260ºC	Matte Sn e3	RoHS Compliant

Notes:

1. θJA with the exposed pad soldered to a PCB land with (6) 12mil thermal vias connected to an internal ground plane which is one of the 2 center layers on a 4 layer board .



	DIMENSION IN INCHES			DIMENSION IN MM		
SYM	MIN	NOM	MAX	MIN	NOM	MAX
A	0.056	0.058	0.061	1.42	1.47	1.55
A1	0.001	0.004	0.005	0.025	0.102	0.127
A2	0.051	0.054	0.057	1.30	1.37	1.45
b	0.014	0.016	0.020	0.36	0.41	0.51
c	0.007	0.008	0.010	0.18	0.20	0.25
D	0.191	0.193	0.195	4.85	4.90	4.95
E1	0.151	0.153	0.155	3.84	3.89	3.94
E	0.234	0.240	0.244	5.94	6.10	6.20
e		0.050			1.27	
L	0.020	0.027	0.032	0.51	0.69	0.81
L1	0.042	0.044	0.046	1.07	1.12	1.17
Ø	0°	–	8°	0°	–	8°
h	0.011	0.015	0.019	0.28	0.38	0.48
D1	0.120	–	0.130	3.05	–	3.30
E2	0.085	–	0.095	2.16	–	2.41

Figure 7 Mechanical Outline - 8L EP SOIC (Exposed Pad)

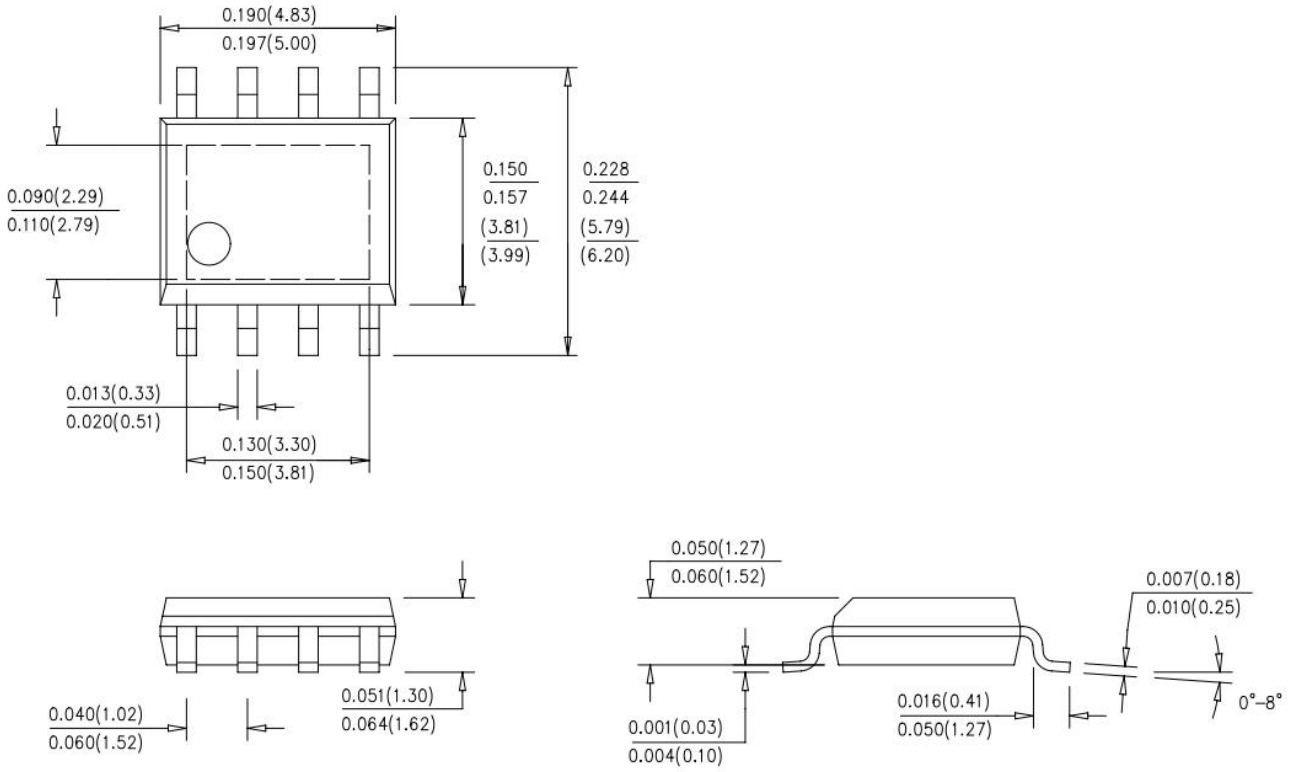


Figure 8 Mechanical Outline - 8L ES SOIC (Exposed Slug)

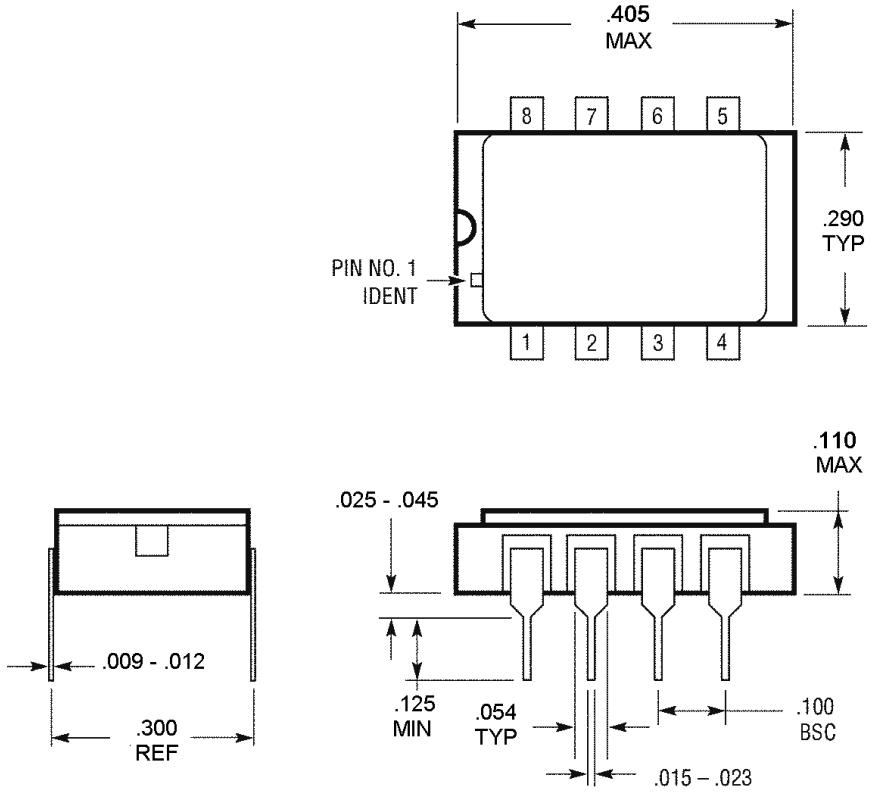


Figure 9 Mechanical Outline - 8L Ceramic Sidebrazed DIP

PROCESS DESCRIPTION

Table 9 Process Flow

PROCESS STEP	STANDARD	BURN-IN
PRE-BURN-IN Electrical Test	N/A	YES
BURN IN (1)	N/A	96hrs @ +125 °C
FINAL ELECTRICAL TEST, Room Temperature	100%	100%
FINAL ELECTRICAL TEST, High Temperature	100% @ +85 or +125°C	100% @ +85 or +125°C
FINAL ELECTRICAL TEST, Low Temperature	0.65% AQL @ -55°C	0.65% AQL @ -55°C

NOTES:

1. Burn-in conditions: 125°C, 96 hrs, V+/V- = +/-15.0V Inputs = 0V, Outputs open.

ORDERING INFORMATION

Table 10 Ordering Information

Part Number	Marking	Package	Output Resistor	Tri State Output	Burn-In	Temperature
DEI1070A-SES-G	DE1070A / ES	8L EP SOIC G	37	No	No	-55 / +85 ºC
DEI1070A-SMS-G	DE1070A / MS	8L EP SOIC G	37	No	No	-55 / +125 ºC
DEI1070A-SMB-G	DE1070A / MB	8L EP SOIC G	37	No	Yes	-55 / +125 ºC
DEI1070A-DMS	DEI1070A / DMS	8L SB DIP	37	No	No	-55 / +125 ºC
DEI1070A-DMB	DEI1070A / DMB	8L SB DIP	37	No	Yes	-55 / +125 ºC
DEI1071A-SES-G	DE1071A / ES	8L EP SOIC G	10	No	No	-55 / +85 ºC
DEI1071A-SMS-G	DE1071A / MS	8L EP SOIC G	10	No	No	-55 / +125 ºC
DEI1071A-SMB-G	DE1071A/MB	8L EP SOIC G	10	No	Yes	-55 / +125 ºC
DEI1071A-DMS	DEI1071A / DMS	8L SB DIP	10	No	No	-55 / +125 ºC
DEI1071A-DMB	DEI1071A / DMB	8L SB DIP	10	No	Yes	-55 / +125 ºC
DEI1072A-SES-G	DE1072A / ES	8L EP SOIC G	0	No	No	-55 / +85 ºC
DEI1072A-SMS-G	DE1072A / MS	8L EP SOIC G	0	No	No	-55 / +125 ºC
DEI1072A-SMB-G	DE1072A / MB	8L EP SOIC G	0	No	Yes	-55 / +125 ºC
DEI1072A-DMS	DEI1072A / DMS	8L SB DIP	0	No	No	-55 / +125 ºC
DEI1072A-DMB	DEI1072A / DMB	8L SB DIP	0	No	Yes	-55 / +125 ºC
DEI1072A-YES-G	DEI / 1072AYES	8L ES SOIC G	0	No	No	-55 / +85 ºC
DEI1073A-SES-G	DE1073A / ES	8L EP SOIC G	37	Yes	No	-55 / +85 ºC
DEI1073A-SMS-G	DE1073A / MS	8L EP SOIC G	37	Yes	No	-55 / +125 ºC
DEI1073A-SMB-G	DE1073A / MB	8L EP SOIC G	37	Yes	Yes	-55 / +125 ºC
DEI1073A-DMS	DEI1073A / DMS	8L SB DIP	37	Yes	No	-55 / +125 ºC
DEI1073A-DMB	DEI1073A / DMB	8L SB DIP	37	Yes	Yes	-55 / +125 ºC
DEI1074A-SES-G	DE1074A / ES	8L EP SOIC G	10	Yes	No	-55 / +85 ºC
DEI1074A-SMS-G	DE1074A / MS	8L EP SOIC G	10	Yes	No	-55 / +125 ºC
DEI1074A-SMB-G	DE1074A / MB	8L EP SOIC G	10	Yes	Yes	-55 / +125 ºC
DEI1074A-DMS	DEI1074A / DMS	8L SB DIP	10	Yes	No	-55 / +125 ºC
DEI1074A-DMB	DEI1074A / DMB	8L SB DIP	10	Yes	Yes	-55 / +125 ºC
DEI1075A-SES-G	DE1075A / ES	8L EP SOIC G	0	Yes	No	-55 / +85 ºC
DEI1075A-SMS-G	DE1075A / MS	8L EP SOIC G	0	Yes	No	-55 / +125 ºC
DEI1075A-SMB-G	DE1075A / MB	8L EP SOIC G	0	Yes	Yes	-55 / +125 ºC
DEI1075A-DMS	DEI1075A / DMS	8L SB DIP	0	Yes	No	-55 / +125 ºC
DEI1075A-DMB	DEI1075A / DMB	8L SB DIP	0	Yes	Yes	-55 / +125 ºC