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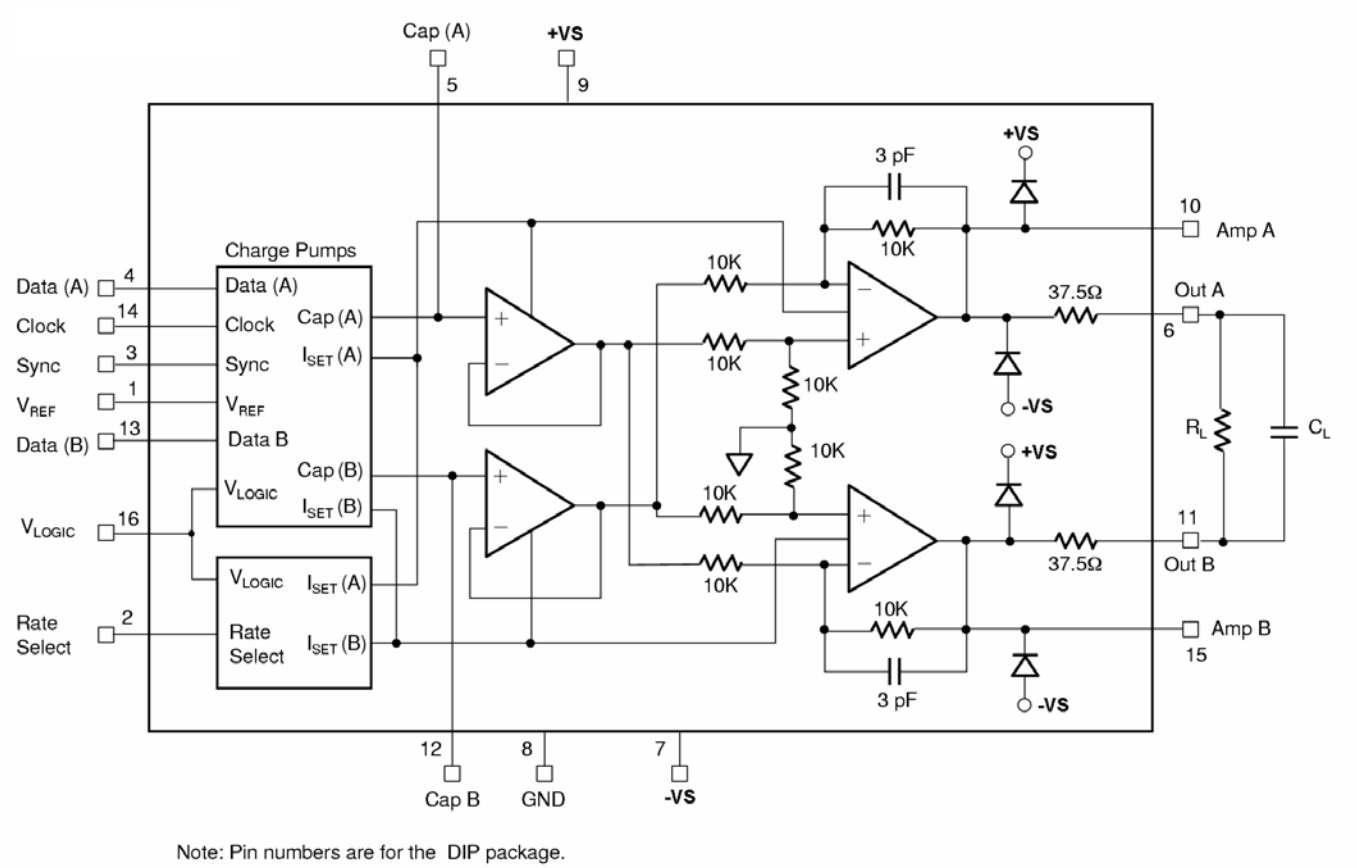
DEI3182A
ARINC 429 DIFFERENTIAL LINE DRIVER

FEATURES

- Adjustable rise and fall times
- Low supply current
- Capable of driving 30 nF || 400Ω
- Digitally selectable 12.5 or 100 kbit/sec data rate
- Adjustable output voltages swing
- Output over-voltage protected
- Short circuit tolerant
- TTL and CMOS compatible inputs
- MIL-STD-883B burn-in screening available
- Package Options:16L SB DIP, 16L CERDIP, 28L CLCC
- Direct replacement for Fairchild/Raytheon RM3182A

FUNCTION DIAGRAM



Note: Pin numbers are for the DIP package.

Description

The DEI3182A is a complete differential line driver IC. When Data A = Data B or Sync or Clock Signal is low, the driver forces the output to a Voltage Null level (0V ± 250 mV). Designed to address the ARINC 429 Standard, the DEI3182A has output rise and fall times that can be adjusted by the selection of an external capacitor (C_A or C_B) and an output voltage range adjustable through an externally applied V_{REF} signal. All logic inputs and sync control inputs are TTL/CMOS compatible. The device is constructed on a monolithic IC using a junction-isolated bipolar process. SiCr resistors in the internal bias circuitry provide for stable bias currents and a tighter tolerance of output impedance. The DEI3182A is available in 16-lead ceramic side-brazed DIP and can be ordered with MIL-STD-883B burn-in screening.

Functional Description

The device contains three main functional blocks. The first block is a digital section used to decode the ARINC Clock, Synchronization, and Data inputs as shown in Block Diagram. This block takes these inputs and channels the data to the charge pump circuits. The logical relationship for these pins is presented in Table 1.

Table 1. I/O Truth Table

Sync	Clock	Data A	Data B	Out A	Out B	Comments
X	L	X	X	0V	0V	Null
L	X	X	X	0V	0V	Null
H	H	L	L	0V	0V	Null
H	H	L	H	-VREF	+VREF	Low
H	H	H	L	+VREF	-VREF	High
H	H	H	H	0V	0V	Null

The second functional block is a charge pump circuit that is used to control the output waveform and its timing characteristics. This is achieved through charging and discharging a capacitor with a known current. The capacitor is user selectable, and is connected between C_A or C_B pins and ground. A rate select pin (digital input) enables to set the rise and fall time. If this pin is tied to ground, the device functions in the high rate. This mode is recommended if the user does not have an application requiring data rate switching. In the table below, recommended capacitor values are given for each possible data combination.

Table 2. Rate Select Pin Truth Table

Rate Select	C_A C_B (pf)	10% to 90% Rise/Fall time (µS)	Ca/Cb nom. charge current (uA)	Data Rate (Kbits/sec)	Comments
Logic 0	68*	1.0 – 2.0	210	100	High Rate
Logic 1	68*	5 - 15	30	12-14.5	Low Rate
Logic 0	470	5 - 15	210	12-14.5	Low Rate
Logic 1	470	N/A	30	N/A	Not Used

* Does not include the assumed 10pf for PCB trace and IC lead capacitance.

The last functional block of the device consists of a voltage follower and a high power output differential amplifier. The voltage follower buffers the signals presented at the charge caps and presents the mirrored signal to the difference amplifier to drive the ARINC line. Two different outputs are available from the differential amplifiers: Amp A, Amp B, and Out A, Out B. The outputs Amp A and Amp B are the direct outputs of the power amplifier. The outputs Out A and Out B include 37.5Ω series resistors added to minimize bus reflections by matching the power amplifier's output impedance to the cable's impedance of 75Ω . Amp A and Amp B may be used to customize the output impedance of the device. These outputs can also be used to enhance the device's drive capability. For example, driving the standard 30 nF || 400Ω load defined in the ARINC specifications (see output drive capability and capacitive loads for more details). All outputs are protected from voltage spikes with diodes connected between the output pins and the supply lines.

Output Drive Capability and Capacitive Loads

The Traditional Approach

The DEI3182A is capable of driving a high capacitive/resistive load. If complete ARINC compliance is required then Out A and Out B pins are recommended to maintain the output impedance. In this configuration, driving the full ARINC load of 30nF || 400Ω the output characteristic takes on the transfer function of a low pass filter due to the internal 37.5Ω resistor, the line resistance and the capacitance associated with the cable. This will result in a lower rise/fall time of the device. Equation 1.1 relates the output voltage at Out A and Out B to the voltage at the power amplifier's output. Output A is taken for this example: The output as a function of

frequency is given by equation 1.1

$$1.1 \quad OutA = \frac{AmpA\ Z_L /2}{(Z_L/2) + R_{OUT}}$$

Where: $R_{OUT} = 37.5\Omega$ and $Z_L = R_L \| C_L$

The output as a function of Frequency is given by Equation 1.2.

$$1.2 \quad A_{OUT}(j\omega) = Amp\ A(j\omega) \left[\frac{R_L}{R_L + 2R_{OUT}(1+ j\omega C_L R_L)} \right]$$

Using equation 1.2, a time constant can be determined for the given application which is shown in equation 1.3.

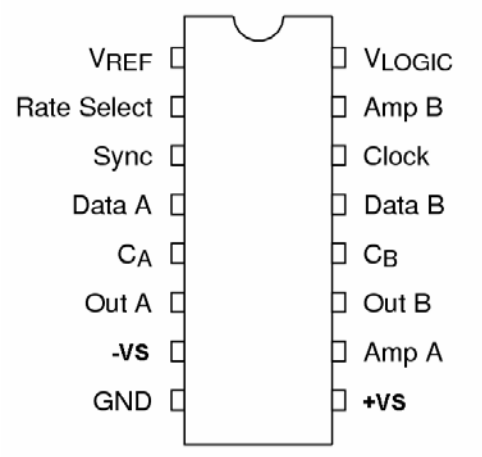
$$1.3 \quad \tau = (R_{OUT} \| R_L) C_L$$

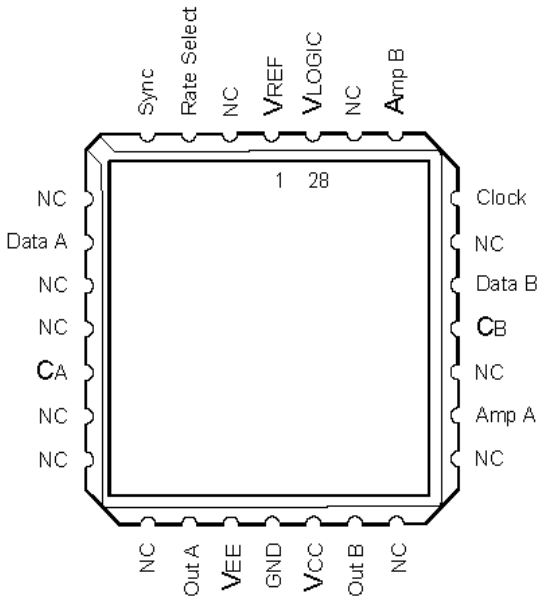
So, for the maximum loading condition of 30nF || 400Ω the resulting time constant is 1.9 µs. This shows that with a maximum load, the output waveform is greatly affected by the low pass filter combination of the ROUT || RL resistor and the load capacitance.

A New Option: Amp A/Amp B

The DEI3182A also provides the user the option of connecting the data line directly to the power output amplifiers thus bypassing the internal 37.5Ω resistance of the device and matching the line more precisely. For example, using a 1% 37.5Ω resistor allows better control of the output impedance. By applying the load directly to the power amplifiers output pins, the resulting waveform is virtually unchanged when driving other loads. There may be applications where these pins present a more desirable result. For instance, if the line that the chip is driving is short, then the parasitic components of the line can be neglected, and power amplifier can be tied directly to the lines. This option can be utilized to achieve a greater noise immunity through bypassing the internal resistors.

Pin Assignments





Absolute Maximum Ratings

Parameter		Min.	Max.	Units
Supply Voltage:	+VS to -VS		+36	V
	+VS to GND		+20	V
	-Vs to GND	-20		V
V_{LOGIC} Threshold Voltage		0	+7	V
V_{REF} Voltage		0	+6	V
Logic Input Voltage		-0.5	V_{LOGIC} + 0.5	V
AMP A/B Transient Pulse: 150uS pulse applied through an external 37.5Ω resistor. (1)		-70	+70	V
Storage Temperature Range		-65	+150	°C
Operating Temperature Range		-55	+125	°C
Junction Temperature		-55	+175	°C
Lead Soldering Temperature (60 sec.)			+300	°C

Note:

1. Sample tested on each wafer lot.

Thermal Characteristics

(Still air, soldered into PC board)

Parameter	16-Lead Side-brazed DIP	16-Lead CERDIP	28-Lead LCC
Thermal Resistance, θ_{Ja}	70°C/W	70°C/W	60°C/W
Thermal Resistance, θ_{JC}	28°C/W	28°C/W	25°C/W

Recommended Operating Conditions

Symbol	Parameters	Min.	Max.	Units
$+V_S$	Positive Supply Voltage	13.5	16.5	V
$-V_S$	Negative Supply Voltage	-16.5	-13.5	V
V_{LOGIC}	V_{LOGIC} Supply Voltage	4.5	5.5	V
V_{REF}	V_{REF} Voltage	4.75	5.25	V
T_{op}	Case Temperature	-55	125	ºC

Electrical Characteristics

Symbol	Parameters	Test Conditions (1,2)	Min.	Max.	Units
		POWER SUPPLIES			
I_{CC}	Positive Supply Current	+VS = 16.5V, -VS = -16.5V, VLOGIC = VREF = 5.5V, DATAA =CLOCK=SYNC=VIH DATAB=RATE = VIL Outputs = HI, unloaded	4.0	18	mA
I_{EE}	Negative Supply Current	+VS = 16.5V, -VS = -16.5V, VLOGIC = VREF = 5.5V, DATAA =CLOCK=SYNC=VIH DATAB=RATE = VIL Outputs = HI, unloaded	4.0	18	mA
I_{LOGIC}	V_{LOGIC} Supply Current	+VS = 16.5V, -VS = -16.5V, VLOGIC = VREF = 5.5V, DATAA =CLOCK=SYNC=VIH DATAB=RATE = VIL Outputs = HI, unloaded	150	300	µA
I_{REF}	V_{REF} Supply Current	+VS = 16.5V, -VS = -16.5V, VLOGIC = VREF = 5.5V, DATAA =CLOCK=SYNC=VIH DATAB=RATE = VIL Outputs = HI, unloaded	-800	-100	µA
		LOGIC INPUTS			
V_{IH}	Logic 1 Input Voltage	Functional Tests	2.0		V

Symbol	Parameters	Test Conditions (1,2)	Min.	Max.	Units
V_{IL}	Logic 0 Input Voltage	Functional Tests		0.5	V
I_{IH}	Logic 1 Input Current	V_{IN} = 2.0V, +Vs=+15V, -Vs=-15V, VLOGIC=VREF=4.5V		1	µA
I_{IL}	Logic 0 Input Current	V_{IN} = 0.5V, +Vs=+15V, -Vs=-15V, VLOGIC=VREF=5.5V	-645	-50	nA
C_I	Input Capacitance	(3)		15	pF
		A429 OUTPUTS			
V_{OH}	Output Voltage High	Outputs open, referenced to Ground, Vref =5.0V, Supplies = min to max	4.75	5.25	V
V_{OL}	Output Voltage Low	Outputs open, referenced to Ground, Vref =5.0V, Supplies = min to max	-5.25	-4.75	V
V_{NULL}	Output Voltage Null	Outputs open, referenced to Ground, Vref =5.0V, Supplies = min to max	-250	+250	mV
Rout	Output Resistance	Tc = 25ºC TC = -55ºC to +125ºC Rout = ΔVout/ΔIout Vout measured at 0mA & 10mA	33.7 33	41.2 44	Ohms
Trf-hi	HI rate rise/fall time	RATE = VIL, Ca/Cb = 68pf, Cload = 50pf 10 to 90% (4)	1.0	2.0	uS
Trf-lo	LO rate rise/fall time	RATE = VIH, Ca/Cb = 68pf, Cload = 50pf 10 to 90% (4)	5.0	15.0	uS
		CAPACITOR PINS			
I_{CL}	Low Rate Capacitor Current	Rate Sel = '1', CA (CB) = 2.5V, HL edge currents are negative	20	60	uA
I_{CH}	High Rate Capacitor Current	Rate Sel = '0', CA (CB) = 2.5V, HL edge currents are negative	138	277	uA
		SHORT CIRCUIT CONDITIONS			
I_{SC}	Output Short Circuit Current	A_{OUT} and/or B_{OUT} shorted line-to-line or to GND. Outputs HI or LOW.	100	156	mA
I_{SC+VS}	+V_S Short Circuit Current	A_{OUT} and/or B_{OUT} shorted line-to-line or to GND. Outputs HI or LOW.	100	165	mA
I_{SC-VS}	-V_S Short Circuit Current	A_{OUT} and/or B_{OUT} shorted line-to-line or to GND. Outputs HI or LOW.	100	165	mA

Notes:
1. Unless otherwise indicated, +VS = +15V, -VS = -15V, VREF = +5V, VLOGIC = +5V, Rate Select = 0V, RL = Open Circuit, CL = 0 pF, and -55°C < Tcase < +125°C.
2. Unless otherwise indicated, currents flowing into DUT are positive, currents flowing out of DUT are negative, and voltages are referenced to Ground.
3. Guaranteed by design. Not production tested
4. Sample tested.

Typical Power Dissipation Characteristics

(+VS = +15V, -VS = -15V, VREF = +5V, TA = + 25°C, CA = CB = 68pF)

Data Rate (Kbits/sec)	Load	Rate Select	Positive Supply Current	Negative Supply Current	VLOGIC Supply Current	Total Power Dissipation
0 –100	Open Circuit	Logic 1,0	5.7 mA	4.9 mA	214 µA	160 mW
12.5 – 14	Full Load(1)	Logic 1	19.6 mA	22.7 mA	200 µA	655 mW
100	Full Load(1)	Logic 0	39.1 mA	38.4 mA	200 µA	1165 mW

Note:
1. RL = 400Ω, CL = 0.03 µF (see Block Diagram).

Applications

Heat Sinking / Air Flow and Short Circuit Protection

The user application will determine if and how much heat sinking/air flow will be required for the DEI3182A. Consideration must be given to ambient temperature, load conditions and output voltage swing. In addition, power consumption increases with increased operating frequency. Use the numbers given in the Thermal Characteristics Table to determine that the maximum allowable junction temperature of 175°C is not exceeded.

Outputs Out A and Out B are short circuit protected by the internal 37.5Ω back termination resistors. During a short circuit of the output to either power supply or ground, the device must be able to dissipate the generated heat. For example, if the output is shorted to ground and +VS = +15V, the device must dissipate 15V x 0.165A = 2.5W. An appropriate heat sink is required in this situation. Note that the Amp A and Amp B outputs are not short circuit protected. Shorting these pins to either power supply or ground will cause failure of the device. An added external resistor will protect the circuit by limiting the current.

Power Supply Considerations

Three power supplies are required to operate the DEI3182A in a typical ARINC 429 bus application: +15V for +VS, -15V for -VS, and +5V for both VREF and VLOGIC. The differential output swing of the DEI3182A is equal to 2 x VREF. Using +5V gives a differential output swing of 10V. If a different output voltage swing is required, an additional power supply is needed to set VLOGIC. Each power supply pin should be decoupled to ground using a high quality 10 µF tantalum capacitor. This is especially true when driving a large capacitive or resistive loads. The decoupling capacitors should be located as close to the device pins as possible to eliminate the wiring inductance.

Typical ARINC 429 Application

Figure 1 shows typical switching waveform for the DEI3182A in any configuration. Figure 2 depicts connections for a ARINC 429 high speed bus driver application. This circuit shows the complete configuration for a 100 Kbits/sec, 10V differential output swing using the terminated output pins.

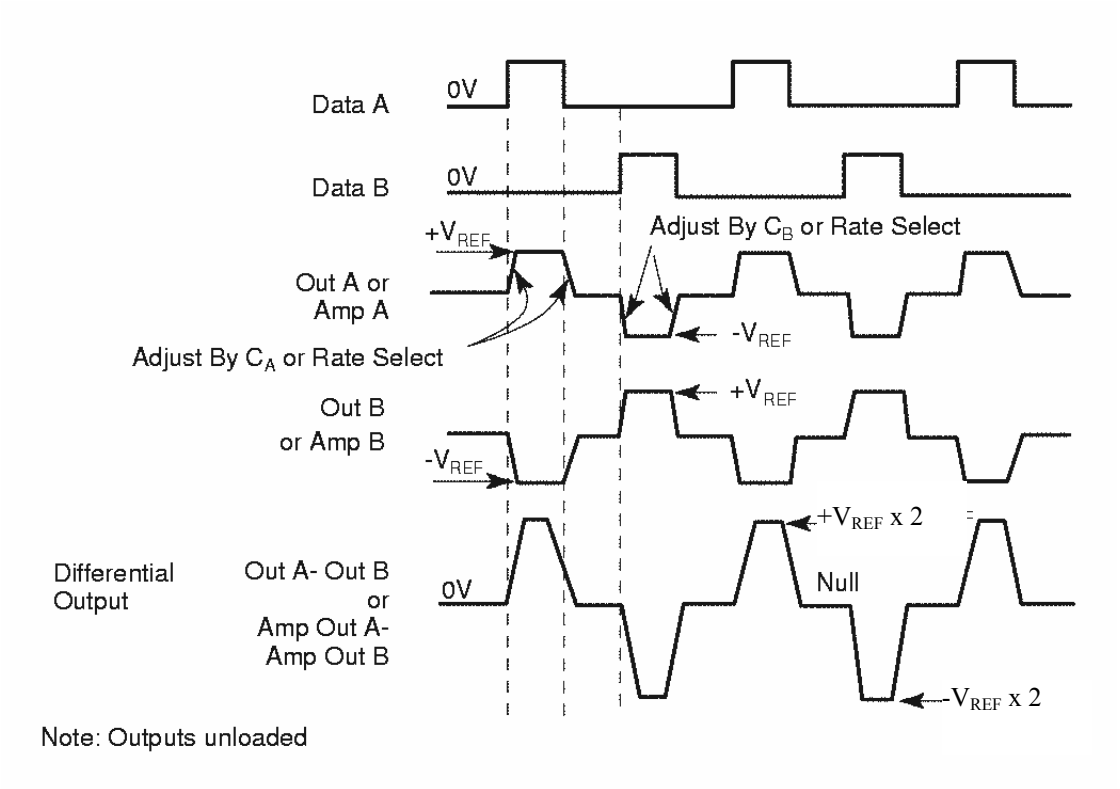


Figure 1. Switching Waveforms

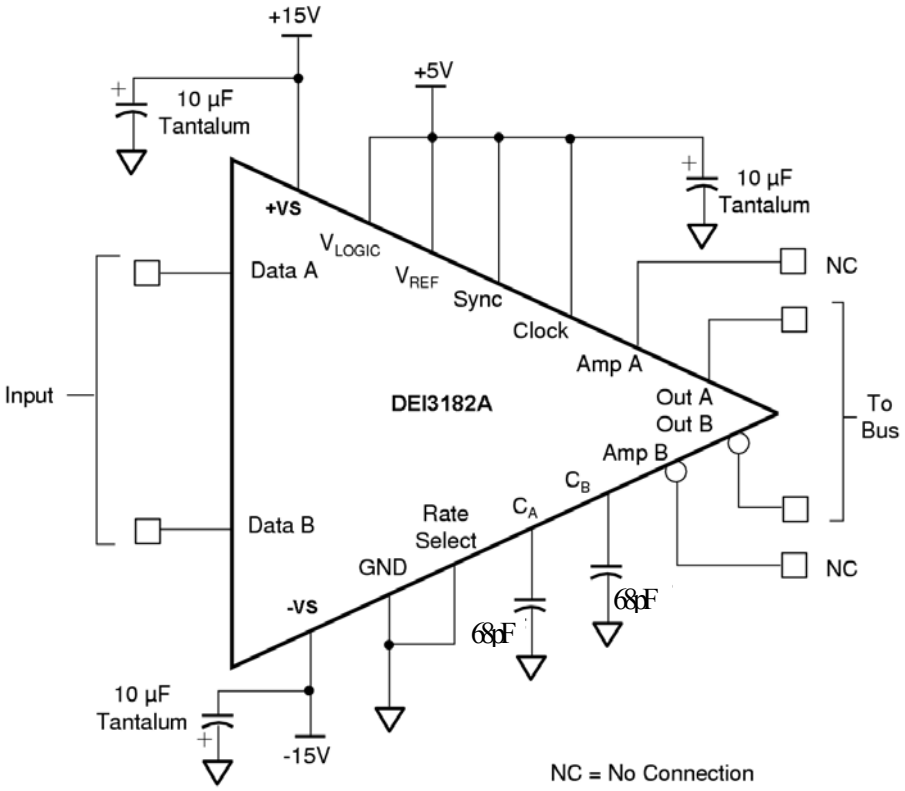
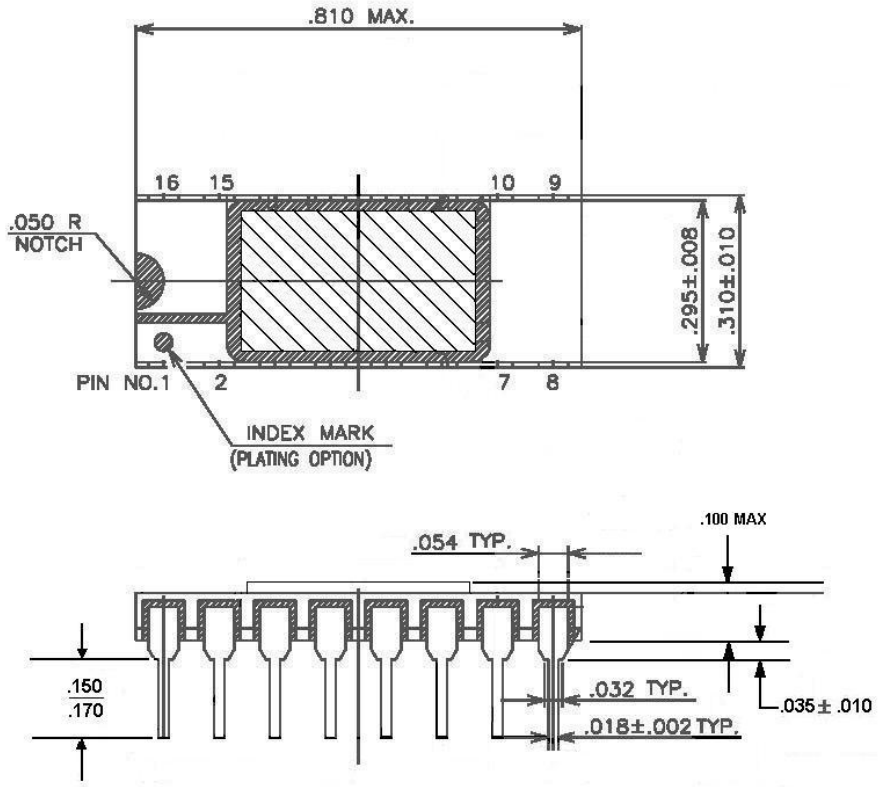


Figure 2. ARINC 429 Bus Driver Applications (100 kb/s Mode)

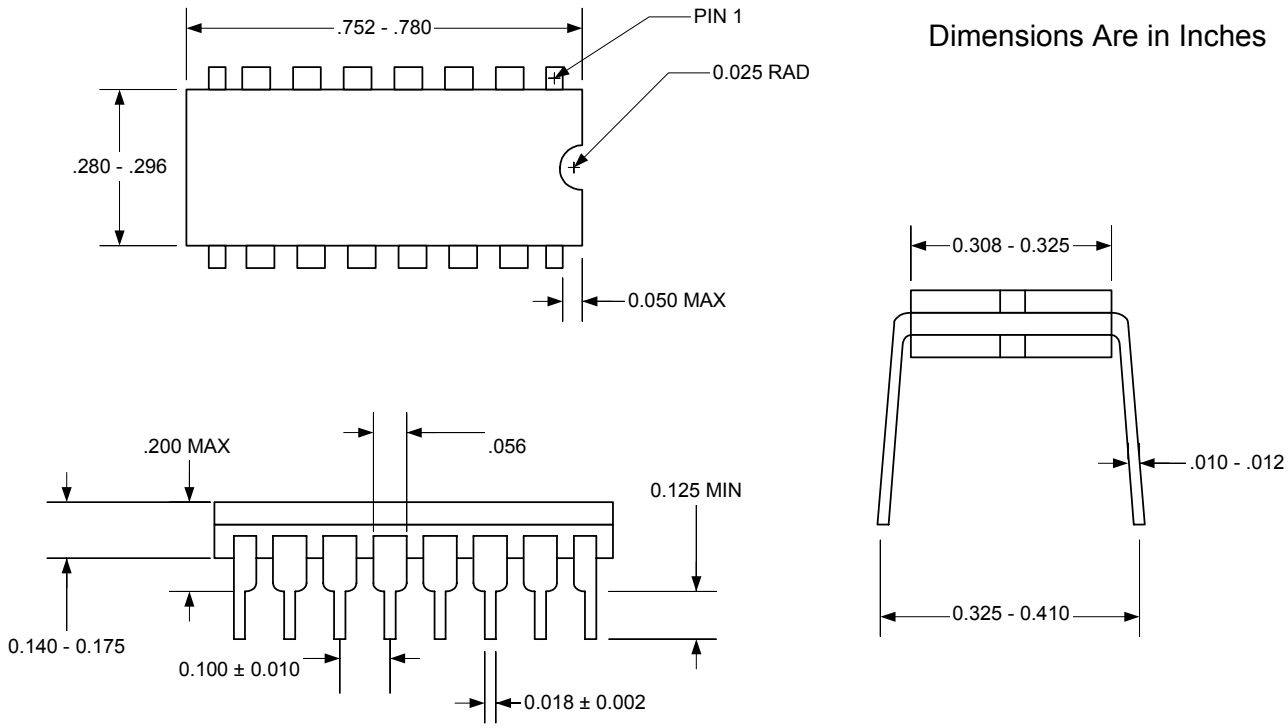
Mechanical Dimensions

16-Lead Side-Braze Ceramic DIP

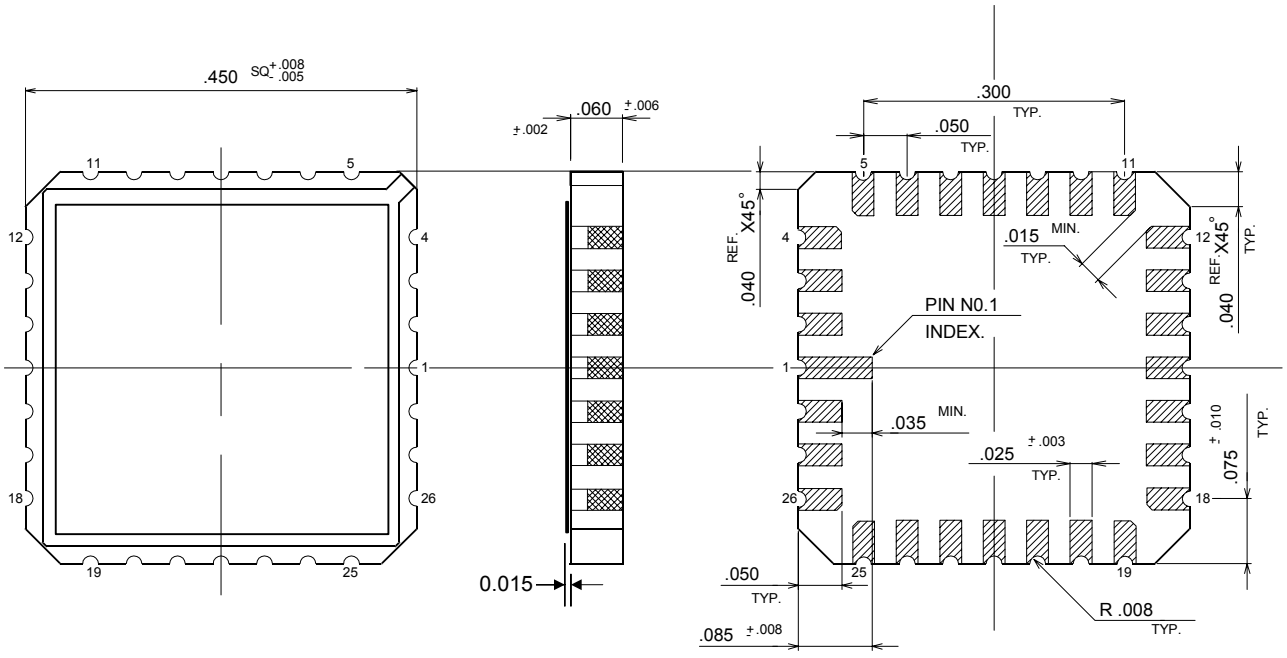


Lead Finish:
Au plated with Sn63/Pb37 solder dip covering the lead to the seating plane.

16-Lead CERDIP



28-Lead CLCC



Lead Finish:

Au plated with Sn63/Pb37 solder dip.

Process Flow

Process Step	Standard	Burn-In
THERMAL CYCLE MIL-STD-883B M1010.4 Condition B	10 Cycles	10 Cycles
CONSTANT ACCELERATION MIL-STD-883B M2001, Method D	YES	YES
GROSS & FINE LEAK MIL-STD-883B M1014.10	YES	YES
PRE-BURN-IN Electrical Test	NO	YES
BURN IN MIL-STD-883B M1015 Condition A	NO	160hrs @ +125 °C
FINAL ELECTRICAL TEST, Room Temperature	100%	100%
FINAL ELECTRICAL TEST, High Temperature	100% @ +125°C	100% @ +125°C
FINAL ELECTRICAL TEST, Low Temperature	0.65% AQL @ -55°C	0.65% AQL @ -55°C

Ordering Information

Part Number	Package	Operating Temperature Range	Burn In
DEI3182A-DMS	16-Lead Side-braze Ceramic DIP	-55°C to + 125°C	N
DEI3182A-DMB	16-Lead Side-braze Ceramic DIP	-55°C to + 125°C	Y
DEI3182A-CMS	16-Lead CERDIP	-55°C to + 125°C	N
DEI3182A-CMB	16-Lead CERDIP	-55°C to + 125°C	Y
DEI3182A-EMS	28 Lead Ceramic LCC	-55°C to + 125°C	N
DEI3182A-EMB	28 Lead Ceramic LCC	-55°C to + 125°C	Y

Note: The –CMB/-DMB/-EMB parts may be marked as –CMS /–DMS/-EMS with a “B” stamp to denote burn-in.