Device
Engineering
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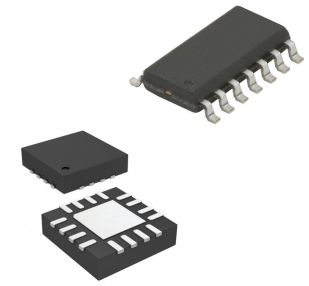
DEI5090 SINGLE-RAIL ARINC 429 LINE DRIVER

FEATURES



- Operates from single +3.3V power supply.
- Both +5V and -5V are generated on-chip.
- TTL/CMOS TO ARINC 429 Line Drivers.
- 5V/3.3V logic level compatible inputs with 4KV HBM ESD protection
- Rate control input set Hi (100KBS) or Lo (12.5KBS) speed slew rates.
- Drives full ARINC load.
- Output resistors: 5 Ohms or 37.5 Ohms.
- Operating temperature: industrial (-55 to +85°C) or extended (-55 to +125°C)
- Packages (RoHS):
  - 16L SOICN
  - 16L 4x4mm QFN

GENERAL DESCRIPTION

The DEI5090 line driver is a CMOS integrated circuit designed to directly drive the ARINC 429 avionics' serial digital data bus. The device converts TTL/CMOS serial input data to the tri-level RZ bipolar differential modulation format of the ARINC bus. A TTL/CMOS control input selects the output slew rate for HI (100KBS) and LOW (12.5KBS) speed operation. No external timing capacitors are required.

The part includes a dual polarity voltage doubler, allowing it to operate from a single +3.3V supply using only four external capacitors.

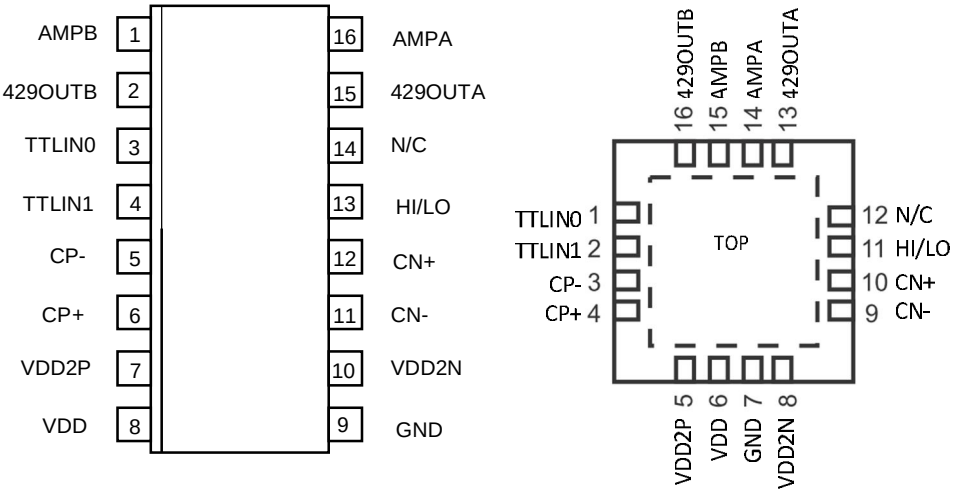


Figure 1 DEI5090 SOIC and QFN Pinout

Table 1 TERMINAL DESCRIPTIONS

NAME	FUNCTION	DESCRIPTION
AMPB	429 OUTPUT	5Ω ARINC 429 format serial digital data output B
429OUTB	429 OUTPUT	37.5Ω ARINC 429 format serial digital data output B
TTLIN0	LOGIC INPUT	Serial digital data input 0 (10 KΩ pull down resistor)
TTLIN1	LOGIC INPUT	Serial digital data input 1 (10 KΩ pull down resistor)
CP-	ANALOG OUTPUT	VDD2P flyback capacitor negative terminal
CP+	ANALOG OUTPUT	VDD2P flyback capacitor positive terminal
VDD2P	ANALOG OUTPUT	Voltage doubler positive output (+6.6V for +3.3V supply)
VDD	POWER INPUT	+3.3V
GND	POWER INPUT	Ground
VDD2N	ANALOG OUTPUT	Voltage inverter output (-6.6V for +3.3V supply)
CN-	ANALOG OUTPUT	VDD2N flyback capacitor negative terminal
CN+	ANALOG OUTPUT	VDD2N flyback capacitor positive terminal
HI/LO	LOGIC INPUT	Slew rate control. (10 KΩ pull down resistor)
N/C	No Connect	
429OUTA	429 OUTPUT	37.5Ω ARINC 429 format serial digital data output A
AMPA	429 OUTPUT	5Ω ARINC 429 format serial digital data output A

FUNCTIONAL DESCRIPTION

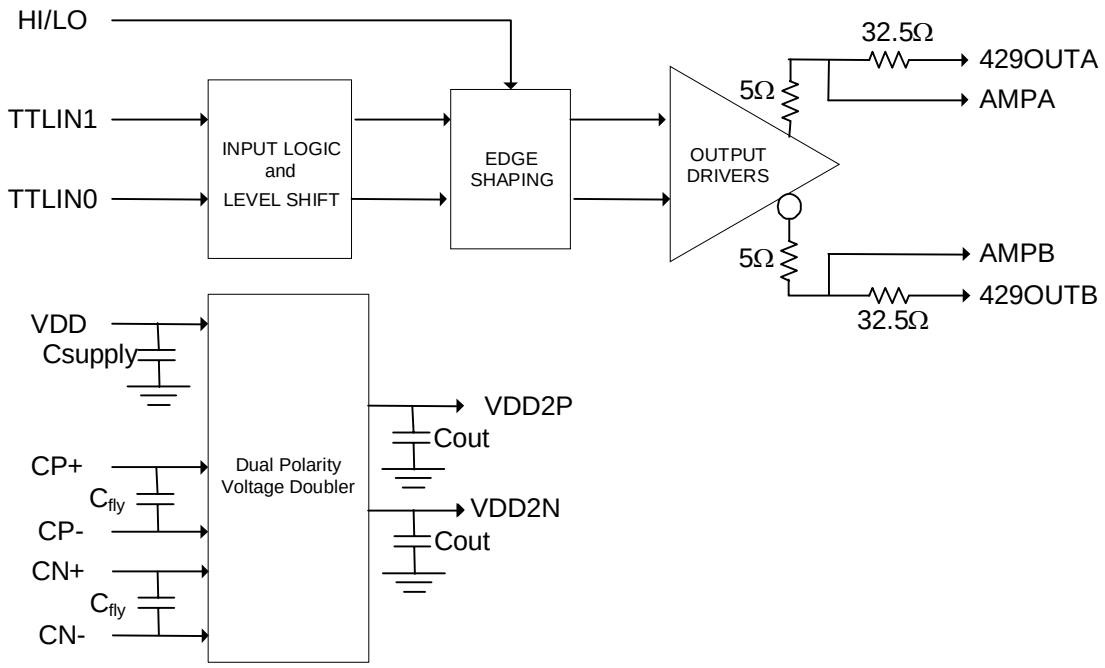


Figure 2 Block Diagram

Table 2 Speed Control Function

HI/LO	OUTPUT TRANSITION TIME
0	10us (12.5 KBS data)
1	1.5us (100KBS data)

Table 3 Transmit Data Function

TTLIN1	TTLIN0	429OUTA	429OUTB	NOTES
0	0	0V	0V	Null output
0	1	-5V	5V	Zero output
1	0	5V	-5V	One output
1	1	Hi-Z	Hi-Z	Hi-Z output

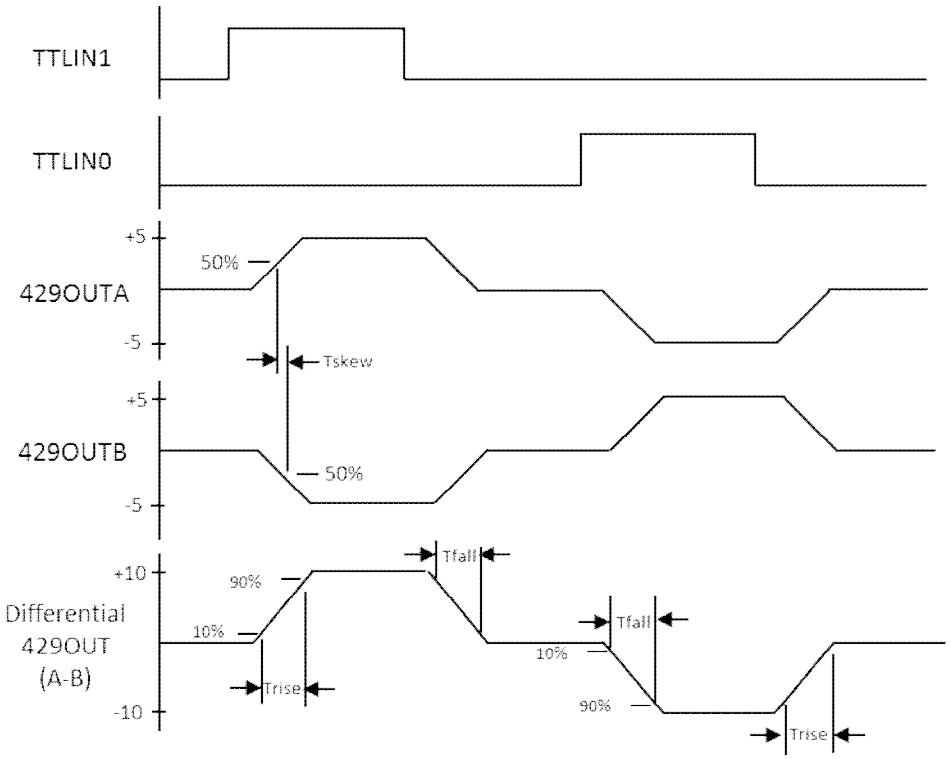


Figure 3 Timing Waveforms

ELECTRICAL DESCRIPTION

Table 4 Absolute Maximum Ratings

PARAMETER	MIN	MAX	UNITS
VDD Supply Voltage	-0.3	+5	V
Storage Temperature	-65	+150	°C
Input Voltage TTLIN and HI/LO Inputs 429OUT Outputs	 GND – 0.3 VDD2N – 0.3	 5V + 0.3 VDD2P + 0.3	 V V
Junction Temperature: Tjmax, Plastic Packages (Limited by molding compound Tg)		145	°C
ESD per JEDEC A114-A Human Body Model Logic Input Pins Other pins		4000 2000	V
Peak Body Temperature (Pb Free solder profile)		260	°C

Notes:
1. Stresses above absolute maximum ratings may cause permanent damage to the device.
2. The device is tolerant of one or both outputs shorted to Ground and of both outputs shorted together.
3. Voltages are referenced to Ground

Table 5 Recommended Operating Conditions

PARAMETER	SYMBOL	CONDITIONS
Supply Voltage	VDD	+3.13 to +3.46V
Operating Temperature -xEx variants -xMx variants	T_{OP}	 -55 to +85 °C -55 to +125 °C

Table 6 Electrical Characteristics

Conditions (Unless otherwise noted):
Temperature: -55°C to +85°C (-xEx) or -55°C to +125°C (-xMx) VDD = +3.13V to +3.46V

PARAMETER	TEST CONDITION	SYMBOL	MIN	NOM	MAX	UNITS
LOGIC INPUTS						
Input Voltage, Logic 1		V_{IH}	2.0			V
Input Voltage, Logic 0		V_{IL}			0.8	V
Input Current	VIN = 0.1V	I_{IL}	-20		20	uA
Input Current	VIN = 3.46V	I_{IH}	260	346	433	uA
ARINC OUTPUTS						
ARINC Output Voltage (Differential) One Null Zero	Differential Output Voltage = 429OUTA – 429OUTB. No Load.	 V_{DIF1} $V_{DIFnull}$ V_{DIF0}	 9.0 -0.5 -11.0	 10.0 0 -10.0	 11.0 +0.5 -9.0	 V V V
ARINC Output Voltage (Single Ended) Hi Null Lo	Referenced to Ground No Load.	 Vo_{HI} $Vo_{null,}$ Vo_{LO}	 4.5 -0.25 -5.5	 5.0 0 -5.0	 5.5 +0.25 -4.5	 V V V
Output Resistance: 429OUT pins AMP pins	Room Temperature	Rout		 37.5 5		 Ohms Ohms
ARINC Output Tri-State Current	TTLIN0= TTLIN1= VDD -5.75V < VOUT < 5.75V	Ihiz	-1.0		1.0	uA
Output Slew Rate Hi Speed	HI/LO = 1 No Load 10% to 90% voltage amplitude of differential output.	T_{rise} T_{fall}	1.0	1.5	2.0	us
Output Slew Rate Lo Speed	HI/LO = 0 No Load 10% to 90% voltage amplitude of differential output.	T_{rise} T_{fall}	5	10	15	us
Output skew time between A and B outputs.	HI/LO = 1 Measured at 50% voltage amplitude of both outputs.	T_{skew}			200	ns

Conditions (Unless otherwise noted):
Temperature: -55°C to +85°C (-xEx) or -55°C to +125°C (-xMx) VDD = +3.13V to +3.46V

PARAMETER	TEST CONDITION	SYMBOL	MIN	NOM	MAX	UNITS
SUPPLY CURRENT						
Quiescent Operating Supply Current:	VDD=3.3V HI/LO = 0 or 1 TTLIN0=TTLIN1= 0V No Load -xEx (85°C) -xMx (125°C)	I_{VDD}		45	 75 85	mA
VOLTAGE DOUBLER						
Start-up transient (VDD2P, VDD2N)	10% of VDD to 50% of VDD2P/N	T_{START}			10	ms
Operating Switching Frequency		F_{SW}		250		KHz
Worst case maximum voltage doubler output	VDD = 3.6V, T= -55C, Open load	$V_{DD2P(max)}$			6.92	V
Ratio of bulk storage to fly-back capacitors	C_{OUT}/C_{FLY}	C_{OUT} /C_{FLY}	2.2	10		-
Fly-back capacitor Capacitance ESR	 [0.5, 1.0]MHz	C_{FLY}	1.0	4.7	 500	 uF mΩ
Bulk storage capacitor Capacitance ESR	 [0.5, 1.0]MHz	C_{OUT}	2.2	47	 300	 uF mΩ
VDD By-pass capacitor		C_{SUPPLY}		68		uF

DESIGN CONSIDERATIONS

Power Supply and Voltage Doubler Capacitors

C_{SUPPLY} (see Figure 2): The VDD supply should be decoupled with a 68uF or larger tantalum or ceramic capacitor to source the voltage doubler ripple current, and a 0.1uF ceramic capacitor to provide high frequency filtering. The ripple current can be in the range of 100s of ma during peak loading.

C_{FLY}: The two fly-back capacitors transfer energy from the charge pump inverters to the rectifiers. 4.7uf 10V X7R low DF ceramic capacitors are recommended. They should be in close proximity to the IC to minimize power loss and noise due to routing impedance. It may be beneficial to include parallel 0.1uf caps to minimize high frequency impedance.

C_{OUT}: The two voltage doubler output capacitors filter the charge pump rectifier outputs. They should be at least 10x capacitance of the $C_{FLY.}$ 47uf 10V/16V X5R/X7R low DF ceramic capacitors are recommended. They should be in close proximity to the IC to minimize power loss and noise due to routing impedance. It may be beneficial to include parallel 0.1uf caps to minimize high frequency impedance.

Transient Voltage Protection

The DEI5090 Line Driver requires external components to achieve immunity from surges such as those defined by DO160 Section 22, “Lightning Induced Transient Susceptibility”. Typical surge protection includes silicon Transient Voltage Suppressor (TVS) devices and may include part of the 37.5 Ohms output resistance as external resistors to limit the surge current.

The DEI5090 has a robust output stage which includes large driver devices and clamp diodes to the VDD2P and VDD2N power rails as shown in figure 4. It withstands surge currents of ±0.5A for 175us without damage when powered with +3.3V supplies. At that surge current, the diodes clamp at ~1V above (below) the VDD2P (VDD2N) supply rail. ~350mA flows to the VDD2N (VDD2P) supply through the output amplifier, and ~150mA flows to the VDD2P (VDD2N) internal supply through the clamp diode. The outputs may be damaged by surges greater than 1A / 175us. At that current, the diode clamps at ~1.8V above (below) the supply.

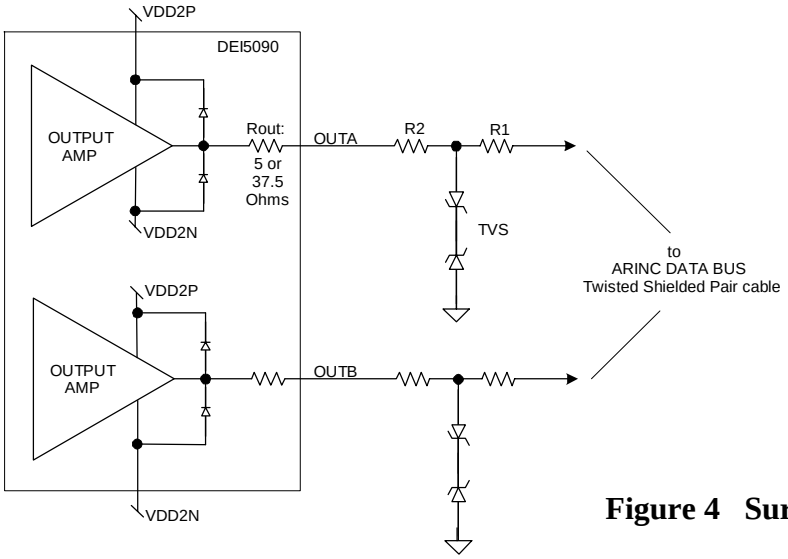


Figure 4 Surge Protection Network

The external lightning protection network should be designed to meet the specific requirements and constraints of the application equipment. The protection network should limit the OUTA/B pin surge current to the 0.5A / 175us maximum. The generalized circuit of figure 4 represents several TVS protection network options:

- The on-chip Rout value is 5 or 37.5 Ohms
- Select the total output resistance, Rout + R1 + R2 = 37.5 Ohms to meet ARINC bus requirements
  - Select R1 = 20Ω, R2 = 12.5Ω, Rout = 5Ω to use low TVS with surge current rating (small TVS devices)
  - Select R1 = 0Ω, Rout + R2 = 37.5Ω to use high TVS clamp voltage (20V + VDD2P/VDD2N)
  - If the VDD2P/VDD2N internal supplies are un-powered or below operating voltage during the surge event, large currents may flow through the internal clamp diodes and damage the driver. If the application requires lightning immunity while un-powered, Select R1 = 0Ω, Rout + R2 = 37.5Ω, and select the TVS clamp voltage for <20V.
- Select TVS devices for the following
  - TVS Surge power/current rating must withstand the application requirements for Lightning Induced Transient Levels and Waveforms. Microsemi Corporation publishes an application note specific to the DO160 lightning requirements (Micronote 126).
  - Select low capacitance TVS devices to minimize the load on the line driver. (Examples: Microsemi LC and HSMBJSA series TVS) This is a priority for Hi Speed ARINC applications where the low capacitance is important for optimum signal integrity and power consumption. Note that the maximum total capacitance on the ARINC bus is 30nF line to line.
  - Select the TVS clamp voltage at the lightning surge conditions such that the voltage/current into the DEI5090 OUT pin is within the safe region.
- If R1 is used to limit the TVS surge current, the resistor must withstand the surge current and voltage.

Some general considerations related to Lightning Immunity:

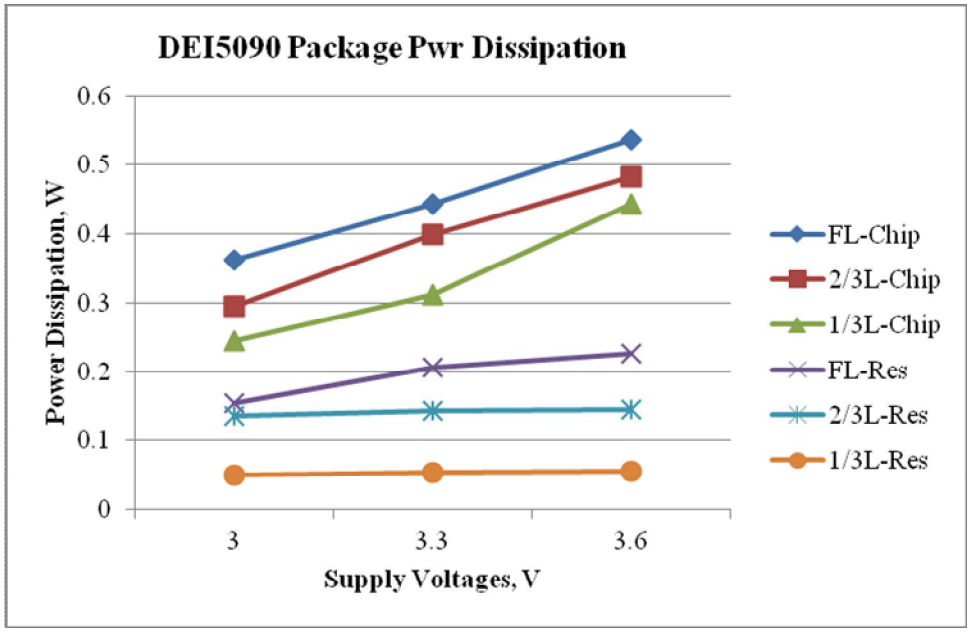
- Analyze the TVS high current signal and ground return path to insure adequate surge current capability. The IR voltage and L*di/dt voltage in the ground return will add additional stress beyond the TVS clamp voltage.
- Observe suitable PCB design rules for traces subject to high voltage and high current surges.
- When possible, locate TVS devices close to the equipment connector to minimize the length of the surge voltage/current traces within the equipment.
- The shields of ARINC 429 data bus cables should be terminated to aircraft ground at all ends and at all bulkhead disconnects.

Package Power Dissipation

Good thermal management is fundamental to Line Driver device reliability. It is particularly important in designs operating at the HI speed data rate (100KBS) with high capacitive loads as this produces maximum power dissipation. It is inappropriate to continuously operate the plastic package above 145°C. Like all microcircuits, long term reliability is improved with lower operating temperatures.

The Line Driver's operating Tj is determined by internal power dissipation, package thermal resistance, and ambient temperature. The typical chip and internal 32.5Ω resistor power dissipation (Pd) simulation results are shown in Figure 5 with following variables:

- Data Rate – The Hi Speed (100KBS) rate produces maximum power dissipation
- Load – Full ARINC 429 load is 30nF‖400 Ω line-to-line, 2/3 load is 20nF‖600 Ω line-to-line, and 1/3 load is 10nF‖1200 Ω line-to-line.
- Supply Voltages are 3.6V, 3.3V, and 3.0V at 25°C.
- Rout configuration – The power dissipated in the two 37.5Ω output resistors is internal to the IC.



Note:

1. 100% Data Duty Cycle.
2. Full Load: 400 Ω//30nF, Mid Load: 600 Ω//20nF, Light Load: 1200 Ω//10nF

Figure 5 DEI5090 Chip and Internal 32.5Ω Resistor Power Dissipation vs Load

PACKAGE DESCRIPTIONS

Table 7 Package Characteristics

PACKAGE TYPE	PACKAGE REF	THERMAL RESIST. θ_{JC} / θ_{JA} (ºC/W)	JEDEC MOISTURE SENSITIVITY LEVEL & PEAK BODY TEMP	LEAD FINISH MATERIAL / JEDEC Pb-Free CODE	Pb Free DESIGNATION
16L SOIC NB G	16 NB SOIC G	29 / 73	MSL 1 260ºC	NiPdAu e4	RoHS Compliant
16L QFN 4X4 G	16 QFN G	10 / (1)	MSL 3 260ºC	NiPdAu e4	RoHS Compliant

Notes:
1. θ_{JA} is optimum with the exposed pad soldered to a PCB land with thermal vias connected to an internal ground plane.

16 Lead SOIC NB G

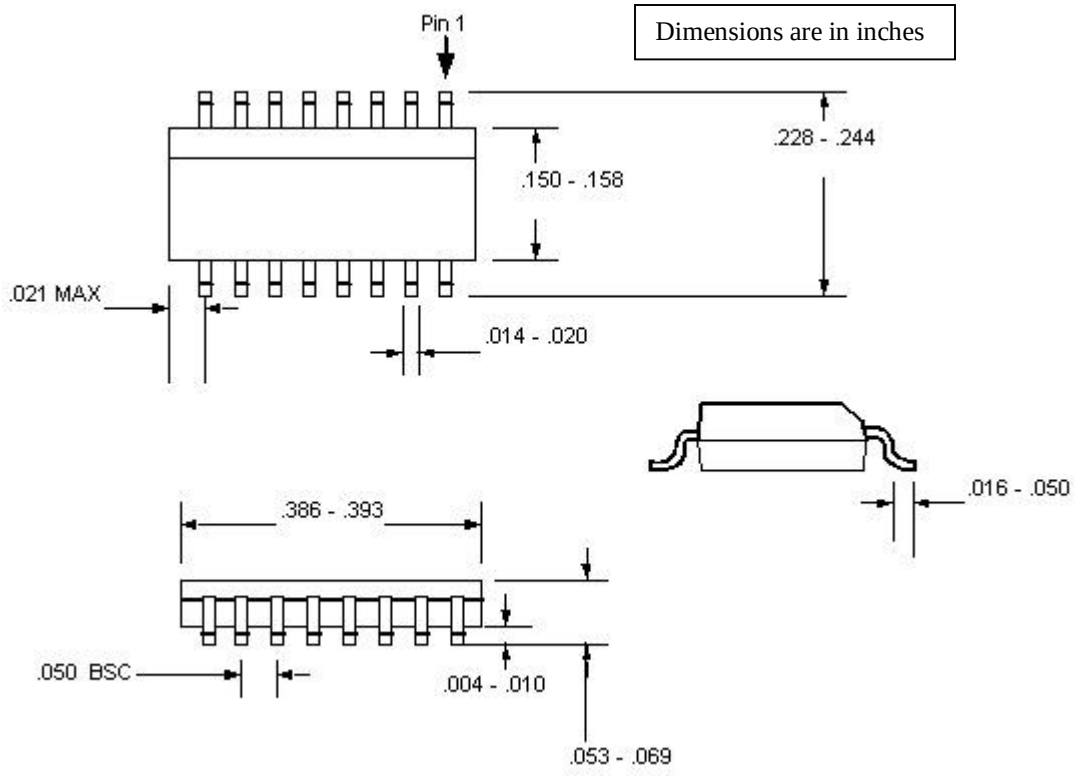


Figure 6 16L SOIC NB G Package Outline

16 Lead QFN 4.0 x 4.0

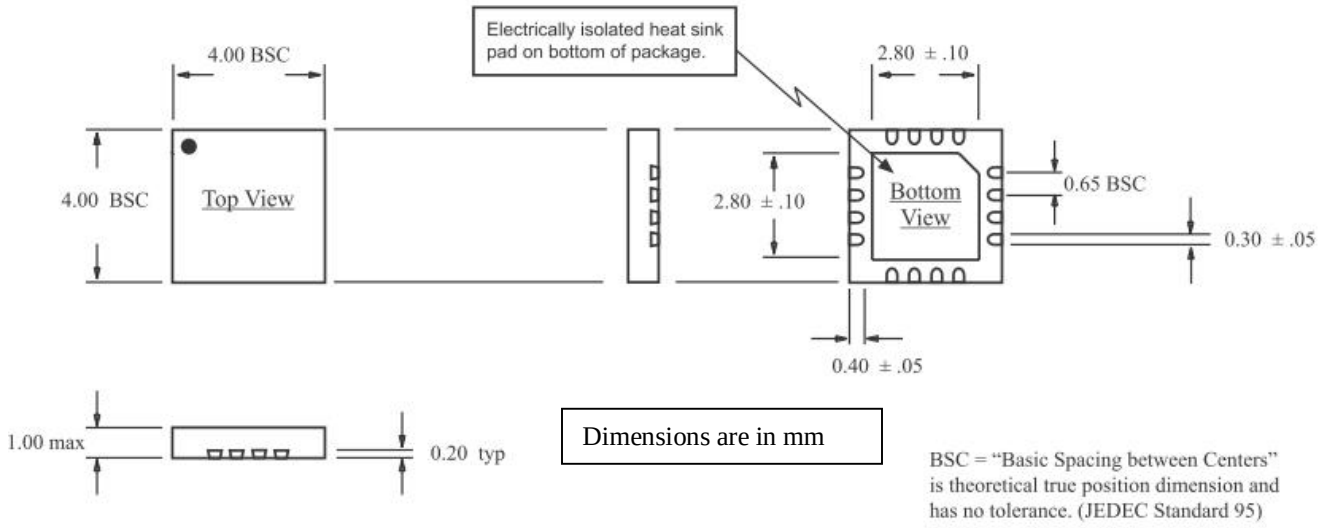


Figure 7 16L QFN 4x4 G Package Outline

ORDERING INFORMATION

Part Number	Marking	Package	Temperature
DEI5090-SES-G	DEI5090 /SES	16L SOIC NB G	-55 / +85 ºC
DEI5090-SMS-G	DEI5090 / SMS	16L SOIC NB G	-55 / +125 ºC
DEI5090-MES-G	DEI5090 / MES	16L 4X4 QFN G	-55 / +85 ºC
DEI5090-MMS-G	DEI5090 / MMS	16L 4X4 QFN G	-55 / +125 ºC