Device
Engineering
Incorporated

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DEI1041
ARINC 429 LINE RECEIVER

FEATURES

- ARINC 429 to TTL/CMOS logic line receiver
- Drop-in replacement for HI-8588 and HI-8588-10
- Operates from single 5 V ±10% or 3.3 V ±10% power supply
- ARINC inputs internally protected to lightning requirements of DO-160 Level 3 pin injection
- ARINC inputs withstand inadvertent short to 115 Vac on inputs
- Operates in high noise environment
  - Input Common Voltage Range: ± 20 V
  - 2 V minimum Input hysteresis
- Logic level TEST inputs bypass analog inputs.
- High input resistance allows use of external series resistors to support:
  - Lightning protection beyond Level 3
  - Fault isolation
- Package: 8L SOIC

TERMINAL DESCRIPTION

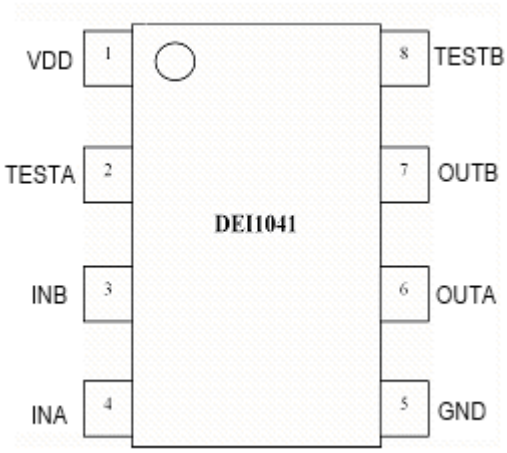


Table 1 Terminal Description

PIN	NAME	DESCRIPTION
4	INA	429 INPUT. ARINC 429 format serial digital data “A” input
3	INB	429 INPUT. ARINC 429 format serial digital data “B” input
2	TESTA	LOGIC INPUT. Test input A
8	TESTB	LOGIC INPUT. Test input B
6	OUTA	LOGIC OUTPUT. CMOS/TTL format serial digital data “A” output
7	OUTB	LOGIC OUTPUT. CMOS/TTL format serial digital data “B” output
1	VDD	POWER INPUT. 5 V OR 3.3V
5	GND	POWER INPUT. Ground

FUNCTIONAL DESCRIPTION

The DEI1041 is a BiCMOS device which contains one ARINC 429 differential line receiver. It translates incoming ARINC 429 data bus signals (tri-level RZ bipolar differential modulation) to a pair of TTL/CMOS logic outputs. It meets the requirements of the ARINC 429 Digital Information Transfer Standard. Refer to Figure 1 "DEI1041 Block Diagram and Truth Table".

The device is designed to operate in a high noise environment. Inputs are accepted over a ±20 V common mode voltage range and the receivers provide over 2 V of hysteresis. Circuit speed is optimized to reject high frequency transients.

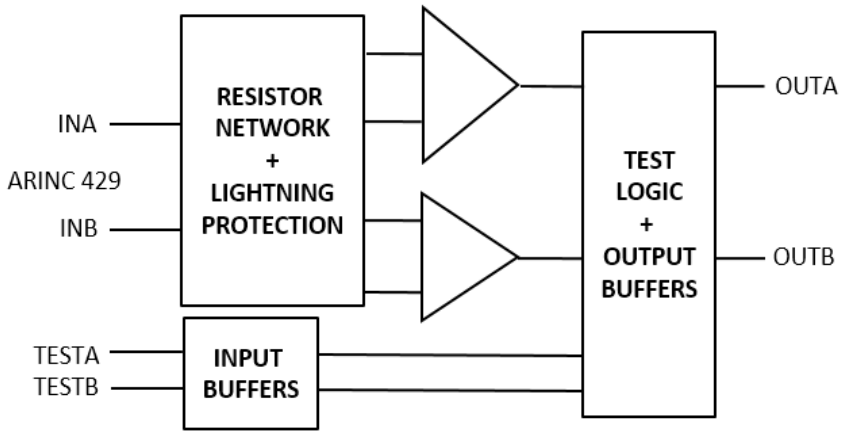
All ARINC input pins are designed with internal protection from damage due to transients meeting the lightning induced transient requirements of DO-160 Level 3 pin injection. The ARINC inputs may optionally be connected to ARINC bus through external 10 kΩ series resistors. These resistors may be added in combination with transient voltage suppressors to achieve lighting protection beyond the Level A3 limits due to high input impedance.

The ARINC input pins are designed with internal protection from damage due to lighting induced transients of DO-160 Level 3 pin injection. The protection incorporates on-chip high value resistors to minimize IR heating and high-voltage dielectric isolation to withstand the voltage transients.

Higher protection levels can be achieved with the addition of external TVS devices between the inputs and ground, or alternately, TVS devices in combination with series current limiting resistors between the ARINC bus and the IC/TVS node. The series resistors reduce the power requirement and size of the TVS. Resistor values up to 10 kΩ are feasible.

The ARINC inputs withstand inadvertent short to 115 Vac aircraft power without sustaining damage.

The DEI1041 provides logic level TEST inputs for built in system test. They force the receiver outputs to the specified ZERO, ONE or NULL state. The ARINC inputs are ignored when the device is in test mode.



TEST INPUTS		ARINC INPUTS	OUTPUTS	
TESTA	TESTB	INA-INB	OUTA	OUTB
0	0	≥ 6.5	1	0
0	0	≤ -6.5	0	1
0	0	-2.5 to 2.5	0	0
0	1	X	0	1
1	0	X	1	0
1	1	X	0	0

Figure 1 DEI1041 Block Diagram and Truth Table

Table 2 Recommended Operating Conditions

PARAMETER	SYMBOL	CONDITIONS
Supply Voltage	VDD	5 V ±10% 3.3 V ±10%
Logic Input Levels	TESTA,B	0 to VDD
Operating Temperature -SES -SMS	Ta	 -55 to 85 °C -55 to 125 °C

Table 3 Absolute Maximum Rating

PARAMETER	MIN	MAX	UNIT
Supply Voltage (with respect to GND)	-0.3	7.0	V
Input Voltage, continuous (ARINC Inputs)	-40	40	V
Logic Input and Outputs	–0.3	VDD + 0.3	V
Lightning Protection (ARINC 429 Channel Inputs) Waveform 3 (2) Waveform 4, 5A (2) (3)	 -600 -300	 600 300	V
Power Dissipation @ 85 °C		500	mW
ESD per JEDEC JS-001 Human Body Model (HBM)		1C	Class
Storage Temperature	-65	150	˚C
Junction Temperature, Tjmax		145	˚C
Peak Body Temperature		260	˚C

Notes:
1. Stresses above these limits can cause permanent damage.
2. Per DO160, Sect 22 Level 3 pin injection. See Figures 4-6.
3. Inputs can be protected to withstand higher stress by adding series resistors and shunt TVS on inputs. Inputs withstand 1500 V Waveform 5A when clipped ≤ 600 V.

Table 4 Electrical Characteristics

Conditions: Temperature: -55 °C to 85 °C (SES), 55 °C to 125 °C (SMS) VDD = 5 V ±10% or 3.3 V ±10%						
PARAMETER	TEST CONDITION	SYMBOL	MIN	NOM	MAX	UNIT
ARINC INPUTS						
ARINC ONE Input Voltage	V(INA – INB) For OUTA = 1, OUTB = 0	V_{ONE}	6.5	10	13	V
ARINC NULL Input Voltage	V(INA – INB) For OUTA = OUTB = 0	V_{NULL}	-2.5	0	2.5	V
ARINC ZERO Input Voltage	V(INA – INB) For OUTA = 0, OUTB = 1	V_{ZERO}	-6.5	-10	-13	V
Input Hysteresis		V_{HY}	2			V
Input Common Mode Voltage Range	ONE, NULL, ZERO	V_{CM}	-20		20	V
Input Resistance INA to INB	VDD open, shorted to GND or 5 V (1)	R_{IN}	280	780		kΩ
Input Resistance INA or INB to GND	VDD open, shorted to GND or 5 V	R_S	140	390		kΩ
Input Capacitance INA to INB	VDD open, shorted to GND or 5 V (1)	C_{IN}			10	pF
Input Capacitance INA or INB to GND	VDD open, shorted to GND or 5 V (1)	C_S			10	pF
TEST INPUTS						
Logic 0 Voltage		V_{IL}			0.8	V
Logic 1 Voltage		V_{IH}	2.0			V
Logic 0 Current	V_{IL} = 0.8 V	I_{IL}			20	µA
Logic 1 Current	V_{IH} = 2.0 V	I_{IH}			25	µA
LOGIC OUTPUTS						
OUTPUT HIGH VOLTAGE TTL	I_{OH} = -5 mA (VDD = 5.0 V) I_{OH} = -5 mA (VDD = 3.3 V) TTL Compatible	V_{OH}	2.4			V
OUTPUT LOW VOLTAGE TTL	I_{OL} = 5 mA (VDD = 5.0 V)	V_{OL}			0.4	V

Conditions: Temperature: -55 °C to 85 °C (SES), 55 °C to 125 °C (SMS) VDD = 5 V ±10% or 3.3 V ±10%						
PARAMETER	TEST CONDITION	SYMBOL	MIN	NOM	MAX	UNIT
OUTPUT HIGH VOLTAGE CMOS	I_{OH} = 100 µA CMOS Compatible	V_{OH}	VDD – .05			V
OUTPUT LOW VOLTAGE CMOS	I_{OL} = 100 µA CMOS Compatible	V_{OL}			.05	V
SUPPLY CURRENT						
V_{DD} Current	Data Rate = 0 MHZ INA/B = open, OUTA/B = open, VDD = 5.5 V or 3.63 V	I_{DD}		0.4	5	mA

Notes:
1. Guaranteed by design, not production tested.
2. Current flowing into device is positive. Current flowing out of device is negative. All voltages are with respect to GND unless otherwise noted.

Table 5 Switching Characteristics

PARAMETER	TEST CONDITION (1)	SYMBOL	MAX	MAX	UNIT
			VDD 3.3 V	VDD 5 V	
INA/B to OUT A/B Prop Delay	TESTA = TESTB = 0 C_L = 50 pF	t_{LH}	1000	900	ns
INA/B to OUT A/B Prop Delay	TESTA = TESTB = 0 C_L = 50 pF	t_{HL}	1000	900	ns
Matching of t_{LH} and t_{HL}		Dtp	500	500	ns
OUTA/B rise time	10% to 90%, C_L = 50 pF	t_r	50	25	ns
OUTA/B fall time	10% to 90%, C_L = 50 pF	t_f	50	25	ns
TESTA/B to OUTA/B Prop delay	C_L = 50 pF	t_{TOH}	100	60	ns
TESTA/B to OUTA/B Prop delay	C_L = 50 pF	t_{TOL}	100	60	ns

Notes:
1. Sample tested.

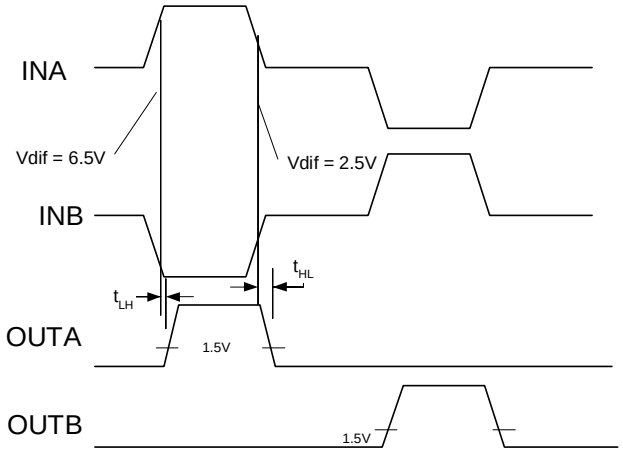


Figure 2 ARINC 429 Input to Logic Output Switching Waveform

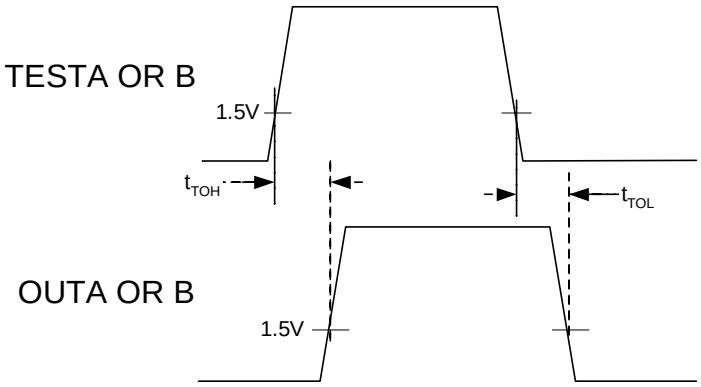


Figure 3 TEST Input to Logic Output Switching Waveform

LIGHTNING TRANSIENT NOTES:

1. Voc = Peak Open Circuit Voltage available at the calibration point.
2. Isc = Peak Short Circuit Current available at the calibration point.
3. Amplitude tolerances: +10%, -0%.
4. The ratio of Voc to Isc is the generator source impedance to be used for generating the waveforms.

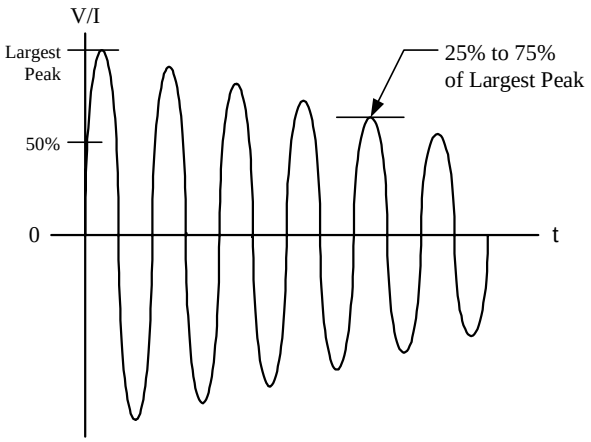


Figure 4 DO160 Lightning Induced Transient Voltage Waveform #3.
Voc = 600 V, Isc = 24 A, Frequency =1 MHZ ±20%

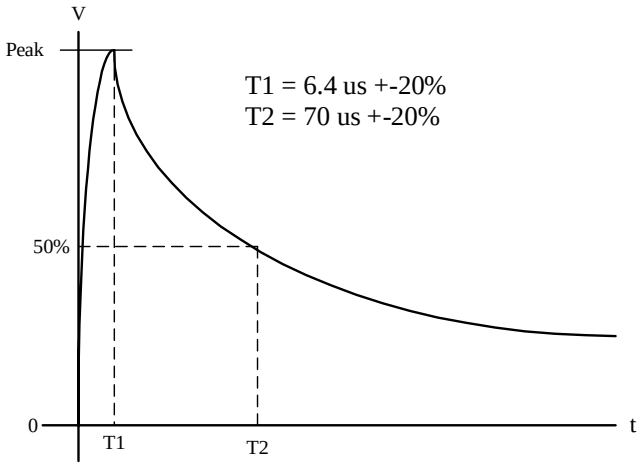


Figure 5 DO160 Lightning Induced Transient Voltage Waveform #4.
Voc = 300 V, Isc = 60 A

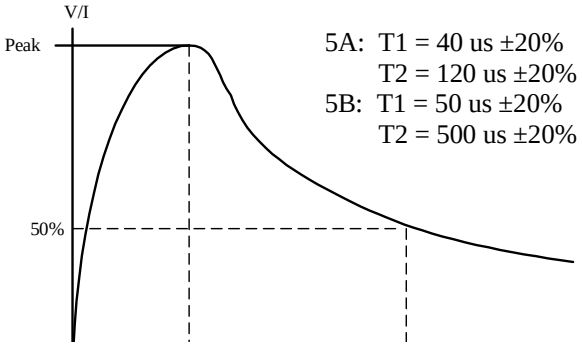


Figure 6 DO160 Lightning Induced Transient Voltage Waveform #5.
Voc = 300 V, Isc = 300 A

PACKAGE DESCRIPTION

Table 6 Package Characteristics

CHARACTERISTIC	VALUE
REFERENCE	8L NB SOIC G
Θ_{JA} (4 layer PCB with Power Planes)	55 °C/W
Θ_{JC}	24 °C/W
JEDEC MOISTURE SENSITIVITY LEVEL	MSL 1 / 260 °C
LEAD FINISH MATERIAL / JEDEC Pb-free CODE	NiPdAu e4
Pb-Free DESIGNATION	RoHS Compliant
JEDEC REFERENCE	MS-012-AC

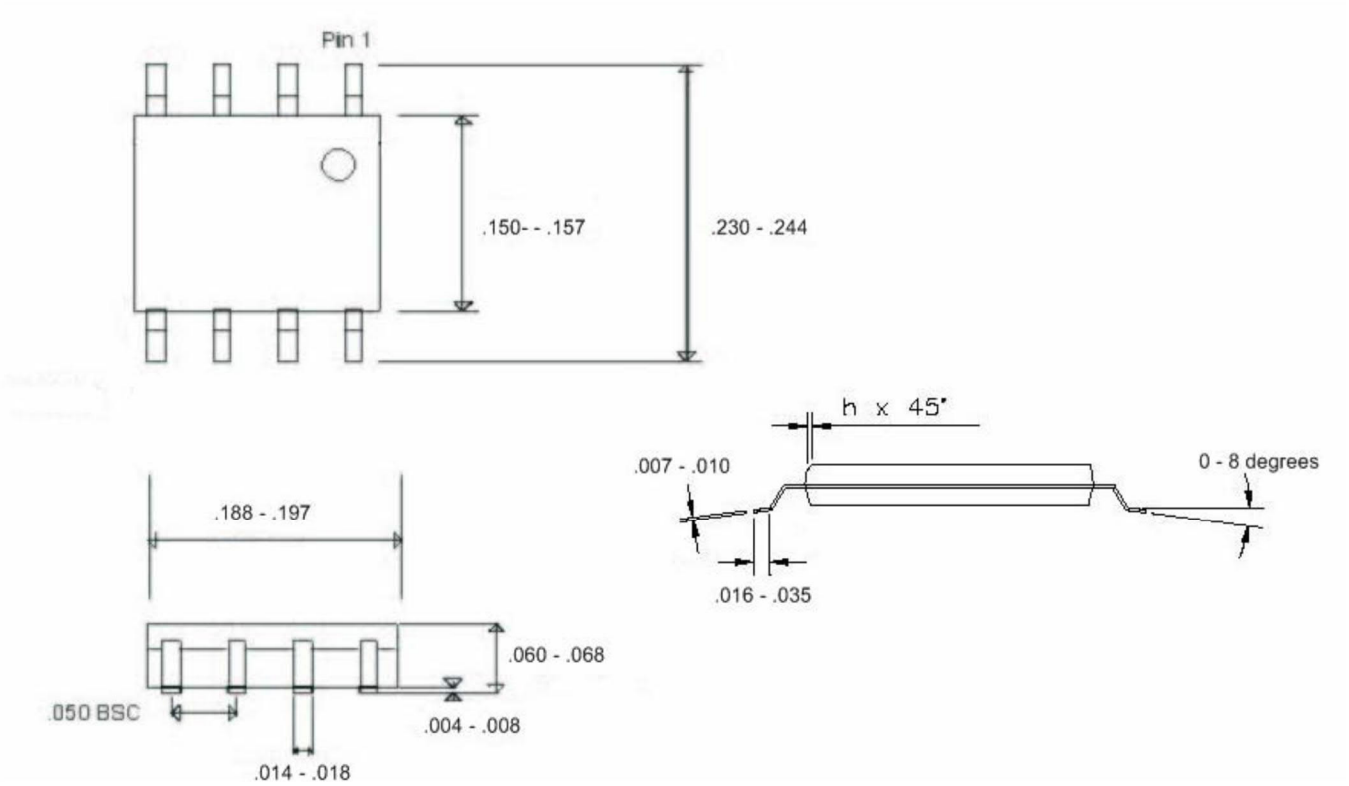


Figure 7 Mechanical Outline, 8L NB SOIC G

PROCESS FLOW

Table 7 Process Flow

PROCESS STEP	PLASTIC STANDARD	PLASTIC BURN-IN
PRE-BURN-IN Electrical Test	N/A	YES
BURN IN (1)	N/A	96 h @ 125 °C
FINAL ELECTRICAL TEST, Room Temperature	100%	100%
FINAL ELECTRICAL TEST, High Temperature	100% @ 85 or 125 °C	100% @ 85 or 125 °C
FINAL ELECTRICAL TEST, Low Temperature	0.65% AQL @ -55 °C	0.65% AQL @ -55 °C

NOTES:
1. Burn-in conditions: 125 °C, 96 h, VDD = 5.0 V, Inputs = 0 V, Outputs open.

ORDERING INFORMATION

Table 8 Ordering Information

DEI PN	PART MARKING (1)	TEMPERATURE RANGE	BURN-IN	PACKAGE TYPE
DEI1041-SES-G	DEI1041 YYWWE4 SES	-55/+85 °C	NO	8L NB SOIC G
DEI1041-SMS-G	DEI1041 YYWWE4 SMS	-55/+125 °C	NO	8L NB SOIC G
DEI1041-SMB-G	DEI1041 YYWWE4 SMB	-55/+125 °C	YES	8L NB SOIC G

NOTES:
1. Lot code marked on bottom. (e4) after Date Code denotes Pb Free category.