Device
Engineering
Incorporated

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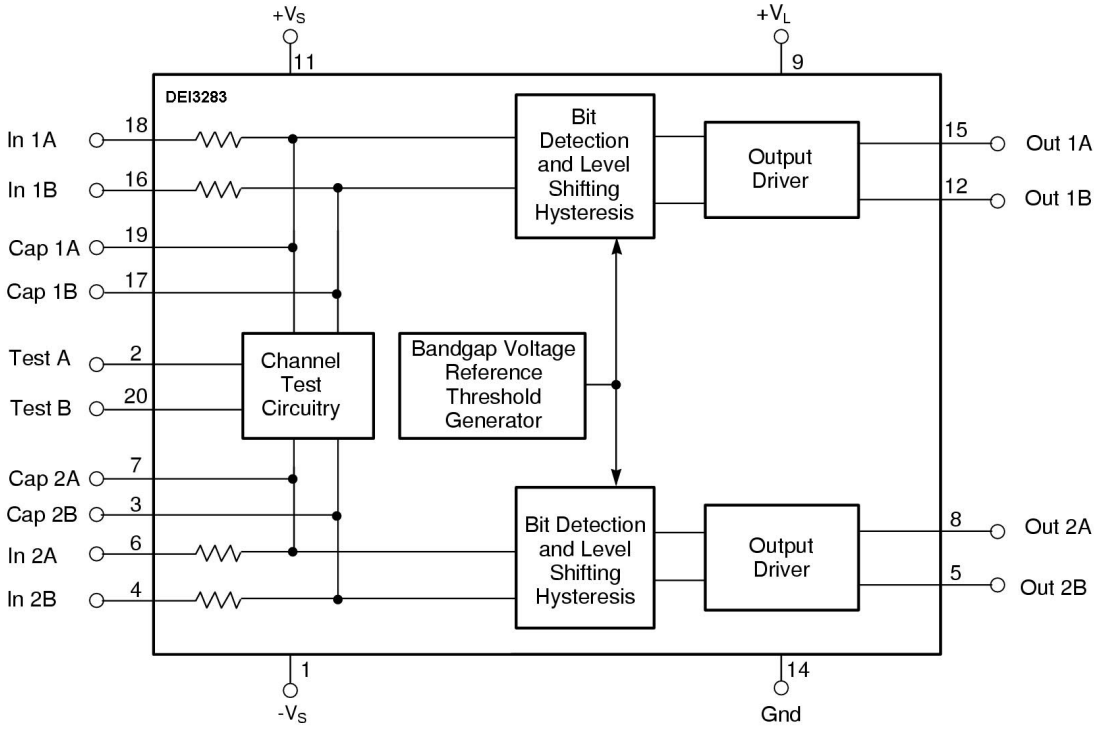
DEI3283
DUAL ARINC 429 LINE RECEIVER

FEATURES

- Two separate analog receiver channels
- Converts ARINC 429 levels to serial data
- ARINC 429 inputs withstand +/-200 V
- TTL inputs to test complete analog/digital RX function
- TTL and CMOS compatible outputs
- Low power dissipation
- Internal band gap voltage reference
- MIL-STD-883B burn-in screening available
- Package Options: 20 Lead ceramic DIP, 20 Terminal ceramic LCC, and 20 Lead SOIC
- Direct replacement for Fairchild/Raytheon RM3283 and RM3183 and Holt HI-8482

FUNCTION DIAGRAM



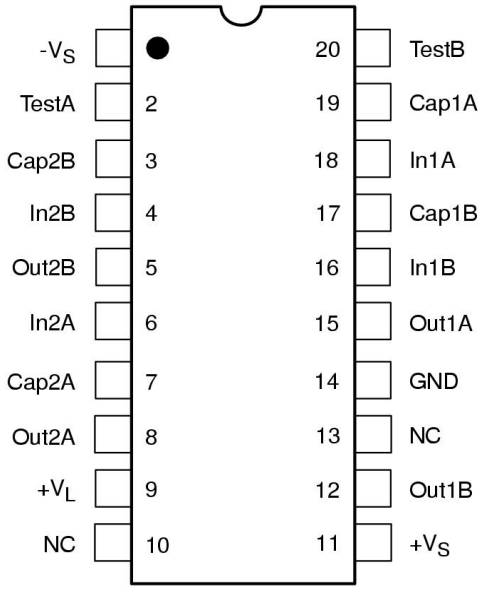
GENERAL DESCRIPTION

The DEI3283 consists of two analog ARINC 429 receivers which take differentially encoded ARINC level data and convert it to serial TTL level data. The DEI3283 provides two complete analog ARINC receivers with no external components required. Input level shifting thin film resistors and bipolar technology allow ARINC input voltage transients up to ±200 V without damage to the DEI3283. Each channel is identical, featuring symmetrical propagation delays for better high-speed performance. Input common mode rejection is excellent and threshold voltage is stable, independent of supply voltage. Data outputs are TTL and CMOS compatible. Two TTL compatible test inputs used to test the ARINC channels are available. They can be used to override the ARINC input data and set the channel outputs to a known state.

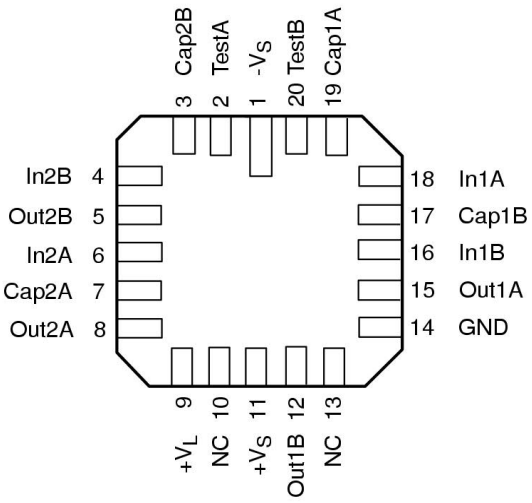
The DEI ARINC line driver family IC's are companion chips to the DEI3283 line receiver. Together they provide the analog functions needed for the ARINC 429 interface.

PIN ASSIGNMENTS

DIP and SOIC
Top View



LCC
Top View



PIN	NAME	DESCRIPTION
1	-Vs	Supply Voltage (-15 V)
2	TEST A	Logic Input, see functional characteristics.
3	CAP2B	A429 INPUT, Ch 2, B Capacitor node
4	IN2B	A429 INPUT, Ch 2, B input
5	OUT2B	Logic Output, Ch 2, B's output
6	IN2A	A429 INPUT, Ch 2, A input
7	CAP2A	A429 INPUT, Ch 2, A Capacitor node
8	OUT2A	Logic Output, Ch 2, A's output

PIN	NAME	DESCRIPTION
9	+VL	Supply Voltage (+5 V)
10	NC	
11	+VS	Supply Voltage (+15 V)
12	OUT1B	Logic Output, Ch 1, B's output
13	NC	
14	GND	Supply Return
15	OUT1A	Logic Output, Ch 1, A's output
16	IN1B	A429 INPUT, Ch 1, B input
17	CAP1B	A429 INPUT, Ch 1, B Capacitor node
18	IN1A	A429 INPUT, Ch 1, A input
19	CAP1A	A429 INPUT, Ch 1, A Capacitor node
20	TESTB	Logic Input, see functional characteristics.

FUNCTIONAL DESCRIPTION

The DEI3283 contains two discrete ARINC 429 receiver channels. Each channel contains three main sections: an input signal conditioning network, a window comparator, and a logic output buffer stage. A test function is common to both channels

The input network comprises resistors and current switching circuits. It conditions the ARINC inputs with over-voltage protection, test signal injection, and biasing suitable for the comparators. The network provides excellent input common mode rejection.

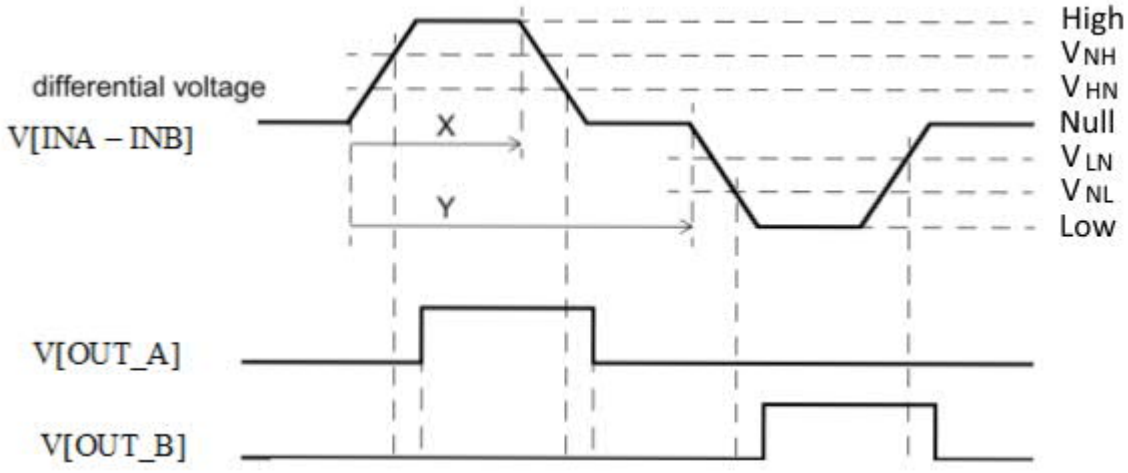
The window comparators detect ARINC pulse transitions in the signals from the input network. An ARINC input "High" state results in a logic 1 on OUT_A, and an ARINC input "Low" state results in a logic 1 on OUT_B. An ARINC input "Null" state forces both outputs to logic 0. Threshold and hysteresis voltages are generated by a band gap voltage reference to maintain stable switching characteristics over temperature and power supply variations.

The logic output buffer stage generates TTL/CMOS compatible logic outputs.

For built-in test capability, the TESTA/B inputs are provided to force the outputs to a predetermined state regardless of the ARINC input state. The test stimulus exercises the window comparators and logic output buffers; the ARINC input signals are not affected. If the test inputs are not used, they should be grounded.

FUNCTIONAL CHARACTERISTICS

ARINC INPUTS V(A) – V(B)	TEST INPUTS		OUTPUTS		OUTPUT STATE
	TEST A	TEST B	OUT_A	OUT_B	
Null	0	0	0	0	Null
Low	0	0	0	1	Low
High	0	0	1	0	High
X	0	1	0	1	Low
X	1	0	1	0	High
X	1	1	0	0	Null



PARAMETER	ARINC 429 CHARACTERISTICS (100KBS)		
	MIN	MAX	UNIT
Time Y	9.75	10.25	us
Time X	4.87	5.13	us
Pulse rise time	0.5	2	us
Pulse fall time	0.5	2	us
VHigh	+7.25	11	V diff
VNH		+6.5	V diff
VHN	+2.5		V diff
VNull	-0.5	+0.5	V diff
VLN		-2.5	V diff
VNL	-6.5		V diff
VLow	-11	-7.25	V diff

ABSOLUTE MAXIMUM RATINGS

PARAMETER		MIN	MAX	UNIT
Supply Voltage:	+VS to -VS		+36	V
	+VS to GND		+20	V
	-Vs to GND	-20		V
+VL Voltage			+7	V
Logic Input Voltage		-0.3	+VL + 0.3	V
ARINC 429 Input Voltage		-200	+200	V
Temperature Range	Storage	-65	+150	°C
	Operating	-55	+125	°C
Junction Temperature	Ceramic	-55	+175	°C
	Plastic	-55	+145	
Lead Soldering Temperature (60 s)	DIP, LCC		+300	°C
Peak Body Temperature, J-STD-020	SOIC		+260	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER		MIN	MAX	UNIT
+Vs	Positive Supply Voltage		13.5	16.5	V
-Vs	Negative Supply Voltage		-16.5	-13.5	V
+VL	+VL Supply Voltage		4.5	5.5	V
Top	Case Temperature:	-xMx	-55	+125	°C
		-xAx	-40	+125	°C
		-xEx	-55	+85	°C

ELECTRICAL CHARACTERISTICS

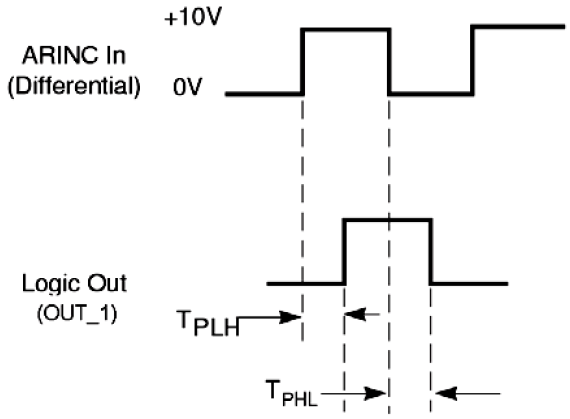
SYMBOL	PARAMETER	CONDITIONS (1,2)	MIN	MAX	UNIT
		POWER SUPPLIES			
ICC	+VS (+15 V) Supply Current	Supply = +/- 16.5 V, VI = 5.0 V, Test Inputs = 0 V Test Inputs = 5 V	 3.5 3.5	 6.0 6.0	mA
IEE	-Vs (-15V) Supply Current	Supply = +/- 16.5 V, VI = 5.0 V, Test Inputs = 0 V Test Inputs = 5 V	 7.5 11.0	 12.0 18.5	mA
IL	+VL (+5V) Supply Current	Supply = +/- 16.5 V, VI = 5.0 V, Test Inputs = 0 V Test Inputs = 5 V	 4.5 10.8	 9.0 17.6	mA
		A429 INPUTS			
VNH	NULL to 1 transition, V(INA) – V(INB)	Supply = +/-15.0V, VI = 5.00 V Test inputs = 0 V VINB = -2.50 V	5.70	6.30	V
VHN	1 to NULL transition, V(INA) – V(INB)	Supply = +/-15.0V, VI = 5.00V Test inputs = 0 V VINB = -2.50 V	4.50	5.50	V
VHHYS	1 to NULL transition hysteresis	VNH-VHN	0.8	1.2	V
VNL	NULL to 0 transition, V(INA) – V(INB)	Supply = +/-15.0 V, VI = 5.00 V Test inputs = 0 V VINB = +2.50 V	-6.30	-5.70	V
VLN	0 to NULL transition, V(INA) – V(INB)	Supply = +/-15.0 V, VI = 5.00 V Test inputs = 0 V VINB = +2.50 V	-5.50	-4.50	V
VLHYS	0 to NULL transition hysteresis	VNL-VLN	-1.2	-0.8	V
VCM	Input common mode voltage range		-13	+13	V
RINGND	Input resistance, Input to GND	Unpowered, INA to GND, INB to GND	20	30	kΩ
RIN	Input resistor, INA to CAPA, INB to CAPB	Unpowered INA to CAPA, INB to CAPB	8.5	11.5	kΩ
CIN	Input capacitance	INA or INB to GND (3)		10	pF

SYMBOL	PARAMETER	CONDITIONS (1,2)	MIN	MAX	UNIT
		TEST LOGIC INPUTS			
VIH	LOGIC 1 input voltage	Functional Test	2.0		V
VIL	LOGIC 0 input voltage	Functional Test		0.9	V
IIH	LOGIC 1 input current	VIH = 5 V Supply = +/-15.0 V, VI = 5.00 V	0	600	µA
IIL	LOGIC 0 input current	VIL = 0.8V Supply = +/-15.0 V, VI = 5.00 V	0	50	µA
		LOGIC OUTPUTS			
VOH	LOGIC 1 output voltage	Vsupply = +/-15.0 V, VI = 5.0 V IOH = -100 uA (Room Temp) IOH = -2.8 mA	 4.0 3.5		 V V
VOL	LOGIC 0 output voltage	Vsupply = +/-15.0 V, VI = 5.0 V IOL = 100 uA (Room Temp) IOL = 2.0 mA		 0.1 0.8	 V V
Tr	Output rise time	CL = 60 pF (4)	10	70	ns
Tf	Output Fall Time	CL = 60 pF (4)	10	70	ns
TPLH	Prop delay, A429 to LH output	A429 In = 0 to 10 V (4) CAPA, CAPB, OUT CL = 60 pF		1500	ns
TPHL	Prop delay, A429 to HL output	A429 In = 0 to 10 V (4) CAPA, CAPB, OUT CL = 60 pF		1500	ns
DTP	Matching of TPLH and TPHL	|TPLH-TPHL| (4)		500	ns
TPTLH	Prop delay, TESTA/B to LH output	CL = 60 pF, VIN = 0.8 V / 2.0 V (4)	400	600	ns
TPTHL	Prop delay, TESTA/B to HL output	CL = 60 pF, VIN = 0.8 V / 2.0 V (4)	800	1300	ns

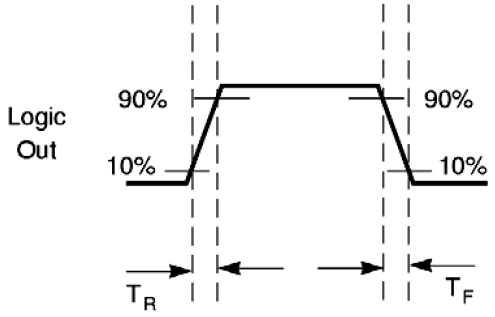
Notes:

1. Unless otherwise noted, currents flowing in to DUT are positive, Currents flowing out of DUT are negative, Voltages are referenced to Ground.
2. Unless otherwise noted, Tcase = -55 °C to +125 °C for -xMx, -40 °C to +125 °C for -xAx, and -55 °C to +85 °C for –xEx versions; +VS = +13.5 to 16.5 V, -Vs = -13.5 to –16.5 V, +VL = 4.5 to 5.5 V.
3. Guaranteed by design. Not production tested.
4. Sample tested.

AC TEST WAVEFORMS



Propagation Delay



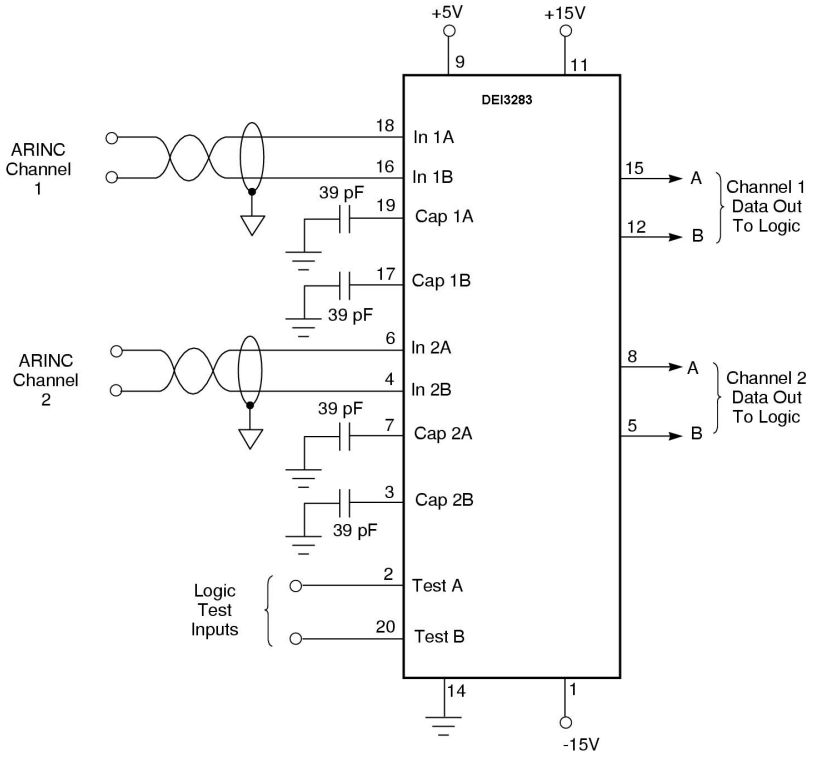
Rise/Fall Times

APPLICATION INFORMATION

The typical connections for the DEI3283 are shown in the figure below. Dual ±15 VDC supplies are recommended for the +VS/-VS supplies. Decoupling of all supplies should be done near the IC to avoid propagation of noise spikes due to switching transients. The ground connection should be sturdy and isolated from large switching currents to provide as quiet a ground reference as possible. The noise filter capacitors are optional and are added to provide extra noise immunity by limiting bandwidth of the input signal before it reaches the window comparator stage. Two capacitors are used for each channel and they must be the same value. The suggested capacitor value for a 100 kHz operation is 39 pF. For lower data rates, larger values of capacitance may be used to yield better noise performance. To get optimum performance, the following equation can be used to calculate capacitor value for a specific data rate:

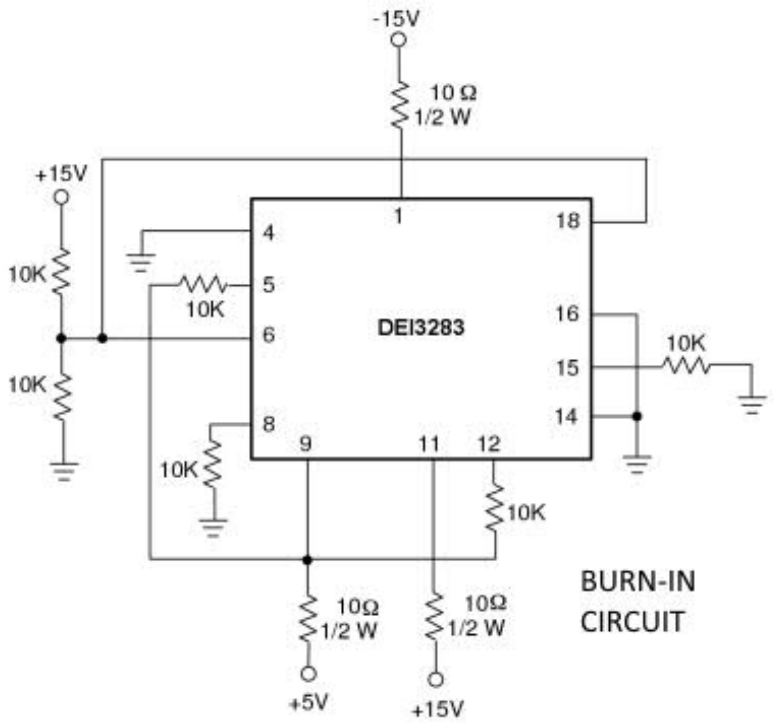
$$C_{FILTER} = \frac{3.95 \times 10^{-6}}{F_O}$$

Where C_{FILTER} is the capacitor value in pF, and F_O is the input frequency (10 kHz ≤ FO ≤ 150 kHz).



PROCESS FLOW

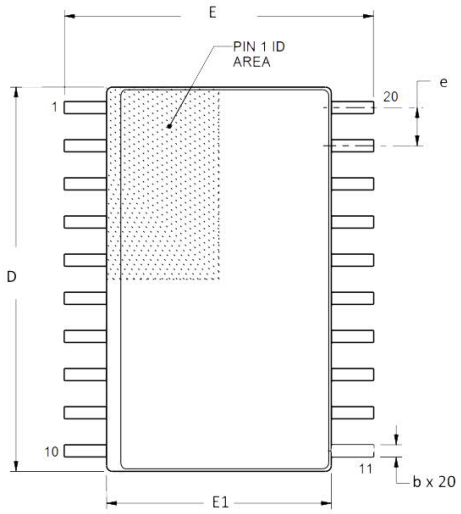
PROCESS STEP	PLASTIC STANDARD	CERAMIC STANDARD	PLASTIC BURN-IN	CERAMIC BURN-IN
THERMAL CYCLE MIL-STD-883 M1010 Cond B	NO	10 Cycles	NO	10 Cycles
CONSTANT ACCELERATION MIL-STD-883 M2001 Method D	N/A	YES	N/A	YES
GROSS & FINE LEAK MIL-STD-883 M1014	N/A	YES	N/A	YES
PRE-BURN-IN Electrical Test	N/A	N/A	YES	YES
BURN IN MIL-STD-883 M1015 Cond A	N/A	N/A	160 hrs @ +125 °C	160 hrs @ +125 °C
FINAL ELECTRICAL TEST, Room Temperature	100%	100%	100%	100%
FINAL ELECTRICAL TEST, High Temperature	100% @ +85 or +125 °C	100% @ +125°C	100% @ +85 or +125 °C	100% @ +125 °C
FINAL ELECTRICAL TEST, Low Temperature	0.65% AQL @ -55 or -40 °C	0.65% AQL @ -55 °C	0.65% AQL @ -55 or -40 °C	0.65% AQL @ -55 °C

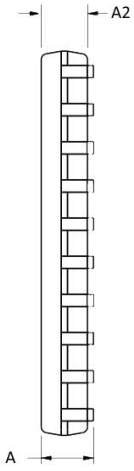


PACKAGE CHARACTERISTICS

PACKAGE TYPE / CHARACTERISTIC	20L CERAMIC LCC	20L CERDIP	20L CERDIP GREEN	20L SOIC GREEN
Reference (see ordering info)	20 CLCC	20 CERDIP	20 CERDIP G	20 SOIC G
JEDEC MO Reference	MO-047	MS-030-A-AE	MS-030-A-AE	MS-013-AE
THERMAL RESISTANCE: Θ_{JA} (4 layer PCB) Θ_{JC}	85 °C/W 30 °C/W	70 °C/W 28 °C/W	70 °C/W 28 °C/W	85 °C/W 30 °C/W
JEDEC Moisture Sensitivity Level (MSL)	Hermetic	Hermetic	Hermetic	MSL 1 / 250 °C
Lead Finish Material / JEDEC Pb-free code	SnPb solder dip na	SnPb solder dip na	SnAgCu solder dip e1	NiPdAu plate e3
Pb-Free designation	Not Pb-free	Not Pb-free	Pb free	RoHS Compliant

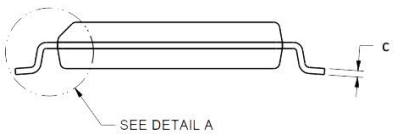
20L SOIC Package

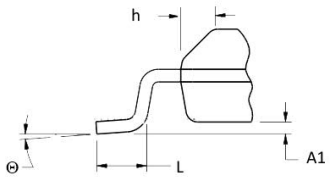




	DIMENSIONS IN INCHES			DIMENSIONS IN MM		
SYM	MIN	NOM	MAX	MIN	NOM	MAX
A	0.098	0.101	0.104	2.49	2.57	2.64
A1	0.005	0.009	0.012	0.13	0.23	0.30
A2	0.089	0.092	0.095	2.26	2.34	2.41
b	0.012	0.016	0.020	0.30	0.41	0.51
c	0.008	0.010	0.013	0.20	0.25	0.33
D	0.499	0.503	0.507	12.7	12.8	12.9
E1	0.291	0.295	0.299	7.39	7.49	7.59
E	0.400	0.404	0.414	10.16	10.26	10.52
e		0.050			1.27	
L	0.016	-	0.050	0.41	-	1.27
L1	0.051	0.055	0.059	1.30	1.40	1.50
Θ	0	-	8	0	-	8
h	0.010	0.015	0.020	0.25	0.38	0.50
N		20			20	

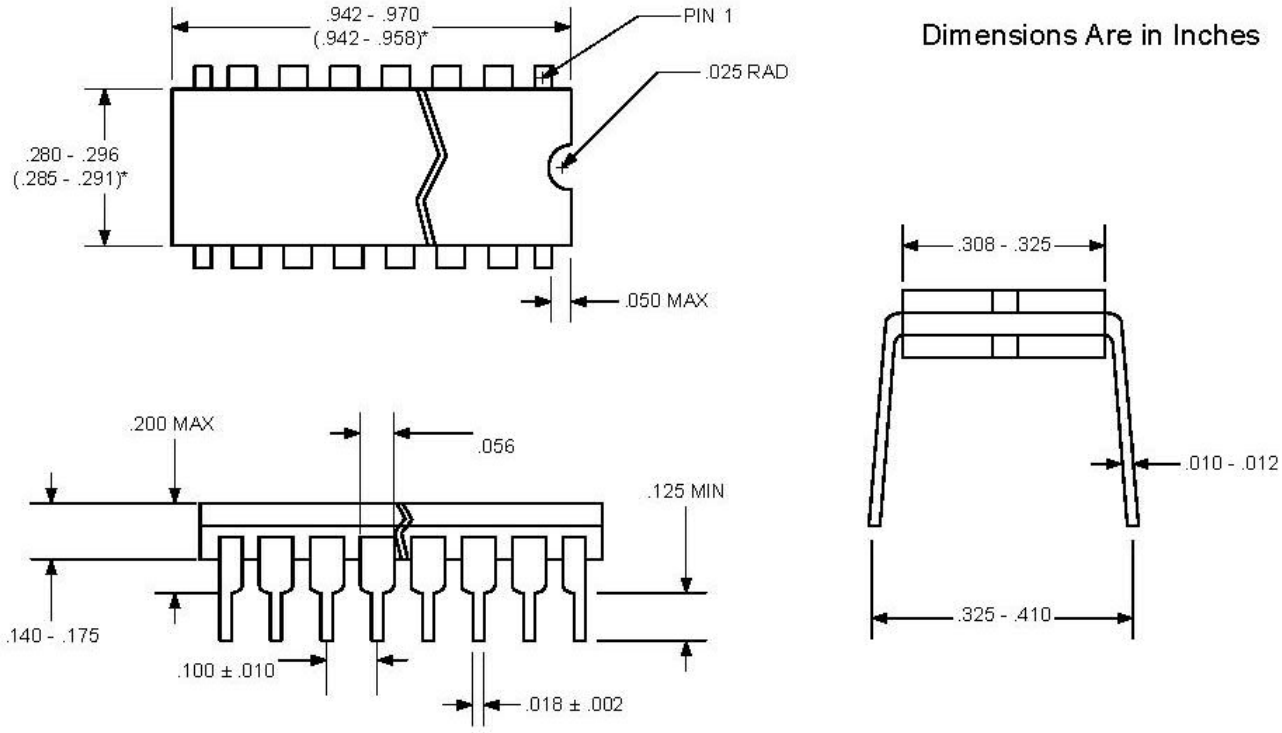
NOTES:
1. DIMENSIONS DO NOT INCLUDE MOLD FLASH PROTRUSIONS OR BURRS.
2. COPLANARITY SHALL NOT EXCEED 0.004 ".



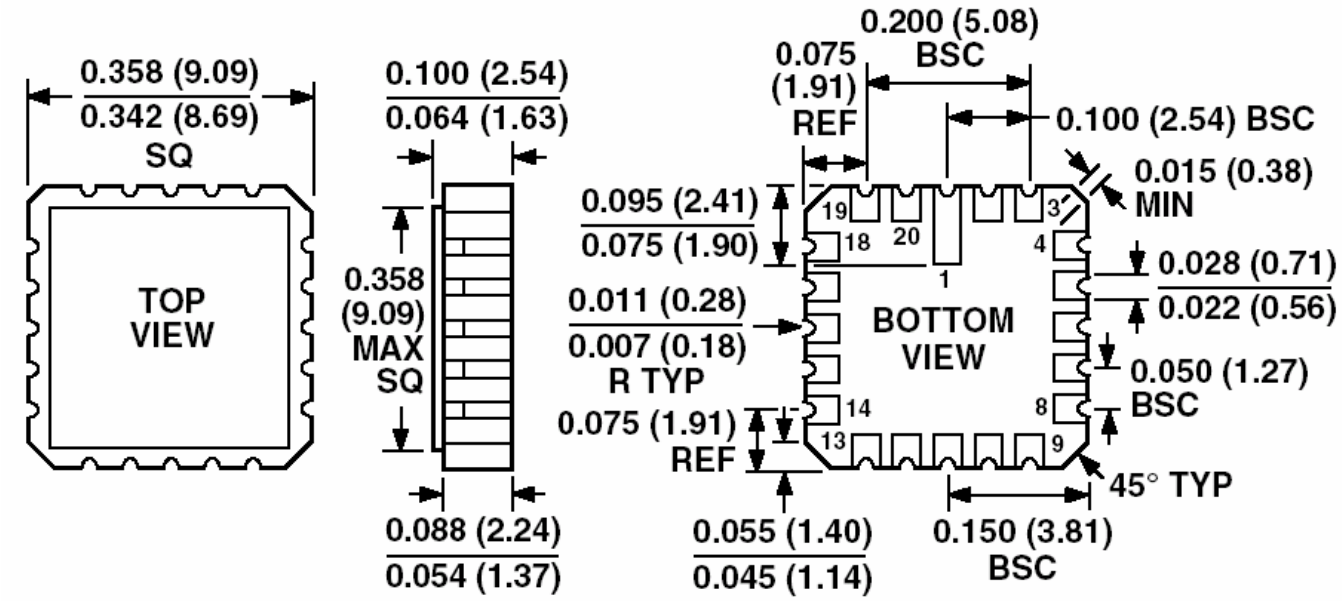


DETAIL A
TYPICAL

20L CERDIP Package



20L Ceramic LCC Package



ORDERING INFORMATION

PART NUMBER	MARK	PACKAGE	OPERATING TEMPERATURE	BURN IN
DEI3283-CMB	DEI3283-CMB	20 CERDIP	-55 °C to +125 °C	Y
DEI3283-CMB-G	DEI3283-CMB E1	20 CERDIP G	-55 °C to +125 °C	Y
DEI3283-CMS	DEI3283-CMS	20 CERDIP	-55 °C to +125 °C	N
DEI3283-CMS-G	DEI3283-CMS E1	20 CERDIP G	-55 °C to +125 °C	N
DEI3283-EMB	DEI3283-EMB	20 CLCC	-55 °C to +125 °C	Y
DEI3283-EMS	DEI3283-EMS	20 CLCC	-55 °C to +125 °C	N
DEI3283-SAS-G	DEI3283-SAS e3	20 SOIC G	-40 °C to +125 °C	N
DEI3283-SAB-G	DEI3283-SAB e3	20 SOIC G	-40 °C to +125 °C	Y
DEI3283-SES-G	DEI3283-SES e3	20 SOIC G	-55 °C to +85 °C	N
DEI3283-SMS-G	DEI3283-SMS e3	20 SOIC G	-55 °C to +125 °	N

Notes:
1. All packages marked with Lot Code and Date Code. “E1” or “E3” after Date Code denotes Pb-Free category.
2. The –CMB/-EMB/-SAB parts may be marked as – CMS/-EMS/-SAS with a “B” stamp to denote burn-in.