Device
Engineering
Incorporated

6031 South Maple Avenue
Tempe, AZ 85283
Phone: (480) 303-0822
Fax: (480) 303-0824
E-mail: admin@deiaz.com

DEI1044A, DEI1045A
QUAD ARINC 429
LINE RECEIVER

FEATURES

- Quad ARINC 429 to TTL/CMOS logic line receivers
- Drop-in replacement for DEI1044 / DEI1045
- Drop-in replacement for HI-8444/5PS_, HI-8444/5PS_ -10 & HI-8454/5P
- Operates from single +5 V or 3.3 V power supply
- ARINC input internally protected to lightning requirements of DO-160 level 3 pin injection
- ARINC inputs withstand inadvertent short to 115 Vac
- Operates with optional external serial resistors on the ARINC inputs up to 15 kΩ
  - Supports lightning protection beyond level 3
  - Provides resistive fault Isolation
- Operates in high noise environment
  - ±20 V input common mode voltage range
  - 2 V minimum input hysteresis
- DEI1044A has TTL/CMOS test inputs
- Package: 20L 4.4 mm TSSOP

FUNCTIONAL DESCRIPTION

The DEI1044A and DEI1045A are quad ARINC 429 Line Receiver ICs implemented in BiCMOS technology. They contain four differential line receivers. Each receiver channel translates incoming ARINC 429 data bus signals to a pair of TTL/CMOS outputs. Each receiver operates independently, is lightning protected, and meets requirements of the *ARINC 429 Digital Information Transfer Standard*.

The DEI1044A IC includes two TEST inputs for built in system test. They force the outputs of all receivers to the specified ZERO, ONE or NULL state. The ARINC inputs are ignored when the device is in test mode. The DEI1045A does not have TEST inputs.

The DEI1044A/1045A Quad Line Receiver can be used in conjunction with Device Engineering's family of avionics products in interfacing the ARINC 429 data bus.

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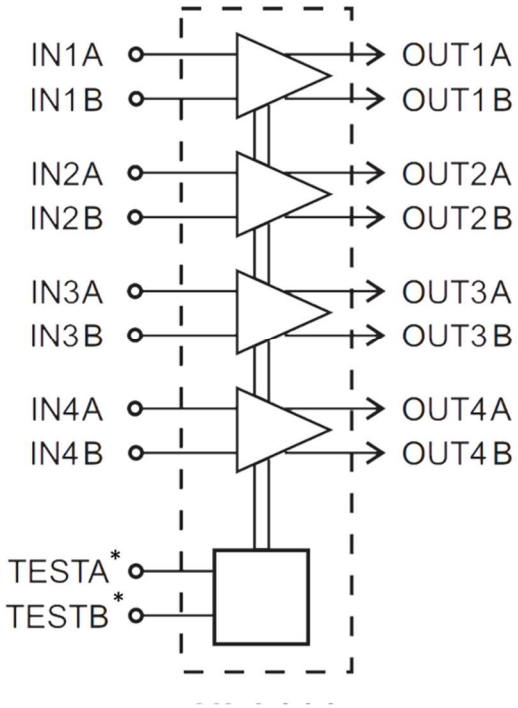
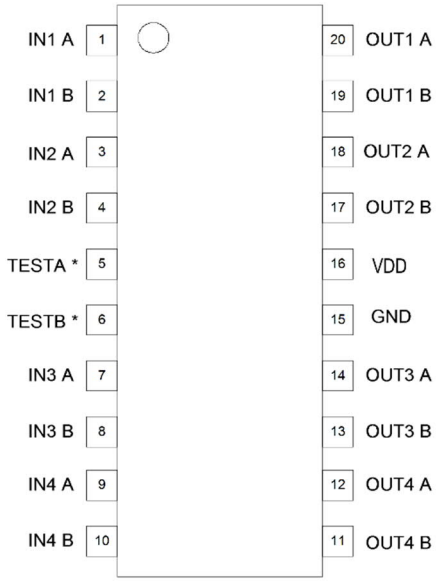


Figure 1 Function Diagram

Table 1 Function Table

TESTA	TESTB	IN_NA - IN_NB	OUT_NA	OUT_NB
L	L	ONE +10 V	H	L
L	L	ZERO -10 V	L	H
L	L	NULL 0 V	L	L
L	H	X	L	H
H	L	X	H	L
H	H	X	L	L
Test Inputs are internally set to L on DEI1045A				



*Pins 5 & 6 are “No Connect” on DEI1045A

Figure 2 Pinout

ELECTRICAL DESCRIPTION

Table 2 Absolute Maximum Ratings

PARAMETER	MIN	MAX	UNIT
Supply Voltage (VDD)	-0.3	7.0	V
Input Voltage, continuous (ARINC Inputs)		115	Vac
Input Voltage (Test Inputs)	– 0.3	VDD + 0.3	V
Power Dissipation @ 85 °C		350	mW
Lightning Protection (ARINC Inputs) (2) Waveform 3 Waveform 4 and 5A	 -630 -360	 +630 +360	 V V
Peak Body Temperature		260	°C
Storage Temperature	-65	+150	°C
ESD JS-001 HBM	1C		Class

NOTES:
1. Stresses above these limits can cause permanent damage.
2. Per DO160, Sect 22 Level 3 pin injection. See Figures 5 – 7.

Table 3 Recommended Operating Conditions

PARAMETER	SYMBOL	CONDITIONS
Supply Voltage	VDD	+5 V ±10% +3.3 V ±10%
Logic Input Levels	TESTA,B	0 to VDD
Operating Temperature- -TES -TMS	Top	-55 to +85°C -55 to +125°C

Table 4 Electrical Characteristics

Conditions: Temperature: -55 °C to +85 °C (-TES); -55 °C to +125 °C (-TMS)
VDD = +5 V ±10% or 3.3 V ±10%

PARAMETER	TEST CONDITION	SYMBOL	MIN	MAX	UNIT
ARINC INPUTS (with external series resistors of 0 to 15 kΩ)					
INA – INB = Logic +1	OUTA = 1	V_{+1}	6.5	13	V
INA – INB = Logic -1	OUTB = 1	V_{-1}	-6.5	-13	V
INA – INB = Logic Null	OUTA = 0 OUTB = 0	V_{NULL}	-2.5	2.5	V
Input Hysteresis		V_{HY}	2.0	4.0	V
Input Common Mode Voltage Range	Logic +1, Null, Logic -1	V_{CM}	-20	+20	V
Input Resistance INA to INB	VDD open, Shorted to GND or +5 V (1)	R_{IN}	400		kΩ
Input Resistance INA or INB to GND	VDD open, Shorted to GND or +5 V	R_S	200		kΩ

Conditions: Temperature: -55 °C to +85 °C (-TES); -55 °C to +125 °C (-TMS)
VDD = +5 V ±10% or 3.3 V ±10%

PARAMETER	TEST CONDITION	SYMBOL	MIN	MAX	UNIT
Input Capacitance INA to INB	VDD open, Shorted to GND or +5 V (1)	C_{IN}		10	pF
Input Capacitance INA or INB to GND	VDD open, Shorted to GND or +5 V (1)	C_S		10	pF
LOGIC INPUTS					
Logic 0 Voltage		V_{IL}		0.8	V
Logic 1 Voltage		V_{IH}	2.3		V
Logic 0 Current	V_{IL} = 0.8	I_{IL}		10	µA
Logic 1 Current	V_{IH} = 2.0	I_{IH}		30	µA
LOGIC OUTPUTS					
Output High Voltage TTL	I_{OH} = -5 mA @ VDD = 5 V I_{OH} = -1.5 mA @ VDD = 3.3 V	V_{OH}	2.4		V
Output Low Voltage TTL	I_{OL} = 5 mA @ VDD = 5 V I_{OL} = 1.5 mA @ VDD = 3.3 V	V_{OL}		0.4	V
Output High Voltage CMOS	I_{OH} = 100 µA	V_{OH}	VDD – 0.05		V
Output Low Voltage CMOS	I_{OL} = 100 µA	V_{OL}		0.05	V
SUPPLY CURRENT					
VDD Current	Inputs and Outputs open	I_{DD}	0.5	2.5	mA

Notes:
1. Guaranteed by design, not production tested.
2. Current flowing into device is positive. Current flowing out of device is negative. All voltages are with respect to GND unless otherwise noted.

Table 5 Switching Characteristics

PARAMETER	TEST CONDITION (1-3)	SYMBOL	MIN	MAX	UNIT
INA/B to OUTA/B Prop Delay	TESTA = TESTB = 0 C_L = 50 pF	t_{LH} t_{HL}		900	ns
Matching t_{LH} to t_{HL}	Calculated	Dtp		500	ns
OUTA/B rise/fall time	10% to 90%, C_L = 50 pF	t_r t_f		50	ns
TESTA/B to OUTA/B Prop delay	C_L = 50 pF	t_{TOH} t_{TOL}		100	ns

Notes:
1. Over rated supply voltage and temperature
2. Sample tested.
3. Refer to Figures 3 - 4

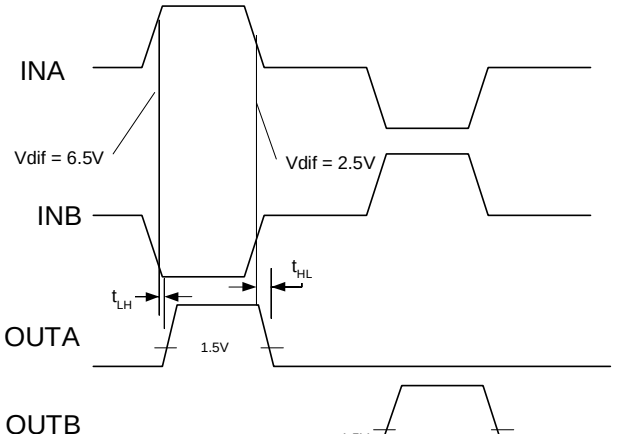


Figure 3 ARINC 429 Input to Logic Output Switching Waveform

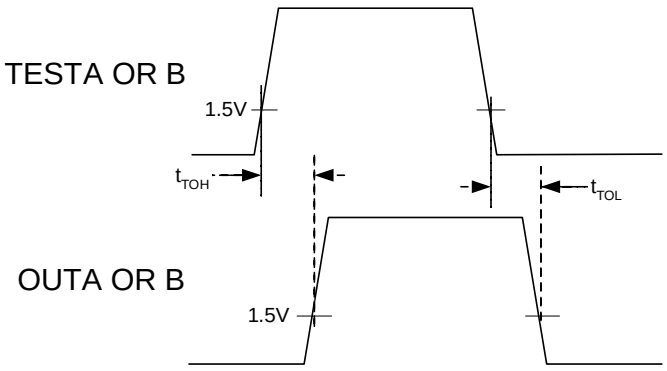


Figure 4 TEST Input to Logic Output Switching Waveform

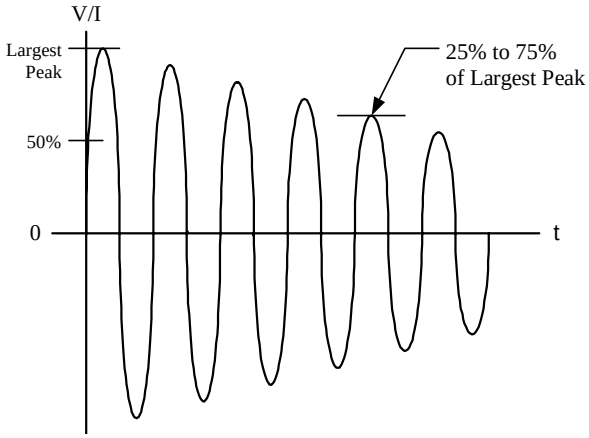


Figure 5 DO160 Lightning Induced Transient Voltage Waveform #3.

Voc = 600 V, Isc = 24 A, Frequency =1 MHZ +-20%

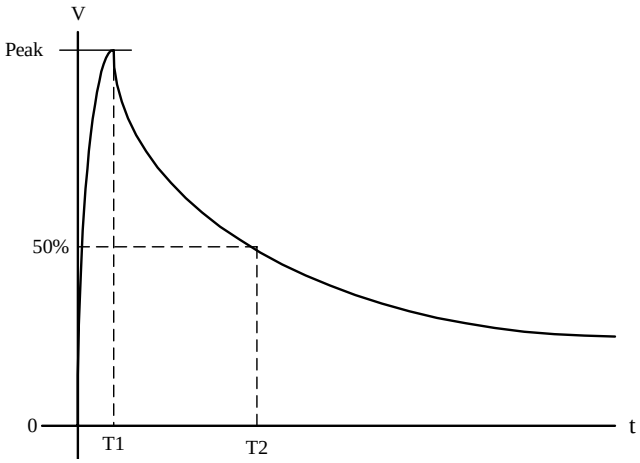


Figure 6 DO160 Lightning Induced Transient Voltage Waveform #4.

Voc = 300 V, Isc = 60 A

LIGHTNING TRANSIENT NOTES:

1. Voc = Peak Open Circuit Voltage available at the calibration point.
2. Isc = Peak Short Circuit Current available at the calibration point.
3. Amplitude tolerances: +10%, -0%.
4. The ratio of Voc to Isc is the generator source impedance to be used for generating the waveforms.

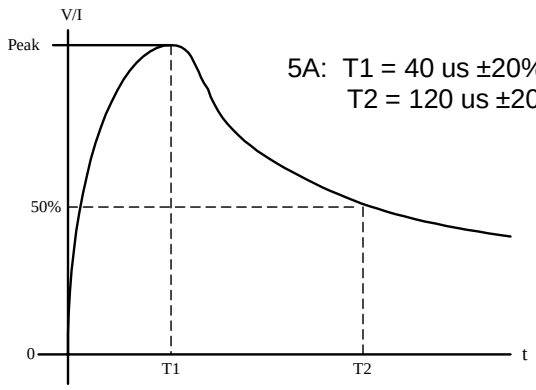
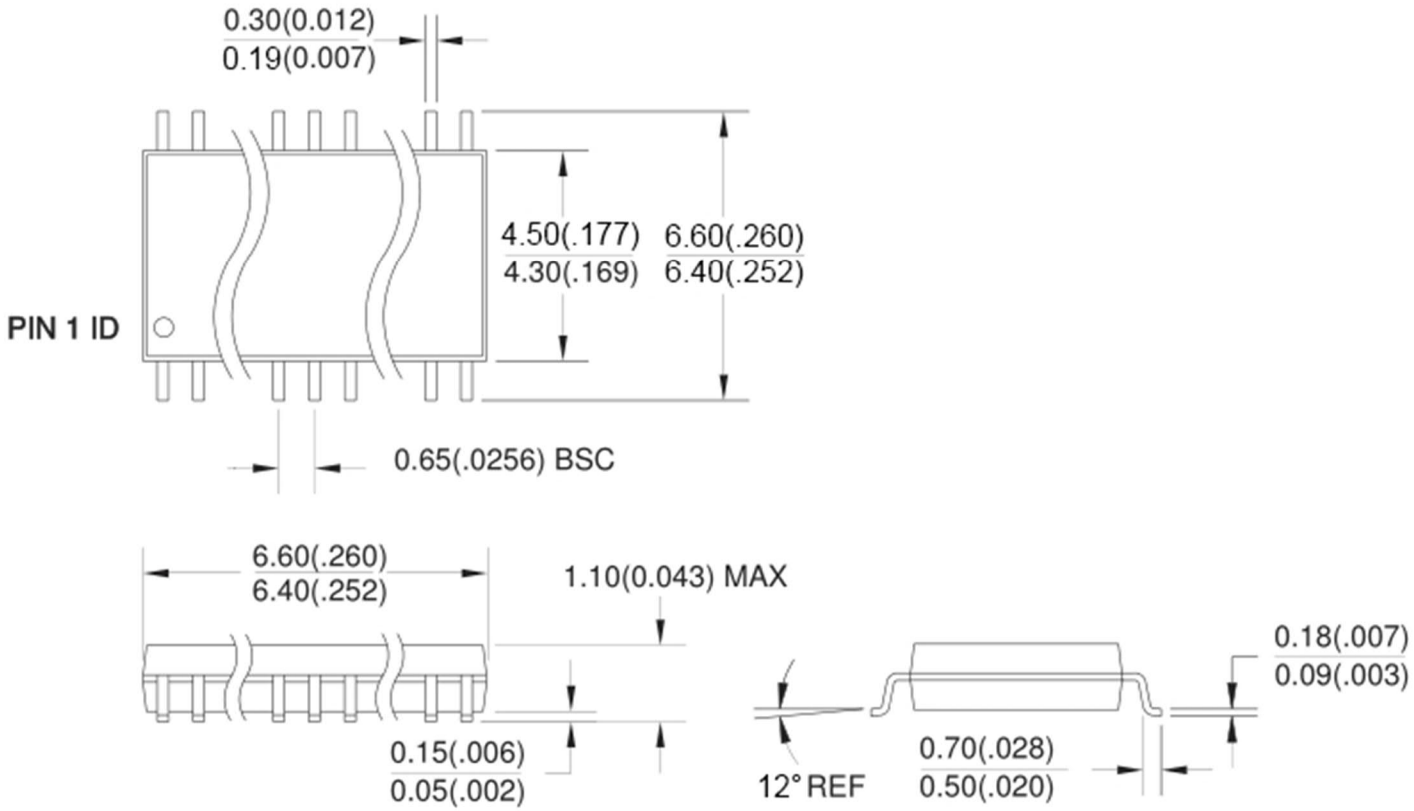


Figure 7 DO160 Lightning Induced Transient Voltage Waveform #5.

Voc = 300 V, Isc = 300 A

PACKAGE DESCRIPTION

20L TSSOP



Dimensions in mm (inch)

Figure 10: Outline Drawing

Table 6 Package Characteristics

PACKAGE TYPE	20L TSSOP
THERMAL RESISTANCE: Θ_{JA} (4 layer PCB with Power Planes) Θ_{JC}	 90 °C/W 17 °C/W
JEDEC MOISTURE SENSITIVITY LEVEL (MSL)	MSL 1 / 260 °C
LEAD FINISH MATERIAL / JEDEC Pb-free CODE	NiPdAu e4
Pb-Free DESIGNATION	RoHS Compliant
JEDEC REFERENCE	MO-153-AC

ORDERING INFORMATION

Table 7 Ordering Information

DEI PART NUMBER	MARKING (1)	PACKAGE	TEMPERATURE RANGE	TEST INPUTS
DEI1044A-TES-G	DEI1044AE (e4)	20L TSSOP G	-55 / +85 °C	YES
DEI1044A-TMS-G	DEI1044AM (e4)	20L TSSOP G	-55 / +125 °C	YES
DEI1045A-TES-G	DEI1045AE (e4)	20L TSSOP G	-55 / +85 °C	NO
DEI1045A-TMS-G	DEI1045AM (e4)	20L TSSOP G	-55 / +125 °C	NO

Notes:
1. All packages marked with Lot Code and Date Code. (e4) after Date Code denotes Pb Free category.

Table 8 Screening Process

SCREENING	METHODS
ELECTRICAL TEST:	
ROOM TEMPERATURE	100%
HIGH TEMPERATURE	100% @ +85 or 125 °C
LOW TEMPERATURE	0.65% AQL @ -55 °C