Device
Engineering
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DEI1084/1085
ARINC 429 ENHANCED TRANSCEIVER

FEATURES

- ARINC specification 429 compatible
- 3.3 V / 5.5 V supply operation
- Dual receiver and single transmitter interface
- 32nd transmit bit can be data or parity
- Self test mode
- Pin compatible with HI3584 & HI8584
- Programmable label recognition
- On-chip 16 label memory for each receiver
- 32 x 32 FIFO for transmitter and each receiver
- Independent data rate selection for transmitter and each receiver
- Status register
- Data scramble control
- Package Options: 52L QFP, 52L CQFJ, & 64L MLPQ

GENERAL DESCRIPTION

The DEI1084 is a CMOS ARINC 429 Transceiver IC. It is pin compatible with the Holt HI-3584 and HI-8584 products.

The DEI2084/85-Mxx versions are alternate package pin-outs of the DEI1084/85-Mxx to provide access to the /TXSEL output in the MLPQ package.

The enhancements relative to the DEI1016 transceiver include: 32x32 bit FIFO for transmitter, 32x32 bit FIFO for each receiver, a status register, label recognition capability, bit timing feature and choice of scrambled or unscrambled ARINC data output.

The DEI1085 version requires external serial 10 kΩ resistors on the receiver inputs. This simplifies the implementation of external lightning protection networks.

The DEI1084 version has on-chip 10 kΩ resistors and do not require external resistors on the inputs.

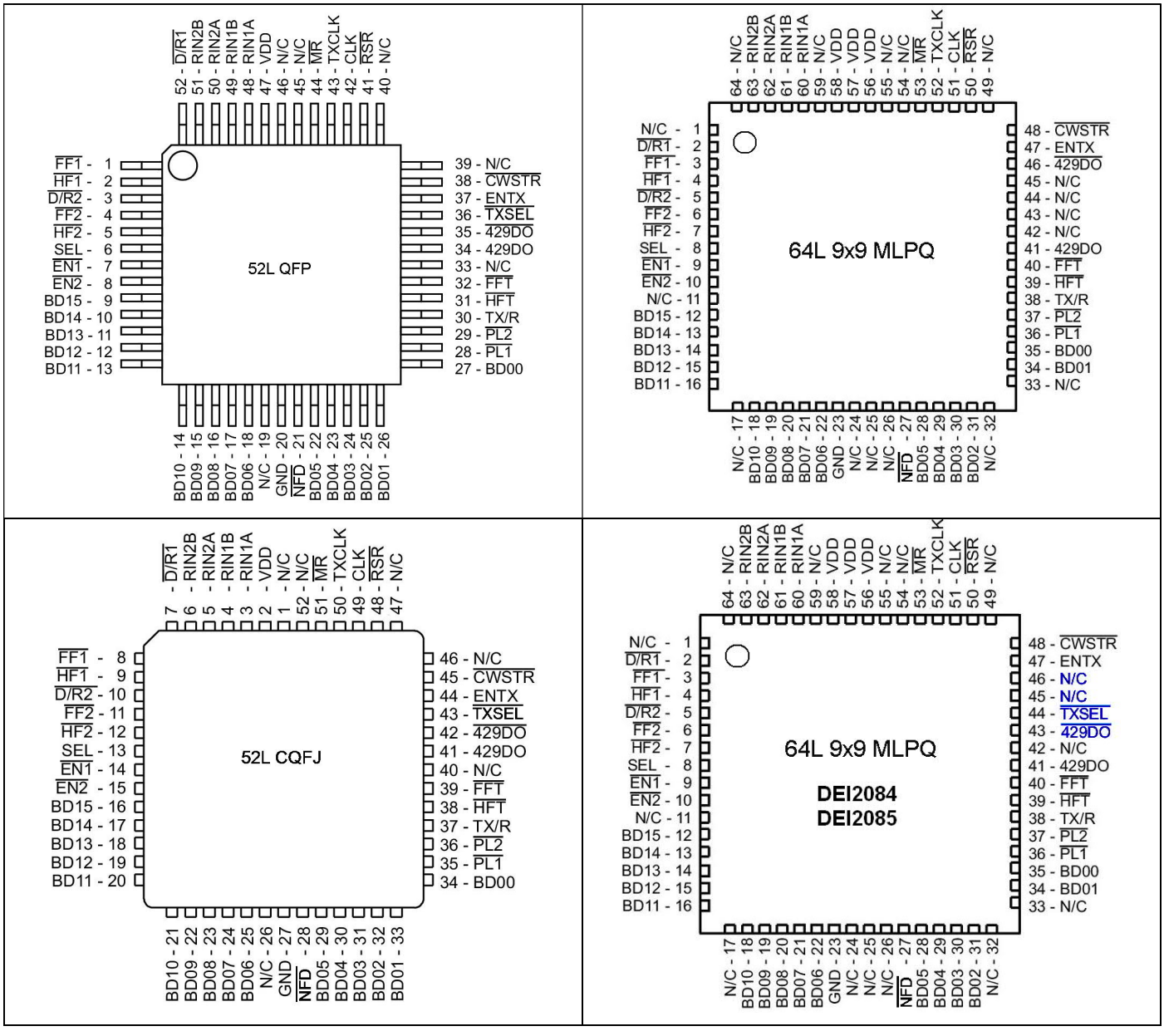
TERMINAL DESCRIPTIONS AND PIN ASSIGNMENTS

Table 1: DEI1084 Pin Description

QFP PIN	CQFJ PIN	MLPQ 1084/5	MLPQ 2084/5	SIGNAL	FUNCTION	DESCRIPTION
47	2	56 57 58		VDD	POWER	Power Input: +3 V or +5 V.
48	3	60		RIN1A	INPUT	ARINC receiver 1 positive input.
49	4	61		RIN1B	INPUT	ARINC receiver 1 negative input.
50	5	62		RIN2A	INPUT	ARINC receiver 2 positive input.
51	6	63		RIN1B	INPUT	ARINC receiver 2 negative input.
52	7	2		/DR1	OUTPUT	Receiver 1 data flag ready.
1	8	3		/FF1	OUTPUT	Receiver 1 FIFO full.
2	9	4		/HF1	OUTPUT	Receiver 1 FIFO half full.
3	10	5		/DR2	OUTPUT	Receiver 2 data flag ready.

QFP PIN	CQFJ PIN	MLPQ 1084/5	MLPQ 2084/5	SIGNAL	FUNCTION	DESCRIPTION
4	11	6	6	/FF2	OUTPUT	Receiver 2 FIFO full.
5	12	7	7	/HF2	OUTPUT	Receiver 2 FIFO half full.
6	13	8	8	SEL	INPUT	Receiver data byte selection (0 = BYTE 1) (1 = BYTE 2).
7	14	9	9	/EN1	INPUT	Data Bus control enables receiver 1 data to output.
8	15	10	10	/EN2	INPUT	Data Bus control enables receiver 2 data to output.
9 10 11 12 13 14 15 16 17 18 22 23 24 25 26 27	16 17 18 19 20 21 22 23 24 25 29 30 31 32 33 34	12 13 14 15 16 18 19 20 21 22 28 29 30 31 34 35	12 13 14 15 16 18 19 20 21 22 28 29 30 31 34 35	BD15:14 BD13:12 BD11:10 BD09:08 BD07:06 BD05:04 BD03:02 BD01:00	I/O	Data Bus.
20	27	24 25 26	24 25 26	GND	POWER	Power and signal ground.
21	28	27	27	/NFD	INPUT	No frequency discrimination if low (pull up)
28	35	36	36	/PL1	INPUT	Latch enable for byte 1 entered from data bus to transmitter FIFO.
27	36	37	37	/PL2	INPUT	Latch enable for byte 2 entered from data bus to transmitter FIFO. Must follow /PL1.
30	37	38	38	TX/R	OUTPUT	Transmitter ready flag. Goes low when ARINC word loaded into FIFO. Goes high after transmission and FIFO empty.
31	38	39	39	/HFT	OUTPUT	Transmitter FIFO half full.
32	39	40	40	/FFT	OUTPUT	Transmitter FIFO full.
34	41	41	41	429DO	OUTPUT	“ONES” data output from transmitter.
35	42	46	43	/429DO	OUTPUT	“ZEROS” data output from transmitter.
36	43	-	44	/TXSEL	OUTPUT	Transmitter Speed Select Status. Hi = High speed, Lo = Low speed. Inverted control word “TXSEL”.
37	44	47	47	ENTX	INPUT	Enable transmission.
38	45	48	48	/CWSTR	INPUT	Clock for control word register.
41	48	50	50	/RSR	INPUT	Read status register if SEL = 0, read control register if SEL = 1 (pull up)
42	49	51	51	CLK	INPUT	Master clock input.
43	50	52	52	TX CLK	OUTPUT	Transmitter clock equal to master clock (CLK), divided by either 10 or 80.
44	51	53	53	/MR	INPUT	Master reset.

QFP PIN	CQFJ PIN	MLPQ 1084/5	MLPQ 2084/5	SIGNAL	FUNCTION	DESCRIPTION
19 33 39 40 45 46	1 26 40 46 47 52	1 11 17 24 25 26 32 33 42 43 44 45 49 54 55 59 64	1 11 17 24 25 26 32 33 42 43 44 45 49 54 55 59 64	NC		No connection in IC



FUNCTIONAL DESCRIPTION

ANALOG FRONT END WITH LIGHTNING PROTECTION

The analog front end (AFE) implements the analog detection portion of the receiver circuit. The ARINC 429 characteristic describes RX detection levels as follows.

STATE	DIFFERENTIAL VOLTAGE
ONE	+6.5 V to +13 V
NULL	+2.5 V to -2.5 V
ZERO	-6.5 V to -13 V

The AFE detects the received ARINC line signal and converts it into a stream of digital logic levels. It consists of a pair of differential comparators per receiver capable of ±10 V of common mode rejection. The AFE is powered by an on chip 2.5 V voltage regulator. This makes the part capable of operating from a supply voltage ranging from 2.97 V to 5.5 V. The DEI1085 version parts bypass 10 kΩ of the input resistors, facilitating the use of 10 kΩ external series resistors to provide lightning immunity without impacting the input resistance specifications.

Lightning transient protection is provided at the receiver input pins. The receiver input pins, in combination with external 10 kΩ resistors, provide immunity to DO160 Level 3 Lightning Induced Transients. (These include the 600 V peak damped sinusoid and 300V/150µs pulse). This immunity is provided by the external 10 kΩ resistors combined with the on-chip Zener diodes located within the receiver input network. During a voltage transient, the diodes shunt current to ground and drop most of the transient voltage across the external resistors, thus protecting the chip's input pins.

When the internal resistor wire bond option is used, the application must provide Transient Voltage Suppressor (TVS) devices to limit transient voltage to ±120 V.

16 BIT DATA BUS

A 16 Bit parallel bi-directional tri-state data bus provides communication to the host.

SERIAL INTERFACE

The DEI1084 consists of two receive channels and one transmit channel. Each receive channel operates independently of each other and the transmitter. The receive data is asynchronous to the transmitter data and can also be at a different data rate than the transmitter.

TRANSMITTER

The transmitter clock is free running and in phase with the transmitter data. The transmitter data (DO(A) and DO(B)) are TTL level signals. There are always at least 4 null bits between data words. An external ARINC line driver is required to interface the transmitter to the ARINC serial data bus.

RECEIVER

The receiver signals (DI(A) and DI(B)) are differential, bipolar, return-to-zero logic signals. The ARINC channels can be connected directly to the receiver with no external components.

CONTROL REGISTER

A 16-bit control register is used to configure the device. The control register bits CR0 – CR15 are loaded from BD00 – BD15 when /CWSTR is pulsed low. The control register contents are output on the data bus when SEL = 1 and /RSR is pulsed low. Each bit of the control register has the following function:

Table 2: Control Register Bit definition

CR Bit	FUNCTION	POL	DESCRIPTION
CR0	Receiver 1 Data Clock Select	0	Data rate HI = CLK/10
		1	Data rate LO = CLK/80
CR1	Label Memory Read/ Write	0	Normal operation
		1	Load 16 labels using /PL1, /PL2 Read 16 labels using /EN1, /EN2
CR2	Enable Label Recognition (Receiver 1)	0	Disable label recognition
		1	Enable label recognition
CR3	Enable Label Recognition (Receiver 2)	0	Disable label recognition
		1	Enable label recognition
CR4	Enable 32nd bit as parity	0	Transmitter 32nd bit is data
		1	Transmitter 32nd bit is parity

CR Bit	FUNCTION	POL	DESCRIPTION
CR5	Self Test	0	The 429DO and /429DO digital outputs are internally connected to the Rx logic inputs
		1	Normal operation
CR6	Receiver 1 decoder	0	Receiver 1 decoder disabled
		1	ARINC bits 9 and 10 must match CR7 and CR8
CR7	-	-	If receiver 1 decoder is enabled, the ARINC bit 9 must match this bit
CR8	-	-	If receiver 1 decoder is enabled, the ARINC bit 10 must match this bit
CR9	Receiver 2 decoder	0	Receiver 2 decoder disabled
		1	ARINC bits 9 and 10 must match CR10 and CR11
CR10	-	-	If receiver 2 decoder is enabled, the ARINC bit 9 must match this bit
CR11	-	-	If receiver 2 decoder is enabled, the ARINC bit 10 must match this bit
CR12	Invert Transmitter parity	0	Transmitter 32nd bit is Odd parity
		1	Transmitter 32nd bit is Even parity
CR13	Transmitter data clock select	0	Data rate = HI = CLK/10
		1	Data rate = LO = CLK/80
CR14	Receiver 2 Data clock Select	0	Data rate = HI = CLK/10
		1	Data rate = LO = CLK/80
CR15	Data format	0	Scramble ARINC data
		1	Unscramble ARINC data

STATUS REGISTER

The device contains a 9-bit status register which can be interrogated to determine the status of the ARINC receivers, data FIFOs and transmitter. The contents of the status register are output on BD0 - BD08 when the /RSR pin is taken low and SEL = 0. Unused bits are output as zeros. The following table defines the status register bits.

Table 3: Status Register Bit Definition

SR Bit	FUNCTION	POL	DESCRIPTION
SR0	Data ready (Receiver 1)	0	Receiver 1 FIFO empty
		1	Receiver 1 FIFO contains valid data. Resets to zero when all data has been read. /DR1 pin is the inverse of this bit
SR1	FIFO half full (Receiver 1)	0	Receiver 1 FIFO holds less than 16 words
		1	Receiver 1 FIFO holds at least 16 words. /HF1 pin is the inverse of this bit
SR2	FIFO full (Receiver 1)	0	Receiver 1 FIFO not full
		1	Receiver 1 FIFO full. To avoid data loss, the FIFO must be read within one ARINC word period. /FF1 pin is the inverse of this bit.
SR3	Data ready (Receiver 2)	0	Receiver 2 FIFO empty
		1	Receiver 2 FIFO contains valid data. Resets to zero when all data has been read. /DR2 pin is the inverse of this bit
SR4	FIFO half full (Receiver 2)	0	Receiver 2 FIFO holds less than 16 words
		1	Receiver 2 FIFO holds at least 16 words. /HF2 pin is the inverse of this bit
SR5	FIFO full (Receiver 2)	0	Receiver 2 FIFO not full
		1	Receiver 2 FIFO full. To avoid data loss, the FIFO must be read within one ARINC word period. /FF2 pin is the inverse of this bit.
SR6	Transmitter FIFO empty	0	Transmitter FIFO not empty
		1	Transmitter FIFO empty
SR7	Transmitter FIFO full	0	Transmitter FIFO not full

SR Bit	FUNCTION	POL	DESCRIPTION
		1	Transmitter FIFO full. /FFT pin is the inverse of this bit
SR8	Transmitter FIFO half full	0	Transmitter FIFO contains less than 16 words
		1	Transmitter FIFO contains at least 16 words. /HFT pin is the inverse of this bit

DATA FORMAT

Control register bit CR15 is used to control how individual bits in the received or transmitted ARINC word are mapped to the data bus during data read or write operations. Table 4 describes this mapping:

Table 4: Parallel Data Bus Format, Scrambled & Not Scrambled

DATA BUS	ARINC BIT CR15 = 0		ARINC BIT CR15 = 1	
	WORD1	WORD2	WORD1	WORD2
BD00	8 Label	14	1 Label	17
BD01	7 Label	15	2 Label	18
BD02	6 Label	16	3 Label	19
BD03	5 Label	17	4 Label	20
BD04	4 Label	18	5 Label	21
BD05	3 Label	19	6 Label	22
BD06	2 Label	20	7 Label	23
BD07	1 Label	21	8 Label	24
BD08	32 Parity	22	9 SDI	25
BD09	30	23	10 SDI	26
BD10	31	24	11	27
BD11	9 SDI	25	12	28
BD12	10 SDI	26	13	29
BD13	11	27	14	30
BD14	12	28	15	31
BD15	13	29	16	32 Parity

BIT TIMING

The ARINC 429 characteristic describes the RX acceptance timing as follows.

	HIGH SPEED	LOW SPEED
BIT RATE	100 kbps ± 1%	12K to 14.4 kbps
RISE TIME	1.5 ± 0.5 µs	10 ± 5 µs
FALL TIME	1.5 ± 0.5 µs	10 ± 5 µs
PULSE WIDTH	5 µs ± 5%	34.5 to 41.7 µs

1. Key to the performance of timing checking logic is an accurate 1 MHZ clock source. Less than 0.1% tolerance is recommended.

2. The sampling shift registers are 10 bits long and must show three consecutive Ones, Zeros or Nulls to be considered valid data. Additionally, for data bits, the One or Zero in the upper bits of the sampling shift registers must be followed by a Null in the lower bits within the data bit time. For a Null in the word gap, three consecutive Nulls must be found in both the upper and lower bits of the sampling shift register. In this manner the minimum pulse width is guaranteed.

3. The Word Gap timer samples the Null shift register every 10 input clocks (80 for low speed) after the last data bit of a valid reception. If the Null is present, the Word Gap counter is incremented. A count of 3 will enable the next reception.

4. Each data bit must follow its predecessor by not less than 8 samples and no more than 12 samples. In this manner the bit rate is checked. With exactly 1 MHZ clock frequency, the acceptable data bit rates are as follows:

If the /NFD pin is HI, the device accepts signals that meet these specifications and rejects signals outside the tolerances. The way this is achieved is described below:

Bit Rate (kbps)	/NFD=HI		/NFD=LO
	LO Speed	HI Speed	
Bit Rate Min	10.4	83	0.1
Bit Rate Max	15.6	125	500

If /NFD pin is held low, frequency discrimination is disabled and any data stream totaling 32 bits is accepted even with gaps between bits. The protocol still requires a word gap as defined in 4 above.

RECEIVER PARITY

The receiver parity circuit counts Ones received, including the parity bit. If the result is odd, then "0" will appear in the 32nd bit.

RETRIEVING DATA

Once ARINC 32-bit word is recognized, the receiver logic check for correct decoding and label matching prior to loading the word into (or reject the word from) the 32 x 32 receiver FIFO. If CR2 or CR3 is/are ONE, then ARINC words with have matching labels

will be accepted into Receiver FIFO. If CR6 or CR9 is/are ONE, then ARINC words with matching decoder value (CR7, CR8 for RX1) and (CR10, CR11 for RX2) will be accepted into Receiver FIFO. The following table describes this operation:

Table 5: RX Data Filter Logic

CR2(3)	ARINC WORD MATCHES LABEL	CR6(9)	ARINC WORD BITS 9&10 MATCH CR7&8 (10&11)	FIFO
0	X	0	X	Load FIFO
1	No	0	X	Ignore data
1	Yes	0	X	Load FIFO
0	X	1	No	Ignore data
0	X	1	Yes	Load FIFO
1	Yes	1	No	Ignore data
1	No	1	Yes	Ignore data
1	No	1	No	Ignore data
1	Yes	1	Yes	Load FIFO

Once a valid ARINC word is loaded into the FIFO, the DATA READY FLAG will be turned on; /DR1 or /DR2 (or both) will go low. The data flag for a receiver will remain low until all ARINC words are retrieved and the Receiver FIFO is empty.

When data ready in Receiver FIFO, data can be retrieved by activating (/EN1, SEL) or (/EN2, SEL) to output the receiver data to the 16-bit parallel bus (see table 1). Example to retrieve Receiver 1 data, first set (SEL = 0, then /EN1 = 0) to place WORD1 on the 16-bit bus. Release the 16-bit bus with (/EN1 = 1). Next set (SEL =1, then /EN1 = 0) for WORD2. Last, release the 16-bit bus with (/EN1 = 1). Use (/EN2) for Receiver 2 data retrieval.

Up to 32 ARINC words may be loaded into each receiver's FIFO. The /FF1 (/FF2) pin will go low when the receiver 1 (2) FIFO is full. Failure to retrieve data from a full FIFO will cause the next valid ARINC word received to overwrite the existing data in FIFO location 32.

A FIFO half full flag /HF1 (/HF2) goes low if the FIFO contains 16 or more received ARINC words. The /HF1 (/HF2) pin is intended to act as an interrupt flag to the systems external microprocessor, allowing a 16-word data retrieval routine to be performed, without the user needing to continually poll the status register bits.

RECEIVERS

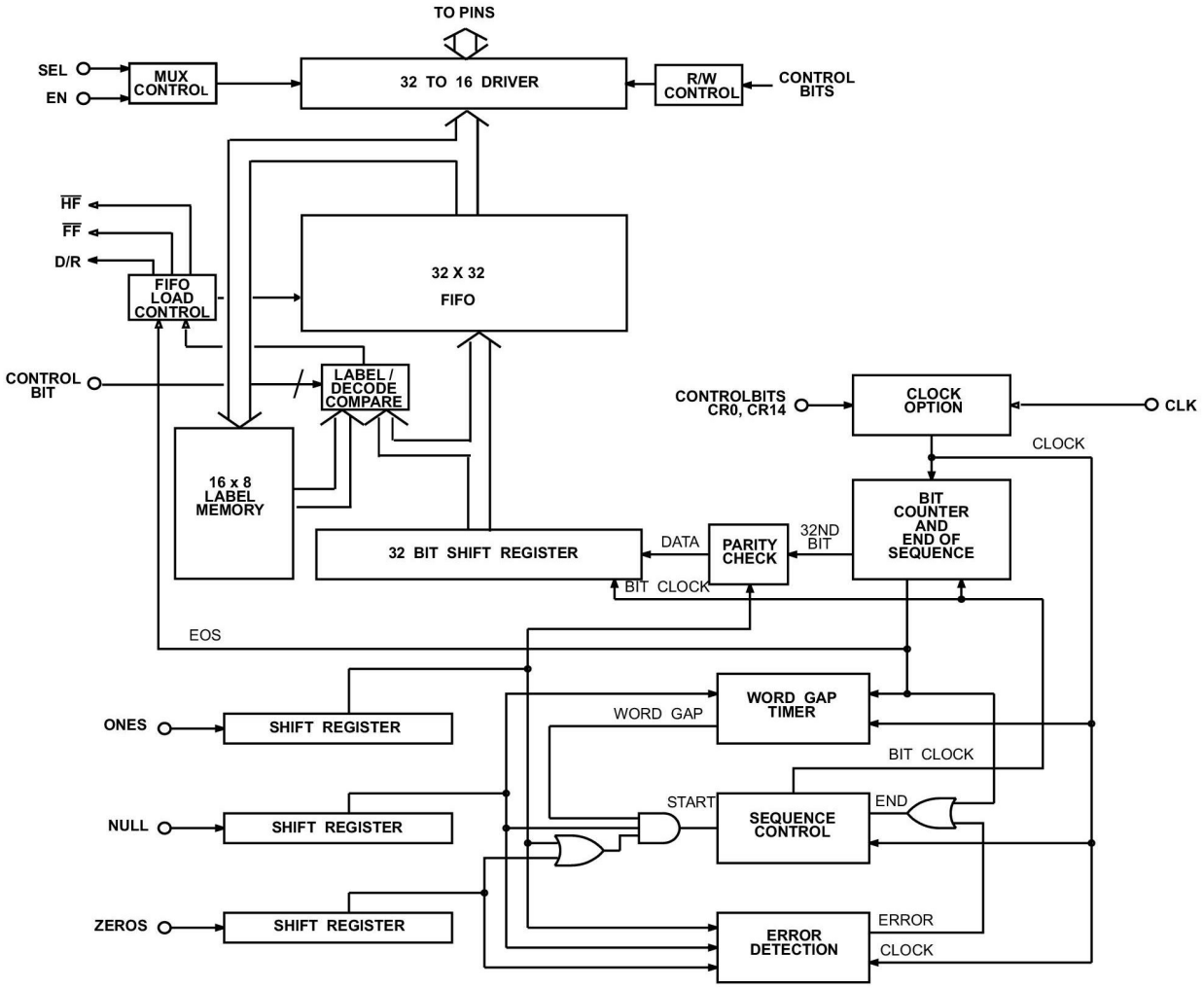


Figure 1 Receiver Function Diagram

LABEL RECOGNITION

The chip compares the incoming label to the stored labels if label recognition is enabled. If a match is found, the data is processed. If a match is not found, no indicators of receiving ARINC data are presented. Note that 00 (Hex) is treated in the same way as any other label value. Label bit significance is not changed by the status of control register bit CR15. Label bits BD00 – BD07 are always compared to receive ARINC bits 1- 8 respectively.

LOADING LABELS

When writing to, or reading from the label memory, SEL must be set HIGH. Write to control register with Enable Label Read/Write (set CR1 = 1) and Disable Label recognition (set CR2,3 = 0) during the label write sequence. Then the next 16 writes of data (/PL pulsed low) load the label data into each location of the label memory from the BD00 – BD07 pins. The /PL1 pin is used to write label data for receiver 1 and /PL2 for receiver 2. Always write to all 16 location of label memory to ensure that no previous unwanted label memory residual affect the label recognition. Note that ARINC word reception is suspended during the label memory write sequence. Therefore, CR1 of control register has to be written with zero before returning to normal operation.

READING LABELS

When writing to, or reading from the label memory, SEL must be set HIGH. Write to control register with Enable Label Read/Write (set CR1 = 1) and Disable Label recognition (set CR2,3 = 0) during the label read sequence. Then the next 16 data reads of the selected receiver (/EN taken low) are labels. /EN1 is used to read labels for receiver 1, and /EN2 to read labels for receiver 2. Label data is presented on BD00 – BD07. All 16 locations should be accessed, and CR1 must be written to zero before returning to normal operation.

TRANSMITTER

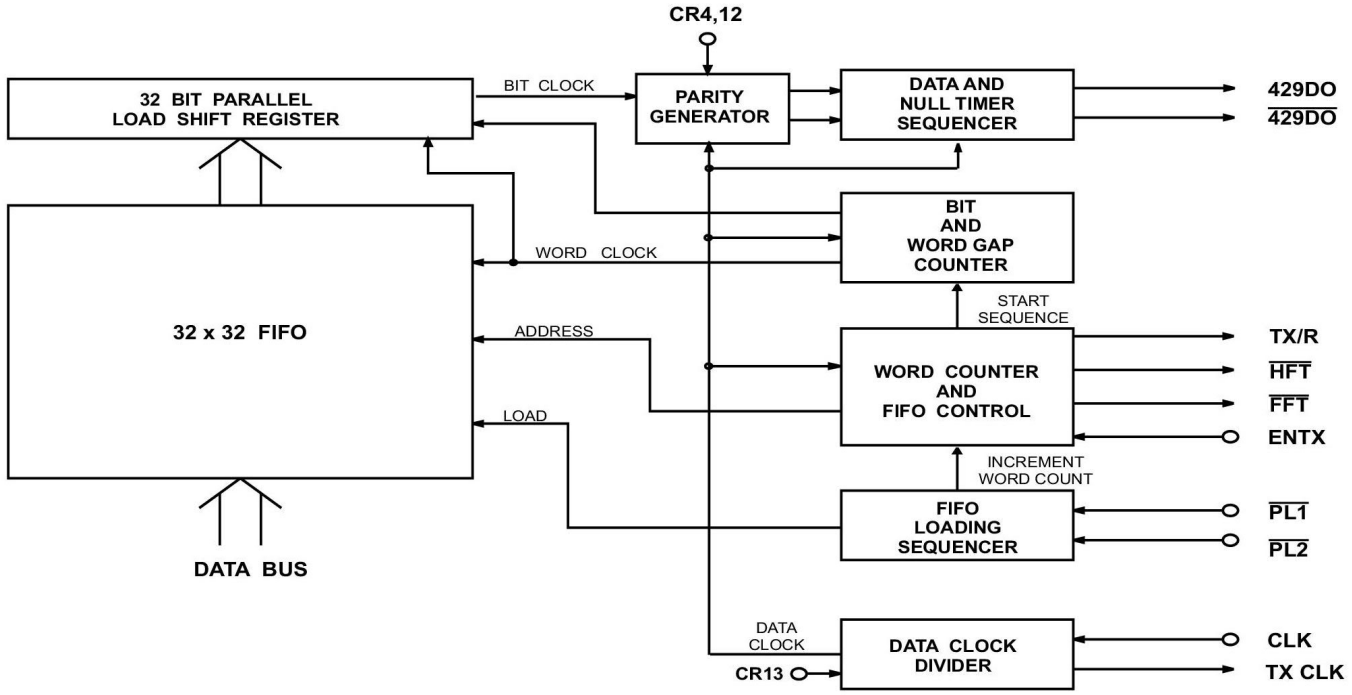


Figure 2 Transmitter Function Diagram

FIFO OPERATION

Prior to loading FIFO (TX Buffer), do these (sequence does not matter):

Hold ENTX at Low to stop enable transmission

Check if TX/R is low (which means TX Buffer is empty).

When the FIFO is empty and ENTX low, then proceed to load FIFO with /PL1 and /PL2.

Otherwise asserting /PL1 and /PL2 has not data loading effect to the FIFO.

The FIFO is loaded sequentially by first pulsing /PL1 to load byte 1 and then /PL2 to load byte 2. The control logic automatically loads the 31 bit word (or 32 bit word if CR4 = 0) in the next available position of the FIFO. If TX/R, the transmitter ready flag is high (FIFO empty), then up to 32 words, each 31 or 32 bits long, may be loaded. If TX/R is low, then only the available positions may be loaded. If all 32 positions are full, the /FFT flag is asserted and the FIFO ignores further attempts to load data.

A transmitter FIFO half-full flag /HFT is provided. When the transmit FIFO contains less than 16 words, /HFT is high, indicating to the system microprocessor that a 16 ARINC word block write sequence can be initiated.

In normal operation (CR4 = 1), the 32nd bit transmitted is a parity bit. Odd or even parity is selected by programming control register bit CR12 to a zero or one. If CR4 is programmed to a 0, the all 32 bits of data loaded into the transmitter FIFO are treated as data and are transmitted.

DATA TRANSMISSION

Set ENTX to high to enable transmission, the FIFO positions are incremented with the top register loading into the data transmission shift register. Within 2.5 data clocks the first data bit appears at 429DO and /429DO. The 32 bits in the data transmission shift register (or 31 bits plus parity bit) are presented sequentially to the outputs in the ARINC 429 format with the following timing:

	HI SPEED	LO SPEED
ARINC Data Bit Time	10 Clocks	80 Clocks
Data Bit Time	5 Clocks	40 Clocks
Null Bit Time	5 Clocks	40 Clocks
Word Gap Time	40 Clocks	320 Clocks

The word counter detects when all loaded positions have been transmitted and sets the transmitter ready flag, TX/R, high. Once the transmission start it will continue till the TX FIFO is empty. Setting ENTX to low at the mid point of transmission does not stop the transmission.

TRANSMITTER PARITY

The parity generator counts the Ones in the 31 bit word. If control register bit CR12 is set low, the 32nd bit transmitted will make parity odd. If the control bit is high, the parity is even. Setting CR4 to zero bypasses the parity generator and allows 32 bits of data to be transmitted.

MASTER RESET

On a Master Reset data transmission and reception are immediately terminated, all three FIFOs cleared as are the FIFO flags at the device pins and in the Status Register. The Control Register is not affected by a Master Reset.

SELF TEST

If control register bit CR5 is set low, the transmitter serial output data are internally connected to each of the two receivers, bypassing the analog interface circuitry. Data is passed unmodified to receiver 1 and inverted to receiver 2. The serial data from the transmitter is always present on the 429DO and /429DO outputs regardless of the state of CR5.

SYSTEM OPERATION

The two receivers are independent of the transmitter. Therefore, control of data exchanges is strictly at the option of the user. The only restrictions are:

1. The receive data will be overwritten if the receiver FIFO is full and at least one location is not retrieved before the next complete ARINC word is received.
2. The transmitter FIFO can store 32 words maximum and ignores attempts to load additional data if full.

REPEATER OPERATION

Repeater mode of operation allows a data word that has been received by the device to be placed directly into the transmitter FIFO. Repeater operation is like normal receiver operation. In normal operation, either byte of a received data word may be read from the receiver latches first by use of SEL input. During repeater operation however, the lower byte of the data word must be read first. This is necessary because, as the data is being read, it is also being loaded into transmitter FIFO which is always loaded with the lower byte of data word first. Signal flow for repeater operation is shown in the timing diagram section.

TIMING DIAGRAMS

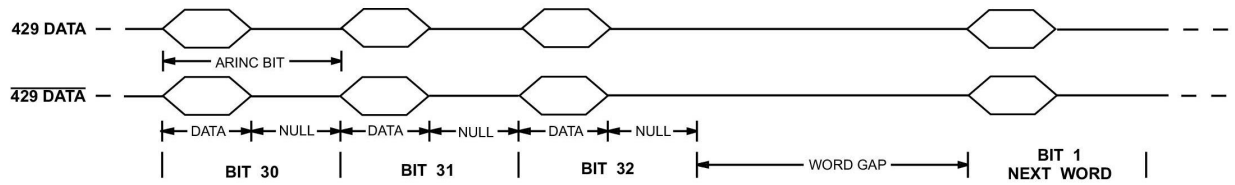


Figure 3 Data Rate Example

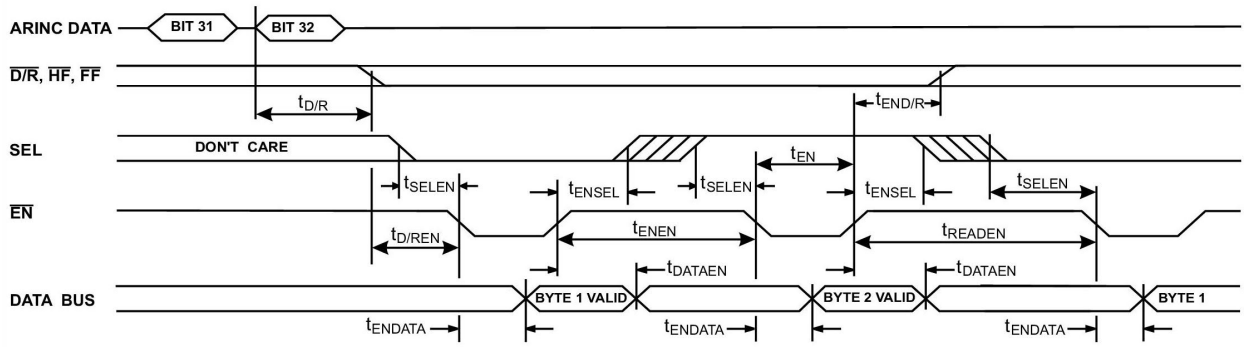


Figure 4 Receiver Operation

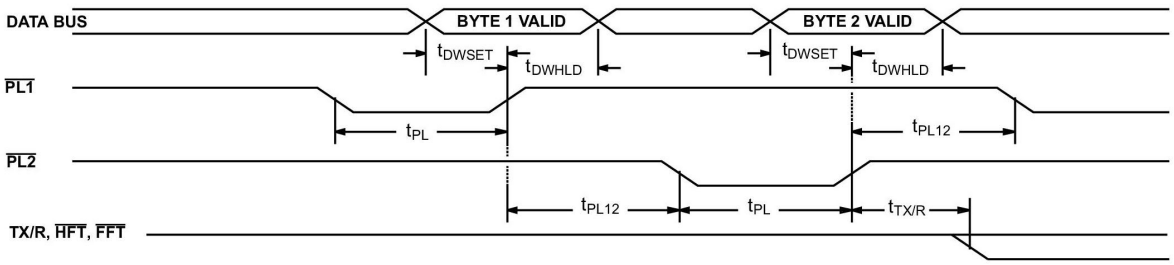


Figure 5 Transmitter Operation

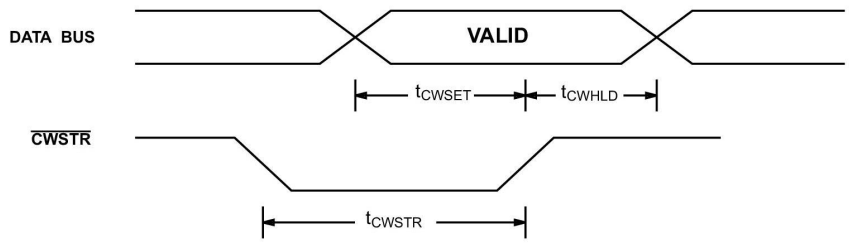


Figure 6 Load Control Word

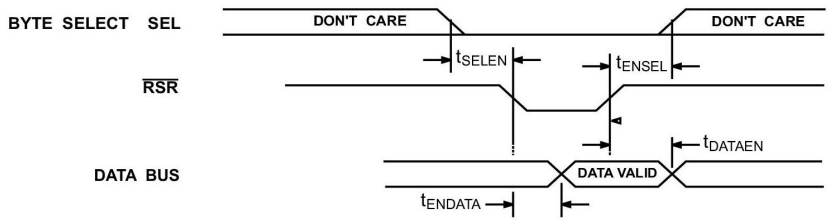


Figure 7 Status Register Read Cycle

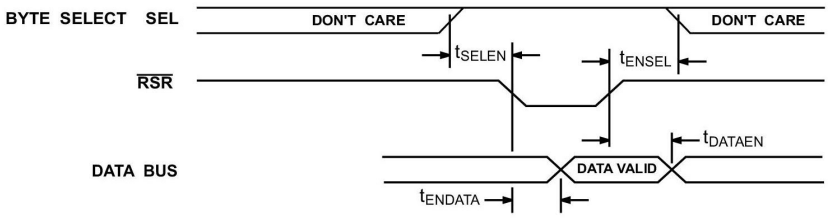


Figure 8 Control Register Read Cycle

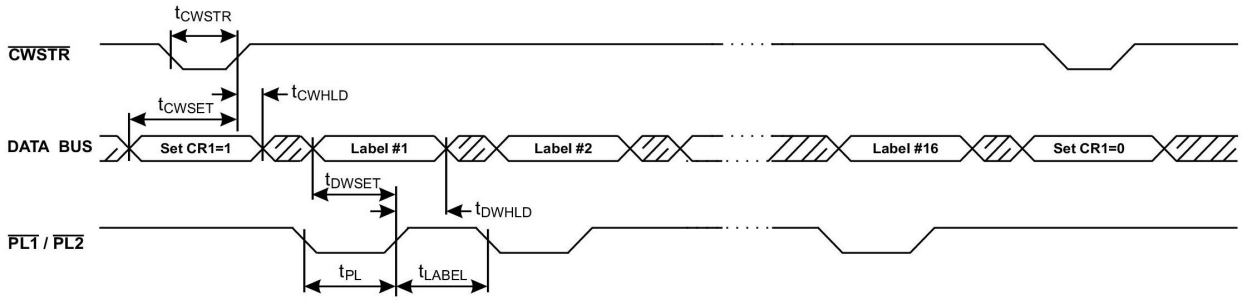


Figure 9 Label Memory Load Sequence

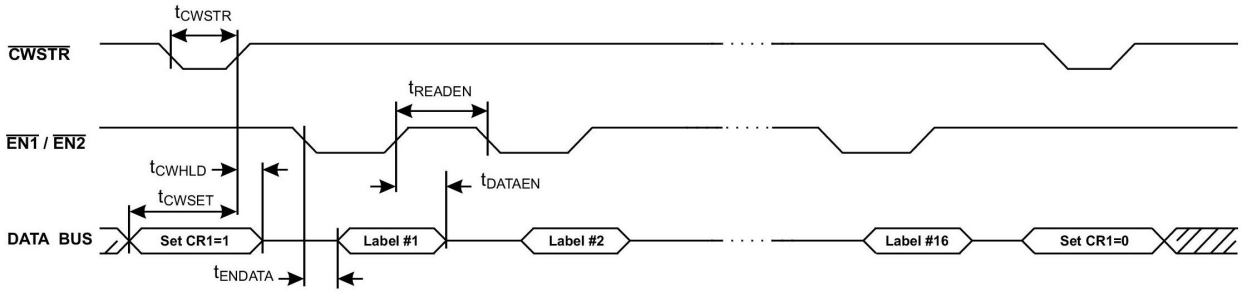


Figure 10 Label Memory Read Sequence

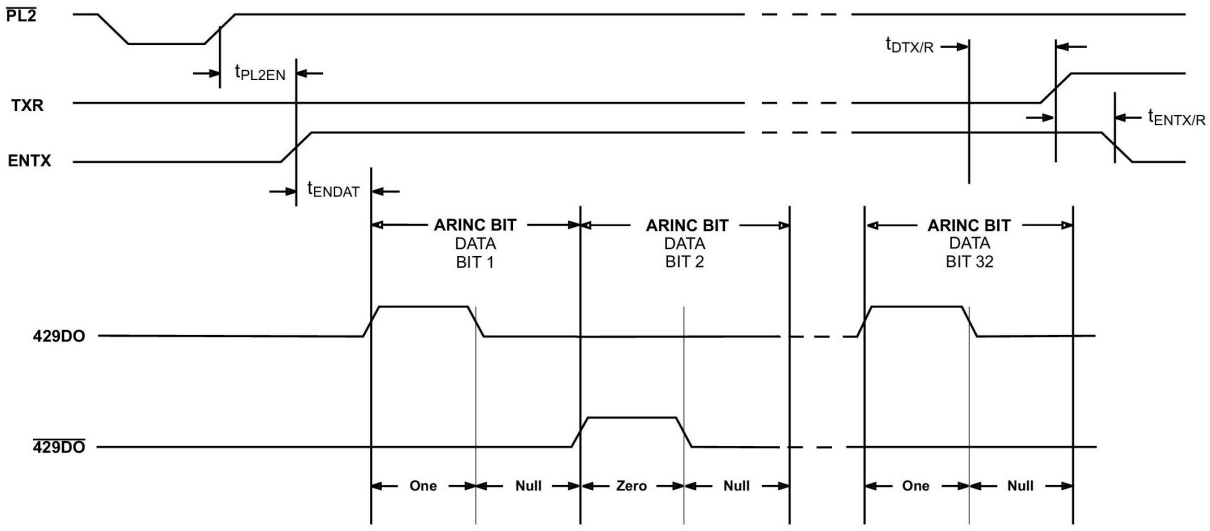


Figure 11 Transmitting Data

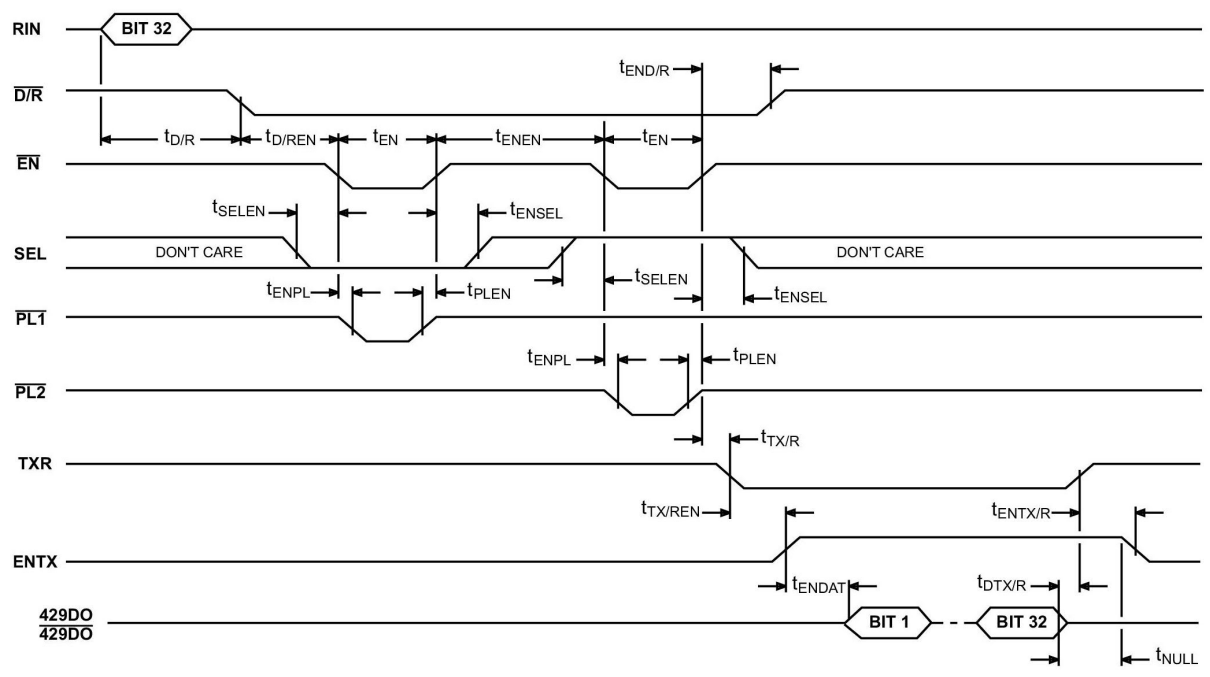


Figure 12 Repeater Operation

ELECTRICAL CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS

Table 6 Absolute Maximum Ratings

PARAMETER	SYMBOL	MIN	MAX	UNIT
Supply Voltage	VDD	-0.5	+7.0	V
DC Input Voltage, Logic inputs	VIN-logic	-0.6	VDD + 0.6	V
DC Input Voltage, RX pins: RIN[1A/1B/2A/2B] aka DI[1A/1B/2A/2B] RIN[1A/1B/2A/2B]E aka DI[1A/1B/2A/2B]E at external 10 kΩ series resistor	 VIN-rx VIN-rxe		 ±120 ±120	 V
Clamp diode current, any pin except RX inputs			±25	mA
DC Output Current per pin			±25	mA
DCV or GND current per pin			±50	mA
Storage Temperature	Tstg	-65	+150	°C
Junction Temperature, operating	TJmax		+145	°C
Notes: ESD protection is provided on all pins per 2KV HBM specification, except the receiver input pins. These will be limited to input resistor rupture voltage of ~1 kV.				

OPERATING CONDITIONS

Table 7 Operating Conditions

PARAMETER	SYMBOL	MIN	MAX	UNIT
Supply Voltage	VDD	3.0	5.5	V
Logic Input Voltage	VIH VIL	0.7*VDD -0.5	VDD+0.5 0.8	V
ARINC Input Voltage (Differential)	NULL ONE ZERO	-2.5 6.5 -13	2.5 13 -6.5	
Operating Temperature -xEx -xMx	Top	-55 -55	+85 +125	°C

DC CHARACTERISTICS

Table 8 DC Characteristics

Conditions: Ta = -55 to +125 °C, Vdd = 3.3 V ±10% and 5 V ±10%						
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
ARINC INPUTS: RIN[1A/1B/2A/2B] aka DI[1A/1B/2A/2B] or RIN[1A/1B/2A/2B] aka DI[1A/1B/2A/2B]E with external 10K Ohm resistors						
Differential Input Voltage ONE ZERO NULL	 Vil Vil Vnull		 6.5 -13 -2.5	 10 -10 0	 -13 -6.5 2.5	V
Common Mode Input Voltage	Vcm		-10		10	V
Input Resistance: Differential To GND To VDD	 RI RG RH		 24 12 12	 132 67 7500	 200 100	kΩ
Input Capacitance	CI				20	pF
LOGIC INPUTS						
Input Voltage HI	VIH	VDD = 3.0 V to 5.5 V	0.7*VDD		VDD+0.5	V
Input Voltage LO	VIL	VDD = 3.0 V to 5.5 V	-0.5		0.8	V
Input Pull-up Current, /NFD. /RSR pins	IPU			-100		µA
Input Currents, all others pins	IIN		-10		10	µA
LOGIC OUTPUTS						
Output Voltage: TTL Logic 1 Output Voltage: CMOS Logic 1 Output Voltage: TTL Logic 0 Output Voltage: CMOS Logic 0	VOH-T VOH-C VOL-T VOL-C	IOH = -4 mA IOH = -100 uA IOL = 4 mA IOL = 100 uA	VDD -0.5 VDD -0.1		 0.4 0.1	V
Output Capacitance:	Cout				10	pF
OPERATING SUPPLY CURRENT						
VDD = 3.3V or 5V	IDD	Fck = 1 MHZ		4* (VDD-2.7)	10	mA
Supply Voltage	VDD		3.0		5.5	V

TIMING CHARACTERISTICS

Table 9 General AC Characteristics

PARAMETER	SYMBOL	DATA RATE 100 kbps		DATA RATE 12.5 kbps		UNIT
		MIN	MAX	MIN	MAX	
1MCK Frequency	f1MCK	0.99	1.01	0.99	1.01	MHZ
1MCK Duty Cycle	CKDC	40	60	40	60	%
1MCK Rise/Fall Time	TCRF		10		10	ns
Transmitter Data Rate (1MCK = 1 MHZ)	TDR	99	101	12.4	12.6	kbps
Receiver Data Rate (1MCK = 1 MHZ) (DATA = 50% BIT/ 50% NULL TIME)	RDR	83.3	125	10.2	15.6	kbps
Receiver Data Rate w/ No Frequency Discrimination (/NFD=0)	/NFD	71.4	166	8.77	19.2	kbps

Table 10 3.3VDD AC Characteristics

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
CONTROL WORD TIMING					
Pulse Width: /CWSTR Setup: DATA BUS Valid to /CWSTR Hi Hold: /CWSTR Hi to DATA BUS Hi-Z	t_{CWSTR} t_{CWSET} t_{CWHLD}	80 60 40			ns
RECEIVER FIFO AND LABEL READ TIMING					
Delay: Start ARINC 32nd bit to /DR Lo: High Speed Low Speed	 $t_{D/R}$ $t_{D/R}$			 16 128	µs
Delay: /DR Lo to /EN Lo Delay: /EN Hi to /DR Hi	$t_{D/REN}$ $t_{END/R}$	0	 60	 150	ns
Setup: SEL to /EN Lo Hold: SEL to /EN Hi	t_{SELEN} t_{ENSEL}	20 20			ns
Delay: /EN Lo to DATA BUS Valid Delay: /EN Hi to DATA BUS Hi-Z	t_{ENDATA} t_{DATAEN}		80	140 100	ns
Pulse Width: /EN1 or /EN2 Spacing: /EN Hi to next /EN Lo (Same Word) Spacing: /EN Hi to next /EN Lo (Next Word)	t_{EN} t_{ENEN} t_{READEN}	120 140 1033			ns
TRANSMITTER FIFO AND LABEL WRITE TIMING					
Pulse Width: /PL1 or /PL2	t_{PL}	80			ns
Setup: DATA BUS Valid to/PL Hi Hold: /PL Hi to DATA BUS Hi-Z	t_{DWSET} t_{DWHLD}	60 40			ns
Spacing: /PL1 to /PL2 Spacing between Label Write pulses	t_{PL12} t_{LABEL}	40 60			ns
Delay: /PL2 Hi to TX/R Lo	$t_{TX/R}$			100	ns
TRANSMISSION TIMING					
Spacing: /PL2 Hi to ENTX Hi	t_{PL2EN}	0			ns
Delay: 32nd ARINC Bit to TX/R Hi	$t_{DTX/R}$			50	ns
Spacing: TX/R Hi to ENTX Lo	$t_{ENTX/R}$	0			ns
REPEATER OPERATION TIMING					
Delay: /EN Lo to /PL Lo	t_{ENPL}	0			ns
Hold: /PL Hi to /EN Hi	t_{PLEN}	0			ns

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
Delay: TX/R Lo to ENTX Hi	$t_{TX/REN}$	0			ns
MASTER RESET PULSE WIDTH	t_{MR}	80			ns
ARINC DATA RATE AND BIT TIMING				± 1	%

Table 11 5VDD AC Characteristics

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
CONTROL WORD TIMING					
Pulse Width: /CWSTR	t_{CWSTR}	80			ns
Setup: DATA BUS Valid to /CWSTR Hi	t_{CWSET}	60			
Hold /CWSTR Hi to DATA BUS Hi-Z	t_{CWHLD}	40			
RECEIVER FIFO AND LABEL READ TIMING					
Delay: Start ARINC 32nd bit to /DR Lo:					µs
High Speed	$t_{D/R}$			16	
Low Speed	$t_{D/R}$			128	
Delay: /DR Lo to /EN Lo	$t_{D/REN}$	0			ns
Delay: /EN Hi to /DR Hi	$t_{END/R}$		20	100	
Setup: SEL to /EN Lo	t_{SELEN}	20			ns
Hold: SEL to /EN Hi	t_{ENSEL}	20			
Delay: /EN Lo to DATA BUS Valid	t_{ENDATA}		80	140	ns
Delay: /EN Hi to DATA BUS Hi-Z	t_{DATAEN}			100	
Pulse Width: /EN1 or /EN2	t_{EN}	120			ns
Spacing: /EN Hi to next /EN Lo (Same Word)	t_{ENEN}	140			
Spacing: /EN Hi to next /EN Lo (Next Word)	t_{READEN}	1033			
TRANSMITTER FIFO AND LABEL WRITE TIMING					
Pulse Width: /PL1 or /PL2	t_{PL}	80			ns
Setup: DATA BUS Valid to/PL Hi	t_{DWSET}	60			ns
Hold: /PL Hi to DATA BUS Hi-Z	t_{DWHLD}	40			
Spacing: /PL1 to /PL2	t_{PL12}	40			ns
Spacing between Label Write pulses	t_{LABEL}	60			
Delay: /PL2 Hi to TX/R Lo	$t_{TX/R}$			100	ns
TRANSMISSION TIMING					
Spacing: /PL2 Hi to ENTX Hi	t_{PL2EN}	0			ns
Delay: 32nd ARINC Bit to TX/R Hi	$t_{DTX/R}$			50	ns
Spacing: TX/R Hi to ENTX Lo	$t_{ENTX/R}$	0			ns
REPEATER OPERATION TIMING					
Delay: /EN Lo to /PL Lo	t_{ENPL}	0			ns
Hold: /PL Hi to /EN Hi	t_{PLEN}	0			ns
Delay: TX/R Lo to ENTX Hi	$t_{TX/REN}$	0			ns
MASTER RESET PULSE WIDTH	t_{MR}	50			ns
ARINC DATA RATE AND BIT TIMING				± 1	%

PACKAGE DESCRIPTION

Table 12 Package Characteristics

PACKAGE TYPE	PACKAGE REF	THERMAL RESIST. θ_{JC} / θ_{JA} (°C/W)	JEDEC MOISTURE SENSITIVITY LEVEL & PEAK BODY TEMP	LEAD FINISH MATERIAL / JEDEC Pb-FREE DESIGNATION	Pb FREE DESIGNATION	JEDEC MO
52L METRIC QUAD FLAT PACK	52L MQFP G	21 / 65	MSL 3 260 ºC	Matte Sn e3	RoHS Compliant	MS-022-AC
52L CERAMIC QUAD FLAT J-LEAD	52 CQFJ	TBD	HERMETIC	Au e4	Pb Free solder terminals	
64L 9X9 MICRO LEAD PACK QUAD	64 9X9 MLPQ G	10 / 30	MSL 3 260 ºC	Matte Sn e3	RoHS Compliant	MO-220-VMMD

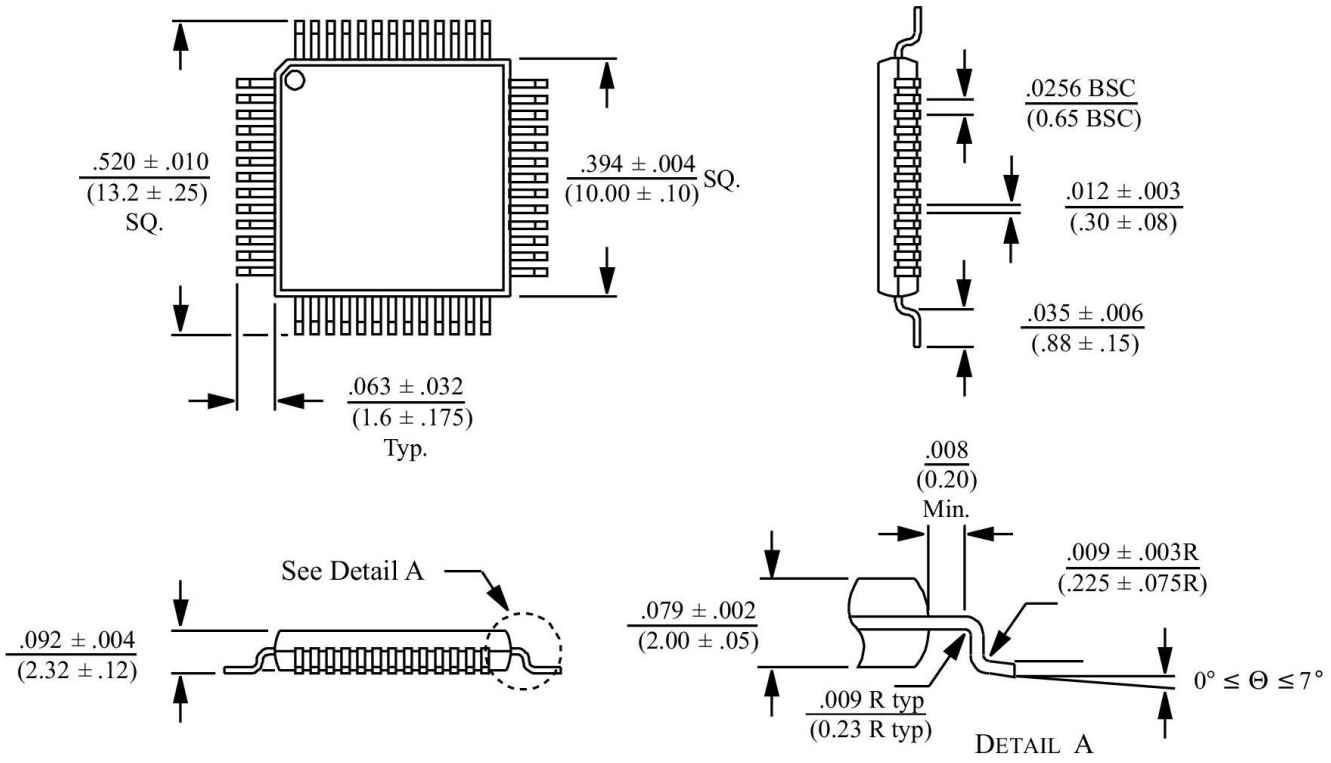


Figure 13 52L MQFP G

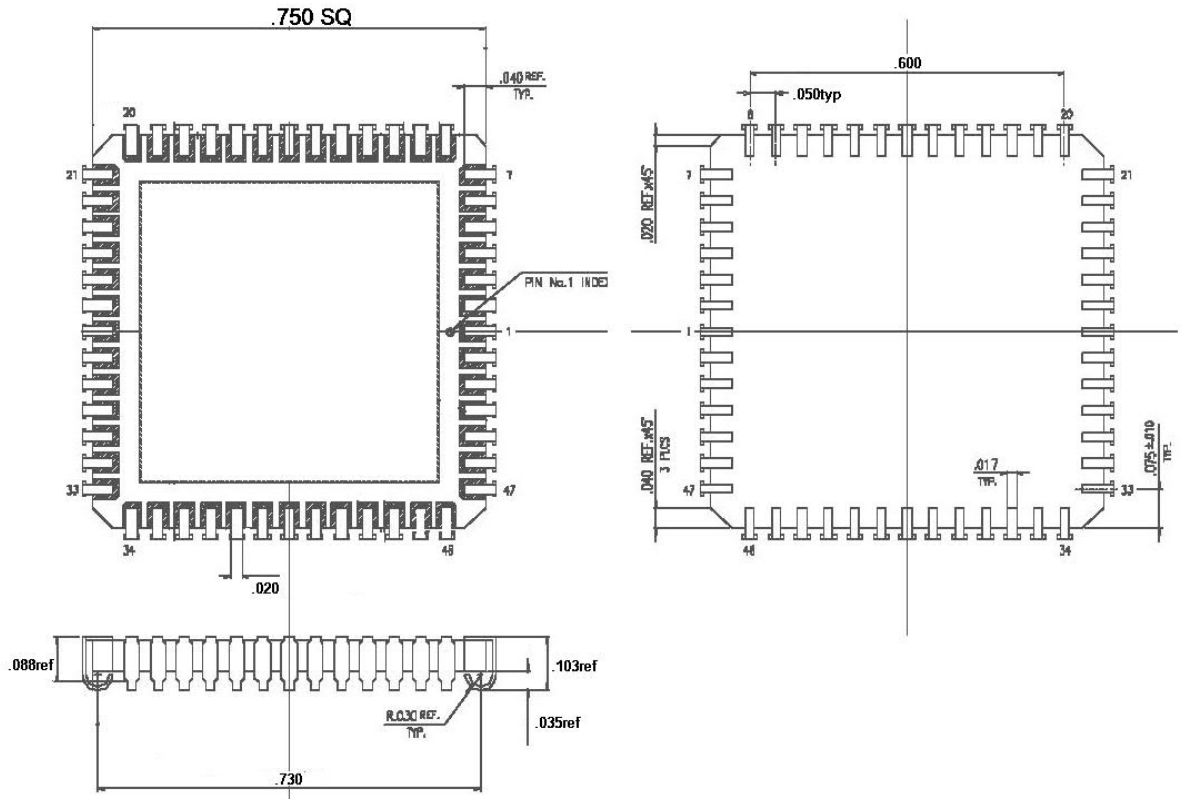
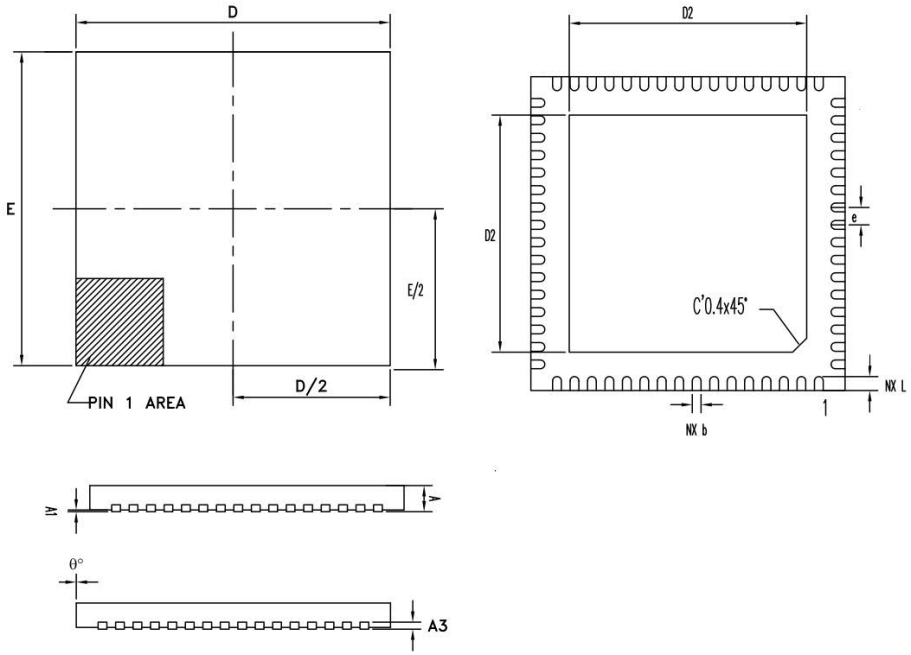


Figure 14 52L CQFJ



JEDEC#	MO-220I/WMMD			
TYPE	64 LEAD			
Dimension	mm		mils	
SYMBOL	Min	Max	Min	Max
A	0.85	0.95	33.46	37.40
A1	0	0.05	0	1.97
A3	0.175	0.225	6.89	8.86
D	8.9	9.1	350.39	358.27
E	8.9	9.1	350.39	358.27
D2	6.75	6.85	265.75	269.69
E2	6.75	6.85	265.75	269.69
e	0.5 BSC		19.69 BSC	
NX b	0.20	0.30	7.87	11.81
NX L	0.35	0.45	13.78	17.72
θ°	0°	4°	0°	4°
ND	16			
NE	16			

NOTE: The heat sink on bottom of package must be left floating or connected to GND. Do NOT connect to VDD.

Figure 15 64L 9x9 MLPQ G

ORDERING INFORMATION

Table 13 Ordering Information

PART NUMBER	MARK	PACKAGE	BURN IN	10 kΩ RESISTOR	TEMPERATURE
DEI1084-QES-G	DEI1084-QES	52L MQFP G	No	internal	-55 / +85 °C
DEI1084-QMS-G	DEI1084-QMS	52L MQFP G	No	internal	-55 / +125 °C
DEI1084-MES-G	DEI1084-MES	64L MLPQ G	No	internal	-55 / +85 °C
DEI1084-UMS	DEI1084-UMS	52L CQFJ	No	internal	-55 / +125 °C
DEI1085-QES-G	DEI1085-QES	52L MQFP G	No	external	-55 / +85 °C
DEI1085-QMS-G	DEI1085-QMS	52L MQFP G	No	external	-55 / +125 °C
DEI1085-MES-G	DEI1085-MES	64L MLPQ G	No	external	-55 / +85 °C
DEI1085-UMS	DEI1085-UMS	52L CQFJ	No	external	-55 / +125 °C
DEI2084-MES-G	DEI2084-MES	64L MLPQ G	No	internal	-55 / +85 °C
DEI2085-MES-G	DEI2085-MES	64L MLPQ G	No	external	-55 / +85 °C
DEI2084-MMS-G	DEI2084-MMS	64L MLPQ G	No	internal	-55 / +125 °C
DEI2085-MMS-G	DEI2085-MMS	64L MLPQ G	No	external	-55 / +125 °C