Device
Engineering
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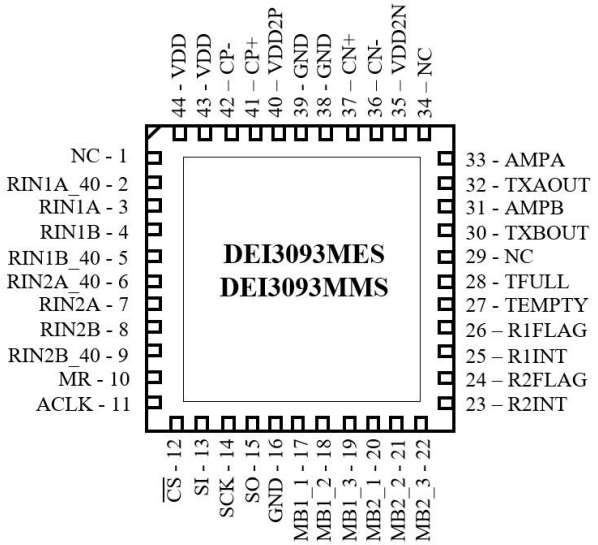
DEI3093

ARINC 429 Tranceiver with 2RX + 1TX, SPI Interface and single 3.3V supply

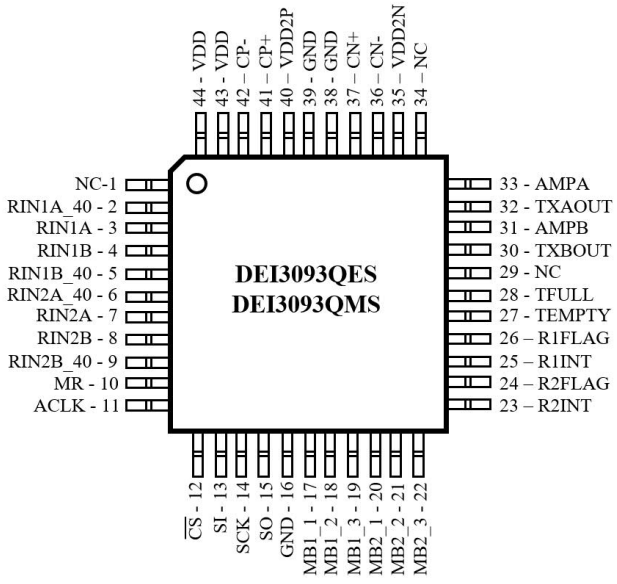
FEATURES

- **ARINC 429 Transceiver with SPI interface to host and single 3.3V supply**
- **TX includes:**
  - **ARINC 429 Line Driver**
  - **32 word FIFO**
- **Dual RXs include:**
  - **ARINC 429 Line Receiver with lighting protection**
  - **32 word FIFO**
  - **Label filter for any label combination**
  - **Three priority label registers**
- **10 MHz Serial Peripheral Interface (SPI) for control/status and data IO**
- **On-chip DC/DC converter for ARINC 429 voltages**
- **Package:**
  - **44L QFN 7x7mm**
  - **44L PQFP 10 x10mm body**
- **Temperature range:**
  - **-55 to +85°C**
  - **-55 to +125°C**

PIN ASSIGNMENTS



44L QFN (top view)



44L PQFP (top view)

GENERAL DESCRIPTION

The DEI3093 is an ARINC 429 transceiver (2RX/1TX) CMOS integrated circuit. It provides the interface between an ARINC 429 avionics data bus and a Serial Peripheral Interface (SPI) enabled host such as a microcontroller or ASIC. The four SPI control/data signals are CMOS/TTL compatible. The IC operates from a single 3.3V power supply.

The ARINC 429 interface comprises two receivers and one transmitter. Each receiver offers user-programmable label recognition for up to 256 possible labels, a 32 x 32 Receive FIFO, three Priority Label quick-access single-buffered registers and an on-chip analog line receiver. The RX inputs in conjunction with external 40KΩ resistors are tolerant of DO160 Level 3 pin injection stress. Figure 1 shows a detailed block diagram of the device.

The transmitter offers a 32 x 32 Transmit FIFO and built-in line driver. The line driver operates from a single 3.3V supply and includes an on-chip DC/DC converter to generate the voltage levels needed to drive the ARINC 429 bus directly. The output resistor options provide flexibility in applying TVS lighting protection of the line driver.

The SPI interface provides access to the on-chip control/status and data registers. The control registers configure the application options of the transmitter, receivers, RX filters, RX priority registers, clock divider and the flag/interrupt outputs. Status registers indicate the state of the FIFOs (RX and TX) and RX priority registers. The RX and TX status may be monitored via programmable interrupt and status pins and/or by polling status registers via the SPI interface. Table 1 below provides a complete list of pin number functional description along with the pin numbers. Pins 1, 29, and 34 are non-connected (NC) pins.

PIN FUNCTION DESCRIPTIONS

Table 1 Pin Function Description

SIGNAL	FUNCTION	DESCRIPTION	PULL UP / DOWN	PIN #
RIN1A-40	INPUT	Alternate ARINC receiver 1 positive input. Requires external 40KΩ resistor		2
RIN1A	INPUT	ARINC receiver 1 positive input. Direct connection to ARINC 429 bus		3
RIN1B	INPUT	ARINC receiver 1 negative input. Direct connection to ARINC 429 bus		4
RIN1B-40	INPUT	Alternate ARINC receiver 1 negative input. Requires external 40KΩ resistor		5
RIN2A-40	INPUT	Alternate ARINC receiver 2 positive input. Requires external 40KΩ resistor		6
RIN2A	INPUT	ARINC receiver 2 positive input. Direct connection to ARINC 429 bus		7
RIN2B	INPUT	ARINC receiver 2 negative input. Direct connection to ARINC 429 bus		8
RIN2B-40	INPUT	Alternate ARINC receiver 2 negative input. Requires external 40KΩ resistor		9
MR	INPUT	Master Reset. A positive pulse clears Receive and Transmit data FIFOs and flags	50KΩ pull-down	10
ACLK	INPUT	Master timing source for the ARINC 429 receiver and transmitter	50KΩ pull-down	11
$\overline{CS}$	INPUT	Chip Select. Data is shifted into SI and out of SO when $\overline{CS}$ is low.	50KΩ pull-up	12
SI	INPUT	SPI interface serial data input	50KΩ pull-down	13
SCK	INPUT	SPI Clock. Data is shifted into or out of the SPI interface using SCK	50KΩ pull-down	14
SO	OUTPUT	SPI interface serial data output		15
GND	POWER	Chip 0V supply		16, 38, 39
MB1_1	OUTPUT	Goes high when Receiver 1, Priority Label Mail Box 1 contains a message		17
MB1_2	OUTPUT	Goes high when Receiver 1, Priority Label Mail Box 2 contains a message		18
MB1_3	OUTPUT	Goes high when Receiver 1, Priority Label Mail Box 3 contains a message		19
MB2_1	OUTPUT	Goes high when Receiver 2, Priority Label Mail Box 1 contains a message		20
MB2_2	OUTPUT	Goes high when Receiver 2, Priority Label Mail Box 2 contains a message		21
MB2_3	OUTPUT	Goes high when Receiver 2, Priority Label Mail Box 3 contains a message		22
R2INT	OUTPUT	Receiver 2 programmable Interrupt pin		23
R2FLAG	OUTPUT	Goes high as defined by Flag / Interrupt Assignment Register		24
R1INT	OUTPUT	Receiver 1 programmable Interrupt pin		25
R1FLAG	OUTPUT	Goes high as defined by Flag / Interrupt Assignment Register		26
TEMPTY	OUTPUT	Goes high when the Transmit FIFO is empty		27
TFULL	OUTPUT	Goes high when the Transmit FIFO contains the maximum 32 ARINC 429 words		28
TXBOUT	OUTPUT	ARINC line driver negative output. Direct connection to ARINC 429 bus		30
AMPB	OUTPUT	Alternate ARINC line driver negative output. Requires external 32.5Ω resistor		31
TXAOUT	OUTPUT	ARINC line driver positive output. Direct connection to ARINC 429 bus		32
AMPA	OUTPUT	Alternate ARINC line driver positive output. Requires external 32.5Ω resistor		33
VDD2N	CONVERTER	DC/DC negative voltage output		35
CN-	CONVERTER	DC/DC converter fly capacitor for VDD2N		36
CN+	CONVERTER	DC/DC converter fly capacitor for VDD2N		37
VDD2P	CONVERTER	DC/DC positive voltage output		40
CP-	CONVERTER	DC/DC converter fly capacitor for VDD2P		41
CP+	CONVERTER	DC/DC converter fly capacitor for VDD2P		42
VDD	POWER	Chip 3.3V supply		43, 44

FUNCTION DIAGRAM

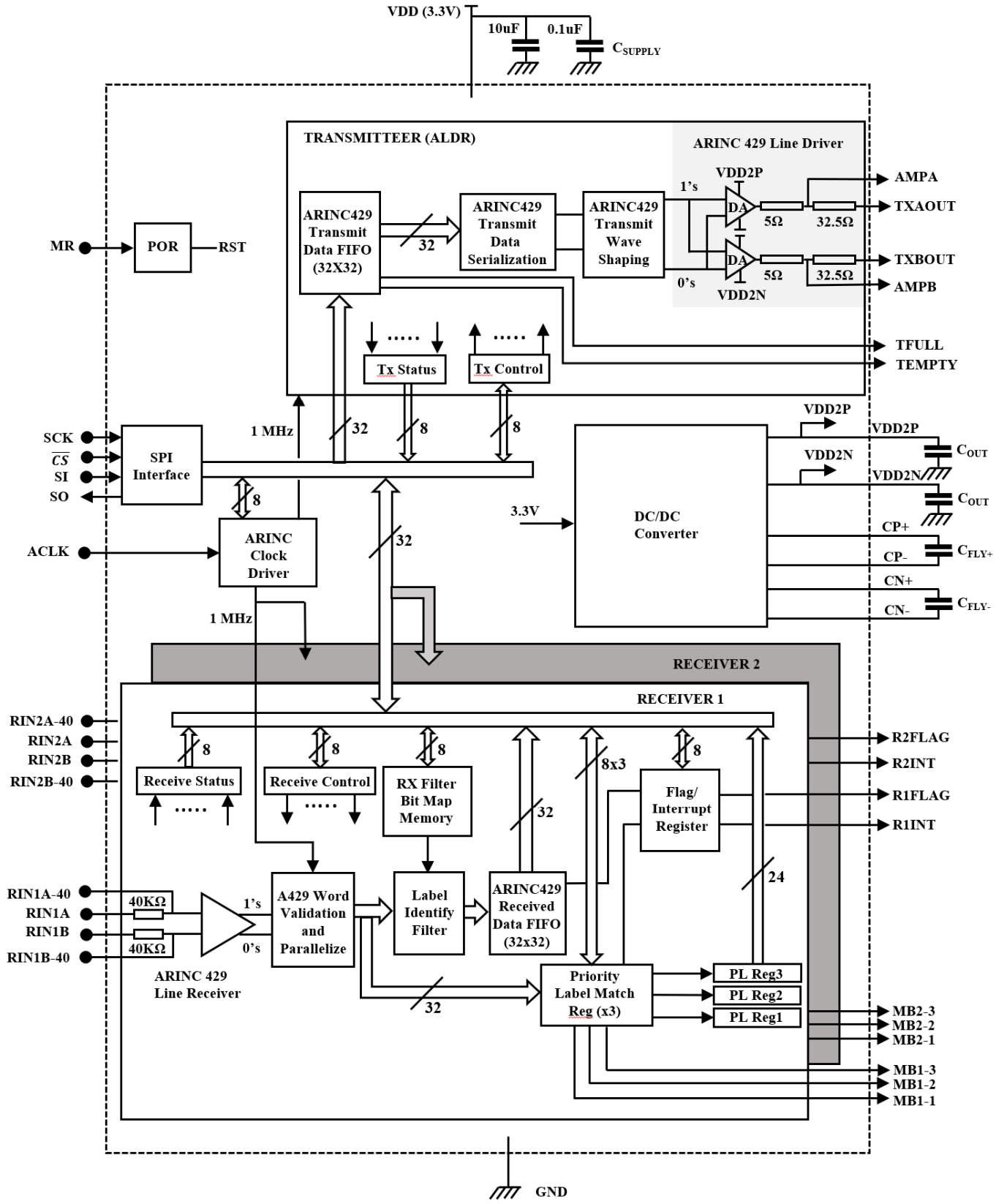


Figure 1 Function Diagram

SPI INSTRUCTION FORMAT AND DATA PROTOCOLS

The DEI3093 Serial Peripheral Interface (SPI) provides host access to internal registers and data FIFOs. A system with single MASTER HOST connected to multiple DEI3093 as slaves can be implemented with multiple Chip Select ($\overline{CS}$) lines. The other lines can be shared among master and slaves. The shared lines are Serial Clock (SCK), Serial Data Input (SI) and Serial Data Output (SO). A daisy chain loop SPI slave system will not work for DEI3093. Figure 2 is showing the interconnects to $\overline{CS}$ needed for multi-slave use.

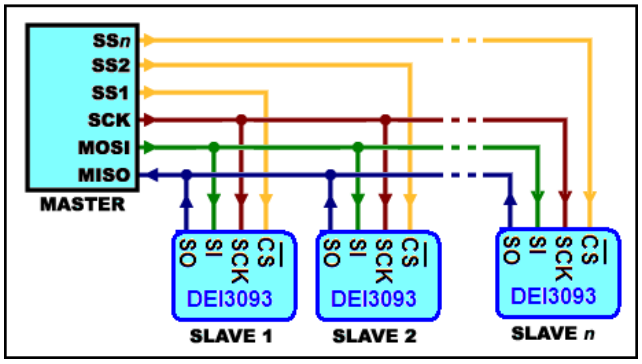


Figure 2 SPI multi-slave example

The DEI3093 operates in SPI mode 0 where input data for each device (master and slave) is clocked on the rising edge of SCK, and output data for each device changes on the falling edge (CPHA = 1, CPOL = 0). The DEI3093 SPI can be clocked at up to 10MHz.

The DEI3093 SPI format is "big endian" where the most significant bit of the data word is transferred first. Figure 3 shows the format of the SPI instruction byte.

SPI operations begin with the host asserting $\overline{CS}$ followed by writing (shifting into SI) a one byte Op-Code. Then depending on the Op-Code Write or Read functions, write or read data (shift into SI pin or out from SO pin) by clocking SCK for 8 cycles per byte of the operation's byte count. Refer to Table 2: "SPI Instruction Definition" for the required number of bytes. Release $\overline{CS}$ after each instruction. Do not chain multiple instructions into single assertions of $\overline{CS}$.

The DEI3093 SPI interface operates in HALF-DUPLEX mode, which means data travels one direction at a time. Figure 4 and Figure 5 show the sequence of $\overline{CS}$, SCK, SI and SO of the DEI3093.

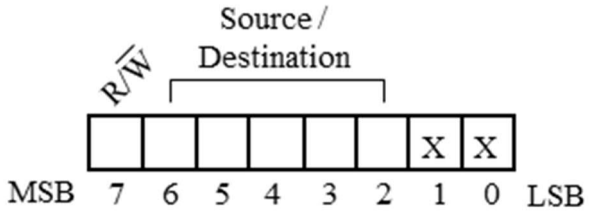
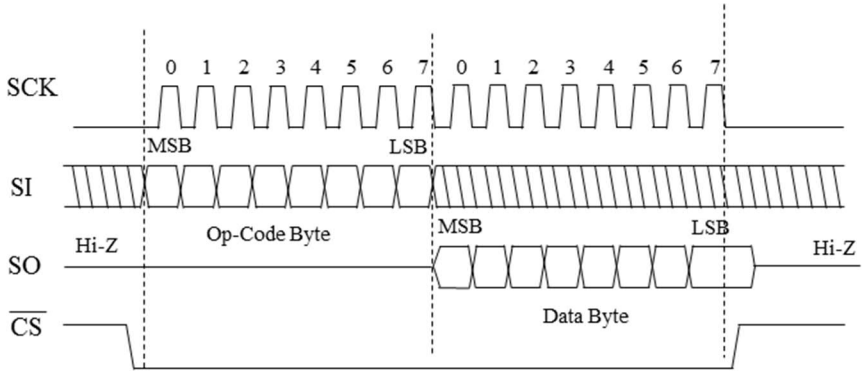


Figure 3 SPI Instruction Format

SPI Instructions are of a common format. The first bit of the Command Byte (Op-Code) specifies whether the instruction is a write "0" or read "1" transfer. The next five bits (6th to 2nd bits) specify the source or destination of the associated data byte(s), and the least significant two bits of the command byte are "don't care". These bit values are not decoded.



Host may continue to assert $\overline{CS}$ here to read or write sequential word(s) when allowed by the instruction. Each word needs 8 SCK clocks.

Figure 4 SPI RD single-byte protocol

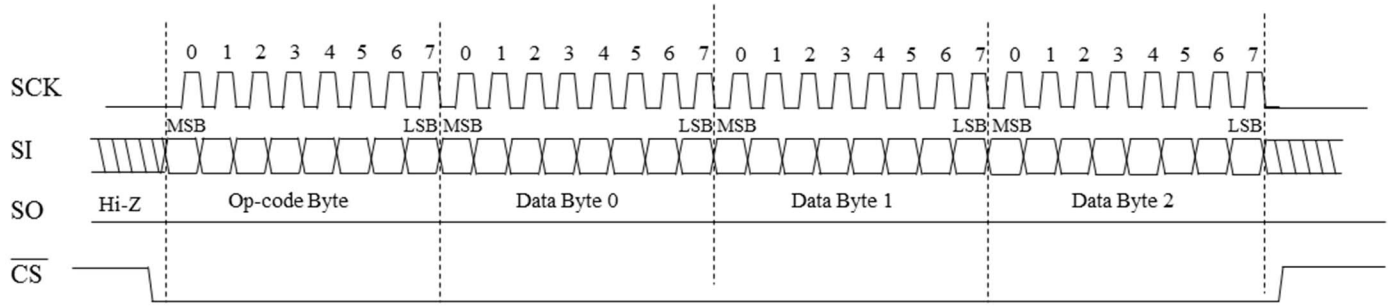


Figure 5 SPI Write 3-byte protocol

SPI INSTRUCTION DEFINITIONS

Table 2 SPI Instruction Definition

Op-Code	NAME	R/W	Bytes	DESCRIPTION
0x04	MRST	W	0	Software controlled Master Reset
0x08	WTCR	W	1	Write Transmit Control Register
0x0C	WTFF	W	4	Write ARINC 429 message to Transmit FIFO
0x10	W1CR	W	1	Write Receiver 1 Control Register
0x14	W1LM	W	32	Write label values to Receiver 1 label memory
0x18	W1PL	W	3	Write Receiver 1 Priority Label Match Registers. The data field consists of three eight-bit labels
0x24	W2CR	W	1	Write Receiver 2 Control Register
0x28	W2LM	W	32	Write label values to Receiver 2 label memory
0x2C	W2PL	W	3	Write Receiver 2 Priority Label Match Registers. The data field consists of three eight-bit labels
0x34	WFIAR	W	1	Write Flag / Interrupt Assignment Register
0x38	WACL	W	1	Write ACLK Division Register
0x40	ENT	W	0	Transmit current contents of Transmit FIFO if Transmit Control Register bit 5 (TMODE) is a “0”
0x44	SRST	W	0	Software Reset. Clears the Transmit and Receive FIFOs and the Priority Label Registers
0x48	LM1AL	W	0	Set all bits in Receiver 1 label memory to a “1”
0x4C	LM2AL	W	0	Set all bits in Receiver 2 label memory to a “1”
0x80	RTST	R	1	Read Transmit Status Register
0x84	RTCR	R	1	Read Transmit Control Register
0x90	R1ST	R	1	Read Receiver 1 Status Register
0x94	R1CR	R	1	Read Receiver 1 Control Register
0x98	R1LM	R	32	Read label values from Receiver 1 label memory
0x9C	R1PL	R	3	Read Receiver 1 Priority Label Match Registers
0xA0	R1FF	R	4	Read one ARINC 429 message from the Receiver 1 FIFO
0xA4	R1MB1	R	3	Read Receiver 1 Priority Label Register #1, ARINC 429 bytes 2, 3 & 4 (bits 9 - 32)
0xA8	R1MB2	R	3	Read Receiver 1 Priority Label Register #2, ARINC 429 bytes 2, 3 & 4 (bits 9 - 32)
0xAC	R1MB3	R	3	Read Receiver 1 Priority Label Register #3, ARINC 429 bytes 2, 3 & 4 (bits 9 - 32)
0xB0	R2ST	R	1	Read Receiver 2 Status Register
0xB4	R2CR	R	1	Read Receiver 2 Control Register
0xB8	R2LM	R	32	Read label values from Receiver 2 label memory
0xBC	R2PL	R	3	Read Receiver 2 Priority Label Match Registers
0xC0	R2FF	R	4	Read one ARINC 429 message from the Receiver 2 FIFO
0xC4	R2MB1	R	3	Read Receiver 2 Priority Label Register #1, ARINC 429 bytes 2, 3 & 4 (bits 9 - 32)
0xC8	R2MB2	R	3	Read Receiver 2 Priority Label Register #2, ARINC 429 bytes 2, 3 & 4 (bits 9 - 32)
0xCC	R2MB3	R	3	Read Receiver 2 Priority Label Register #3, ARINC 429 bytes 2, 3 & 4 (bits 9 - 32)
0xD0	RFIAR	R	1	Read Flag / Interrupt Assignment Register
0xD4	RACLK	R	1	Read ACLK Division Register

SPI AND ARINC 429 BUS MESSAGE FORMAT

ARINC 429 messages consist of a 32-bit sequence as shown below. The first eight bits that appear on the ARINC 429 bus are the label byte. The next twenty three bits comprise a data field which presents data in a variety of formats defined in the ARINC 429 standard. The last bit transmitted is an odd parity bit.

ARINC 429 data is transmitted between the DEI3093 and host microcontroller using the four-wire Serial Peripheral Interface (SPI). A read or write operation consists of a single-byte Op-Code followed by the data. When writing to the transmit FIFO or reading from the receive FIFOs, the SPI data field is four bytes. Figure 6 and Figure 7 show how the SPI data bytes are mapped to the ARINC 429 message.

ARINC 429 specifies the MSB of the label as ARINC bit 1. Conversely, the data field MSB is bit 31. So the bit significance of the label byte and data fields are opposite.

Of the 8 bit opcode field, the upper 6 bits of the Opcode field are fully decoded but the lower 2 bits are not used in the decoding. Therefore, if any of the following opcodes are sent by the SPI Master the Slave device will not respond or be affected: 0x00, 0x1C, 0x30, 0x3C, 0x88, 0x8C, 0xD8, 0xDC, 0xE0, 0xE4, 0xE8, 0xEC, 0xF0, 0xF4, 0xF8 and 0xFC. The lower 2 bits are simply ignored, if these lower 2 bits are non-zero, the message is still decoded using the upper 6 bits only. The device will respond as normal based on the upper 6 bits.

The DEI3093 may be programmed to “flip” the bit ordering of the label byte as soon as it is received and immediately prior to transmission. This is accomplished by setting the TFLIP bit to a “1” in the Transmit Control Register and/or the RFLIP bit in the Receive Control Registers. The RFLIP bit does not control Priority Label Match Registers. Note that when reading ARINC 429 messages from the Priority Label Registers the label byte is omitted to permit a faster read time. The label value will match the value loaded into the Match Register and therefore does not need to be output each time a message is read.

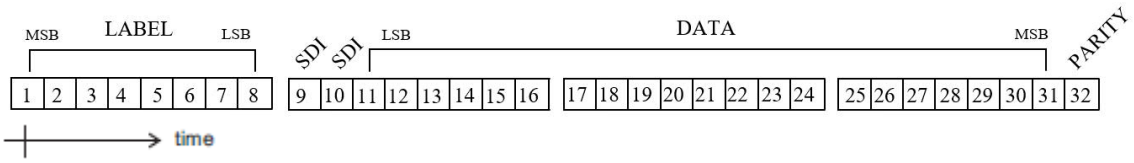
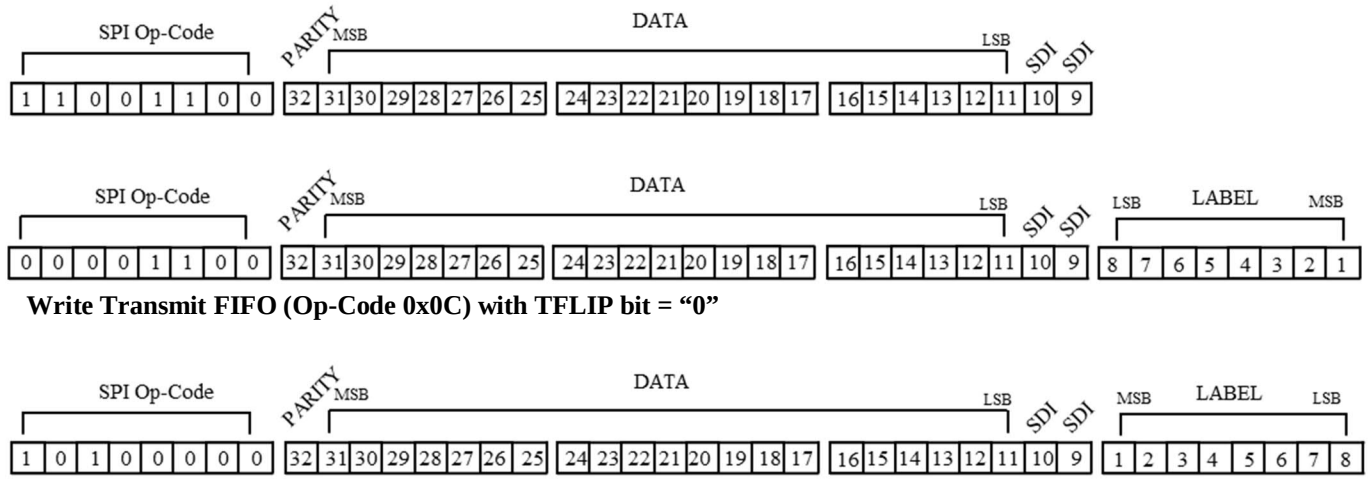


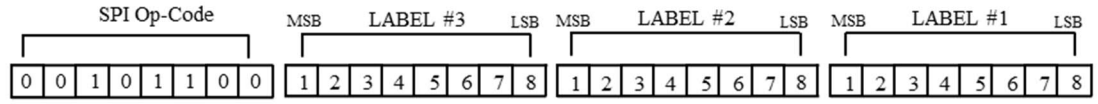
Figure 6 ARINC 429 Message as received/transmitted on the ARINC 429 serial bus



Write Transmit FIFO (Op-Code 0x0C) with TFLIP bit = "0"

Read Receiver 1 FIFO (Op-Code 0xA0) with RFLIP bit = "1

Read Receiver 2 Priority Label Register #3 (Op-Code 0xCC)



Write Receiver 2 Priority Label Match Registers (Op-Code 0x2C) with RFLIP bit = "1" or "0"

Figure 7 ARINC 429 Message as communicated on the SPI bus

CONTROL/STATUS REGISTER FORMATS

Receiver control register

Write Receiver 1 Control Register (W1CR) = 0x10
Write Receiver 2 Control Register (W2CR) = 0x24
Read Receiver 1 Control Register (R1CR) = 0x94
Read Receiver 2 Control Register (R2CR) = 0xB4

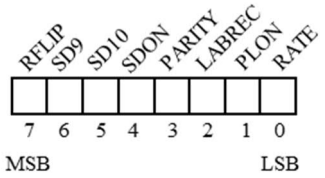


Table 3 Receiver control register definition

BIT	NAME	R/W	DEFAULT	DESCRIPTION
7	RFLIP	R/W	0	Setting this bit reverses the bit order of the first 8 bits of each ARINC 429 message received. See Figure 7 for details.
6	SD9	R/W	0	If the receiver decoder is enabled by setting the SDON bit to a "1", then ARINC 429 message bit 9 must match this bit for the message to be accepted.
5	SD10	R/W	0	If the receiver decoder is enabled by setting the SDON bit to a "1", then ARINC 429 message bit 10 must match this bit for the message to be accepted.
4	SDON	R/W	0	If this bit is set, bits 9 and 10 of the received ARINC 429 message must match SD9 and SD10.
3	PARITY	R/W	0	Received word parity checking is enabled when this bit is set. If "0", all 32 bits of the received ARINC 429 word are stored without parity checking.
2	LABREC	R/W	0	When "0", all received messages are stored. If this bit is set, incoming ARINC message label filtering is enabled. Only messages whose corresponding label filter table entry is set to a "1" will be stored in the Receive FIFO.
1	PLON	R/W	0	Priority Label Register enable. If PLON = "1" the three Priority Label Registers are enabled and received ARINC 429 messages with labels that match one of the three pre-programmed values will be captured and stored in the corresponding Priority Label Mail Boxes. If PLON = "0" the Priority Label matching feature is turned off and no words are placed in the mail boxes.
0	RATE	R/W	0	If RATE is "0", ARINC 429 high-speed data rate is selected. RATE = "1" selects low-speed ARINC 429 data rate (high-speed / 8).

Receiver status register

Read Receiver 1 Status Register (R1SR) = 0x90
Read Receiver 2 Status Register (R2SR) = 0xB0

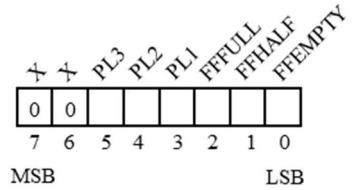


Table 4 Receiver status register definition

BIT	NAME	R/W	DEFAULT	DESCRIPTION
7	X	R	0	Not used, Always reads "0"
6	X	R	0	Not used. Always reads "0"
5	PL3	R	0	This bit is set when a message is received by Priority Label filter #3
4	PL2	R	0	This bit is set when a message is received by Priority Label filter #2
3	PL1	R	0	This bit is set when a message is received by Priority Label filter #1
2	FFFULL	R	0	This bit is set when the Receive FIFO contains 32 ARINC 429 messages
1	FFHALF	R	0	This bit is set when the Receive FIFO contains at least 16 ARINC 429 messages
0	FFEMPTY	R	1	This bit is set when the Receive FIFO is empty

Transmit control register

Write Transmit Control Register (WTCR) = 0x08
Read Transmit Control Register (RTCR) = 0x84

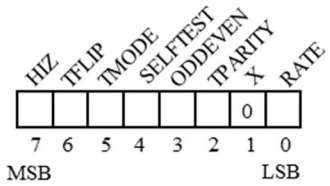


Table 5 Transmit control register definition

BIT	NAME	R/W	DEFAULT	DESCRIPTION
7	HIZ	R/W	0	Setting this bit puts the on-chip line driver outputs to a high-impedance state.
6	TFLIP	R/W	0	Setting this bit reverses the bit order of the first 8 bits of each ARINC 429 message transmitted.
5	TMODE	R/W	0	If TMODE is “0”, data in the transmit FIFO is sent to the ARINC 429 bus only upon receipt of an SPI Op-Code 0x40, transmit enable, command. If TMODE is a “1”, data is sent as soon as it is available.
4	SELFTEST	R/W	0	Setting SELFTEST causes an internal connection to be made looping-back the transmitter outputs to both receiver inputs for self-test purposes. When in self-test mode, the DEI3093 ignores data received on the two ARINC 429 receive channels and holds the on-chip line driver outputs in the NULL state to prevent self-test data being transmitted to other receivers on the bus.
3	ODDEVEN	R/W	0	If the TPARITY bit is set, the transmitter inserts an odd parity bit if ODDEVEN = “0”, or an even if ODDEVEN = “1”.
2	TPARITY	R/W	0	If TPARITY = “0”, no parity bit is inserted and the 32nd transmitted bit is data. When TPARITY is a “1” a parity bit is substituted for bit 32 according to the ODDEVEN bit value.
1	X	R	0	Not used. Always reads “0”
0	RATE	R/W	0	If RATE is “0”, ARINC 429 high-speed data rate is selected. RATE = “1” selects low-speed ARINC 429 data rate (high-speed / 8).

Transmit status register

Read Transmit Status Register (RTSR) = 0x80

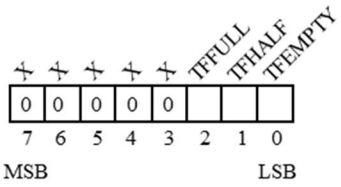
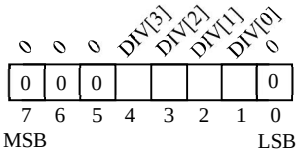


Table 6 Transmit status register definition

BIT	NAME	R/W	DEFAULT	DESCRIPTION
7	X	R	0	Not used. Always reads “0”
6	X	R	0	Not used. Always reads “0”
5	X	R	0	Not used. Always reads “0”
4	X	R	0	Not used. Always reads “0”
3	X	R	0	Not used. Always reads “0”
2	TFFULL	R	0	This bit is set when the Transmit FIFO contains 32 ARINC 429 messages
1	TFHALF	R	0	This bit is set when the Transmit FIFO contains more than 16 ARINC 429 messages
0	TFEMPTY	R	1	This bit is set when the Transmit FIFO is empty

ACLK division register



Write ACLK Division Register (WACLK) = 0x38
Read ACLK Division Register (RACLK) = 0xD4

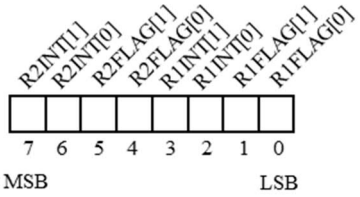
Table 7 ACLK division registers definition

BIT	NAME	R/W	DEFAULT	DESCRIPTION
7	X	R	0	Not Writable Always reads “0”
6	X	R	0	Not Writable Always reads “0”
5	X	R	0	Not Writable Always reads “0”
4 - 1 DIV[3:0]	R/W	0	The value programmed in DIV[3:0] sets the ACLK division ratio (see Table 8)	4 - 1 DIV[3:0]
0	X	R	0	Not Writable Always reads “0”

Table 8 ACLK division

ACLK Input Frequency	ACLK Division Register Value
1 MHz	0x00
2 MHz	0x02
4 MHz	0x04
6 MHz	0x06
8 MHz	0x08
…	…
28 MHz	0x1C
30 MHz	0x1E

FLAG / INTERRUPT assignment register



Write Flag / Interrupt Assignment Register (WFIAR) = 0x34
Read Flag / Interrupt Assignment Register (RFIAR) = 0xD0

Table 9 FLAG / INTERRUPT register definition

BIT	NAME	R/W	DEFAULT	DESCRIPTION
7-6	R2INT[1:0]	R/W	0	The value of R2INT[1:0] defines the function of the R2INT output pin, as follows 00--R2INT goes high for 0.5µs when a valid message is received and placed in the Receiver 2 FIFO or any of the Receiver 2 Priority Label mail boxes 01--R2INT pulses high when a message is received in Receiver 2 Priority Label mail box #1 10--R2INT pulses high when a message is received in Receiver 2 Priority Label mail box #2 11--R2INT pulses high when a message is received in Receiver 2 Priority Label mail box #3
5-4	R2FLAG[1:0]	R/W	0	The value of R2FLAG[1:0] defines the function of the R2FLAG output pin, as follows: 00--R2FLAG goes high when Receiver 2 FIFO is empty 01--R2FLAG goes high when Receiver 2 FIFO contains 32 ARINC 429 words (FIFO is full) 10--R2FLAG goes high when Receiver 2 FIFO contains at least sixteen ARINC 429 words 11--R2FLAG goes high when Receiver 2 FIFO contains one or more words (FIFO not empty)
BIT	**NAME**	**R/W**	**DEFAULT**	**DESCRIPTION**
3-2	R1INT[1:0]	R/W	0	The value of R1INT[1:0] defines the function of the R1INT output pin, as follows: 00--R1INT goes high for 0.5µs when a valid message is received and placed in the Receiver 1 FIFO or any of the Receiver 1 Priority Label mail boxes 01--R1INT pulses high when a message is received in Receiver 1 Priority Label mail box #1 10--R1INT pulses high when a message is received in Receiver 1 Priority Label mail box #2 11--R1INT pulses high when a message is received in Receiver 1 Priority Label mail box #3
1-0	R1FLAG[1:0]	R/W	0	The value of R1FLAG[1:0] defines the function of the R1FLAG output pin, as follows: 00--R1FLAG goes high when Receiver 1 FIFO is empty 01--R1FLAG goes high when Receiver 1 FIFO contains 32 ARINC 429 words (FIFO is full) 10--R1FLAG goes high when Receiver 1 FIFO contains at least sixteen ARINC 429 words 11--R2FLAG goes high when Receiver 1 FIFO contains one or more words (FIFO not empty)

FUNCTIONAL DESCRIPTION

Initialization

The DEI3093 may be initialized to its default state by applying a Master Reset (MRST) via either the MR pin or execution of the SPI Op-Code (0x04). The former is accomplished by applying a 1µs minimum high pulse to the MR pin. This MR by pin or MRST Op-Code is the same as a Power On Reset (POR) that happens upon initial power up to the chip. All control registers and memories are cleared to a known default state during a POR.

MR pin must be pulled high for 1 µs to bring the part to it's default POR state.

Table 10 Master Reset vs Software Reset comparison

ACTION	MR	SR
Terminate any data transmission and reception. Reset ARINC 429 output to NULL. Any partial transmission and reception data will be terminated and lost. Set status registers to empty state.	x	x
Clear all three data FIFOs (2 RX and 1 TX)	x	x
Clear Priority Label Mail Boxes	x	x
Clear all Filter memories and PLM Match Registers	x	
Set all internal registers to their default values	x	

On chip POR is released at approximately 150µs after VDD exceeds approximately 2.5V during power up.

A limited Software Reset (SRST) may be performed by execution of the SPI Op-Code (0x44). This clears only the data values in registers and memory FIFO's.

The Master Reset clears all data and control registers/memory, while the Software Reset only clears data. The actions are summarized below.

ACLK Frequency Setup

The DEI3093 generates a 1MHz internal reference clock from the ACLK input via a programmable frequency divider.

The application must provide ACLK with 1MHz, or any even multiple of 1MHz, up to 30MHz. If other than 1MHz is provided, the ACLK Division Register must be programmed with the Op-code and value defined in Table 7 and Table 8.

For correct ARINC 429 data timing, the reference clock, and therefore the ACLK input, requires 1% minimum frequency accuracy.

This ACLK setup must be performed prior to any other configuration setup to insure correct internal clock timing.

Configuration of ARINC 429 Channels

The Transmit Control Register and Receiver Control Registers are used to configure the ARINC 429 transmission channel and two ARINC 429 receive channels. The registers may be written or read at any time. Refer to the Receiver Control Register (Table 3) and Transmit Control Register (Table 5) descriptions for detailed information.

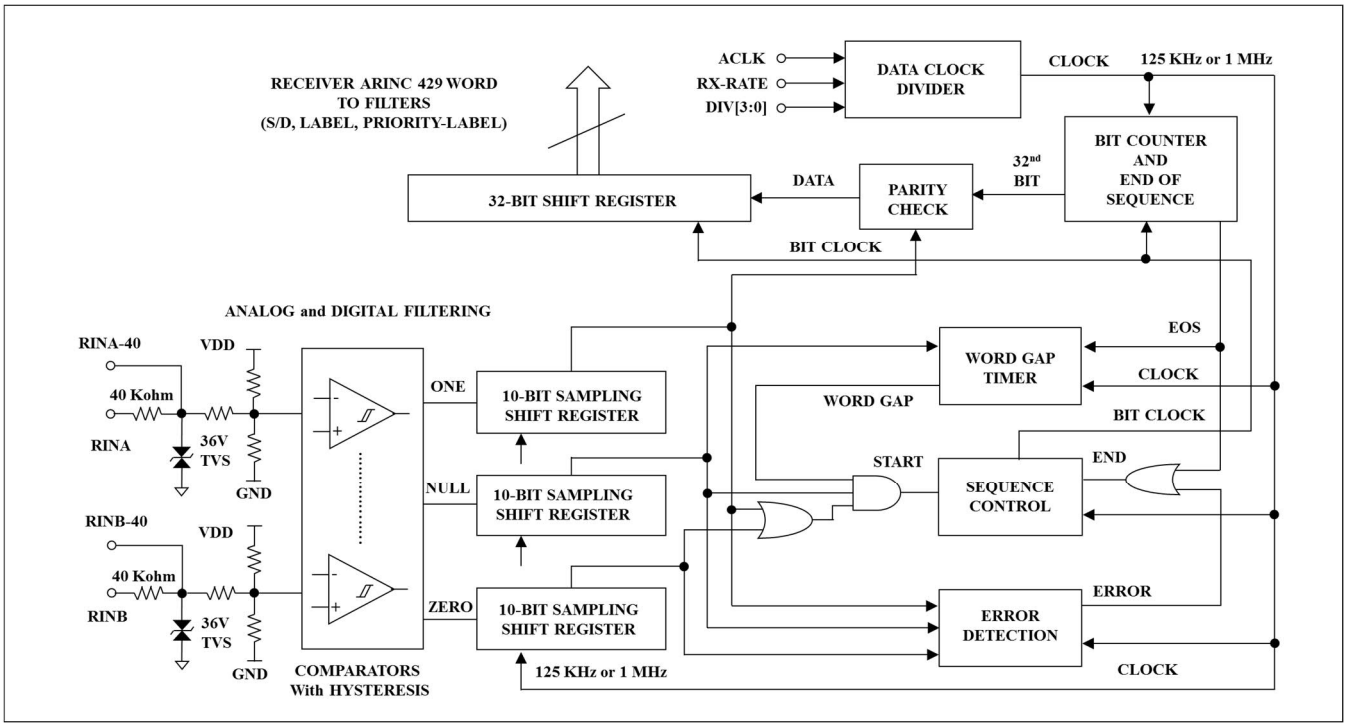


Figure 8 Receiver function diagram

ARINC 429 Receiver (RX)

The DEI3093 has two completely independent ARINC 429 receive channels. Each channel has an on-chip line receiver for direct connection to the data bus. The line receiver detects the ARINC 429 standard signal levels and converts them for deserialization in the RX.

Table 11 ARINC 429 RX Signal Detection Levels

STATE	DIFFERENTIAL VOLTAGE
ONE	+6.5 V TO +13 V
NULL	+2.5 V TO -2.5 V
ZERO	-6.5 V TO -13 V

For operation in the presence of interference, the receiver accepts signals with up to ±25 V of common mode noise.

Receiver External resistor option

The receiver RINxA/RINxB input pins may be connected directly to the ARINC 429 bus, but require additional TVS protection devices to withstand lightning induced transients that would exceed the maximum voltage ratings of the pins.

Another option is to use the RINxA/RINxB-40 inputs. As illustrated in Figure 8, these inputs bypass on-chip 40KΩ resistors. With this option, the pins are connected to the ARINC 429 bus signals through external 40KΩ resistors. The resistors and on-chip clamp diodes will limit the pin voltage and thus sustain DO-160 Level 3 pin injection transients without the need for TVS devices. Higher Level transients can be sustained with the addition of a small external low power TVS clamps.

ARINC 429 Deserialization

The receiver is designed to accept and deserialize the ARINC 429 digital pulse stream with standard ARINC timing characteristics listed below.

Table 12 ARINC 429 Serial Data Timing

	HIGH SPEED	LOW SPEED
BIT RATE	100K BPS ± 1%	12K to 14.5K BPS
PULSE WIDTH	1.5 ± 0.5 µsec	10 ± 5 µsec
RISE TIME	1.5 ± 0.5 µsec	10 ± 5 µsec
FALL TIME	5 µsec ± 5%	34.5 to 41.7 µsec
MIN WORD GAP	4 NULL BITS	

The deserializer, in combination with the line receiver, provides robust noise filtering to accurately detect data in high electrical noise environments. The serial data is sampled at 10x the nominal bit rate frequency derived from ACLK. Samples are processed by a digital filter and logic to perform bit detection, word framing detection and data serialization.

The qualified 32 bit words are presented to the RX FIFO and RX PLM (Priority Label Memory) for appropriate filtering before becoming available to the host.

Legacy Deserialization

For compatibility with some old and proprietary formats similar to ARINC 429, the receiver also accepts an extended bit rate and word gap range indicated in the Table 13.

Table 13 Legacy Bit Rates

	HIGH SPEED	LOW SPEED
ACCEPTED BIT RATE	83K to 125K BPS	10.4K to 15.6K BPS
MIN WORD GAP	3 NULL BITS	

Receiver parity

ARINC 429 receiver parity checking is supported as a means of single bit error detection. It is enabled by setting the Receive Control Register PARITY bit to a “1”. When enabled, the receiver parity circuit counts the number of bits equal to a “1” received, including the parity bit. If the result is odd, a "0" will appear in the 32nd bit position, indicating that no bit error is detected.

If receive parity is enabled and a word is received with even (incorrect) parity, the 32nd bit is overwritten with a “1”, indicating a bit error is detected.

Data filtering and FIFO loading

The DEI3093 may be programmed to filter out (ignore) received words based on their Label field and/or SDI field values. Upon receiving a complete ARINC word, the receiver checks for applicable SDI field value and Label

The word is loaded into the FIFO unless either of these conditions exist:

- The Receiver Control LABREC (LABel RECognition) bit is programmed to “1” and the word’s label field **does not** match a value programmed into the Label Memory filter as “1”.
- The Receiver Control SDON bit is programmed to “1” and the word’s SD field **does not** match the Receive Control Register bits SD10 and SD9.

The Table 14 shows the results for Receive FIFO loading.

An equation for the logic process of loading the message into the FIFO:

$$LOAD = (\overline{LABREC}\ OR\ LMATCH)\ AND\ (\overline{SDON}\ OR\ SDMATCH)$$

LABREC = Label Recognition
LMATCH = Label Match
SDON = Source/Destination Identifier
SDMATCH = Source/Destination Identifier Match

Receiver Status Register

The Receiver Status Register stores the status info of the FIFO. See Table 4 for the bit definitions of the Receiver Status Register.

Each time a valid ARINC 429 word is loaded into the FIFO, the Receive FIFO Status Register FFEMPTY, FFHALF and FFFULL bits are updated. When the FIFO is EMPTY, the FFEMPTY bit is "1" and FFHALF and FFFULL are "0". Once the first received and accepted ARINC 429 word is loaded into the FIFO, FFEMPTY goes low.

A FIFO half-full flag (FFHALF) is high whenever the Receive FIFO has more than 16 words. The FFHALF bit provides a useful indicator to the host CPU that a data retrieval routine may be performed.

Table 14 RX FIFO loading control

LAB REC	Label Match Filter	LABREC Match	SD ON	SD bits 9 10	SD bits Match	FIFO
0	0	Match	0	0	Match	Load
0	0	Match	0	1	Match	Load
0	1	Match	0	0	Match	Load
0	1	Match	0	1	Match	Load
0	0	Match	1	0		
0	0	Match	1	1	Match	Load
0	1	Match	1	0		
0	1	Match	1	1	Match	Load
1	0		0	0	Match	
1	0		0	1	Match	
1	1	Match	0	0	Match	Load
1	1	Match	0	1	Match	Load
1	0		1	0		
1	0		1	1	Match	
1	1	Match	1	0		
1	1	Match	1	1	Match	Load

Reading Data from Receiver FIFO

When Receiver FIFO contains data, FFEMPTY=0. The data can be retrieved via SPI interface with Op-Code 0xA0 (RX1) or 0xC0 (RX2) follow by a 4 byte read.

Receiver FIFO under-run

When FFEMPTY=0, the host system may continuously read data from the Receiver FIFO till FFEMPTY=1. If the host system reads data from the Receiver FIFO at the status of when FFEMPTY=1, the data is invalid.

Receiver FIFO over-run

The Receiver FIFO can hold up to 32 ARINC 429 words. When the FIFO is full, the FFFULL bit of status register goes high. If more valid ARINC 429 words arrive at a FFFULL status, the last word of the Receiver FIFO will be overwritten by new arrival word.

Receiver label recognition

Each receiver has a label recognition filter. To use it, the host loads the 256-bits label look-up table to specify which labeled words will be stored in the Receiver FIFO.

The host programs the Label Memory by executing SPI Op-Code 0x14 (RX1) or 0x28 (RX2), followed by 32 bytes (256-bits) of Label Memory. The Label Memory can be read via SPI using Op-Code 0x98 (RX1) or 0xB8 (RX2) as described in Table 2.

The Label Memory is a 256 bits look-up table with each bit representing the accept/reject disposition of the corresponding labeled word to be loaded into the FIFO. Set bit=1 to accept, and bit=0 to reject the corresponding label. The 256-bit table sequence starts from Label 0xFF, and ends at Label 0x00 in a sequential order. For example, if the first data byte is programmed to 10110010…, then labels FF, FD, FC and F9 will be accepted, and FE, FB, FA and F8 will be rejected.

Receiver priority labels

To enable Priority Label capture, set the PLON bit to "1" in the Receive Control Register. Set the PLON bit to "0" to disable it.

Write Priority Label Match Registers with SPI Op-Code 0x18 (RX1) or 0x2C (RX2), followed by three bytes of label match values. The 1st, 2nd and 3rd bytes correspond to Priority Label Registers #3, #2 and #1 respectively. The match values may be checked by reading the Priority Label Match Registers.

When the Priority Label feature is enabled, the three Priority Label Registers store received data if the incoming ARINC 429 label matches the value stored in Priority Label Match Register #1, # 2 or #3.

When using the Priority Label feature, program all Priority Label Match Registers, including unused registers, to avoid unintended matches occurring on un-programmed Registers. Duplicate the active labels in the unused registers.

Note that Priority Label Registers (mail boxes) are only 24 bits long, the matched label byte is not stored. This allows a shorter and faster access of the data field. Use SPI Op-Codes 0xA4, 0xA8, 0xAC, 0xC4, 0xC8 and 0xCC for Priority Label Registers #1, #2 and #3 of RX1 and RX2 respectively.

The Receive Status Register bits PL1, PL2 and PL3 indicate when Priority Label data is available in the Priority Label Registers. Six status output pins MB1-1 through MB2-3 also indicate when data is available at each of the six Priority Label Registers. The R1INT and R2INT interrupt pins can also be triggered when Priority Labels are captured, see Table 9 Flag/Interrupt Assignment Register definition for further instruction.

Receiver flag / interrupt

The FFEMPTY, FFHALF or FFFULL status bits can also be output on the R1FLAG (RX1) and R2FLAG (RX2) pins. FIFO not empty option may be programmed for the R1FLAG / R2FLAG pins as well.

R1INT / R2INT can be setup up to monitor arrival of data at the receiver FIFO or Priority Label Mail Box. The interrupt pins will generate a single Pulse HIGH, and its pulse width is about the 1MHz clock source pulse width.

For more info, see Table 9 FLAG/INTERRUPT register definition.

Receiver FIFO Half Full Flag operation

This is applicable to the Receiver FIFO Half Full status flag which can be observed by the host controller via the FFHALF bit in the Receive Status Register and/or the RXFLAG pin if programmed to indicate FFHALF (FLAG Register FnFLAG[1:0] = 0b10).

The FFHALF flag may prematurely return a "not half-full" status under a specific condition. The flag is intended to indicate "1" when the RX FIFO has 16 or more words in it, and "0" when less than 16. But in some conditions, the flag will reset to "0" prematurely. This can occur when the FIFO has been filled with 32 words to the FIFO FULL condition. When reading (emptying) the first 16 words of a full FIFO, the FFHALF status may indicate "0" (not half-full) instead of the expected "1".

This situation does not present a problem in typical applications using FFHALF to initiate a process of reading 16 words or reading until the FIFO is empty. Nor does it present a problem when FFFULL is used to initiate a process of reading 32 words or reading until FIFO is empty. But it could present a problem if for some reason the FFHALF status is used for control logic during the first 16 read cycles after a FIFO FULL condition.

ARINC 429 Transmitter (TX)

Transmitter data status

SPI Op-Code 0x0C writes each ARINC 429 word into the Transmit FIFO, at the next available location. If Transmit Status Register bit TFEMPTY equals "1" (FIFO empty), then up to 32 words (32 bits each) may be loaded.

When the Transmit FIFO contain more than 16 words, the TFHALF (Transmit Status Register half-full flag) bit is set to "1". When TFHALF equals "0", the host system can safely initiate a 16-word ARINC 429 write sequence.

Transmit FIFO over-run

The Transmit FIFO can hold up to 32 words. When Transmit FIFO is full, the Transmit Status Register TFFULL bit will be set to "1" or TFULL output pin is also set HIGH. The host system may continuously load data into the Transmit FIFO till it full. Any attempt to load data at TFFULL=1 status will be ignored.

Transmitter parity

When Transmit Control Register bit TPARITY equals "1", the 32nd bit transmitted is an odd parity bit. If TPARITY equals "0", all 32 bits loaded into the Transmit FIFO are treated as data and are transmitted.

The parity generator circuit counts the Ones in the 31-bit word. The 32nd bit transmitted will make parity odd. Setting Transmit Control Register bit TPARITY to "0" bypasses the parity generator, and allows 32 bits of data to be transmitted.

Transmitter self-test

If Transmit Control Register bit SELFTEST equals "1", the transmitter serial output data is internally looped-back into the RX1 and RX2. The data is inverted (complement) into RX2. Data is unmodified from transmitter into RX1. Setting Transmit Control register bit SELFTEST to "1" forces TXAOUT and TXBOUT to the Null state to prevent self-test data from appearing on the ARINC 429 bus.

Data transmission without TMODE

To allow software control the transmission Timing, disable the TMODE by writing Transmit Control Register bit TMODE to "0". Without TMODE, data transmission has to be initiated by SPI Op-Code 0x40 instruction. Once transmission is started it will continue till Transmit FIFO becomes empty, TFEMPTY=1. If any new words are loaded into Transmit FIFO in the midst of transmission while TFEMPTY=0, the new words will be transmitted together. When Transmit FIFO is empty, TFEMPTY=1, any new words loaded into the Transmit FIFO can be only be transmitted with the next SPI Op-Code 0x40 instruction.

Data transmission with TMODE

If Transmit Control Register bit TMODE set to "1", ARINC 429 data is transmitted immediately following the $\overline{CS}$ rising edge of the SPI instruction that loaded data into the Transmit FIFO.

High Impedance Line Driver

The line driver outputs TXAOUT, TXBOUT, AMPA and AMPB may be programmed to a high impedance state, allowing multiple line drivers to be connected to a single ARINC 429 bus. To tri-state the outputs, the HIZ bit in the Transmit Control Register must be programmed to a "1". Note that all other functions of the DEI3093 continue to operate as usual, even though the outputs are tri-stated.

ARINC 429 line driver output

The DEI3093 line driver directly drives the ARINC 429 bus. The two ARINC 429 outputs (TXAOUT and TXBOUT) provide a differential voltage to produce a +10V One, a -10V Zero, and a 0V Null. Refer to ELECTRICAL CHARACTERISTICS table.

The DEI3093 TXAOUT and TXBOUT pins have 37.5Ω resistors in series with each line driver output, and may be directly connected to an ARINC 429 bus. The alternate AMPA and AMPB pins have ~5Ω of internal series resistance and require external 32.5Ω resistors at each pin. AMPA and AMPB pins are typically used in combination with TVS devices and 32.5Ω resistors to implement lightning protected outputs.

ARINC 429 Bit Rate

Transmit Control Register bit RATE controls both the transmit data rate and the slope of the line driver differential output signal. Writing Transmit Control Register bit RATE to "0" causes a 100Kbit/s data rate and a slope of 1.5µs on the ARINC 429 outputs. Setting RATE to "1" causes a 12.5Kbit/s data rate and a slope of 10µs.

ARINC 429 Transmission Format

With reference to the 1MHz (1.0µs) clock source, the TXAOUT and TXBOUT pins will present ARINC 429 format with the following timing of Table 15:

Table 15 Clock Source Counts

	HIGH SPEED	LOW SPEED
ARINC DATA BIT TIME	10 Clocks	80 Clocks
DATA BIT TIME	5 Clocks	40 Clocks
NULL BIT TIME	5 Clocks	40 Clocks
WORD GAP TIME	40 Clocks	320 Clocks

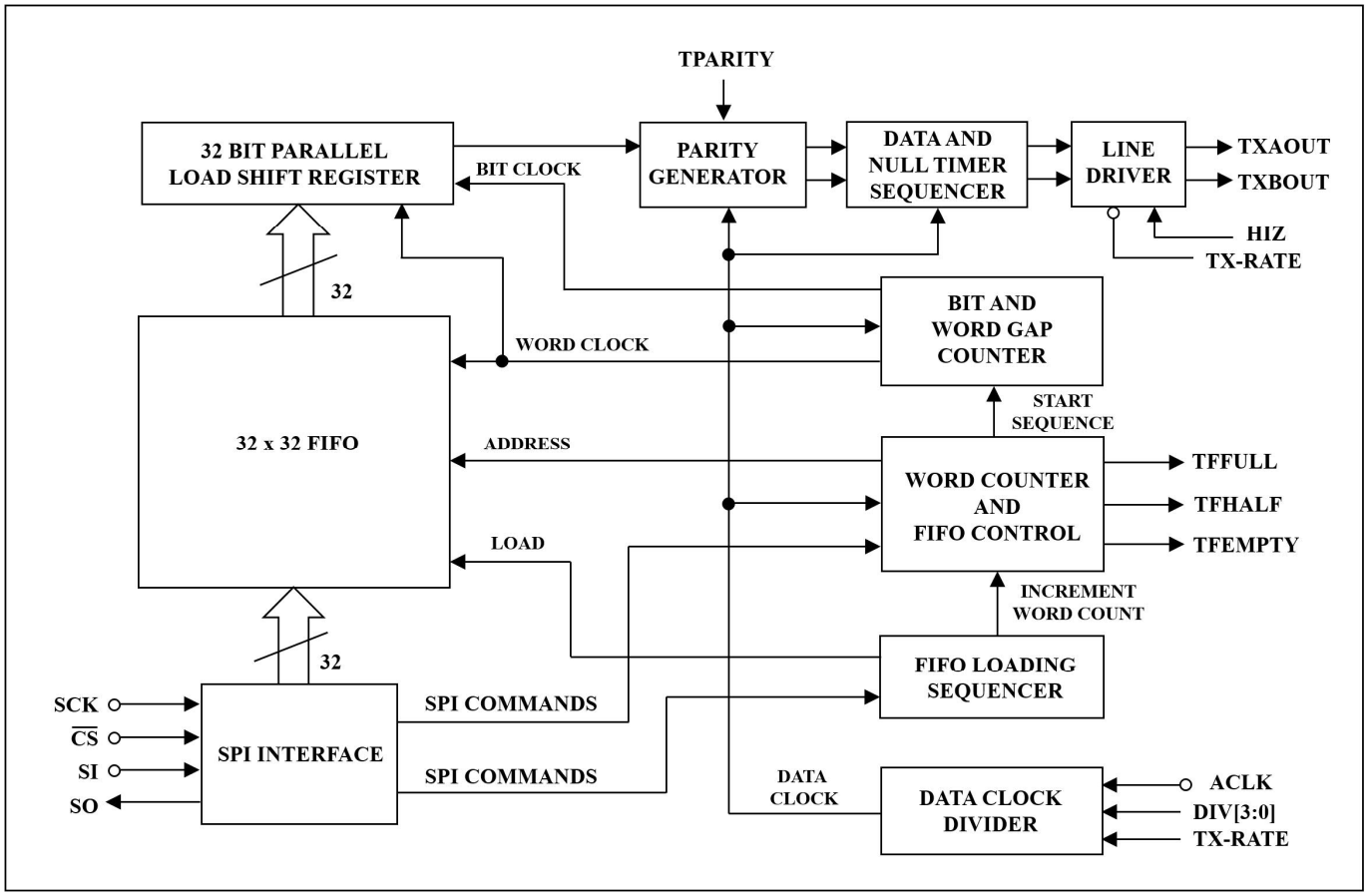


Figure 9 Transmitter function diagram

DC/DC Converter

The integrated DC/DC converter implements a charge pump doubler and inverter to produce ±6.6V rail voltages to supply the line driver producing the VDD2P and VDD2N supplies of ±5V ARINC 429 signal levels.

ABSOLUTE MAXIMUM RATINGS

Table 16 Absolute Maximum Ratings

PARAMETER	SYMBOL	MIN	MAX	UNITS
Supply Voltage	VDD	-0.3	+5.0	V
DC/DC Converter positive voltage output	VDD2P		+7.0	V
DC/DC Converter negative voltage output	VDD2N	-7.0		V
DC Input Voltage at RINxx-xx		-120	+120	V
Voltage at any other pin		-0.3	VDD+0.3	V
DC Current Drain per digital input pin		-10	+10	mA
Storage Temperature	Tstg	-65	+150	°C
Junction Temperature	Tjmax		+145	°C

Note: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

OPERATING CONDITIONS

Table 17 Recommended Operating Conditions

Supply Voltages: VDD	3.3V +/- 5%
Operating Temperature: Extended (-xEx) versions: Military (-xMx) versions:	 -55 °C to +85 °C -55 °C to +125 °C

ELECTRICAL CHARACTERISTICS

Table 18 Electrical Characteristics

PARAMETER	SYMBOL	CONDITIONS[1]	LIMITS			UNIT
			MIN	TYP	MAX	
ARINC 429 RECEIVERS - RIN1A/RIN1B & RIN2A/RIN2B. RIN1A/RIN1B-40 & RIN2A/RIN2B-40 with external 40KΩ						
ARINC differential input: ONE (RIN1A to RIN1B, RIN2A to RIN2B) ZERO NULL	V_{IH} V_{IL} V_{NUL}	Common mode voltages (-25V < V_{CM} < +25V) less than ±25 V with respect to GND	6.5 -13[2] -2.5		13[2] -6.5 2.5	V V V
Input resistance [2] differential to GND to VDD	R_I R_G R_H		12 12 12	350 350 350	- - -	KΩ KΩ KΩ
Input current input sink input source	I_{IH} I_{IL}	(-25V < V_{CM} < +25V) $\|VIH\| = \|VIL\| = 5.5V$	 -200		200 	µA µA
Input capacitance [2] differential to GND to VDD	C_I C_G C_H	(RINxA to RINxB)			20 20 20	pF pF pF
ARINC 429 DRIVER –TXAOUT/TXBOUT. AMPA/AMPB with external 32.5Ω						
ARINC output (Ref. To GND) One or Zero NULL	V_{DOUT} V_{NOUT}	No load and magnitude at pin	4.5 -0.25	5 	 0.25	V V
ARINC output (Differential) One or Zero NULL	V_{DDIF} V_{NDIF}	No load and magnitude at pin	9.0 -0.5	10 	11 0.5	V V
ARINC output current [2]	I_{OUT}	Momentary short-circuit current	80			mA
ARINC output Resistance: TXAOUT/TXBOUT pins AMPA/AMPB pins	*Rout*	Room Temperature		 37.5 5[2]		 Ω Ω
ARINC Output Tri-State Current	I_{HIZ}	TTLIN0/1=VDD2N/P -5.5 V<V_{HIZ}<5.5 V	-10		10	µA
LOGIC INPUTS						
Input voltage: input voltage HI input voltage LO	v_{ih} v_{il}		80%Vdd		 20%Vdd	V V
Input current: Input sink Input source Pull-down current (MR,SI,SCK,ACLK pins) Pull-up current ($\overline{CS}$ pin)	i_{ih} i_{il} i_{pd} i_{pu}	VIN = VDD VIN = GND VIN = VDD VIN = GND	 -1.5 -120	 60 -60	1.5 120 	µA µA µA µA
LOGIC OUTPUTS						
Output voltage: Logic “1” output voltage Logic “0” output voltage	v_{oh} v_{ol}	i_{oh} = 1.0 mA i_{ol} = 1.6 mA	90%Vdd		 10%Vdd	V V
Output Capacitance: [2]	*Co*			6		pF
SUPPLY VOLTAGE						
Supply Current, unloaded	I_{DD}	Transmit in Hi speed mode when output unloaded			50	mA
Supply Current, loaded	I_{DDL}	Transmit in Hi speed mode 400Ω Diff output Load			75	mA
DC/DC CONVERTER						
Start-up transient (VDD2P, VDD2N) [2, 3]	t_{START}				10	ms
Operating Switching Frequency [2]	f_{SW}			250		KHz
Voltage doubler output	V_{DD2P} V_{DD2N}	Open load		6.3 -6.3		V V

Notes:

1. Unless otherwise specified, characteristics are measured under VDD = 3.3V and operating temperature range.
2. Guaranteed by design, not production tested.
3. With minimum capacitance size.

Table 19 Design Information

PARAMETER	SYMBOL	CONDITIONS	MIN	NOM	MAX	UNIT
CAPACITOR REQUIREMENTS (Design Information)						
V+ Fly-back capacitor, non-polarized X7R ceramic, 10V min	C_{FLY+} ESR	 500 KHz	0.47		 500	µF mΩ
V- Fly-back capacitor, non-polarized X7R ceramic 10V min	C_{FLY-} ESR	 500 KHz	2.2		 500	µF mΩ
Two bulk storage capacitors, non-polarized X7R ceramic or tantalum, 10V min	C_{OUT} ESR(COUT)	 500 KHz	10		47 300	µF mΩ
Supply de-coupling capacitors, X7R ceramic or tantalum, 10V min	C_{SUPPLY}	Two parallel capacitors	 10	0.1	 47	µF µF

TIMING CHARACTERISTICS

Table 20 Timing Characteristics

PARAMETER[1]	SYMBOL	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS
SPI INTERFACE TIMING					
SCK clock period [2]	t_{CYC}	100			ns
$\overline{CS}$ active after last SCK rising edge	t_{CHH}	10			ns
$\overline{CS}$ setup time to first SCK rising edge	t_{CES}	10			ns
$\overline{CS}$ hold time after last SCK falling edge	t_{CEH}	10			ns
$\overline{CS}$ inactive between SPI instructions	t_{CPH}	55			ns
SPI SI Data setup time to SCK rising edge	t_{DS}	10			ns
SPI SI data hold time after SCK rising edge	t_{DH}	10			ns
SCK rise time	t_{SCKR}			10	ns
SCK fall time	t_{SCKF}			10	ns
SCK pulse width high	t_{SCKH}	20			ns
SCK pulse width low	t_{SCKL}	25			ns
SO valid after SCK falling edge	t_{DV}			35	ns
SO high-impedance after SCK falling edge	t_{CHZ}			30	ns
MR pulse width	t_{MR}	50			ns
RECEIVER TIMING					
Delay - Last bit of received ARINC word to RX Flag change - Hi Speed Delay - Last bit of received ARINC word to RX Flag change - Lo Speed	t_{RFLG} t_{RFLG}			16 126	µs µs
Receiver data available to SPI interface, RXFLAG to $\overline{CS}$ active	t_{RXR}	0			ns
SPI receiver read FIFO instruction to RXFLAG	t_{CES}	10		t_{CYC}	ns
RXINT pulse width	t_{INTW}		500		ns
$\overline{CS}$ inactive between SPI instructions	t_{CPH}	55			ns
TRANSMITTER TIMING					
SPI transmit data write (FIFO Flag Empty or FULL)	t_{TFLG}			0	ns
FIFO Flag delay after enable transmit instruction – Hi Speed	t_{DATT}			2	µs
FIFO Flag delay to ARINC 429 data output – Hi Speed FIFO Flag delay to ARINC 429 data output – Lo Speed	t_{SDAT} t_{SDAT}	10		40 320	µs µs
ARINC 429 DRIVER slew rates					
High Speed — high to low [2]	t_{fxH}	1.0	1.5	2.0	µs
High Speed — low to high [2]	t_{rxH}	1.0	1.5	2.0	µs
Low Speed — high to low [2]	t_{fxL}	5.0	10.0	15	µs
Low Speed — low to high [2]	t_{rxL}	5.0	10.0	15	µs

Notes:

1. Characteristics are design information. Unless otherwise specified, various timing characteristics are indirectly verified with functional test pattern at VDD = 3.3V and operating temperature range.
2. Timing parameter is statistically sampled/measured at VDD=3.3V in production test.

TIMING DIAGRAMS

SPI timing diagrams

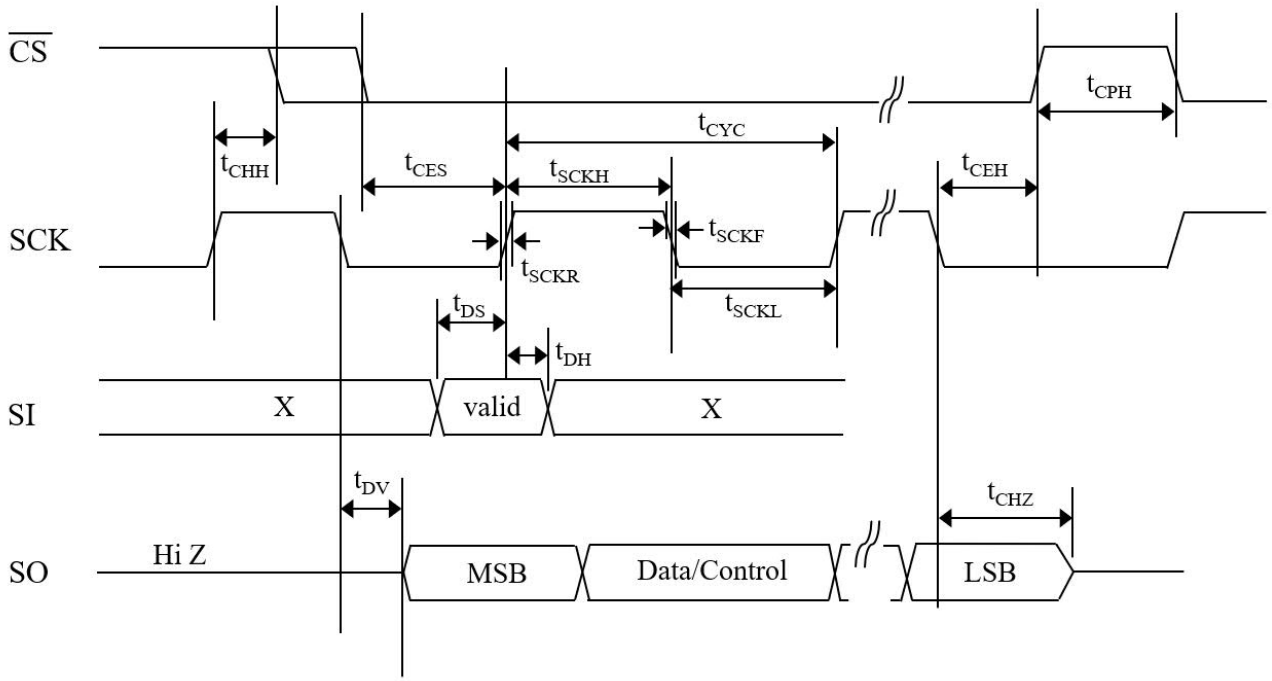
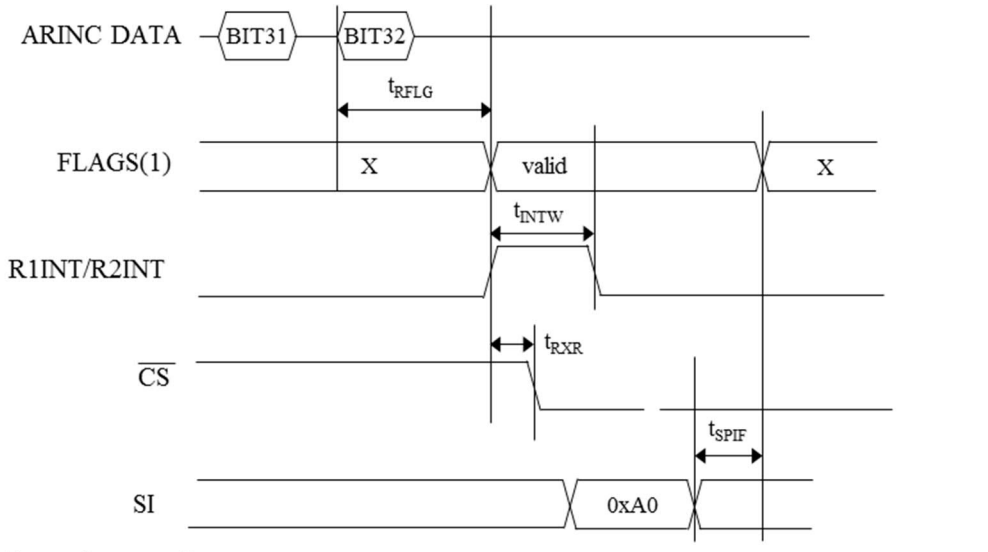


Figure 10 SPI timing

Receiver timing diagram



(1) Receive status flag outputs: R1FLAG, R2FLAG, MB1-1, MB1-2, MB1-3, MB2-1, MB2-2, MB2-3

Figure 11 Receiver timing

Transmitter timing diagram

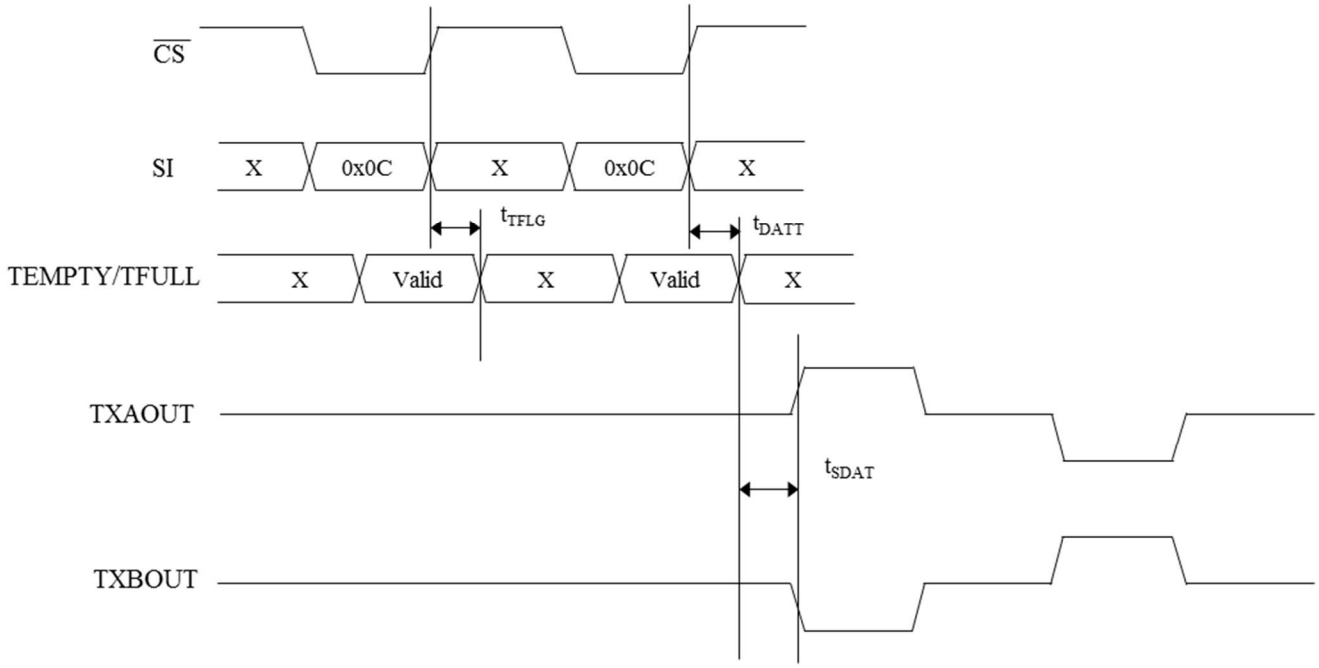


Figure 12 Transmitter timing

ARINC 429 line driver output waveforms

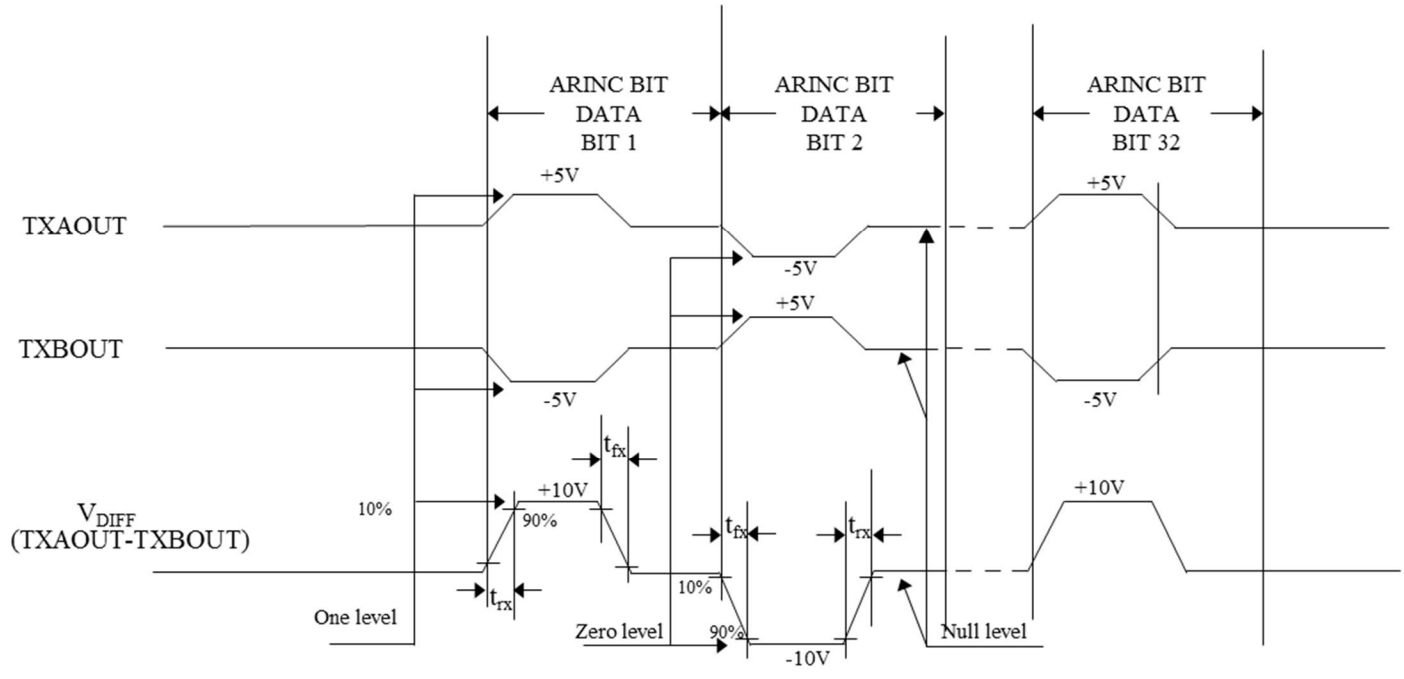


Figure 13 Line driver timing

DESIGN CONSIDERATIONS

Power Supply and Voltage Doubler Capacitors

Refer to Figure 1 Function Diagram and Table 19 Design Information.

C_{SUPPLY}: The VDD supply should be decoupled with a low impedance ceramic or tantalum capacitor to source the voltage doubler ripple current and filter switching currents to the supply. The ripple current can be in the range of hundreds of mA during peak loading.

A parallel 0.1 µF ceramic capacitor is recommended to provide high frequency filtering.

C_{FLY}: The two fly-back capacitors transfer energy from the charge pump inverters to the rectifiers.

C_{OUT}: The two voltage doubler output capacitors filter the charge pump rectifier outputs. Low impedance ceramic capacitors are recommended.

All capacitors should be placed in close proximity to the IC to minimize power loss and noise due to routing impedance. It is beneficial to include 0.1 µF parallel capacitors to minimize high frequency impedance.

Receiver Lightning Transient Protection

The receiver RINxA/RINxB pins are designed to operate when connected directly to ARINC 429 2-wire signal. They require the application to provide appropriate TVS (Transient Voltage Suppression) diodes to meet the application's lightning immunity requirements.

Select TVS devices with:

- Clamp voltage below +/- 100V
- Standoff voltage above +/- 32V to preserve common mode operating range
- Power rating to withstand the application's immunity requirement

The receiver RINxA-40/RINxB-40 pins are designed to operate with application supplied 40KΩ series resistors to the ARINC 429 2-wire signal. This provides DO160 level A3 lightning transient immunity without the need to add TVS diodes.

To achieve higher immunity levels, the application must supply TVS diodes at RINxA-40/RINxB-40 pins. But they can be small low-power devices due to the current limiting provided by the 40KΩ.

Select devices with:

- TVS with standoff voltage above +/- 32V to preserve common mode operating range
- TVS capacitance < 25pF to avoid high speed waveform distortion
- Resistors with adequate pulse voltage rating to withstand the application lightning immunity requirement.

Transmitter Lightning Transient Protection

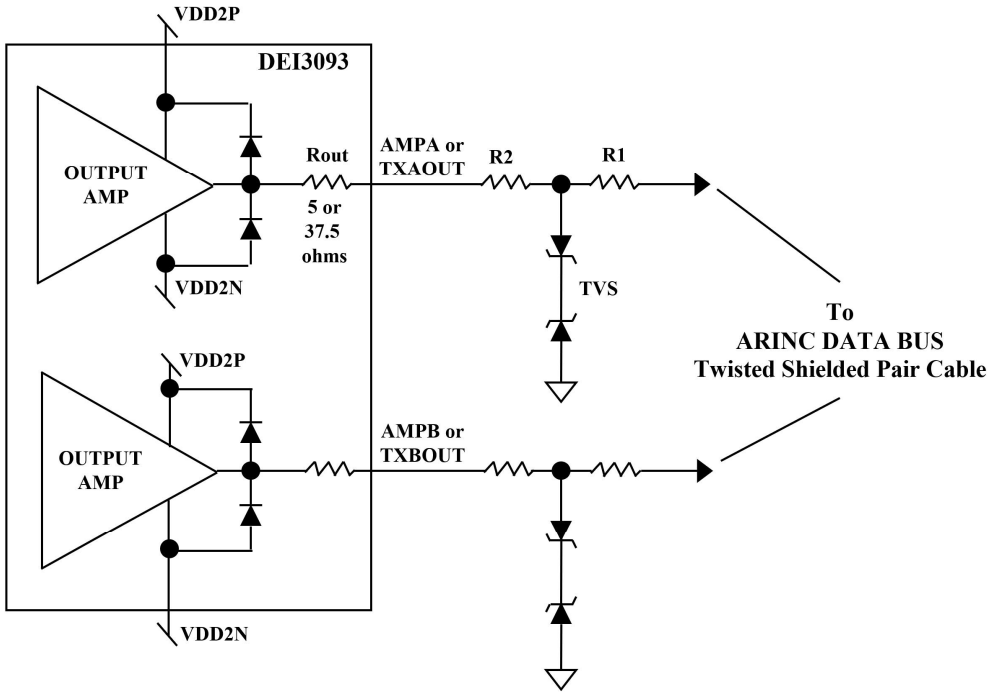


Figure 14 Surge Protection Network

The ARINC 429 Line Driver requires external components to achieve immunity from surges such as those defined by DO160 Section 22, "Lightning Induced Transient Susceptibility". Typical surge protection includes silicon TVS devices and may include part of the 37.5Ω output resistance as external resistors to limit the surge current.

The ARINC 429 Line Driver has a robust output stage which includes large driver devices and clamp diodes to the VDD2P and VDD2N power rails as shown in Figure 14. It withstands surge currents of ±0.5A for 175µs without damage when powered with +3.3V supplies. At that surge current, the diodes clamp at ~1V above (below) the VDD2P (VDD2N) supply rail. ~350mA flows to the VDD2N (VDD2P) supply through the output amplifier, and ~150mA flows to the VDD2P (VDD2N) internal supply through the clamp diode. The outputs may be damaged by surges greater than 1A / 175µs. At that current, the diode clamps at ~1.8V above (below) the supply.

The external lightning protection network should be designed to meet the specific requirements and constraints of the application equipment. The protection network should limit the OUTA/OUTB pin surge current to the 0.5A / 175 µs maximum. The generalized circuit of Figure 14 represents several TVS protection network options:

- The on-chip Rout value is 5 or 37.5Ω
- Select the total output resistance,
  Rout + R1 + R2, = 37.5Ω to meet ARINC bus requirements
  - Select R1 = 20Ω, R2 = 12.5Ω, Rout = 5Ω to use low TVS with surge current rating (small TVS devices)
  - Select R1 = 0Ω, Rout + R2 = 37.5Ω to use high TVS clamp voltage (20V + VDD2P/VDD2N)
  - If the VDD2P/VDD2N internal supplies are un-powered or below operating voltage during the surge event, large currents may flow through the internal clamp diodes and damage the driver. If the application requires lightning immunity while un-powered, Select R1 = 0Ω, Rout + R2 = 32.5Ω, and select the TVS clamp voltage for <20V.
- Select TVS devices for the following.
  - TVS Surge power/current rating must withstand the application requirements for Lightning Induced Transient Levels and Waveforms. Microsemi Corporation publishes an application note specific to the DO160 lightning requirements (Micronote 126).
  - Select low capacitance TVS devices to minimize the load on the line driver. (Examples: Microsemi LC and HSMBJSA series TVS) This is a priority for Hi Speed ARINC applications where the low capacitance is important for optimum signal integrity and power consumption. Note that the maximum total capacitance on the ARINC bus is 30nF line to line.

- Select the TVS clamp voltage at the lightning surge conditions such that the voltage/current into the DEI3093 OUT pin is within the safe region.
- If R1 is used to limit the TVS surge current, the resistor must withstand the surge current and voltage.

Some general considerations related to Lightning Immunity:

- Analyze the TVS high current signal and ground return path to insure adequate surge current capability. The IR voltage and L*di/dt voltage in the ground return will add additional stress beyond the TVS clamp voltage.
- Observe suitable PCB design rules for traces subject to high voltage and high current surges.
- When possible, locate TVS devices close to the equipment connector to minimize the length of the surge voltage/current traces within the equipment.
- The shields of ARINC 429 data bus cables should be terminated to aircraft ground at all ends and at all bulkhead disconnects

ORDERING INFORMATION

Table 21 Ordering Information

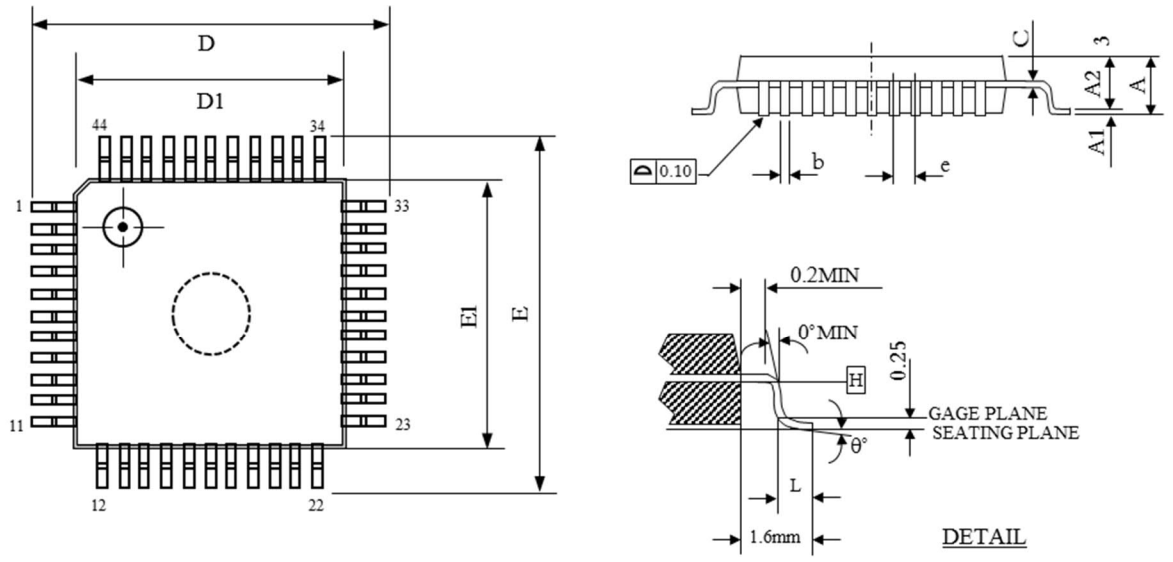
Part Number	Marking	Package	Temperature
DEI3093-QES-G	DEI3093-QES	44L MQFP G	-55 ºC +85 ºC
DEI3093-QMS-G	DEI3093-QMS or -QES + blue dot	44L MQFP G	-55 ºC +125 ºC
DEI3093-MES-G	DEI3093-MES	44L MQFN G	-55 ºC +85 ºC
DEI3093-MMS-G	DEI3093-MMS or -MES + blue dot	44L MQFN G	-55 ºC +125 ºC

PACKAGE DESCRIPTION

Table 22 Package Characteristics

PACKAGE TYPE	PACKAGE REF	THERMAL RESIST. θ_{JC} / θ_{JA} (ºC/W)	JEDEC MOISTURE SENSITIVITY LEVEL & PEAK BODY TEMP	LEAD FINISH MATERIAL / JEDEC Pb-Free DESIGNATION	Pb Free Designation
44L Plastic Quad Flat Pack	44L 10x10 MQFP G	~12 / ~52	MSL 3 260 ºC	Matte Sn e3	RoHS Compliant
44L Quad Flat No Lead	44L QFN 7X7 G	~3 / ~30	MSL 1 260 ºC	Matte Sn e3	RoHS Compliant

Notes:
1. θ_{JA} is optimum with the exposed pad soldered to a PCB land with thermal vias connected to an internal ground plane.



	SYMBOLS	MIN	NOM	MAX
	A	-	-	2.70
	A1	0.25	-	0.50
	A2	1.80	2.00	2.20
1, 2	b (w/o plating)	0.25	0.30	0.35
	D	13.0	13.2	13.40
	D1	9.9	10.0	10.1
	E	13.0	13.2	13.4
	E1	9.9	10.0	10.1
	L	0.73	0.88	0.93
	e		0.80 BSC	
	θ°	0	-	7
	C	0.1	0.15	0.2

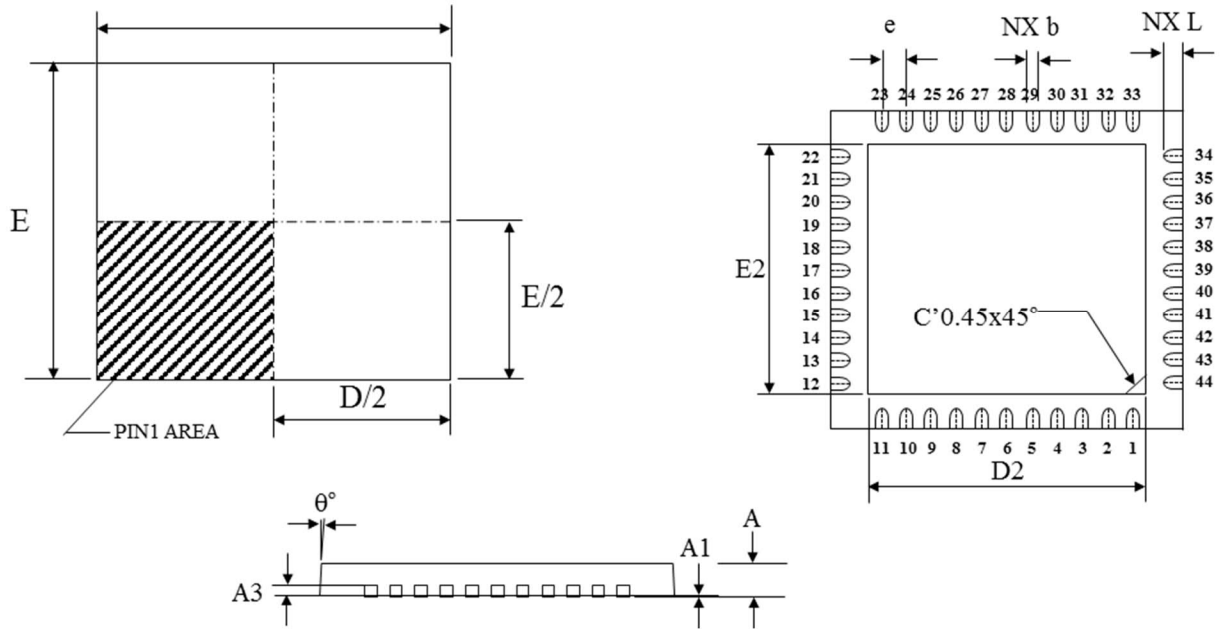
NOTES:
1. JEDEC OUTLINE:MO-108 AA-1

2. DATUM PLANE H IS LOCATED AT THE BOTTOM OF THE MOLD PARTING LINE COINCIDENT WITH WHERE THE LEAD EXITS THE BODY.

3. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25mm PER SIDE. DIMENSIONS D1 AND E1 DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE H.

4. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION.

Figure 15 44L PQFP (Plastic Quad Flat Package) Outline Drawing



JEDEC#	MO2201			
TYPE	44 TQFN			
Dimension	mm		mils	
SYMBOL	MIN	MAX	MIN	MAX
A	0.70	0.80	27.56	31.50
A1	0	0.10	0	3.94
A3	0.175	0.225	6.89	8.86
D	6.90	7.10	271.65	279.53
E	6.90	7.10	271.65	279.53
D2	5.45	5.55	214.57	218.50
E2	5.45	5.55	214.57	218.50
e	0.5 BSC		19.69 BSC	
NX b	0.20	0.30	7.87	11.81
NX L	0.35	0.45	13.78	17.72
θ°	0°	4°	0°	4°
ND	11			
NE	11			

NOTES

1. SPADE WIDTH, LEAD WIDTH AND LEAD THICKNESS EXCLUSIVE OF PLATING MATERIAL.
2. PACKAGE OUTLINE EXCLUSIVE OF MOLD FLASHES AND BURR DIMENSIONS.
3. COMPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS. COMPLANARITY SHALL NOT EXCEED 0.08mm.
4. WARPAGE SHALL NOT EXCEED 0.10mm.
5. THE TERMINAL #1 IDENTIFIER AND TERMINAL NUMBERING CONVENTION SHALL CONFORM TO JESD 95-1 SPP-012. DETAILS OF TERMINAL #1 IDENTIFIER ARE OPTIONAL, BUT MUST BE LOCATED WITHIH THE ZONE INDICATED. THE TERMINAL #1 IDENTIFIER MAY BE EITHER A MOLD OR MARKED FEATURE.
6. ND AND NE REFER TO THE NUMBER OF TERMINALS ON EACH D AND E SIDE RESPECTIVELY.

NOTE: The heat sink on bottom of package must be left floating or connected to GND. Do NOT connect to VDD.

Figure 16 44L QFN Outline Drawing