DEVICE ENGINEERING
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DEI1026
Six Channel Discrete-to-Digital Interface Sensing Open/Ground Signals

Features:

- Senses six Open/Ground Inputs
- Inputs are lightning protected to DO-160 Level 3
- TTL/CMOS-Compatible Tri-State Outputs
- Package / Temperature Options:
  - 16 lead .150" SOIC, -55°C /+85°C
  - 16 lead Ceramic 300mil SOP, -55°C /+125°C

SOIC package option

Functional Description:

The DEI1026 is a six channel discrete-to-digital interface BiCMOS device. It senses six Open/Ground discrete signals of the type commonly found in avionic systems. The inverted 3-state outputs are TTL/CMOS compatible and are enabled by the $\overline{OE}$ and $\overline{CE}$ pins. The inputs are lightning protected to meet the requirements of DO160 Sec 22 Waveforms 3, 4, and 5, Level 3. See figures 5-7. The device is available in a 16 lead .150 SOIC and .300 Ceramic SOP.

With its reliability, low cost, operating range, and lightning protection, the DEI1026 meets a large variety of interface requirements for aerospace applications.

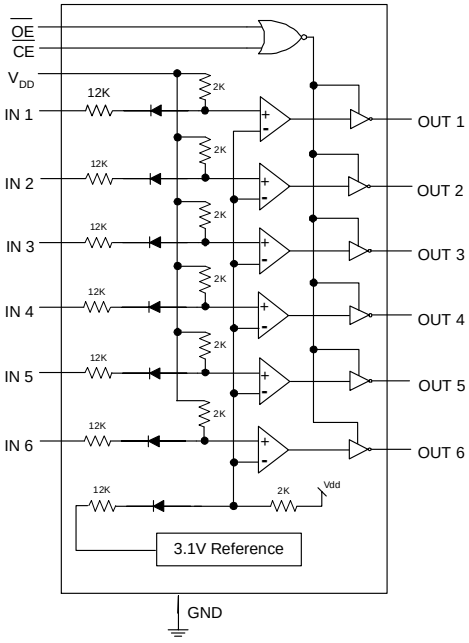


Figure 1: Function Diagram

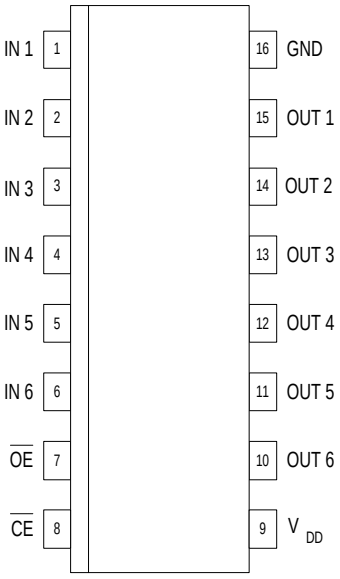


Figure 2: Pinout Diagram

Table 1: Absolute Maximum Ratings				
PARAMETER		**MIN**	**MAX**	**UNITS**
Supply Voltage V_{DD}		-0.3	7.0	V
Discrete Input Voltage (Pins 1-6)		-5	+40 *	V
Digital Input Voltage ($\overline{CE}$ and $\overline{OE}$)		V_{SS} - 0.3	V_{DD} + 0.3	V
Lightning Protection (Pins 1-6) DO160, Waveform 3; Level 3 DO160, Waveforms 4, and 5; Level 3		 -600 -300	 +600 +300	V
Junction Temperature			145	^{o}C
Storage Temperature	Plastic Ceramic	-55 -55	150 150	^{o}C
Operating Free Air Temperature	Plastic Ceramic	-55 -55	85 125	^{o}C
The DEI1026 contains circuitry to protect inputs from damage due to electrostatic discharge. It has been characterized per JEDEC A114-A Human Body Model to Class 1. Observe precautions for handling and storing Electrostatic Sensitive Devices.				
* The DEI1026 will withstand the transient surge DC voltage step function loci limits for category B equipment per MIL-STD-704A.				

Table 2: DEI1026 Device Operating Characteristics						
PARAMETER	**SYMBOL**	**CONDITIONS**	**MIN**	**TYP**	**MAX**	**UNITS**
Supply Voltage	V_{DD}		4.5	5.0	5.5	V
Free Air Operating Temp.	T_A	V_{DD} = 4.5 – 5.5 V Plastic Ceramic	 -55 -55		 85 125	^{o}C
Logic Output Sink Current	I_{OL}	V_{DD} = 4.5 – 5.5 V			5.0	mA
Logic Output Source Current	I_{OH}	V_{DD} = 4.5 – 5.5 V	-5.0			mA

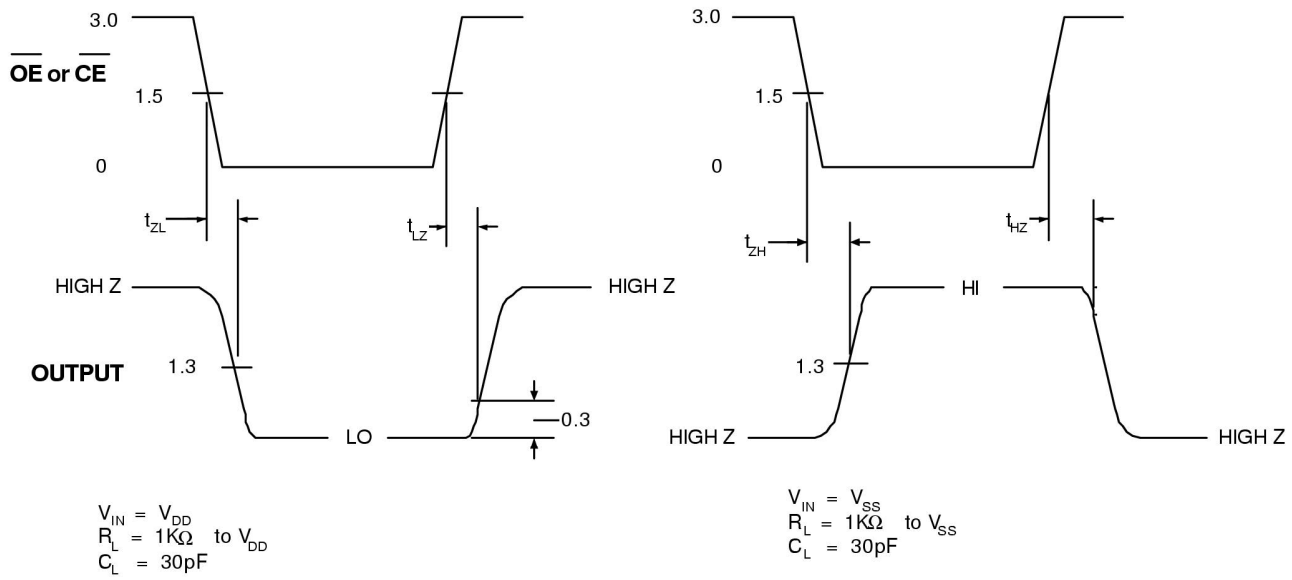
Table 3: DEI1026 Logic Truth Table			
CE (Chip Enable)	**OE (Output Enable)**	**Discrete Input**	**Output**
0	0	Open	0
0	0	Ground	1
1	X	X	High Z
X	1	X	High Z

Table 4A: DEI1026-G (Plastic) Electrical Characteristics (T_A = -55°C to +85°C , V_{DD} = 4.5 to 5.5 V, Unless otherwise noted)						
PARAMETER	**SYMBOL**	**CONDITIONS**	**MIN**	**TYP**	**MAX**	**UNITS**
Power Supply Characteristics						
Supply Current	I_{DD}	$V_{IN} = V_{DD}$ (all inputs) V_{DD} = 5.5 V		5	10	mA
Discrete Input Characteristics						
Ground state input voltage	V_{SG}	Voltage source from input terminal to ground for Logic High Output.			3.0	V
Open state input voltage	V_{SO}	Voltage source from input terminal to ground for Logic Low Output.	3.5			V
Ground state input resistor	R_{IG}	Resistor from input to ground to guarantee Logic High Output.	0		100	Ω
Open state input resistor	R_{IO}	Resistor from input to ground to guarantee Logic Low Output.	100k			Ω
Input source current	I_{IO}	Current sourced into 100 Ohm resistor to Ground.	-100	-330		µA
Reverse leakage current	I_{IR}	V_{IN} = 35 V, V_{DD} = 0 V			100	µA
Logic Input Characteristics						
$\overline{CE}$, $\overline{OE}$ input logic 1 level	V_{IH}		2.0			V
$\overline{CE}$, $\overline{OE}$ input logic 0 level	V_{IL}				0.8	V
DC Output Characteristics						
Output logic 1 level (TTL)	V_{OH}	I_{OH} = -5 mA	2.4			V
Output logic 0 level (TTL)	V_{OL}	I_{OL} = 5 mA (2)			0.4	V
Output logic 1 level (CMOS)	V_{OH}	I_{OH} = -100 µA	V_{DD} – 50mV			V
Output logic 0 level (CMOS)	V_{OL}	I_{OL} = 100 µA			V_{SS} + 50mV	V
Off-state Output Current	I_{OZ}	$\overline{OE}$ = V_{DD} V_{DD} = 5.5 V V_{OUT} = 0 or V_{DD}			+/-10	µA
Switching Characteristics [1]						
I/O propagation delay	t_{HL}, t_{LH}	Refer to Figure 4.			150	ns
Delay from $\overline{CE}$ or $\overline{OE}$ input (with output low) to output HI-Z	t_{LZ}	Refer to Figure 3.			25	ns
Delay from $\overline{CE}$ or $\overline{OE}$ input (with output HI-Z) to output low	t_{ZL}	Refer to Figure 3.			25	ns
Delay from $\overline{CE}$ or $\overline{OE}$ input (with output high) to output HI -Z	t_{HZ}	Refer to Figure 3.			25	ns
Delay from $\overline{CE}$ or $\overline{OE}$ input (with output HI-Z) to output high	t_{ZH}	Refer to Figure 3.			25	ns

Table 4B: DEI1026-WMB (Ceramic) Electrical Characteristics (T_A = -55°C to +125°C, V_{DD} = 4.5 to 5.5 V, Unless otherwise noted)						
PARAMETER	**SYMBOL**	**CONDITIONS**	**MIN**	**TYP**	**MAX**	**UNITS**
Power Supply Characteristics						
Supply Current	I_{DD}	$V_{IN} = V_{DD}$ (all inputs) V_{DD} = 5.5 V		5	10	mA
Discrete Input Characteristics						
Ground state input voltage	V_{SG}	Voltage source from input terminal to ground for Logic High Output.			3.0	V
Open state input voltage	V_{SO}	Voltage source from input terminal to ground for Logic Low Output.	3.5			V
Ground state input resistor	R_{IG}	Resistor from input to ground to guarantee Logic High Output.	0		100	Ω
Open state input resistor	R_{IO}	Resistor from input to ground to guarantee Logic Low Output.	100k			Ω
Input source current	I_{IO}	Current sourced into 100 Ohm resistor to Ground.	-100	-330		μA
Reverse leakage current	I_{IR}	V_{IN} = 35 V, V_{DD} = 0 V			100	μA
Logic Input Characteristics						
$\overline{CE}$, $\overline{OE}$ input logic 1 level	V_{IH}		2.0			V
$\overline{CE}$, $\overline{OE}$ input logic 0 level	V_{IL}				0.8	V
DC Output Characteristics						
Output logic 1 level (TTL)	V_{OH}	I_{OH} = -5 mA	2.4			V
Output logic 0 level (TTL)	V_{OL}	I_{OL} = 5 mA (2)			0.4	V
Output logic 1 level (CMOS)	V_{OH}	I_{OH} = -100 μA	V_{DD} – 50mV			V
Output logic 0 level (CMOS)	V_{OL}	I_{OL} = 100 μA			V_{SS} + 50mV	V
Off-state Output Current	I_{OZ}	$\overline{OE}$ = V_{DD} V_{DD} = 5.5 V V_{OUT} = 0 or V_{DD}			+/-10	μA
Switching Characteristics [1]						
I/O propagation delay	t_{HL}, t_{LH}	Refer to Figure 4.			170	ns
Delay from $\overline{CE}$ or $\overline{OE}$ input (with output low) to output HI-Z	t_{LZ}	Refer to Figure 3.			30	ns
Delay from $\overline{CE}$ or $\overline{OE}$ input (with output HI-Z) to output low	t_{ZL}	Refer to Figure 3.			30	ns
Delay from $\overline{CE}$ or $\overline{OE}$ input (with output high) to output HI -Z	t_{HZ}	Refer to Figure 3.			30	ns
Delay from $\overline{CE}$ or $\overline{OE}$ input (with output HI-Z) to output high	t_{ZH}	Refer to Figure 3.			30	ns

Notes:

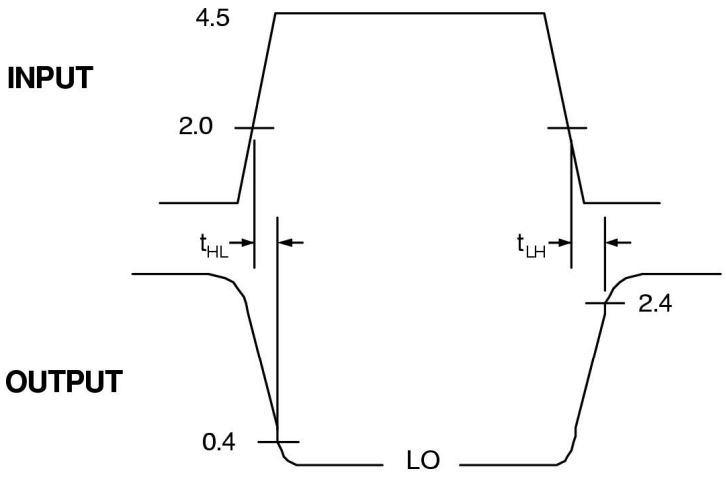
1. Guaranteed by design and not production tested.
2. Limit the sum of all IOL currents to 20ma. The Vsg spec may exceed limit beyond this current.



$V_{IN} = V_{DD}$
$R_L = 1K\Omega$ to V_{DD}
$C_L = 30pF$

$V_{IN} = V_{SS}$
$R_L = 1K\Omega$ to V_{SS}
$C_L = 30pF$

Figure 3: Enable to Output Propagation Delay



$R_L = 1K\ \Omega$ to V_{DD}
$C_L = 30pF$

Figure 4: Input to Output Propagation Delay

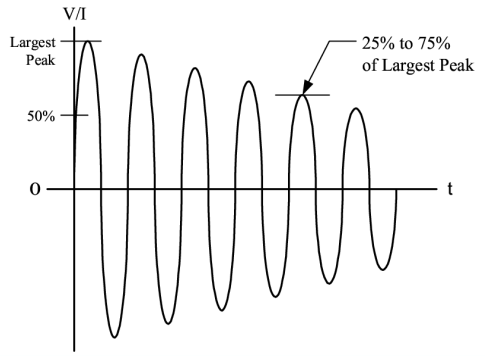


Figure 5: DO160 Voltage Waveform #3
V_{OC} = 600V, I_{SC} = 24A, Frequency = 1.0MHZ ±20%

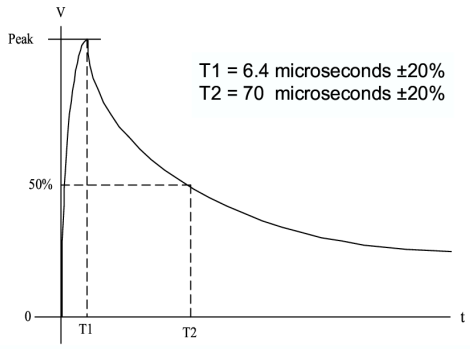


Figure 6: DO160 Voltage Waveform #4
V_{OC} = 300V, I_{SC} = 60A

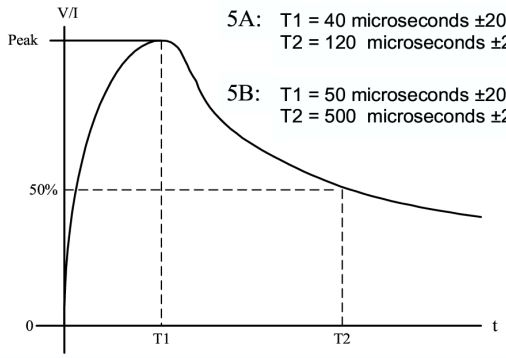


Figure 7: DO160 Voltage Waveform #5
V_{OC} = 300V, I_{SC} = 300A

Notes:
1. V_{OC} = Peak Open Circuit Voltage available at the calibration point.
2. I_{SC} = Peak Short Circuit Current available at the calibration point.
3. Amplitude tolerances: +10%, -0%
4. The ratio of V_{OC} to I_{SC} is the generator source impedance to be used for generator calibration purposes.

PACKAGE TYPE	16 Lead SOIC Narrow Body, Green	16 Lead Ceramic SOP
REFERENCE	16L SOIC NB G	16L CSOP
THERMAL RESISTANCE:		
θ_{JA} (4 layer PCB with Power Planes)	74 °C/W	-
θ_{JC}	24 °C/W	23 °C/W
JEDEC MOISTURE SENSITIVITY LEVEL (MSL)	MSL 1 / 260°C	Hermetic
LEAD FINISH MATERIAL / JEDEC Pb-free CODE	NiPdAu e4	Au e4
Pb-Free DESIGNATION	RoHS Compliant	Pb Free
JEDEC REFERENCE	MS-012-AC	-

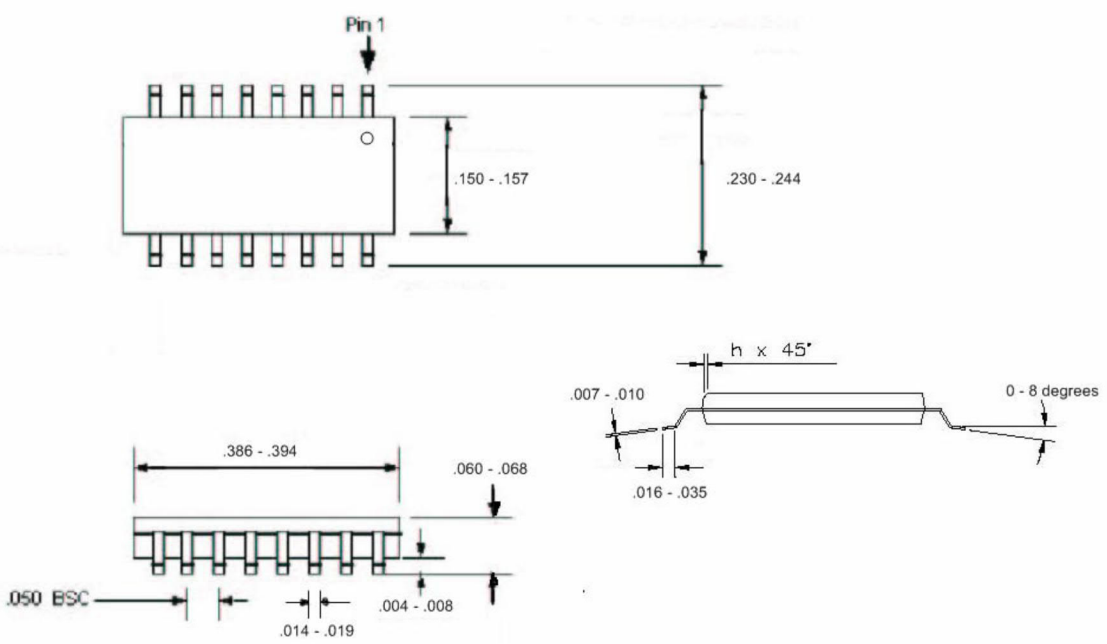


Figure 8: Mechanical Outline, 16 lead SOIC -G Package

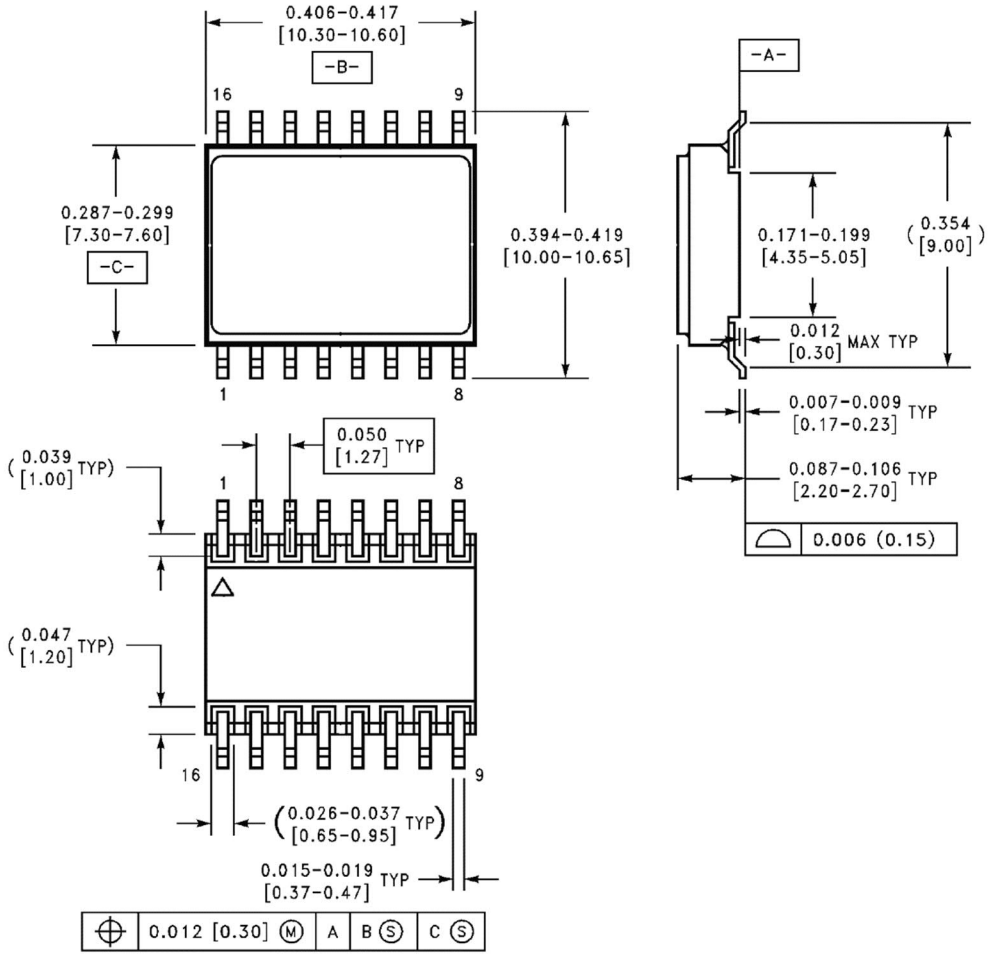


Figure 9: Mechanical Outline, 16 lead Ceramic SOP

Table 6: Ordering Information				
DEI PART NUMBER	**MARKING (1)**	**PACKAGE**	**OP. TEMP. RANGE**	**PROCESSING**
DEI1026-G	DEI1026 E4 (2)	16L SOIC NB G	-55 / +85ºC	Standard
DEI1026-WMB	DEI1026-WMB	16 lead ceramic SOP	-55 / +125ºC	Burn In, 96 hr @125ºC

NOTES:
1. All packages marked with Lot Code and Date Code.
2. "E4" after Date Code Denotes Pb Free category.