SB-3644 DIGITAL-TO-SYNCHRO/RESOLVER PMC INTERFACE CARD HARDWARE MANUAL

MN-3644XXX-001

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Revision	Date	Pages	Description
Pre A	12/2016	All	Preliminary Release
Pre B	2/2017	All	Updated Preliminary Release
Pre C	4/2017	All	Updated Preliminary Release
Rev A	10/2017	All	Initial Release
Rev B	2/2018	20 – 22	Software section updated
Rev C	3/2018	9, 10, 22	Update to Order Information, update to thermal section of spec table.
Rev D	3/2018	16	New Section 4.3.1, added Figure 5.
Rev E	2/2019	20, 22, 23	Updated channel enumeration to align with software, added section on LabVIEW support, updated ordering information
Rev F	4/2019	8, 9, 10	Spec Table header updated

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1 PREFACE

This manual uses typographical conventions to assist the reader in understanding the content. This section will define the text formatting used in the rest of the manual.

1.1 Text Usage

- **BOLD** – indicates important information and table, figure, and chapter references.
- `Courier New –` indicates code examples.
- <…> - indicates user - entered text or commands.

1.2 Standard Definitions

PCI	Peripheral Component Interconnect
PMC	PCI Mezzanine Card

1.3 Special Handling and Cautions

The SB-3644 series uses state-of-the-art components, and proper care should be used to ensure that the device will not be damaged by Electrical Static Discharge (ESD), physical shock, or improper power surges and that precautions are taken to avoid electrocution.

Warnings: Turn off power to the computer hardware and unplug from wall.

NEVER insert or remove card with power turned on.

Ensure that standard ESD precautions are followed. As a minimum, one hand should be grounded to the power supply in order to equalize the static potential.

Do not store disks in environments exposed to excessive heat, magnetic fields or radiation.

1.4 Trademarks

All trademarks are the property of their respective owners.

1.5 What is included in this manual?

This manual contains a complete description of hardware installation and use.

1.6 Technical Support

In the event that problems arise beyond the scope of this manual, you can contact DDC by the following:

US Toll Free Technical Support:
1-800-DDC-5757, ext. 7771

Outside of the US Technical Support:
1-631-567-5600, ext. 7771

Fax:
1-631-567-5758 to the attention of Motion Feedback Technologies Applications

DDC Website:
www.ddc-web.com/ContactUs/TechSupport.aspx

Please note that the latest revisions of Software and Documentation are available for download at DDC's Web Site, www.ddc-web.com.

2 OVERVIEW

The SB-3644 is a Front-I/O PCI Mezzanine Card (PMC) with four channels of synchro and resolver simulation. The SB-3644 utilizes a PCI interface (*Revision 3.0 Compliant 32-bit, 33/66 MHz*). It is available in the industrial operating temperature range.

2.1 Features

Synchro/Resolver Simulation

- Four Independent Digital-to-Synchro/Resolver Channels
  - 0 to 11.8Vrms Synchro/Resolver at 360 Hz to 10 kHz
- Up to 1 Arc Minute Accurate Simulation Channels
- Software Programmable Resolution (10 – 16 bits)
- Self-Test, and Built-in-Test Outputs
- Up to 15 mA Synchro/Resolver Output Drive
- Programmable Dynamic Rotation (up to 7099.2 rps)
- Configurable Two-Speed Simulation
- Loss of Reference Detection

General

- VITA-47 Shock and Vibration Tested
- RoHS Compliant (Lead-free and hazardous substance-free)
- -45º to +85ºC Temperature Range (with 300 LFM airflow)
- Over-Current/Thermal Protection
- 32-bit/66 MHz PCI Rev. 3.0 Compliant Interface
- Operates in 3.3V or 5V PCI Signaling Environments
- Front Panel I/O (68-Pin) Air-Cooled Design
- Only 5V & 3.3V Supply Required (+/-12V not needed)
- Four Pairs of Opto-Isolated Discrete Inputs and Outputs for External Control Functions
- Any Simulation Channel Can be Used as a Sine Reference Oscillator

The card includes **SB-36030Sx Motion Feedback Library** along with code samples and detailed documentation. To install the latest official software from DDC, download via DDC's website at www.ddc-web.com/.

2.2 System Requirements

- PCI-PMC connector supporting 3.3 or 5V PCI signaling
- PCI-PMC connector with +5V and 3.3V supply voltage available
- A supported operating system

2.3 Configuration Options

Table 1. I/O Channel Count and Output Options

Ordering Option	SB-3644			
	Channel Count	Signal Output	Operating Frequency	Accuracy
1	4	0 to 11.8Vrms Synchro/Resolver	360 to 10 kHz	1 arc-minute

2.4 Applications

The SB-3644 PMC card's rugged construction and ability to operate over the industrial temperature range makes it ideal for use in mission computers and other embedded systems. This device can be combined with carrier cards for use in VME or cPCI control systems employing 33/66MHz bus. The card also provides an ideal solution for encoder-based systems that have Synchro or Resolver inputs. The card is a valuable addition to design and test teams involved with synchro or resolver simulation and positioning.

Synchros and resolvers are used in applications such as motor control, industrial automation, robotics, antenna positioning, and valve control. Applications include modern high performance industrial and military position feedback and control systems. Typical motion feedback applications include motor control, machine tool control, antenna control, robotics, and process control systems.

2.5 Mechanical Design

The SB-3644 is a Front-I/O air-cooled PCI Mezzanine Card (PMC) designed to meet or exceed vibration requirements specified in VITA-47 for a class V2 in air-cooled applications. The SB-3644 card also features CCPMC (Conduction Cooled PMC) thermal rails and connector "anti-fretting" mounting holes per VITA-20-2005.

The front panel I/O connector layout uses a 68-pin front panel connection. The board has conduction rails that do not interfere with the front panel connector. The front panel connector includes a metal backshell with fastening thumbscrews.

The SB-3644 is designed to meet or exceed the humidity requirements of ANSI/VITA 47, and has been tested to withstand 95% humidity.

To operate within the specified -40 to +85 ºC operating temperature, supplemental air cooling of 300 LFM (Linear Feet per Minute) in the system is required. The SB-3644 utilizes a custom heat sink design using the conduction cooled rails to efficiently operate within the temperature range.

MTBF (Mean Time Between Failure) report is available upon factory request.

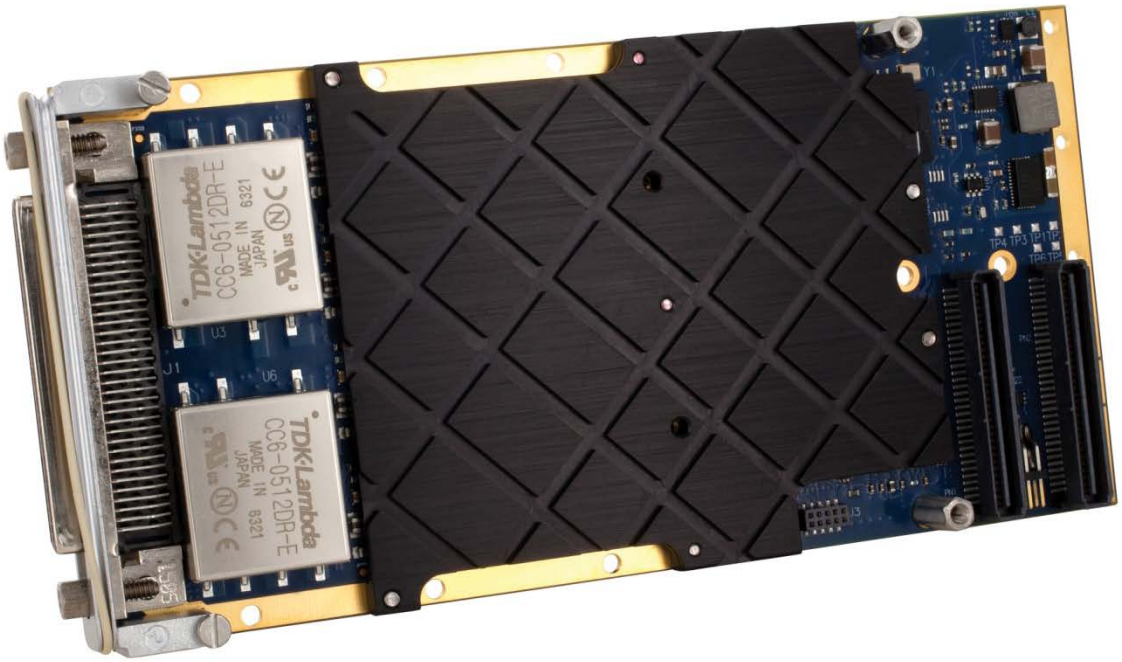

Figure 1. SB-3644 Digital-to-Synchro/Resolver PMC Card

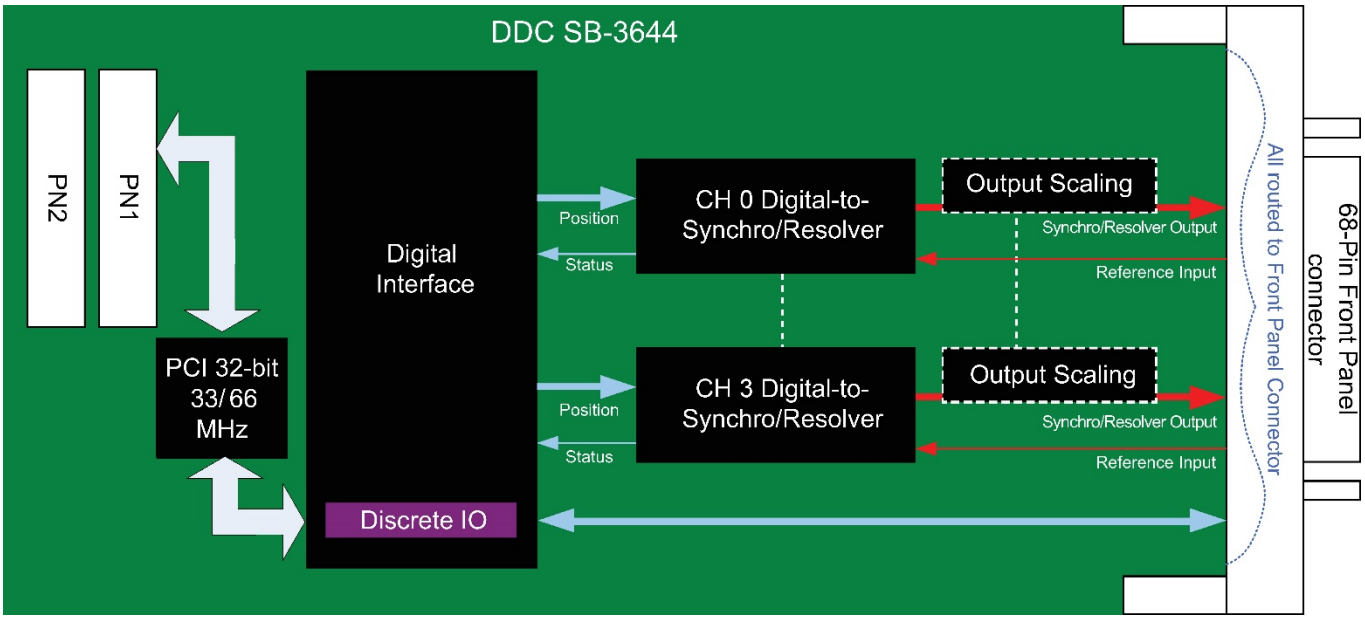

Figure 2. SB-3644 Architecture

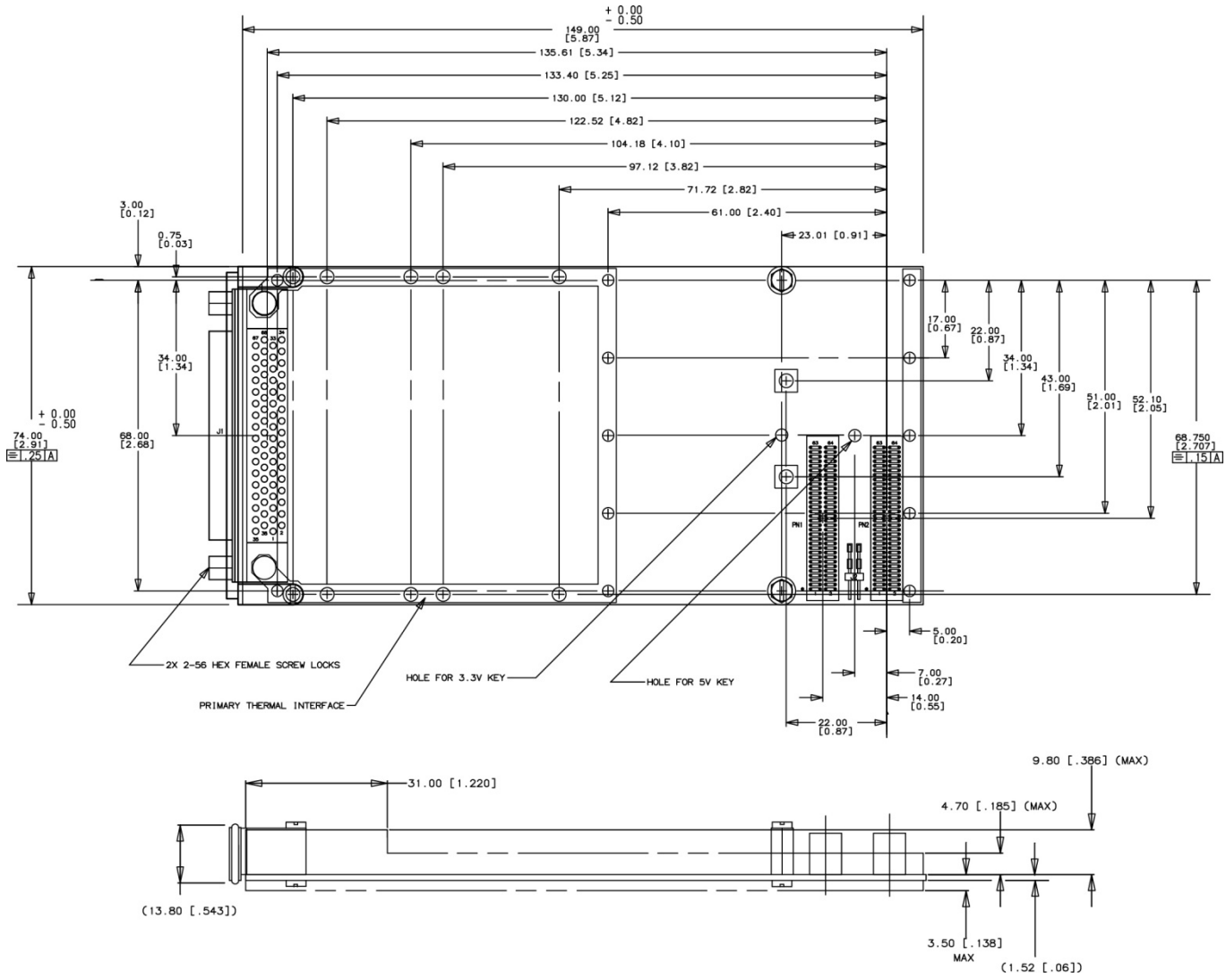

Figure 3. SB-3644 Mechanical Outline

2.6 Specifications

Table 2. SB-3644 Specification Table

These specs apply over the rated power supply, temperature, and reference frequency ranges: 10% signal amplitude variation, and 10% harmonic distortion (for values without a tolerance already specified).

PARAMETER	MIN	TYP	MAX	UNITS
SIMULATION CHANNEL OUTPUTS				
Accuracy		1		Arc-Minutes
Resolution	10		16	Bits
Synchro/Resolver (Differential) Signal Output	0	11.8	12.98	Vrms
Resolver (Single-Ended) Signal Output	0	6.8	7.48	Vrms
Output Drive			15	mA
Available Transformation Ratios				
26Vrms Reference, 11.8Vrms Simulation	0.4084	0.4538	0.4992	
26Vrms Reference, 6.8Vrms Simulation	0.2353	0.2615	0.2877	
6.8Vrms Reference, 6.8Vrms Simulation	0.9	1.0	1.1	
6.8Vrms Reference, 11.8Vrms Simulation	1.557	1.73	1.903	
115Vrms Reference, 11.8Vrms Simulation	0.0923	0.1026	0.1128	
REFERENCE CHANNEL INPUTS				
Operating Frequency Range	360		10k	Hz
CHx_RH_115V_IN & CHx_RL_115V_IN pins (for 0.1026 Transformation Ratio use only)				
Voltage	0	115	120.75	Vrms
Common-mode Range (includes peak Reference signal)			240	V
Z_{in} Single-Ended	635.5			kΩ
Z_{in} Differential	1.3			kΩ
CHx_RH_IN & CHx_RL_IN pins (not for 0.1026 Transformation Ratio use)				
Voltage	0	6.8 or 26	27.3	Vrms
Common-mode Range (includes peak Reference signal)			15/50	V
Z_{in} Single-Ended	99.5			kΩ
Z_{in} Differential	199			kΩ
DYNAMIC ROTATION				
at 10 bit resolution			7099.2	RPS
at 11 bit resolution			3549.6	RPS
at 12 bit resolution			1774.8	RPS
at 13 bit resolution			887.4	RPS
at 14 bit resolution			443.7	RPS
at 15 bit resolution			221.8	RPS

Table 2. SB-3644 Specification Table

These specs apply over the rated power supply, temperature, and reference frequency ranges: 10% signal amplitude variation, and 10% harmonic distortion (for values without a tolerance already specified).

PARAMETER	MIN	TYP	MAX	UNITS
at 16 bit resolution			110.9	RPS
POWER SUPPLY REQUIREMENTS				
Voltages/Tolerances				
+5 V	4.75	5	5.25	V
+3.3 V	3.0	3.3	3.6	V
Current Drain (+5V)				
Idle			0.810	A
100% Load			1.0	A
Current Drain (+3.3V)				
Idle			0.65	A
100% Load			0.825	A
DISCRETE DIGITAL I/O				
V_{IL}			3	V
V_{IH}			30	V
V_{OL}			1.5	V
V_{OH}			30	V
PCI INTERFACE				
Bit Size			32	bits
Clock Speed			66	MHz
Bus Signaling (Universal Bus Voltage)		+ 3.3 / + 5		V
COOLING METHOD				
Air-cooled (Required for industrial temp. range)			300	LFM
THERMAL				
Card Operating Temperature Range (2A0)				
with 300 LFM air-flow	-40		+85	°C
without air-flow, condition of no load or when used to drive DDC SBA	-40		+55	°C
Storage Temperature	-65		+150	°C
MECHANICAL DESIGN				
Shock	Vita-47 / MIL-STD-810, TM516, Class S1 for CC (50 g, 11ms, half-sine, 18 shocks total)			
Vibration	Vita-47/MIL-STD-810, TM514, “V2” (AC)			
Humidity	Vita-47/MIL-STD-810, TM507, Procedure II			
PHYSICAL CHARACTERISTICS				
Size	2.91 x 5.87 x 0.39			in.

Table 2. SB-3644 Specification Table

These specs apply over the rated power supply, temperature, and reference frequency ranges: 10% signal amplitude variation, and 10% harmonic distortion (for values without a tolerance already specified).

PARAMETER	MIN	TYP	MAX	UNITS
		(74.0 x 149.0 x 10.0)		(mm.)
Weight		5.3 (150)		oz. (g)

Notes:

1. The specifications apply over the rated power supply, temperature, and reference frequency ranges.
2. Resolution is 16 bits for all static angles and is software programmable for 10 – 16 bits for dynamic rotation.
3. Typical output voltage assumes a typical reference input voltage. The output voltage is scalable within the specified voltage range by adjusting the reference input. See Section 4.2.1 for more details.
4. Reference Input Frequencies below 360 Hz are possible but are not characterized for accuracy. DC offset voltages will degrade accuracy if a DC reference is applied. LOR and frequency detection will indicate a fault with a DC reference.
5. All power measurements were taken with a 66-MHz PCI bus.
6. Minimum impedance is guaranteed over the operating range, but is not tested.

3 HARDWARE INSTALLATION

The SB-3644 card is a 32-bit, 33/66MHz PCI Local Bus Rev. 3.0 compliant interface target device that may be inserted into any compatible slot. Note that this card is capable of universal PCI signal and automatically defaults to 3.3V or 5V depending on the host bus.

When installing the card, the following should be observed:

- **NEVER** insert or remove the card with the power turned on.
- **ALWAYS** take proper precautions to guard against static damage.
- Use a wrist strap if available, or ensure proper static grounding by touching the power supply cover **WITH POWER OFF**.
- Insert the card at a slight angle so that the connectors first protrude from the rear opening and then gently press the card into the motherboard connector. Secure with proper hardware.
- Make sure that adjacent cabling and wiring do not hinder the airflow around the card.

This card is designed as a Plug-and-Play device and as such, there are no jumpers or switches to be set for address and interrupt selection.

3.1 Hardware Configuration and Operation

The SB-3644 card utilizes the PCI interface, and as such does not require any jumpers or switches to set the Base address or interrupt values. The configuration for Plug-and-Play PCI is performed by the operating system. During the initial power on boot process, the system performs an enumeration of the PCI bus and allocates a resource configuration that satisfies the card requirements. The system will save the configuration information in the SB-3644's PCI configuration space registers. These registers are configured at the factory to contain information that identifies the card type, vendor, required memory sizes, and interrupt resources. When the driver loads, it will access the configuration registers and identify how the system has configured the card. After identifying each of the installed cards, the device driver will enumerate each of the channels on the card and create a configuration structure that defines the allocated address and interrupt. The end user does not need to know this information if using one of the supplied C API libraries to operate the card.

4 DETAILED ARCHITECTURE

4.1 PCI Interface

The card provides a target 32-bit PCI interface, as defined in the PCI Local Bus Specification, Rev 3.0, which operates at clock speeds of up to 66 MHz for applications where a higher bus speed is desired. If a 33 MHz device was placed on a 66 MHz bus, the bus speed would be forced to slow down to 33 MHz. Although synchro/resolver simulation may not require the additional bandwidth of a 66 MHz bus, the SB-3644 66 MHz device allows the base CPU PCI bus to run at 66 MHz, enabling other high-speed devices on the bus to take advantage of the higher bandwidth.

When using the card with the supplied RTL (SB-36030Sx) and drivers there is no need to reference the PCI configuration registers.

Connection to the host is established through the card's Pn1 and Pn2 connectors. PCI 64 bit extension is not supported, the PMC Pn3 for PCI 64 bit extension and Pn4 for user I/O connectors are not populated on the card.

4.1.1 Use with 3.3V or 5V PCI Signaling

The PCI interface signals on the SB-3644 support +3.3V or +5V signaling. The device incorporates both 3.3V and 5V signal keying holes.

4.1.2 Register & Memory Addressing

The SB-3644 PCI interface contains a set of "Type 00h" PCI configuration registers that are used to map the device into the host system. The configuration register space is mapped in accordance with PCI Revision 3.0 specifications. These registers are arranged such that all memory and register space may be addressed through a single PCI function.

Configuration registers implement the Subsystem Vendor and Device ID, and control the Fail-Safe operation of the device. There is one Base Address Register (BAR) used on the design of this card. All BAR mapping is located in PCI configuration register space.

When using this card with DDC's driver and the API library software, the details of these registers and memory addresses are abstracted from the user to provide an easy-to-use High Level "C" programming environment.

4.2 Digital to Synchro / Resolver Channels

4.2.1 Synchro / Resolver Interface

Each output channel is software configurable to provide the following different signal types:

1. Synchro (S1, S2, S3)
2. Differential Resolver (S1, S2, S3, S4)
3. Single-ended Resolver (S2 [Cos], S3 [Sin])

In Differential Resolver mode, S1:S3 is differential sine and S2:S4 is differential cosine.

Unused outputs are inactive (e.g. in Synchro mode, S4 is turned off, in single-ended resolver, S1 & S4 are turned off).

Note: *Unused outputs should never be grounded. AGND (analog ground) should be used as returns for single-ended configuration.*

4.2.1.1 Output Status

The active status of each specific output (S1-S4) for all channels is constantly monitored in an internal register that is accessible through software. This status is dependent on both the output type mode and if the output is in an over-temperature/over-current condition.

For example, if the output type selected is Synchro, S1-S3 should be active while S4 is inactive. If an over-temperature/over-current condition occurs on S1-S3, the outputs will go inactive. The outputs will become active again once the fault condition no longer exists.

The S1-S4 output signal amplifiers utilized in the design have thermal shutdown protection if the junction temperature of the device exceeds 150 ºC, protecting the card from damage. When the amplifier junction temperature cools to 130 ºC, the amplifiers will come out of thermal shutdown.

4.2.2 Synchro / Resolver Output Signal Voltages

The output voltage for each channel is determined by the reference input voltage and transformation ratio. The transformation ratio is software configurable. See Table 3 for the different output voltage configurations.

The 0.1026 Transformation Ratio is only available using the 115Vrms CHx_RH_115V_IN and CHx_RL_115V_IN pins.

Table 3. Output Voltage Configurations				
Board	**Interface**	**Nominal Reference Input Voltage (Vrms)**	**Transformation Ratio (TR)**	**Nominal Output Voltage (Vrms)**
SB-3644	Synchro/Resolver	26	0.4538	11.8
	Single-ended Resolver	26	0.2615	6.8
	Single-ended Resolver	6.8	1	6.8
	Resolver	6.8	2	13.6
	Resolver	115	0.1026	11.8

Note: Do not attempt to scale for higher output voltages by inputting a reference voltage above the maximum voltages specified in the Section 2.6.

4.2.3 Status Detection

4.2.3.1 Reference Input Frequency Detection

Each channel is capable of reporting back the carrier frequency (Hz) that is being applied to its reference inputs (RH/RL). The tolerance on this reading is +/- 5%.

4.2.3.2 Loss of Reference Status

Each channel has the capability to detect for Loss-of-Reference (LOR). If the reference input to a channel falls below a threshold, an internal register flag will be set to logic 1 to indicate an LOR condition.

The LOR threshold for the SB-3644 is dependent on the maximum reference input voltage of the output type selected (Refer to Table 3).

- For a maximum reference input voltage of 26 Vrms, the LOR threshold is 3.8 Vpeak.
- For a maximum reference input voltage of 6.8 Vrms, the LOR threshold is 1 Vpeak.
- For a maximum reference input voltage of 115Vrms (using high-voltage reference input pins), the LOR threshold is 16.9 Vpeak.

4.2.3.3 DC-to-DC Converter Status

There are up to two DC-to-DC converters on the device that are used for the digital-to-Synchro / Resolver channels: converter A for channels 1 and 2 and converter B for channels 3 and 4. Each DC-to-DC converter has over current protection.

If either one goes into an over current condition, a power cycle to the computer will be necessary to restore the device to operational conditions. Each DC-to-DC converter's active status is monitored in a register accessible through software; see SB-36030Sx Software Manual for details. The over-current threshold and delay time of over current condition is not quantified. Under normal operation within the specified parameters, in Table 1, over current/over temperature should not be encountered.

4.2.4 Achieving Higher Output Voltages with an SBA-3500

The output voltage can be amplified for higher voltage and more power by using the SB-3644 in conjunction with the SBA-3500 Synchro Booster Amplifier. By connecting both the SB-3644 and the SBA-3500 to one differential reference source as shown in Figure 4, a user can provide 90Vrms synchro signals at up to 25VA. See SBA-3500 datasheet for detailed product information.

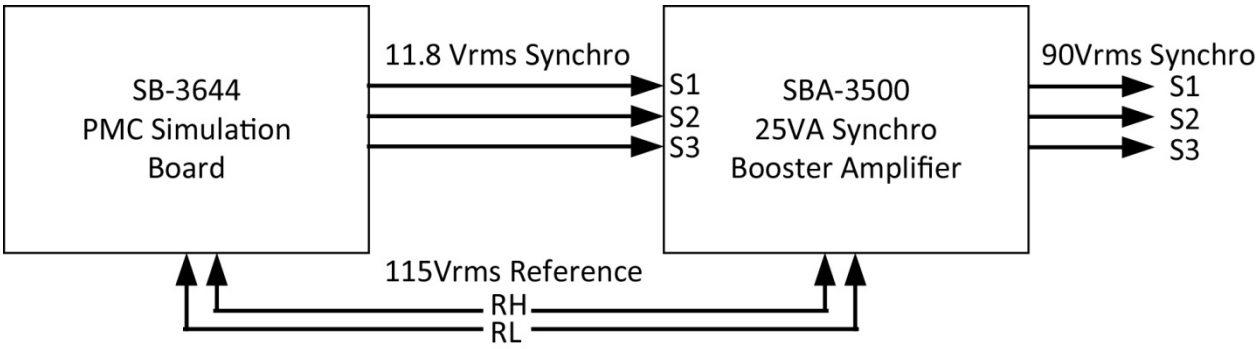

Figure 4. SB-3644 and SBA-3500 Block Diagram

4.2.1 Scaling Lower Output Voltages

The output voltage can be scaled down by lowering the reference input voltage as follows:

Reference Input Voltage = Desired Output Voltage / TR

Example:

Desired Output Voltage = 10 Vrms

Transformation Ratio (TR) = 0.4538

Reference Input Voltage = 10 Vrms / 0.4538

Reference Input Voltage = 22 Vrms

4.3 Additional Functionality

4.3.1 Configuring a Simulation Channel as a Sine Reference Oscillator

Any simulation channel can be used as a sine reference oscillator by providing a DC voltage as the board's reference input. The specific channel is programmed to dynamic mode, simulating a constant rotation. The programmed rotation speed corresponds to a frequency of the AC output waveform, and results in a time-varying voltage waveform. For detailed information on the setup, see Application Note AN/MFT13, available for download at www.ddc-web.com.

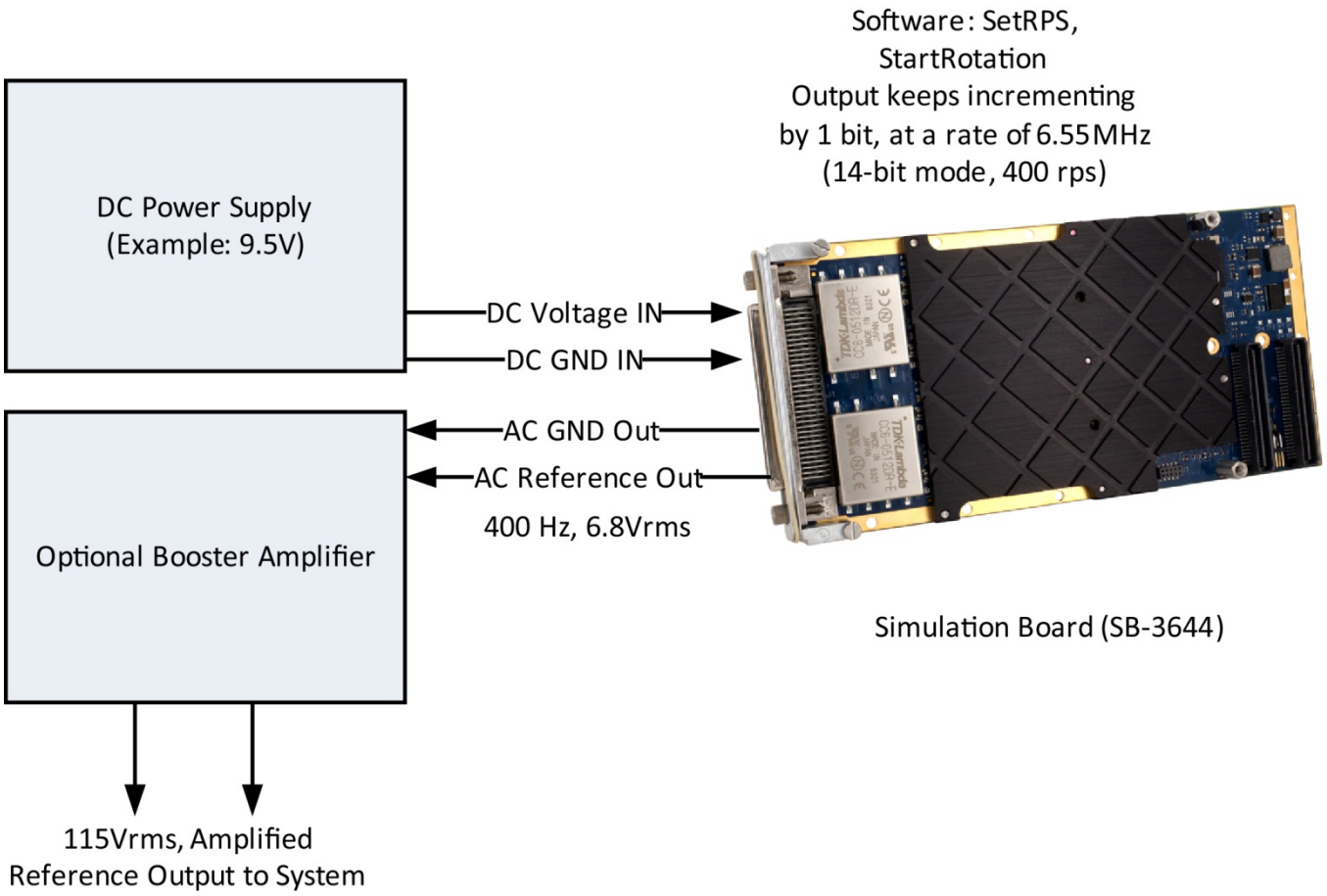

Figure 5. Simulation Board used as Sine Reference Oscillator Block Diagram

4.3.2 Sync Pulse

A sync pulse output is available for each channel and is located on the J1 Front Panel connector. The functionality of the sync pulse depends on whether the channel is in static mode (not rotating) or dynamic mode (rotating).

In static mode, a pulse will occur when an angle is written to the channel.

In dynamic mode, a pulse will occur when the output crosses 0°.

The sync pulse width is 100 µSec.

4.3.3 Self-Test

The device has a built-in self-test capability which uses an internal DC reference to exercise all channels and indicate a pass or fail status for each channel. This information is reported through a register that is accessible through software. See SB-360S03x Software Manual for details.

4.3.4 Two-Speed Mode

Two-speed mode allows resolutions greater than 16 bits to be achieved. Two-speed mode may be implemented for both static angles and rotations. The procedure to use two-speed mode is described in Software Manual SB-36030Sx. For more information on two-speed mode, refer to the Two-Speed Application Note (*AN/MFT-10*), the RD/RDC Applications Manual (MN-19220XX-001) and the Synchro/Resolver Conversion Handbook. These documents are available at www.ddc-web.com.

4.3.5 Discrete I/O

The SB-3644 has 4 discrete inputs and 4 discrete outputs. Outputs are physically driven by the output of the Darlington open-collector drivers. Output pins are opto-isolated by opto-couplers whose output current sinking capability has been increased using a discrete transistor connected in a Darlington configuration. The emitters of all the output transistors are the pins labeled "GND_EXT" on the connector. The inputs are also referenced to these same pins. The opto-isolators provide up to 1500 Vac isolation for the discrete I/O on the card.

The discrete digital I/O can be used for a variety of applications including triggering events, indicating status, or general purpose use.

Refer to SB-36030Sx Software Manual for Discrete I/O operation/control.

4.3.5.1 I/O Characteristics

- Discrete Outputs:
  - Max Output Voltage = 30 V
  - Any single output can drive 100 mA at 25° C
- Discrete Inputs:
  - Input pins are directly connected to inputs of the opto-couplers.
  - Max Input voltage = 30 V
  - Input impedance is approximately 2.7 kΩ with input turned on and high impedance with input approximately less than 3 V

4.4 Card Pinouts

This section delineates the pinouts for the card. The front-panel configuration allows all signals to pass through a 68-pin I/O connector. Note that PCI signal inputs are via Pn1 & Pn2 ports on the PMC connector.

The front panel connector described here contains each channel's Synchro/Resolver Interface Signals, Reference Inputs, and Programmable Digital I/O signals.

Table 4. Signal List

SIGNAL NAME	Direction	Description
CHx_RH_IN	Input	Channel Reference High (up to 26Vrms)
CHx_RL_IN	Input	Channel Reference Low (up to 26Vrms)
CHx_RH_115V_IN	Input	Channel Reference High (up to 115Vrms)
CHx_RL_115V_IN	Input	Channel Reference Low (up to 115Vrms)
CHx_S1	Output	Channel S1 Signal
CHx_S2	Output	Channel S2 Signal
CHx_S3	Output	Channel S3 Signal
CHx_S4	Output	Channel S4 Signal
DIO_x_IN	Input	Discrete Input
DIO_x_OUT	Output	Discrete Output
SYNC_x	Output	Sync Pulse
GND_EXT	Ground	External ground reference connection
AGND	Ground	Analog ground reference connection
DGND	Ground	Digital ground reference connection
EXT_FLASH_WRITE_EN_L	Flashing	For new firmware flashes only. No Connect during normal use
BOOT_SELECT	Flashing	For new firmware flashes only. No Connect during normal use

Note: Within each Signal Name, "x" designates a particular channel number.

4.4.1 Front Panel I/O Connector

The connector (soldered on the board) used for the front-panel I/O connection is a 68-pin (TE/Amp P/N 5787170-7). Pin numbering designations for the connector are as shown in Figure 7.

Figure 6. 68-Pin I/O Connector Photograph

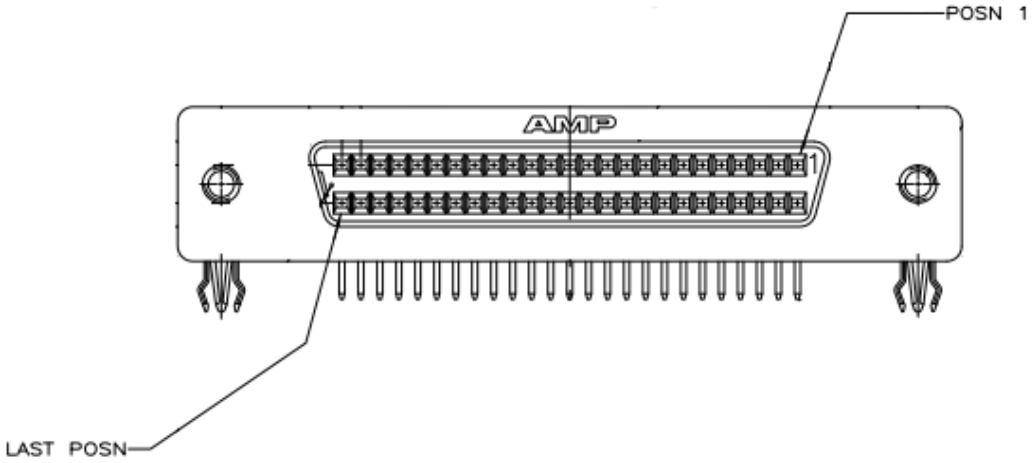

Figure 7. 68-Pin I/O Connector Pin Locations
(Viewed from front panel of card, 1 to 34 top row, 35 to 68 bottom row)

4.4.2 Supplied I/O Mating Connector Components

The SB-3644 is supplied with the I/O mating connector components as listed in Table 5. These components may be used to construct a cable to interface to the I/O on the card. Table 6 lists the Front Panel Connector Pinout.

Table 5. Supplied I/O Mating Connector Components

Connector Description	Part Number (Pickering)	Part Number (DDC)
Pickering SCSI style Micro-D Solder Bucket Connector and Backshell	40-962A-068-SB-M	5301-0987-0001

Table 6. Front Panel Connector Pinout			
PIN	**NAME**	**PIN**	**NAME**
1	CH3_RL_115V_IN	35	CH3_RH_115V_IN
2	CH3_S2	36	CH3_RH_IN
3	CH3_RL_IN	37	DIO_1_IN
4	CH3_S1	38	DIO_2_IN
5	DIO_1_OUT	39	DGND
6	CH43S3	40	DIO_0_IN
7	DIO_2_OUT	41	SYNC_A
8	CH3_S4	42	SYNC_D
9	DIO_3_OUT	43	SYNC_C
10	CH2_S2	44	DIO_3_IN
11	CH2_RL_115V_IN	45	AGND
12	CH2_S1	46	CH2_RL_IN
13	DIO_0_OUT	47	FACTORY
14	CH2_S3	48	SYNC_B
15	CH2_RH_115V_IN	49	AGND
16	CH2_S4	50	EXT_FLASH_WRITE_EN_L
17	CH2_RH_IN	51	BOOT_SELECT
18	CH1_S2	52	GND_EXT
19	GND_EXT	53	GND_EXT
20	CH1_S1	54	AGND
21	GND_EXT	55	GND_EXT
22	CH1_S3	56	AGND
23	CH1_RL_IN	57	GND_EXT
24	CH1_S4	58	DGND
25	CH1_RL_115V_IN	59	DGND
26	CH0_S2	60	DGND
27	CH1_RH_115V_IN	61	DGND
28	CH0_S1	62	AGND
29	CH1_RH_IN	63	AGND
30	CH0_S3	64	AGND
31	GND_EXT	65	AGND
32	CH0_S4	66	AGND
33	CH0_RL_IN	67	CH0_RH_IN
34	CH0_RL_115V_IN	68	CH0_RH_115V_IN

Notes:
1. All AGND and DGND pins are internally common
2. FACTORY indicates a Factory Test Point. Do Not Connect
3. EXT_FLASH_WRITE_EN_L and BOOT_SELECT are for flashing new firmware. No Connect if not flashing
4. SYNC_A is for Channel 0, SYNC_B is for Channel 1, SYNC_C is for Channel 2, SYNC_D is for Channel 3

5 SOFTWARE

Numerous software packages are available for the SB-3644. The DDC software packages are developed to allow shorter design cycles while allowing all SB-3644 functionality to be accessed by user level code.

The available software packages include:

- Motion Feedback C SDK (SB-36030Sx)
- Motion Feedback Application (SB-36000S0)
- Motion Feedback LabVIEW SDK (SB-36030SL)

5.1 Software Overview

5.1.1 Motion Feedback C SDK (SB-36030Sx)

The card is supplied with the SB-36030Sx Motion Feedback C SDK. This software development kit includes a runtime library that provides the user with a hardware abstraction layer for the DDC Motion feedback hardware. This software layer includes the routines that dramatically reduce software development time by providing high-level C functions for the application programmer to interface to the SB-3644 card. C samples are included with the library to demonstrate how the API works with the hardware. Table 7 shows a summary of the supported operating systems.

The ***SB-36030Sx Software Manual*** can be downloaded from the DDC web site at *www.ddc-web.com*.

Table 7. Motion Feedback Library C SDK Part Number Descriptions

Part Number	Operating System
SB-36030S0	Windows
SB-36030S1	Linux

5.1.2 Motion Feedback Application (SB-36000S0)

The card is supplied with the SB-36000S0 Motion Feedback Application. This is a graphical software which runs on Windows.

The ***SB-36000S0 Manual*** can be downloaded from the DDC web site at www.ddc-web.com.

5.1.3 Motion Feedback LabVIEW SDK (SB-36030SL)

The card is supplied with the SB-36030SL Motion Feedback LabVIEW support package. This software development kit includes a set of VIs that provides the user with a hardware abstraction layer for the DDC Motion Feedback hardware in a LabVIEW environment. The Package includes 3 layers of VIs which enable easy application development. Functional user samples are included for common functions.

5.1.4 Troubleshooting the Installation

Usually the installation will be successful, and the self-test function within the sample programs will pass. There are, however, some situations that can cause problems during the installation. The most common are detailed below.

An error is returned when an attempt is made to run any of the samples. This fault is almost always related to an incorrectly assigned device number. Be sure that a device number was correctly assigned through the DDC Card Manager.

If an error is encountered and the device number appears to be correctly assigned, check the operating system. The BIOS setting for a PnP operating system is sometimes set to YES, which can cause a problem. This BIOS option must be set for NO. The operating system, as well as all hardware on your system, will still maintain PnP compatibility; it will not be necessary to manually configure resources for PnP cards.

6 ORDERING INFORMATION

SB-3644 1 F0–2 A0 N

Supplemental Process Requirements:
N = Acrylic Conformal Coating

Cooling Option:
A = Rugged Air Cooled

Operational Temperature:
2 = -40°C to +85°C

I/O Connection:
F = Front Connector I/O
T = PMC on cPCI carrier card

Channel Count and Signal Output Options:

Ordering Option #	Channel Count	Signal Output	Operating Frequency	Accuracy
1	4	0 to 11.8Vrms Synchro/Resolver	360 Hz to 7kHz	1 arc-minute

Notes:
1) The card does not have sockets, all components are soldered down.
2) Contact factory for conduction cooled options.

INCLUDED ACCESSORIES

- Product DVD with SB-3644 manual
- 1 mating connector and backshell

INCLUDED SOFTWARE

(Download available on SB-3644 Product Page at www.ddc-web.com)

SB-36030SX- Motion Feedback C Software Development Kit (SDK)

Operation System:
0 = Windows
1 = Linux OS
L = LabVIEW

SB-36000S0- Motion Feedback Application

STANDARD DDC PROCESSING FOR DISCRETE MODULES/PC BOARD ASSEMBLIES		
TEST	**METHOD(S)**	**CONDITION(S)**
INSPECTION/WORKMANSHIP	IPC-A-610	Class 3
ELECTRICAL TEST	DDC ATP	—