Device
Engineering
Incorporated

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DEI1066
OCTAL GND/OPEN INPUT, SERIAL OUTPUT INTERFACE IC

FEATURES

- Eight GND/OPEN discrete inputs
  - Meet electrical requirements for ABD0100F GND/OPEN discrete input.
  - Hysteresis provides noise immunity
  - Internal pull up resistor with 1mA source current to prevent dry relay contacts.
  - Internal isolation diode
  - Inputs protected from Lightning Induced Transients per DO160D, Section 22, Cat A3 and B3.
- 3-wire serial interface (/CS, CLK, DO)
  - Direct interface to Serial Peripheral Interface (SPI) port.
  - TTL/CMOS compatible inputs and Tristate output
  - 10MHz Data Rate
  - Serial input to expand Shift Register
- Logic Supply Voltage (VCC): 3.3V or 5V
- Analog Supply Voltage (VDD): 5V to 18V
- 16L NB SOIC package

PIN ASSIGNMENTS

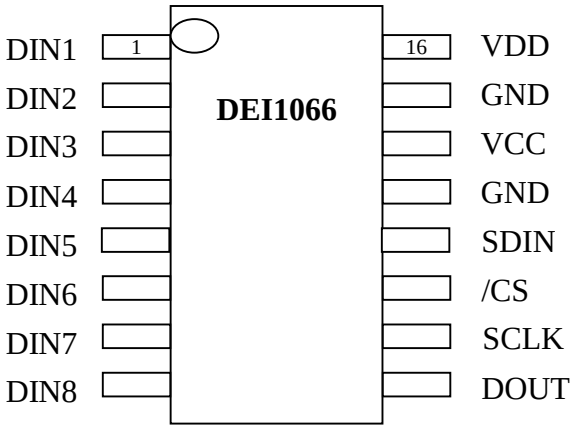


Figure 1 DEI1066 Pin Assignment

DS-MW-01066-01 Rev J
04/18/2018

GENERAL DESCRIPTION

The DEI1066 is an eight-channel discrete-to digital interface BICMOS device. It senses eight Ground/Open discrete signals of the type commonly found in avionic systems. The data is read from the device via an eight-bit serial shift register with 3-state output implemented as a Serial Peripheral Interface (SPI) bus, Mode 0 slave.

Table 1 Pin Descriptions

Pins	Name	Description
8-1	DIN[8:1]	Parallel data inputs. Eight Ground/Open format discrete signals. These have an internal pull-up to VDD. The logic threshold and hysteresis characteristics are determined by the applied VDD voltage.
9	DOUT	Serial data output. This pin is the output from the last stage of the shift register. This is a 3-state output.
10	SCLK	Serial Shift Clock. A low-to-high transition on this input shifts data on the serial data input into the shift register and data in stage 8 is shifted out DOUT, being replaced by the data previously stored in stage 7.
11	/CS	Chip Select. A high-to-low transition on this input loads data from the parallel DIN[8:1] inputs into the shift register. A low level on this input enables the DOUT 3-state output and the shift register. A high level on this input forces DOUT to the high impedance state and disables the shift register so SCLK transitions have no effect.
12	SDIN	Serial Data Input. Data on this input is shifted into the shift register on the rising edge of the SCLK input if the /CS input is low. This input has an internal pull-down resistor to GND.
13	GND	Logic Ground.
14	VCC	Logic Supply Voltage.
15	GND	Analog Ground.
16	VDD	Analog Supply Voltage.

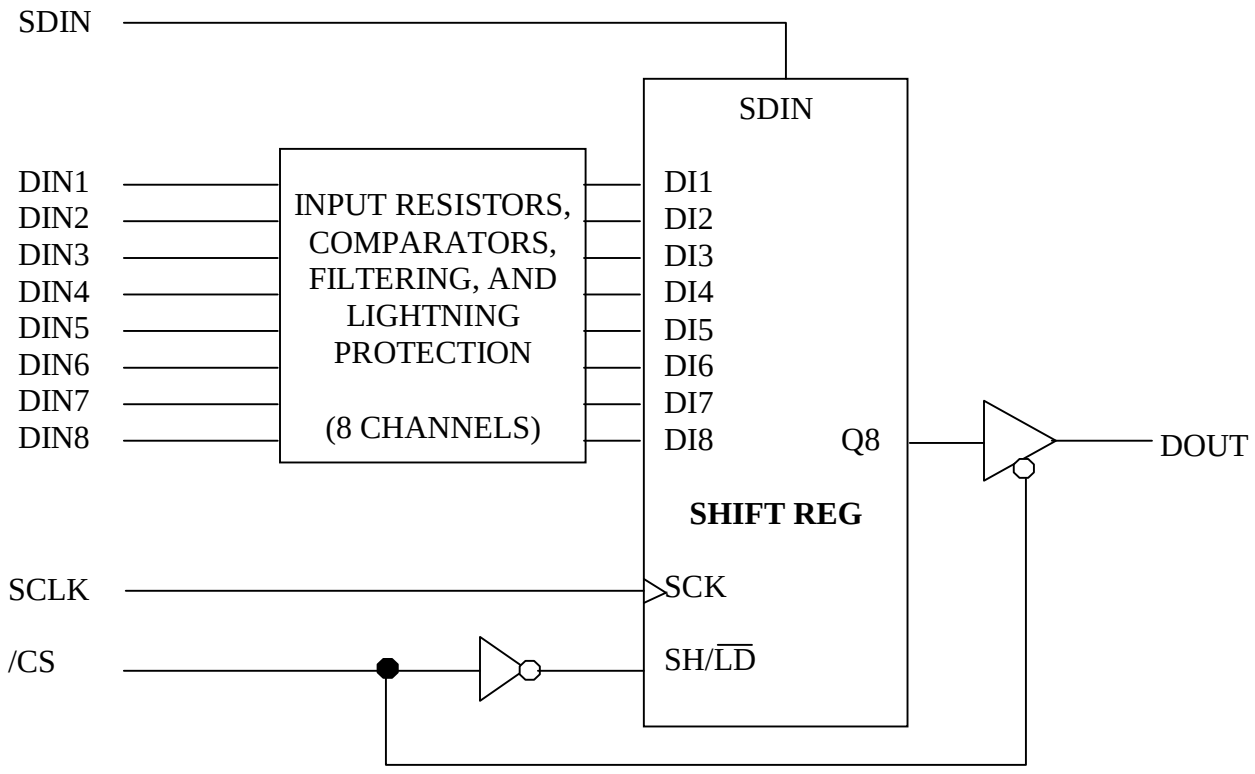


Figure 2 DEI1066 LOGIC DIAGRAM

DIN[8:1] Inputs

Each discrete input consists of the circuit shown in Figure 3. Each DINn signal is conditioned by the resistor / diode network and presented to the comparator IN+. The comparator IN-, and therefore the switching threshold, is developed from the Vdd supply voltage. It includes positive feedback from the comparator output to provide hysteresis. Some notable features are:

- The comparator includes an RC filter to provide noise rejection of transient pulses of up to several us. Thus, there is a relatively large DINx setup time. (Refer to timing parameter tsu2).
- The inputs can withstand continuous input voltages of 40V minimum. The isolation diode breakdown voltage is greater than 50V. The 12K Ohm input resistor is designed to limit diode breakdown current to safe levels during transient events.

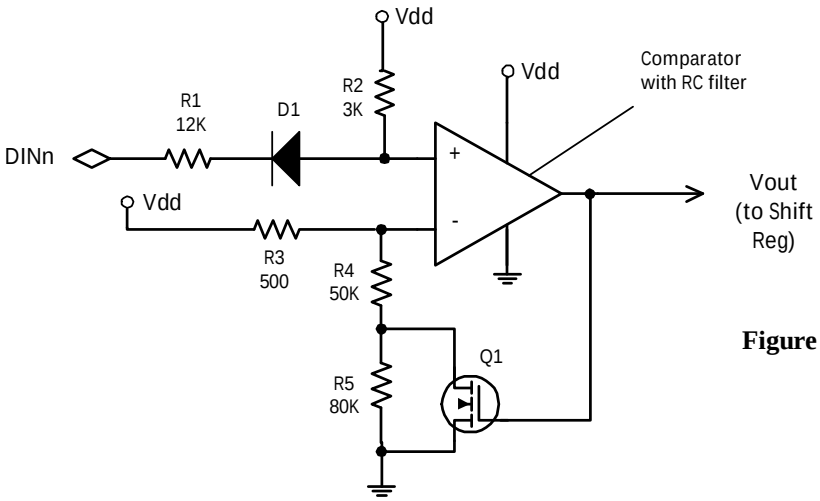


Figure 3 DINn Input Circuit

Table 2 Truth Table

/CS	SCLK	SDIN	DIN[8:1]	SREG Q1	DOUT
1	X	X	X	X	HI-Z
↓	X	X	Sampled into Shift Register	DIN1	Enabled DIN8
0	↑	0	X	0	SREG Q8
0	↑	1	X	1	SREG Q8
0	↓	X	X	No Change	No Change
↑	X	X	X	No Change	Disabled to HI-Z

Serial Interface and Shift Register

The DEI1066 digital interface is an 8-Bit Serial or Parallel-Input / Serial-Output Shift Register with 3-State Output. The control inputs to the shift register are connected as shown in Figure 2 to implement an SPI compatible bus consisting of /CS, SCLK, DOUT, and SDIN. The Figure 4 waveform depicts a typical 8-Bit read cycle where the 8 DIN signals are read on to the serial bus. The Figure 5 waveform demonstrates a daisy-chain application where a 16-Bit read cycle includes the serial data passed through from the SDIN input.

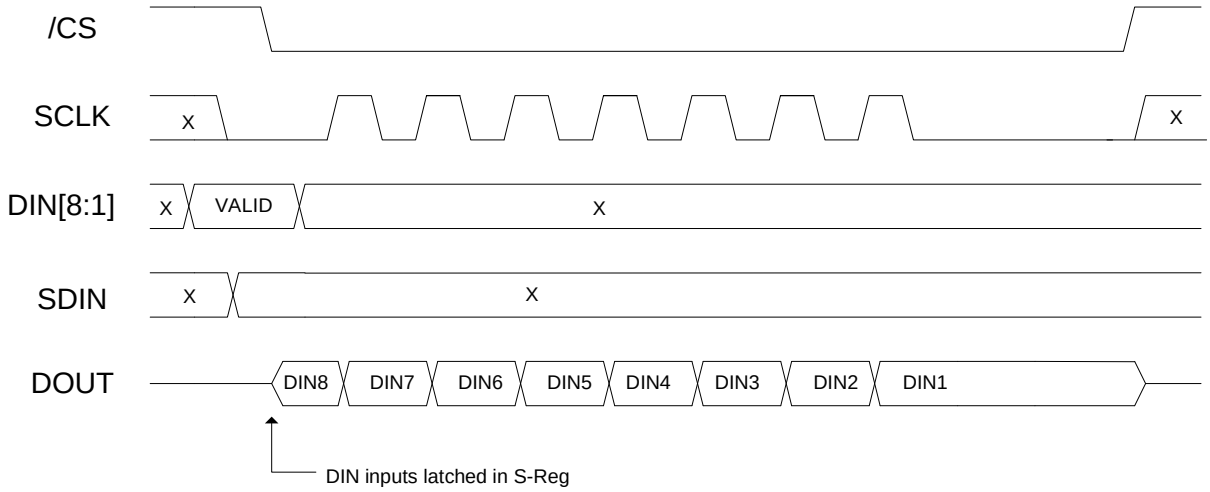


Figure 4 Serial Bus Read Cycle, 8 Bit

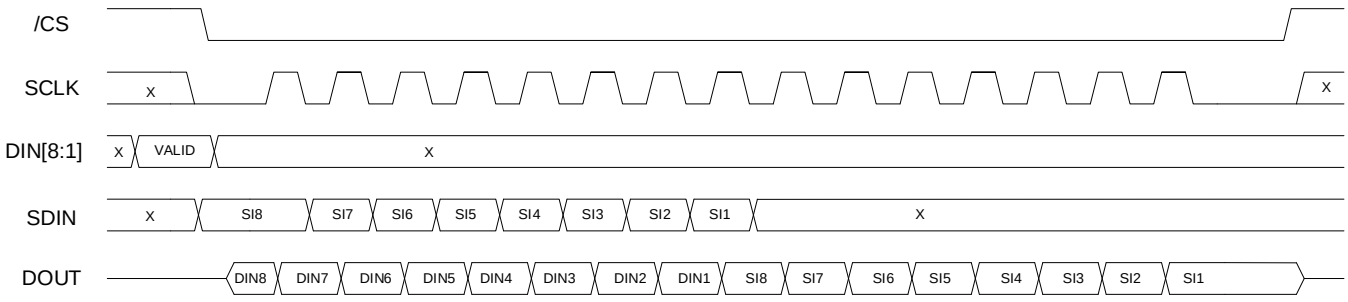


Figure 5 Serial Bus Read Cycle, 16 Bit Daisy Chain

Lightning Protection

DINn inputs are designed to survive lightning induced transients as defined by RTCA DO160D, Section 22, Cat A3 and B3, Waveforms 3, 4, and 5A, Level 3. See waveforms below.

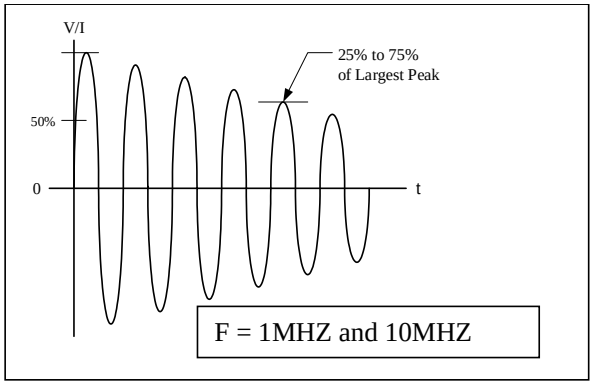


Figure 6 Voltage / Current Waveform 3

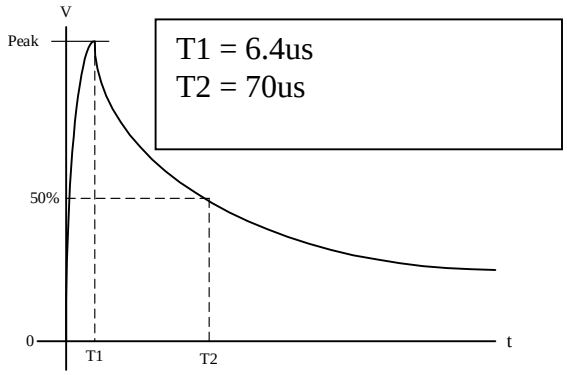


Figure 7 Current / Voltage Waveform 4

Waveform Source Impedance characteristics:

- Waveform 3 Voc/Isc = 600V / 24A => 25 Ohms
- Waveform 4 Voc/Isc = 300 V / 60 A => 5 Ohms
- Waveform 5A Voc / Isc = 300V / 300A => 1 Ohm

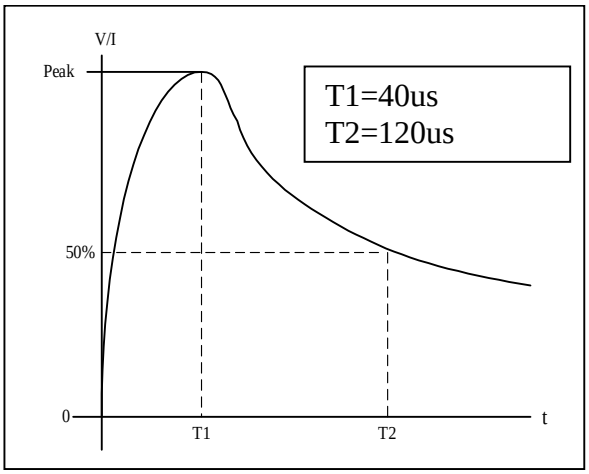


Figure 8 Current / Voltage Waveform 5A

ELECTRICAL CHARACTERISTICS

Table 3 Absolute Maximum Ratings

PARAMETER	MIN	MAX	UNITS
VCC Supply Voltage	-0.3	+7.0	V
VDD Supply Voltage	-0.3	20	V
Input Voltage			
DIN[8:1] Continuous	-5	+40	V
DO160D, Waveform 3, Level 3	-600	+600	V
DO160D, Waveform 4 and 5, Level 3	-300	+300	V
Logic Inputs	-1.5	VCC + 1.5	V
DOUT	-0.5	VCC + 0.5	V
Power Dissipation @ 85 °C: (> 10 Sec)			
16 Lead SOIC		0.8	W
Operating Temperature	-55	+125	°C
Storage Temperature	-65	+150	°C
Junction Temperature	Tjmax	145	°C
ESD per JEDEC A114-A Human Body Model			
Logic and Supply pins		2000	V
DIN pins		1000	

Notes:
1. Stresses above absolute maximum ratings may cause permanent damage to the device.
2. Voltages referenced to Ground

Table 4 Recommended Operating Conditions

PARAMETER	SYMBOL	CONDITIONS
Supply Voltage	VCC VDD	5.0V±10%, 3.3V±10% 5.0 to 18V
Logic Inputs and Outputs		0 to VCC
Discrete Inputs	DIN[8:1]	0 to 40V
Operating Temperature -SES -SMx	Top	 -55 to +85 ºC -55 to +125 ºC

Table 5 DC Characteristics

Symbol	Parameter	Conditions (1) (2)	LIMITS		Unit
			Min	Max	
LOGIC INPUTS AND OUTPUTS					
V_{IH}	HI level input voltage		2.0		V
V_{IL}	LO level input voltage			0.8	V
V_{Ihst}	Input hysteresis voltage, SCLK input	(3)	50		mV
V_{OH}	HI level output voltage	Iout = -20uA	VCC – 0.1		V
		Iout = -4.5mA, -55°C to +85°C -55°C to +125°C	 3.2 3.0		V
V_{OL}	LO level output voltage	Iout = 20uA		0.1	V
		Iout = 4.5mA, -55°C to +85°C -55°C to +125°C		 0.33 0.4	V
I_{IN}	Input leakage Logic inputs except SDIN: SDIN:	Vin = VCC or GND -55°C to +85°C -55°C to +125°C	 -1 -2 -2	 1 2 750	uA
I_{OZ}	Max 3-state leakage current, DOUT	Output in Hi Impedance state. Vout = VCC or GND -55°C to +85°C -55°C to +125°C	 -5 -10	 5 10	uA
C_{in}	Logic input pin Capacitance	(3)		10	pF
C_{out}	DOUT pin capacitance, output in HI-Z state	(3)		15	pF
DISCRETE INPUTS					
V_{IH}	HI level input voltage	VDD = 18V VDD = 5.0V	16.9 4.16		V
V_{IL}	LO level input voltage	VDD = 18V VDD = 5.0V		16.0 3.7	V
V_{Ihst}	Input hysteresis voltage	VDD = 18V VDD = 5.0V	0.59 0.18		V
I_{IH}	HI level input current	DINn = 18V -55°C to +85°C -55°C to +125°C DINn = 40V -55°C to +85°C -55°C to +125°C		 5 10 20 40	uA
I_{IL}	LO level input current	DINn = 0V VDD = 18V VDD = 5.0V	 -1.0 -0.25	 -1.6 -0.5	mA
SUPPLY VOLTAGES					
ICC	Max quiescent logic supply current	Logic inputs = VCC or GND DIN[8:1] = Open -55°C to +85°C -55°C to +125°C		 200 400	uA

Symbol	Parameter	Conditions (1) (2)	LIMITS		Unit
			Min	Max	
IDD	Max quiescent analog supply current	Logic Inputs = VCC or GND DIN[8:1] = Open DIN[8:1] = GND -55°C to +85°C -55°C to +125°C		11 23 24	mA

Notes:
1. Unless otherwise noted, Ta = rated temperature range. VCC = 3.0 to 5.5V. VDD = 5.0 to 18V.
2. Current flowing into device is positive. Current flowing out of device is negative. Voltages are referenced to Ground.
3. By design, not tested.

Table 6 AC Electrical Characteristics

Symbol	Parameter	Conditions (5)	Limits		Unit
			Min	Max	
f_{MAX}	SCLK frequency. (50% duty cycle) (4)	VCC = 3.0V VCC = 4.5V		4.8 24	MHz
	Maximum usable SCLK frequency = 1/(tp2 + tsu3)	VCC = 3.0V VCC = 4.5V		2.8 10.7	
t_W	SCLK pulse width. (50% duty cycle)	VCC = 3.0V VCC = 4.5V	100 20		ns
t_{su1}	Setup time, SCLK low to /CS↓.	VCC = 3.0V VCC = 4.5V	100 50		ns
t_{h1}	Hold time, /CS↓ to SCLK↑.	VCC = 3.0V VCC = 4.5V	20 20		ns
t_{su2}	Setup time, DIN valid to /CS↓.	(6)	1	35	us
t_{h2}	Hold time, /CS↓ to DIN not valid.	(6)	-1		us
t_{su3}	Setup time, SDIN valid to SCLK↑.	VCC = 3.0V VCC = 4.5V	75 20		ns
t_{h3}	Hold time, SCLK↑ to SDIN not valid.	VCC = 3.0V VCC = 4.5V	5 5		ns
t_{p1}	Propagation delay, /CS↓ to DOUT valid. (1)	VCC = 3.0V VCC = 4.5V		250 70	ns
t_{p2}	Propagation delay, SCLK↑ to DOUT valid. (1)	VCC = 3.0V VCC = 4.5V		250 100	ns
t_{p3}	Propagation delay, /CS↑ to DOUT HI-Z. (1) (2) (3)	VCC = 3.0V VCC = 4.5V		200 80	ns
t_{p4}	Delay time between /CS active.	VCC = 3.0V VCC = 4.5V	25 25		ns

Notes:
1. DOUT loaded with 50pF to GND.
2. DOUT loaded with 1K Ohms to GND for Hi output, 1K Ohms to VCC for Low output.
3. Timing measured at 25%VCC for "0" to Hi-Z, 75%VCC for "1" to Hi-Z.
4. By design, not tested
5. Unless otherwise noted: Ta = rated temperature range. VCC = 3.0 to 5.5V. VDD = 5V. VIL = 0V. VIH = VCC. Timing measurement cursers at 50%VCC.
6. t_{su2} represents the maximum possible propagation delay through the input comparator. t_{h2} represents the minimum possible propagation delay through the input comparator. The negative hold time denotes that DIN may change prior to /CS↓ and still be valid data at the Shift Reg.

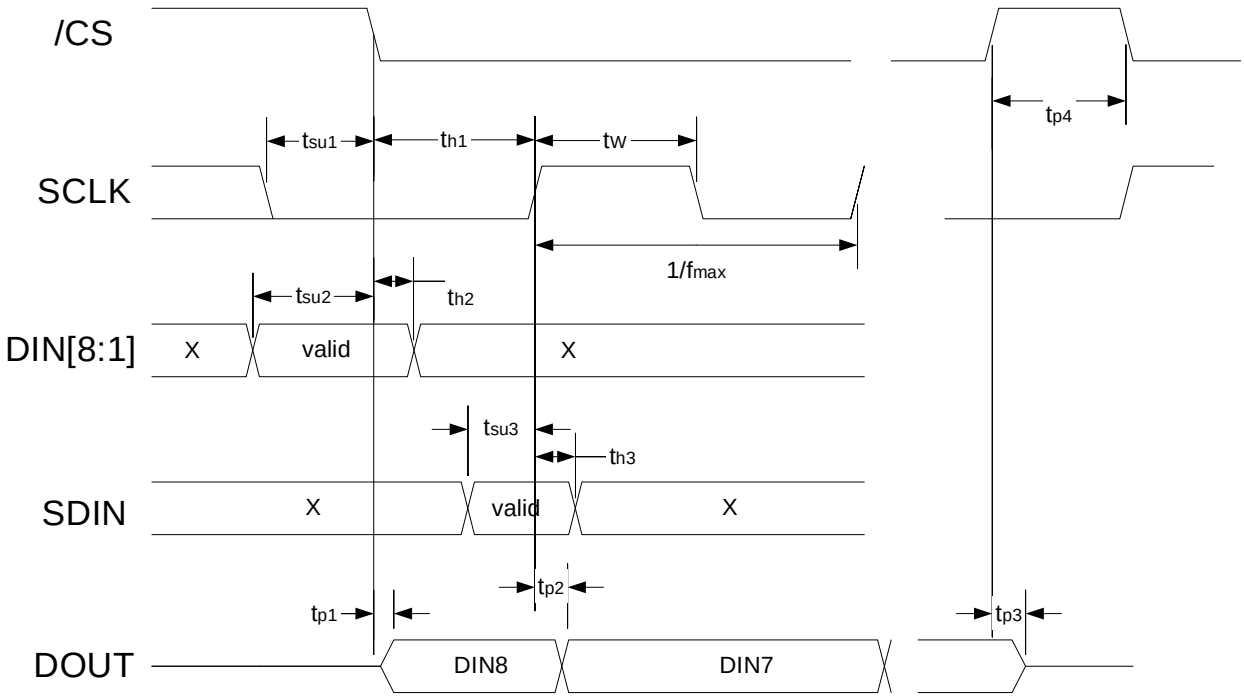
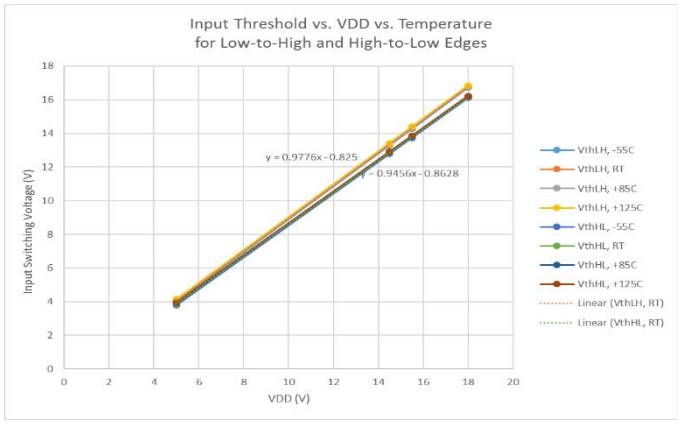
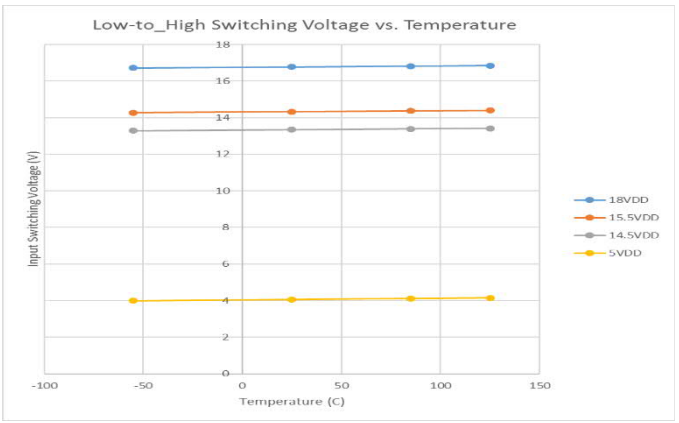
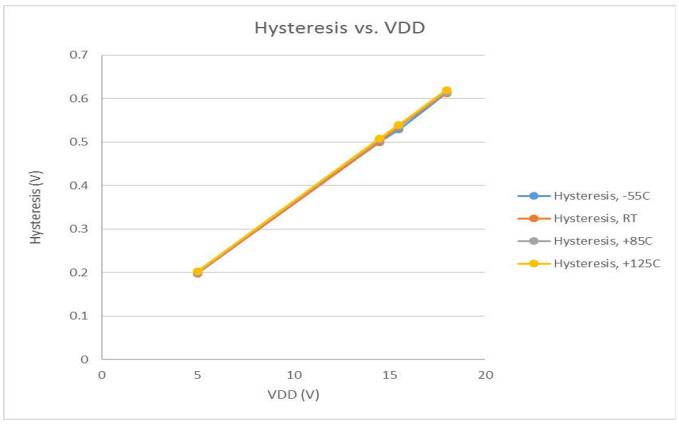


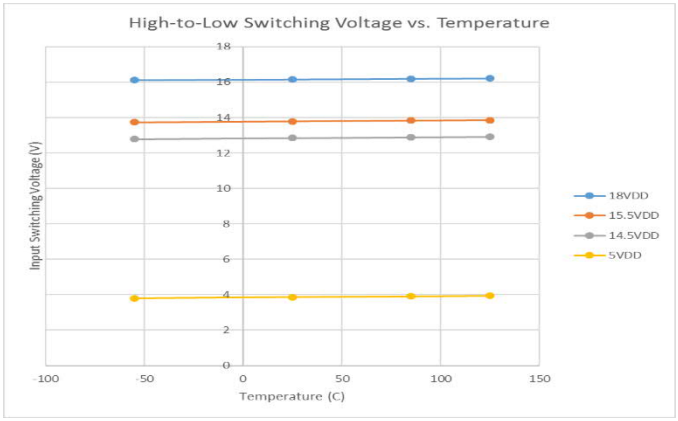
Figure 9 Switching Waveforms

DESIGN INFORMATION









PACKAGE DESCRIPTION

16L Narrow Body SOIC -G Package

Table 7 Package Information

PACKAGE TYPE	16 Lead SOIC Narrow Body, Green
REFERENCE	16L SOIC NB G
THERMAL RESISTANCE:	
θ_{JA} (4 layer PCB with Power Planes)	~74 °C/W
θ_{JC}	~30 °C/W
JEDEC MOISTURE SENSITIVITY LEVEL (MSL)	MSL 1 / 260°C
LEAD FINISH MATERIAL / JEDEC Pb-free CODE	NiPdAu e4
Pb-Free DESIGNATION	RoHS Compliant
JEDEC REFERENCE	MS-012-AC

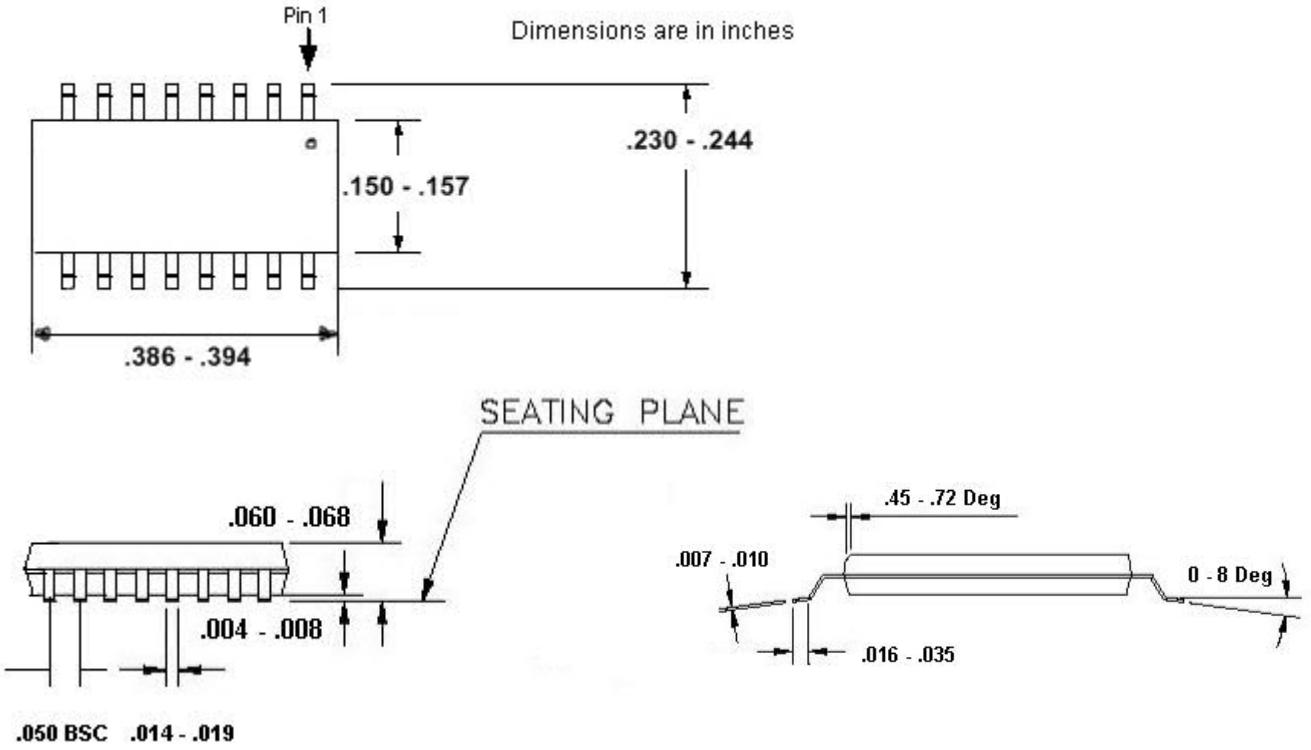


Figure 10 Mechanical Outline, 16L SOIC NB G

ORDERING INFORMATION

Table 8

Part Number	Marking	Package	Burn In	Temperature
DEI1066-SES-G	DEI1066-SES E4	16 SOIC NB G	No	-55 / +85 ºC
DEI1066-SMS-G	DEI1066-SMS E4	16 SOIC NB G	No	-55 / +125 ºC
DEI1066-SMB-G	DEI1066-SMB E4	16 SOIC NB G	96hr / +125 ºC	-55 / +125 ºC