Device
Engineering
Incorporated

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DEI1067

OCTAL GND/OPEN INPUT, SERIAL OUTPUT INTERFACE IC

FEATURES

- Eight GND/OPEN discrete inputs
  - Meets electrical requirements for ARINC 735A GND/OPEN discrete inputs
  - Hysteresis provides noise immunity
  - Internal pull up resistor with 1mA source current to prevent dry relay contacts.
  - Internal isolation diode
  - Inputs protected from Lightning Induced Transients per DO160, Section 22, Level 3 pin injection
- 3-wire serial interface (/CS, CLK, DOUT)
  - Direct interface to Serial Peripheral Interface (SPI) port.
  - TTL/CMOS compatible inputs and Tristate output
  - 10 MHZ Data Rate
  - Serial input to expand Shift Register
- Logic Supply Voltage (VCC): 3.3 V or 5 V
- Analog Supply Voltage (VDD): 15 V ±10%
- Pin compatible with DEI1066
- 16L NB SOIC package

PIN ASSIGNMENTS

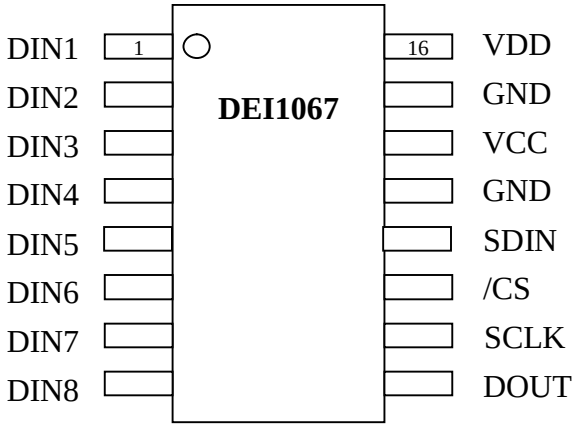

Figure 1 DEI1067 Pin Assignment

FUNCTIONAL DESCRIPTION

The DEI1067 is an eight-channel discrete-to digital interface BICMOS device. It senses eight Ground/Open discrete signals of the type commonly found in avionic systems. The data is read from the device via an eight-bit serial shift register with 3-state output. This serial interface is compatible with the industry standard Serial Peripheral Interface (SPI) bus.

Table 1 Pin Descriptions

PINS	NAME	DESCRIPTION
8-1	DIN[8:1]	Parallel data inputs. Eight Ground/Open format discrete signals. These have an internal pull-up to VDD. The logic threshold and hysteresis characteristics are determined by the applied VDD voltage.
9	DOUT	Serial data output. This pin is the output from the last stage of the shift register. This is a 3-state output.
10	SCLK	Serial Shift Clock. A low-to-high transition on this input shifts data on the serial data input into the shift register and data in stage 8 is shifted out DOUT, being replaced by the data previously stored in stage 7.
11	/CS	Chip Select. A high-to-low transition on this input loads data from the parallel DIN[8:1] inputs into the shift register. A low level on this input enables the DOUT 3-state output and the shift register. A high level on this input forces DOUT to the high impedance state and disables the shift register so SCLK transitions have no effect.
12	SDIN	Serial Data Input. Data on this input is shifted into the shift register on the rising edge of the SCLK input if the /CS input is low. This input has an internal pull-down resistor to GND.
13	GND	Logic Ground.
14	VCC	Logic Supply Voltage.
15	GND	Analog Ground.
16	VDD	Analog Supply Voltage.

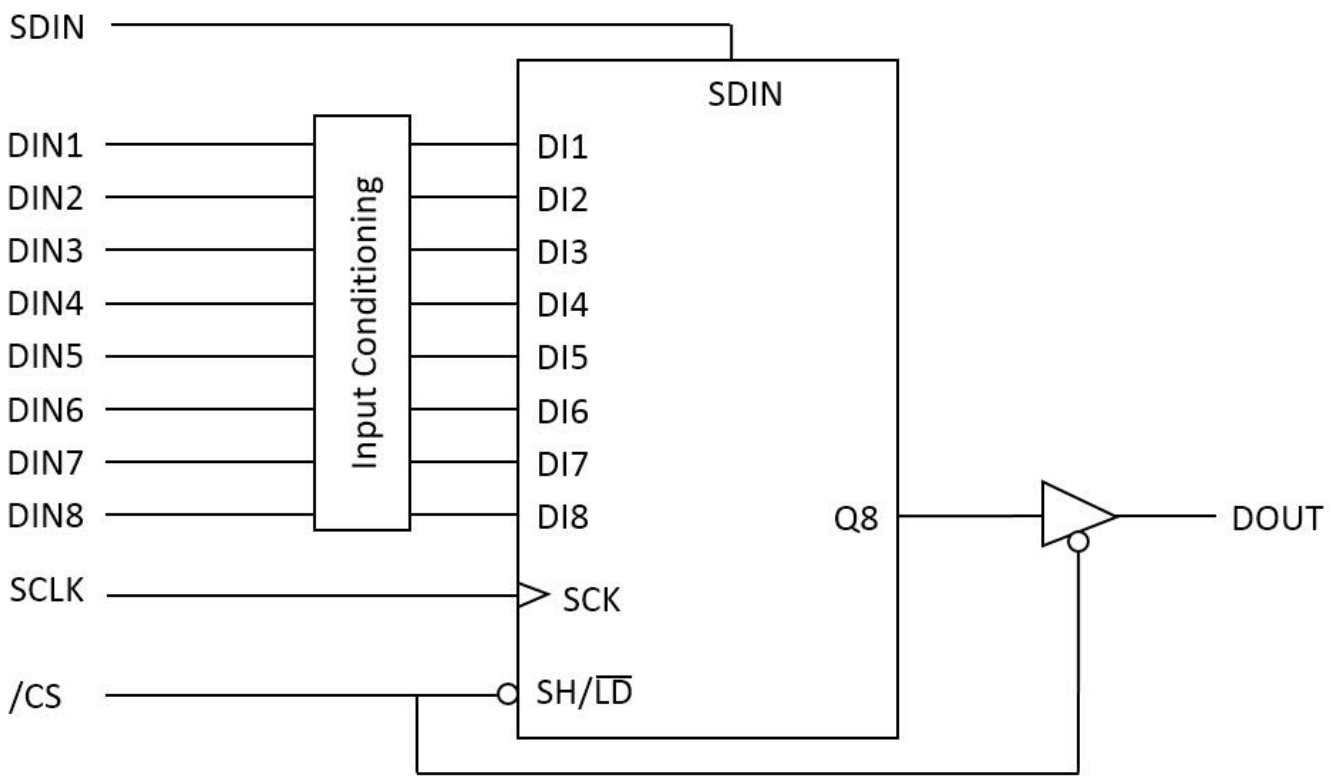

Figure 2 DEI1067 Logic Diagram

Table 2 Truth Table

/CS	SCLK	SDIN	DIN[8:1]	SREG Q1	DOUT
1	X	X	X	X	HI-Z
↓	X	X	Sampled into Shift Register	DIN1	Enabled DIN8
0	↑	0	X	0	SREG Q8
0	↑	1	X	1	SREG Q8
0	↓	X	X	No Change	No Change
↑	X	X	X	No Change	Disabled to HI-Z

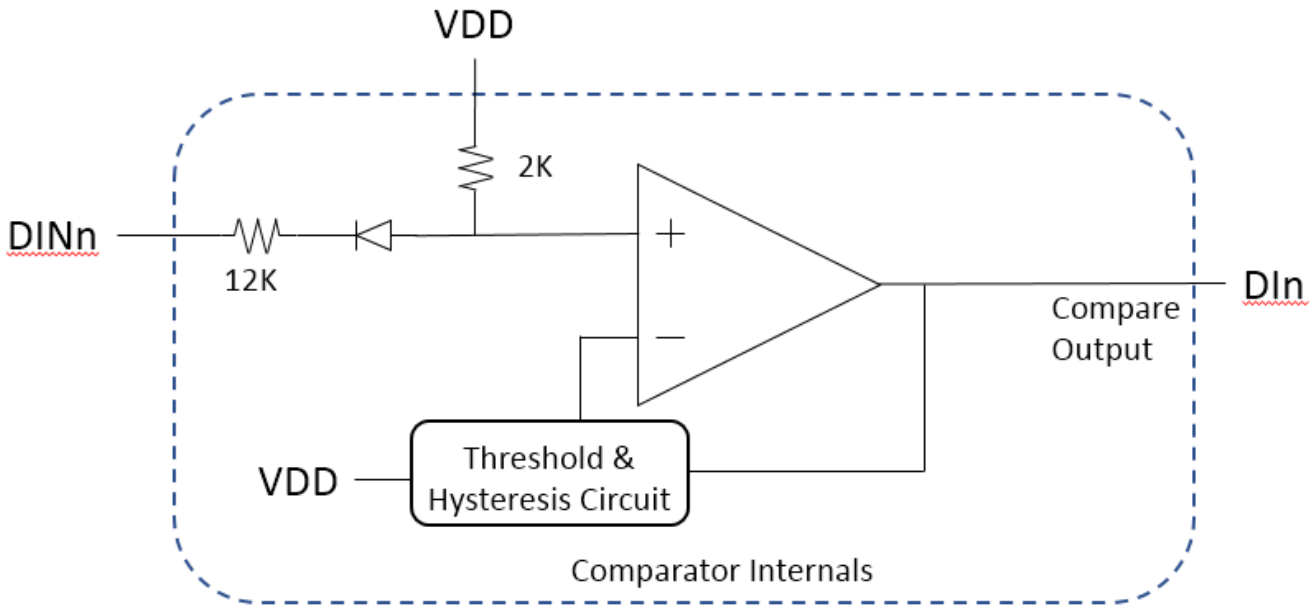

Figure 3 DIN Input Conditioning Circuit

DIN Inputs

The DIN inputs are converted to logic levels via input conditioning circuits and applied to the parallel inputs of an 8-bit serial output shift register. A high level on a DIN input will result in a logic '1' applied to the shift-register and subsequently read out as a '1'.

Each conditioning circuit comprises high voltage pull-up resistors to VDD which are sized to withstand the lightning transients, and an isolation diode to prevent DIN from sinking current. The conditioned input voltage is applied to the voltage comparator + input. A reference voltage is applied to the other. The reference establishes the input switching points; a low-to-high and a high-to-low threshold. These are formed from the VDD supply voltage by resistor dividers. A switch controlled by the comparator output selects the appropriate reference voltage to implement the threshold hysteresis for noise immunity.

Serial Interface and Shift Register

The DEI1067 digital interface is an 8-bit serial or parallel input / serial tri-state output shift-register similar to a 74HC597. The control inputs to the shift register are connected as shown in Figure 2 to implement an SPI compatible bus consisting of /CS, SCLK, DOUT, and SDIN. The Figure 4 waveform depicts a typical 8-Bit read cycle where the 8 DIN signals are read on to the serial bus. The

Figure 5 waveform illustrates a daisy-chain application where a 16-bit read cycle includes the serial data passed through from the SDIN input.

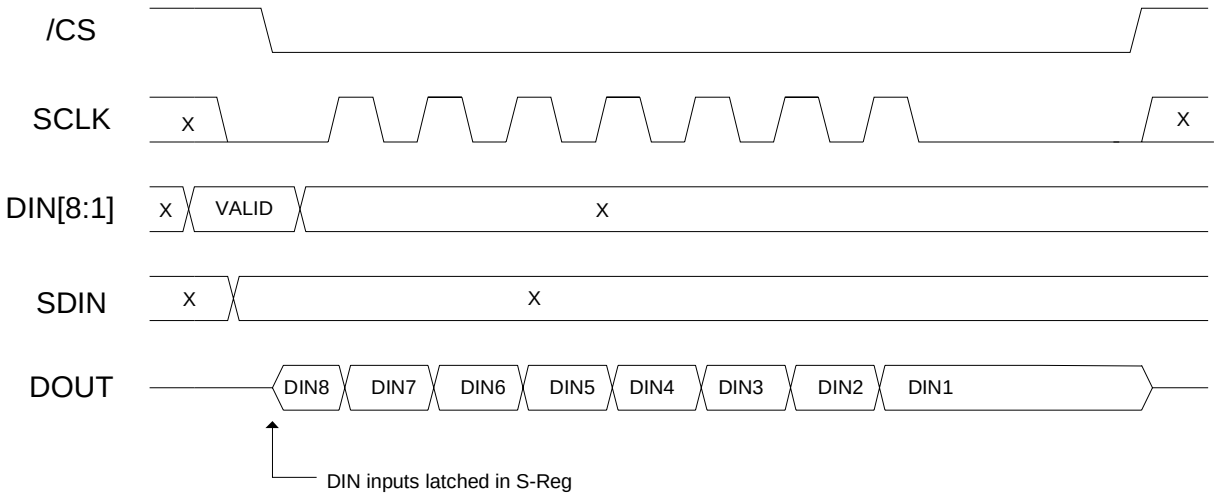

Figure 4 Serial Bus Read Cycle, 8 Bit

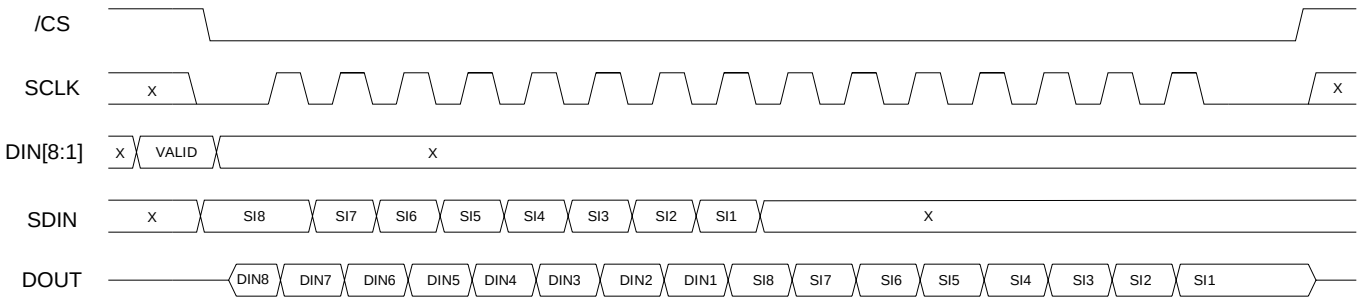

Figure 5 Serial Bus Read Cycle, 16 Bit Daisy Chain

Lightning Protection

DIN inputs are designed to survive lightning induced transients as defined by RTCA DO160, Section 22, Level 3 pin injection waveforms 3, 4, and 5A. See waveforms below.

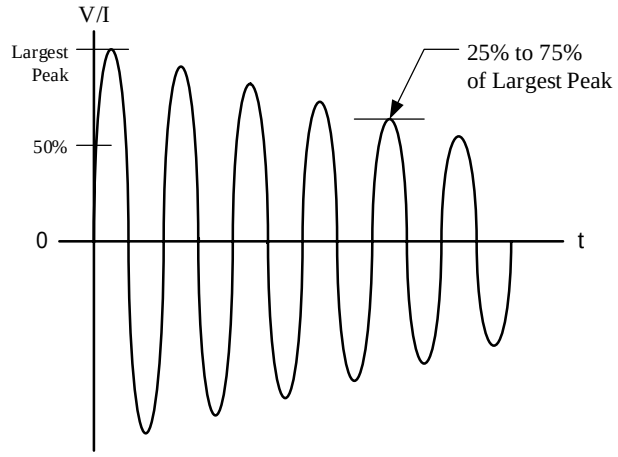

Figure 6 Voltage / Current Waveform 3

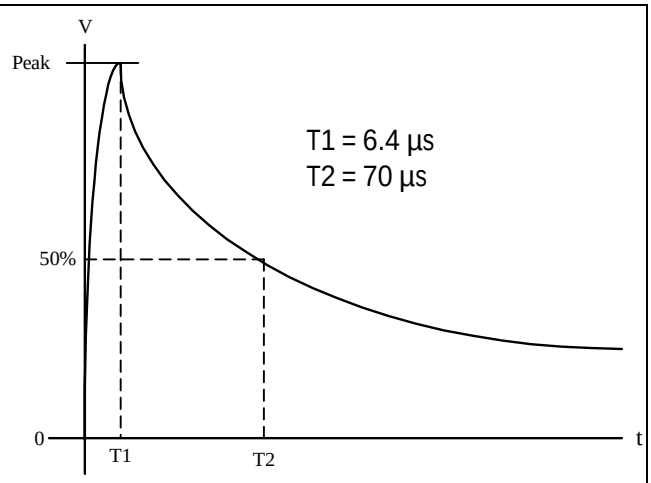

Figure 7 Voltage / Current Waveform 4

Waveform Source Impedance characteristics:

- Waveform 3 Voc / Isc = 600 V / 24 A => 25 Ω
- Waveform 4 Voc / Isc = 300 V / 60 A => 5 Ω
- Waveform 5A Voc / Isc = 300 V / 300 A => 1 Ω

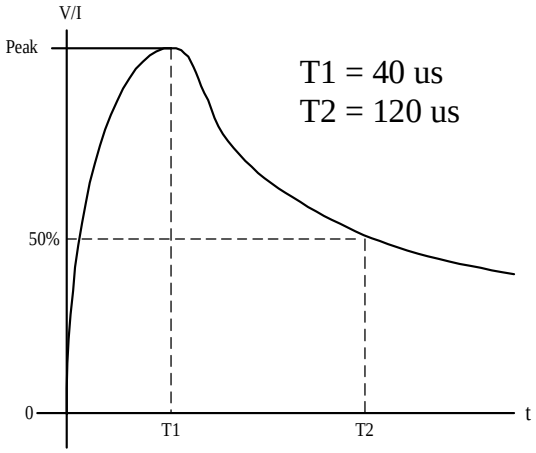

Figure 8 Voltage / Current Waveform 5A

Table 3 Absolute Maximum Ratings

PARAMETER	MIN	MAX	UNITS
VCC Supply Voltage	-0.3	+7.0	V
VDD Supply Voltage	-0.3	20	V
Operating Temperature	-55	+85	°C
Storage Temperature	-65	+150	°C
Input Voltage DIN[8:1] Continuous DO160D, Waveform 3, Level 3 DO160D, Waveform 4 and 5, Level 3 Logic Inputs DOUT	 -5 -600 -300 -1.5 -0.5	 +40 +600 +300 VCC + 1.5 VCC + 0.5	 V V V V V
Power Dissipation @ 85 °C: (> 10 Sec)		0.8	W
Junction Temperature: Tjmax		145	°C
ESD per JEDEC JS-001 Human Body Model (HBM)		1C	Class
Peak Body Temperature (10 sec)		260	°C
Notes: Stresses above absolute maximum ratings may cause permanent damage to the device. Voltages referenced to Ground			

Table 4 Recommended Operating Conditions

PARAMETER	SYMBOL	CONDITIONS
Supply Voltage	VCC VDD	5.0 V ± 10%, 3.3 V ±10% 15 V ± 10%
Logic Inputs and Outputs		0 to VCC
Discrete Inputs	DIN[8:1]	0 to 40 V
Operating Temperature	Ta	-55 to +85 °C

Table 5 Electrical Characteristics

SYMBOL	PARAMETER	CONDITIONS (1)	LIMITS		UNIT
			MIN	MAX	
LOGIC INPUTS AND OUTPUTS					
VIH	HI level input voltage		2.0		V
VIL	LO level input voltage			0.8	V
VHST	Input hysteresis voltage, SCLK input	(3)	50		mV
VOH	HI level output voltage	IOUT = -20 uA	VCC – 0.1		V
		IOUT = -4.5 mA VCC = 4.5 V to 5.5 V	3.2		V
VOL	LO level output voltage	IOUT = 20 uA		0.1	V
		IOUT = 4.5 mA VCC = 4.5 V to 5.5 V		0.4	V
IIN	Input leakage Logic inputs except SDIN. SDIN	DINn = VCC or GND	 -1.0 -1.0	 1.0 750	uA
IOZ	Max 3-state leakage current	Output in Hi Impedance state. DOUT = 0 to VCC	-5.0	5.0	uA
DISCRETE INPUTS					
VIH	HI level input voltage		7.5		V
RIH	HI level DIN-to-GND resistance	Resistor from DIN to GND to guarantee HI input condition.	100		kΩ
IIH	HI level input current	DIN = 7.5 V, VDD = 15 V	-732	-212	uA
VIL	LO level input voltage			3.5	V
RIL	LO level DIN-to-GND resistance	Resistor from DIN to GND to guarantee LO input condition.		10	Ω
IIL	LO level input current	DIN = 0 V, VDD = 15 V	-1.55	-0.45	mA
VHST	Input hysteresis voltage		1.0		V
SUPPLY VOLTAGES					
ICC	Max quiescent logic supply current	Vin(logic) = VCC or GND DIN[8:1] = Open		200	uA
IDD	Max quiescent analog supply current	Vin(logic) = VCC or GND DIN[8:1] = Open DIN[8:1] = GND		 12.8 24	mA

Notes:

1. Ta = -55 to +85 °C. VDD = +15 V ±10%, VCC = 3.0 to 5.5 V unless otherwise noted.
2. Current flowing into device is positive. Current flowing out of device is negative. Voltages are referenced to Ground.
3. Guaranteed by design. Not production tested.

Table 6 Switching Characteristics (4)

SYMBOL	PARAMETER	CONDITIONS (6, 7)	LIMITS		UNIT
			MIN	MAX	
f_{MAX}	SCLK frequency. (50% duty cycle) (5)	VCC = 3.0 V VCC = 4.5 V		4.8 24	MHZ
	Maximum usable SCLK frequency = 1/(tp2 + tsu3)	VCC = 3.0 V VCC = 4.5 V		2.8 10.7	
t_W	SCLK pulse width. (50% duty cycle)	VCC = 3.0 V VCC = 4.5 V	100 20		ns
tsu1	Setup time, SCLK low to /CS↓.	VCC = 3.0 V VCC = 4.5 V	100 50		ns
th1	Hold time, /CS↓ to SCLK↑.	VCC = 3.0 V VCC = 4.5 V	20 20		ns
tsu2	Setup time, DIN valid to /CS↓.		1	35	us
th2	Hold time, /CS↓ to DIN not valid.		-1		us
tsu3	Setup time, SDIN valid to SCLK↑.	VCC = 3.0 V VCC = 4.5 V	75 20		ns
th3	Hold time, SCLK↑ to SDIN not valid.	VCC = 3.0 V VCC = 4.5 V	5 5		ns
tp1	Propagation delay, /CS↓ to DOUT valid. (1)	VCC = 3.0 V VCC = 4.5 V		250 70	ns
tp2	Propagation delay, SCLK↑ to DOUT valid. (1)	VCC = 3.0 V VCC = 4.5 V		250 100	ns
tp3	Propagation delay, /CS↑ to DOUT HI-Z. (1) (2) (3)	VCC = 3.0 V VCC = 4.5 V		200 80	ns
tp4	Delay time between /CS active. (5)	VCC = 3.0 V VCC = 4.5 V	25 25		ns
Cin	Maximum logic input pin Capacitance. (5)			10	pF
Cout	Maximum DOUT pin capacitance, output in HI-Z state. (5)			15	pF

Notes:

1. DOUT loaded with 50 pF to GND.
2. DOUT loaded with 1 kΩ to GND for Hi output, 1 kΩ to VCC for Low output.
3. Timing measured at 25%VCC for "0" to Hi-Z, 75%VCC for "1" to Hi-Z.
4. Sample tested on Iot basis.
5. Not tested
6. Ta = -55 to +85 °C. VDD = +15 V, VIL = 0 V, VIH = VCC unless otherwise noted.
7. Measurements made at 50%VCC.

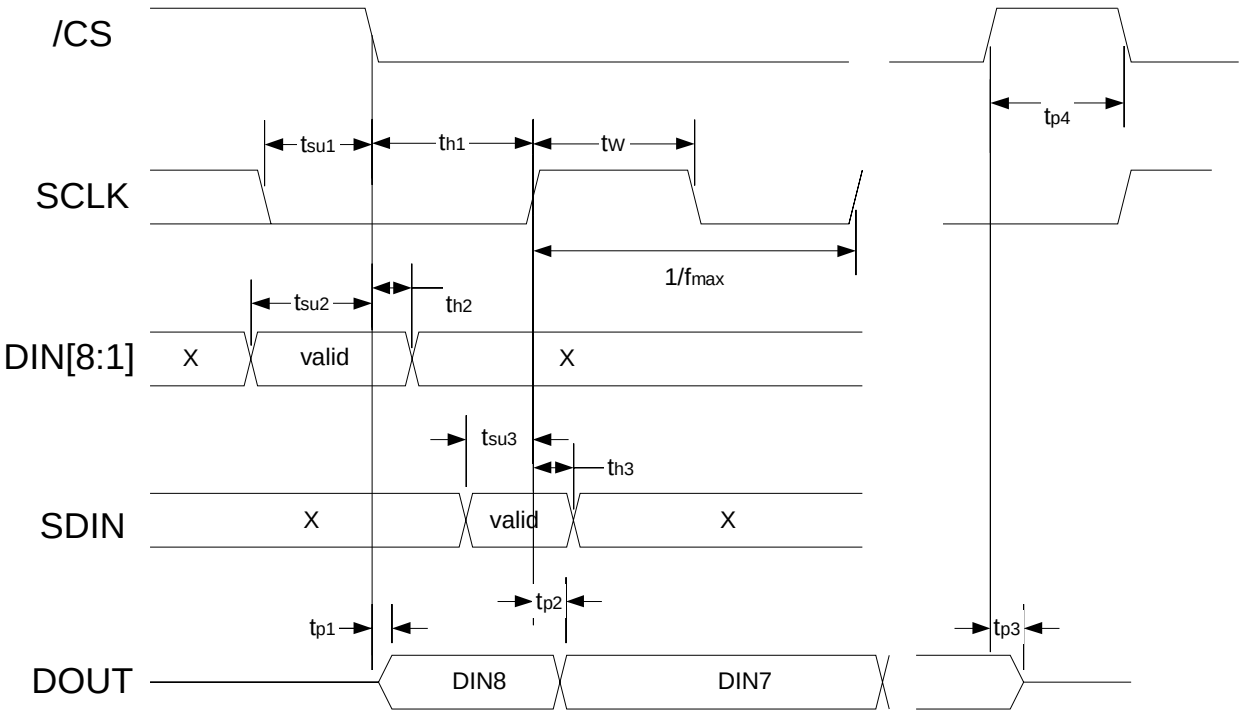

Figure 9 Switching Waveforms

PACKAGE DESCRIPTION

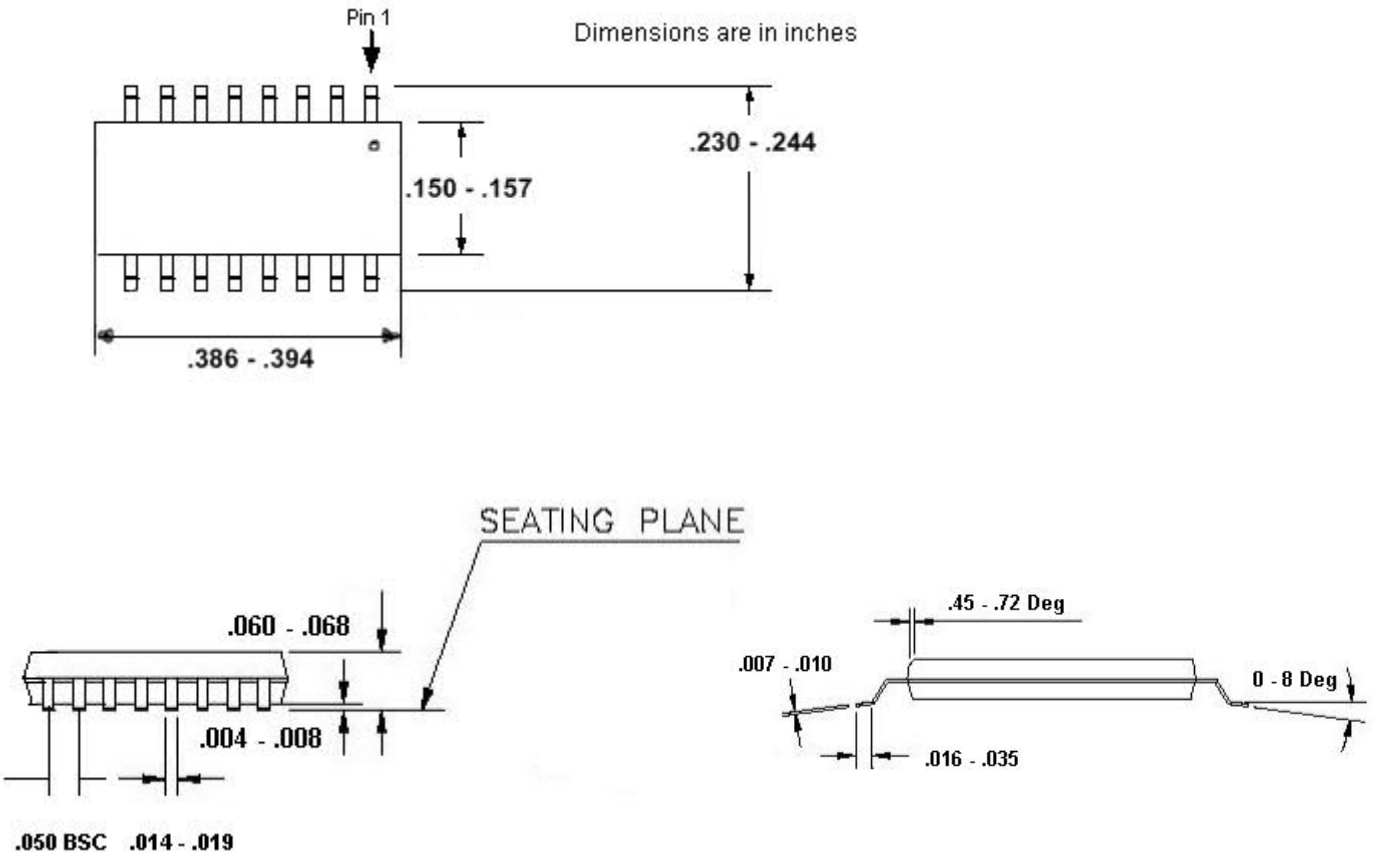

Figure 10: Mechanical Outline

Table 7 Package Information

CHARACTERISTIC	16 SOIC NB G
Moisture Sensitivity	MSL 1 / 260 ˚C
Lead Finish	NiPdAu
RoHS Compliant Materials	Yes
Thermal Resistance: Θja: Θjc:	 74 ˚C/W (Mounted on 4 layer PCB) 30 ˚C/W

ORDERING INFORMATION

Table 8 - ORDERING INFORMATION

PART NUMBER	MARKING	PACKAGE	TEMPERATURE
DEI1067-SES-G	DEI1067-SES (e4)	16 SOIC NB G	-55 / +85 °C
Notes: 1. “e4” after date code denotes “Pb free” category			