Device
Engineering
Incorporated

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DEI1184
8CH PROGRAMMABLE DISCRETE INTERFACE W/ EXT HV PROTECTION

FEATURES

- Eight discrete inputs
  - Individually configurable as either GND/OPEN or 28V/OPEN (or 28V/GND) format input.
  - Input threshold and hysteresis per Airbus ABD0100H specification.
    - GND/OPEN mode: 4.5 V / 10.5 V input levels, 3 V hysteresis
    - 28V/OPEN mode: 6 V / 12 V input levels, 3V hysteresis
  - 1mA input current to prevent dry relay contacts.
  - Internal isolation diode in GND/OPEN mode.
  - Uses external series 3 kΩ resistors on inputs to implement lightning transient immunity of DO160, Section 22 Level 3, and higher levels with the addition of small TVS devices.
- Serial I/O interface to read data register and write configuration register
  - Direct interface to Serial Peripheral Interface (SPI) port.
  - TTL/CMOS compatible inputs and Tristate output
  - 10 MHZ Max Data Rate
  - Serial input to expand Shift Register
- Logic Supply Voltage (VCC): 3.3 V +/-5%
- Analog Supply Voltage (VDD): 15 V +/-10%
- 16L SOIC EP package

PIN ASSIGNMENTS

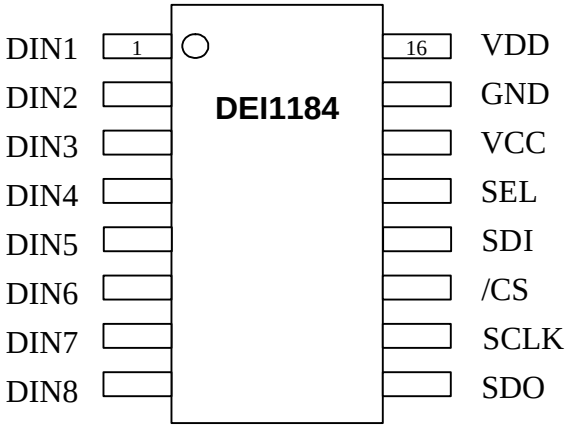


Figure 1 DEI1184 Pin Assignment (16 Lead SOIC)

FUNCTIONAL DESCRIPTION

DEI1184 is an eight-channel discrete-to digital interface IC implemented in an HV DIMOS technology. It senses eight discrete signals of the type commonly found in avionic systems and converts them to serial logic data. Each input can be individually configured as either GND/OPEN or 28V/OPEN format input via a serial data input. The discrete data is read from the device via an eight-bit serial shift register with 3-state output. This serial interface is compatible with the industry standard Serial Peripheral Interface (SPI) bus.

The discrete input circuits are designed to achieve a high level of lightning transient immunity. The application design provides a series 3 kΩ resistor on each discrete input to achieve DO160E Level 3 and WF5A 500 V immunity. Higher immunity levels can be achieved (i.e. Level 5) with the addition of a TVS between the resistor and the input pin.

Table 1 Pin Descriptions

PINS	NAME	DESCRIPTION
1-8	DIN[1:8]	Discrete Inputs. Eight discrete signals which can be individually configured as either GND/OPEN or 28V/OPEN format inputs. Inputs are connected to the external series 3 kΩ resistor as part of front end Lightning Transients protection circuit.
9	SDO	Logic Output. Serial Data Output. This pin is the output from MSB (Bit 8) of the selected shift register (Data/Configuration). It is clocked by the rising edge of SCLK. This is a 3-state output enabled by /CS.
10	SCLK	Logic Input. Serial Shift Clock. A low-to-high transition on this input shifts data on the serial data input into Bit 1 of the selected shift register. The selected shift register is shifted from Bit 1 to Bit 8. Bit 8 of the selected shift register is driven on DOUT.
11	/CS	Logic Input. Chip Select. A low level on this input enables the SDO 3-state output and the selected shift register. A high level on this input forces DOUT to the high impedance state and disables the shift registers so SCLK transitions have no effect. When the Data Register is selected, a high-to-low transition causes the Discrete Input data to be loaded into the Data Register. When the Configuration Register is selected, a low-to-high transition causes the Serial Configuration Register data to be loaded into the parallel configuration outputs.
12	SDI	Logic Input. Serial Data Input. Data on this input is shifted into the LSB (Bit 1) of the selected shift register on the rising edge of the SCLK when /CS input is low.
13	SEL	Logic Input with weak pull-up. Selects between the Data Register and Configuration Register. H = DATA, L = CONF.
14	VCC	Logic Supply Voltage. 3.3 V +/-5%
15	GND	Logic/Signal Ground
16	VDD	Analog Supply Voltage. 15 V +/-10%

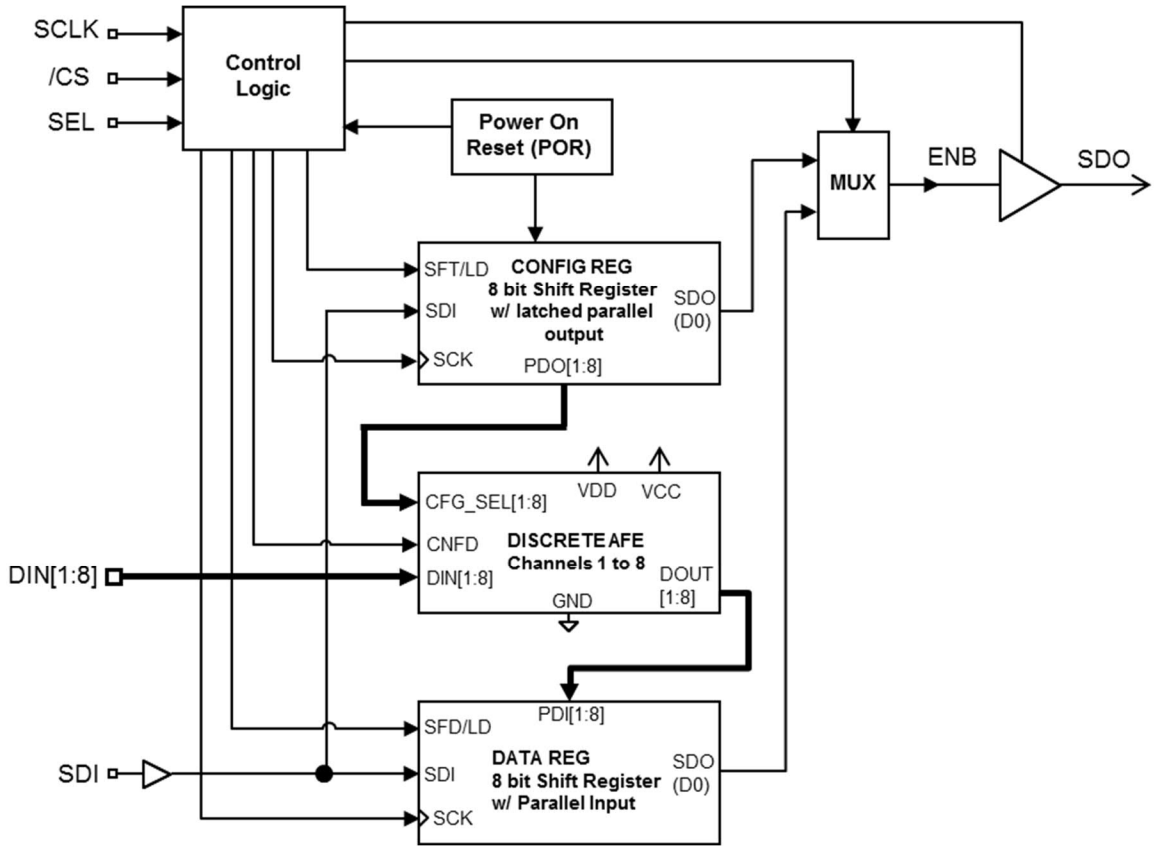
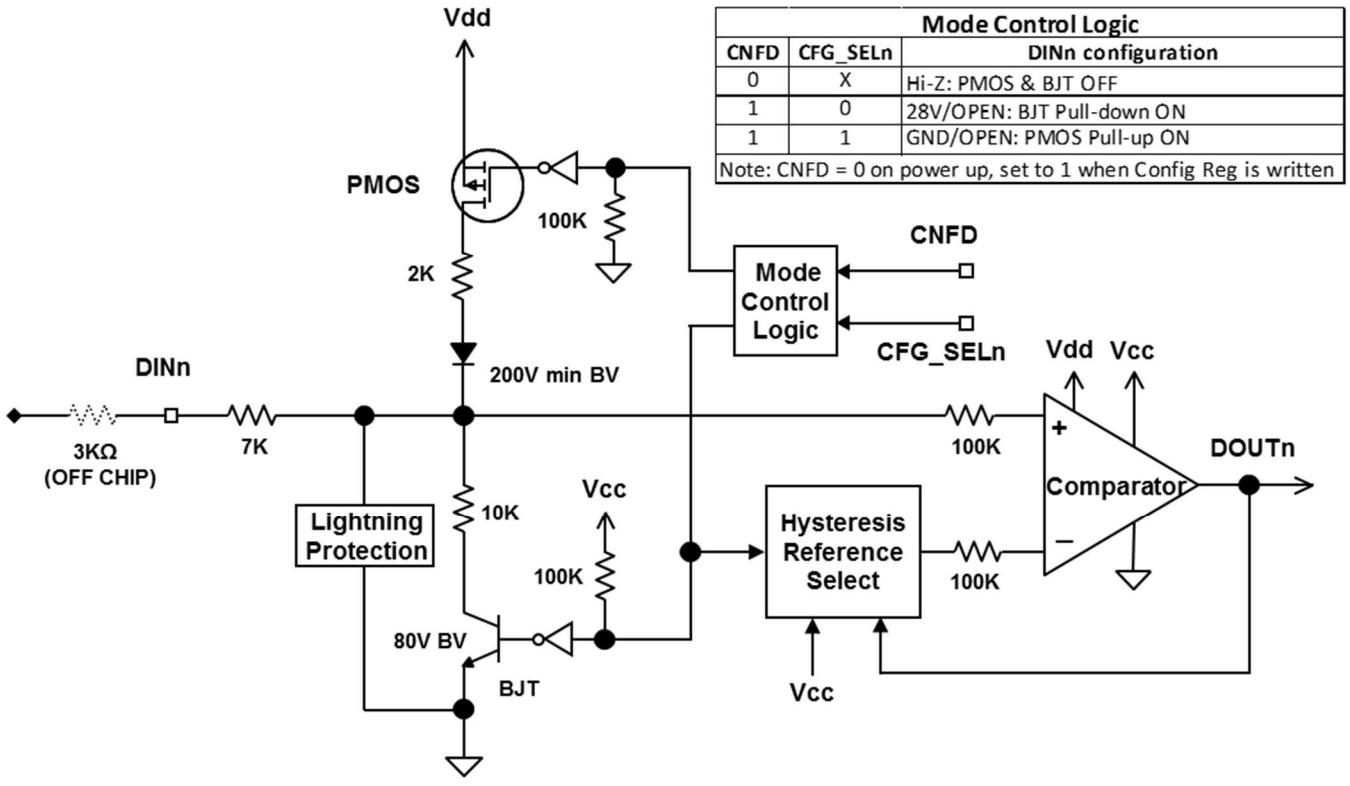


Figure 2 Function Diagram



Mode Control Logic		
CNFD	CFG_SELn	DINn configuration
0	X	Hi-Z: PMOS & BJT OFF
1	0	28V/OPEN: BJT Pull-down ON
1	1	GND/OPEN: PMOS Pull-up ON
Note: CNFD = 0 on power up, set to 1 when Config Reg is written		

Figure 3 Discrete AFE Function Diagram

Table 2 Truth Table

Serial Interface Operation						
SEL	**/CS**	**SCLK**	**SDI**	**DIN[1:8]**	**SDO**	**Description**
X	H	X	X	X	HI Z	Not Selected
H	↓	L	X	Valid	DIN[8]	DR[1:8]← DIN[1:8]
H	L	↑	DR[1]	X	DR[8]	DR[n+1] ← DR[n], DR[1] ← SDI
L	L	↑	CR[1]	X	CR[8]	CR[n+1] ← CR[n], CR[1] ← SDI
L	↑	L	X	X	HI Z	CL[1:8]← CR[1:8]

Legend:
DR = Data Register
CR = Configuration Register
CL = Configuration Latch
X = Don't Care

DIN[1:8] Discrete AFE

The Discrete Input Analog Front End circuit function is represented in Figure 3. Each DINn signal is conditioned by the resistor / diode network and presented to a comparator with hysteresis. The external 3 kΩ resistor is part of the front-end circuitry for achieving threshold and hysteresis requirements while protecting the chip from Lightning Induced Transients. When the input is configured for GND/OPEN operation (By programming the channel's configuration register bit to 1), the pull-up resistor and diode is enabled by turning PMOS switch on and BJT switch off. The comparator reference voltage corresponding to DINn input threshold (shown below) is generated from resistive network. When configured for 28V/OPEN operation, the pull-down resistor is enabled by turning BJT on and PMOS off. The comparator reference voltages for 28V/OPEN operation are configured corresponding to DINn input threshold voltages described below.

Some notable features are:

- The input current is ~1 mA. This current will prevent a "dry" relay contact.
- The input threshold voltage and hysteresis:
  - 28V/OPEN
    - Low- level input voltage: -3.0 V to 6.0 V
    - High level input voltage: 12 V to 49 V
    - Hysteresis: Vhys > 3V
  - GND/OPEN
    - Low- level input voltage: -3.0 V to 4.5 V
    - High level input voltage: 10.5 V to 49 V
    - Hysteresis: Vhys > 3 V
- Input noise immunity is maximized with a combination of voltage hysteresis and use of a slow input voltage comparator.
- The inputs can withstand continuous input voltages of 49 V. The isolation diode breakdown voltage is greater than 42V. The 10 kΩ input resistance, which consists of a 7 kΩ on-chip resistor and a 3 kΩ off-chip resistor, is designed to limit diode breakdown current to safe levels during transient events.

Data Register

The 8-bit Data Register is a "parallel-input, serial-output" register that samples the input channels and reads-out the data to the Serial Data Output. The register is read via the SDO output as described in Figure 4 and Figure 5. A low DIN input level results in a Logic 0, and a high input level results in a Logic 1.

Configuration Register

The 8-bit Configuration Register is a "serial-input, parallel-output with data latch" register that individually configures each AFE input as either GND/OPEN or 28V/OPEN format. The register is programmed via the serial data input as described in Figure 6 and Figure 7. Logic 0 sets the respective input to 28V/OPEN mode (pull-down); Logic 1 sets the respective input to GND/OPEN mode (pull-up). The register is reset to 0's when the VCC Logic Supply voltage transitions from low to high.

Serial Interface

The DEI1184 incorporates a serial IO interface for programming the Discrete Input configuration and for reading the Discrete Input status. Refer to Figure 2. The interface is SPI compatible and consists of /CS, SEL, SCLK, SDO, and SDI signals. Waveform Figures 4 – 7 depict the Data Read sequence and Configuration Write sequence for both 8-Bit cycles and also 16 bit "daisy chain" applications.

Power Up Initialization

The DEI1184 incorporates an on-chip power-on reset (POR) circuit and power sequencing provisions to force the DIN inputs to a high impedance state at power up; the AFE pull-up (PMOS switch in Figure 3) and pull-down (BJT switch in Figure 3) circuits are disabled. The reset circuit monitors the VCC logic supply and forces the AFE to the high impedance state while VCC is stabilizing. It will remain in this state until the Configuration Register is programmed by the first Write Configuration Register cycle, when the pull-up or pull-down state is determined.

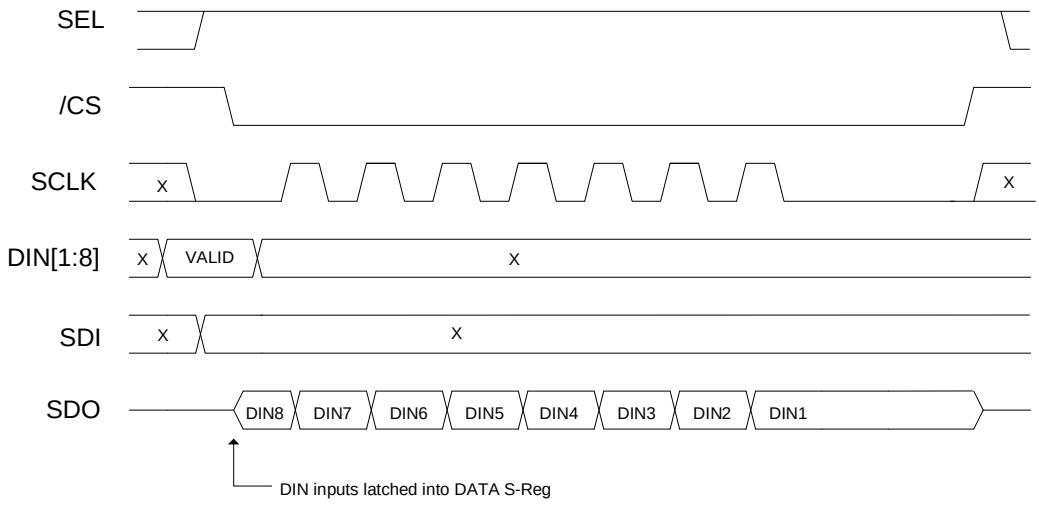


Figure 4 Read Data Register

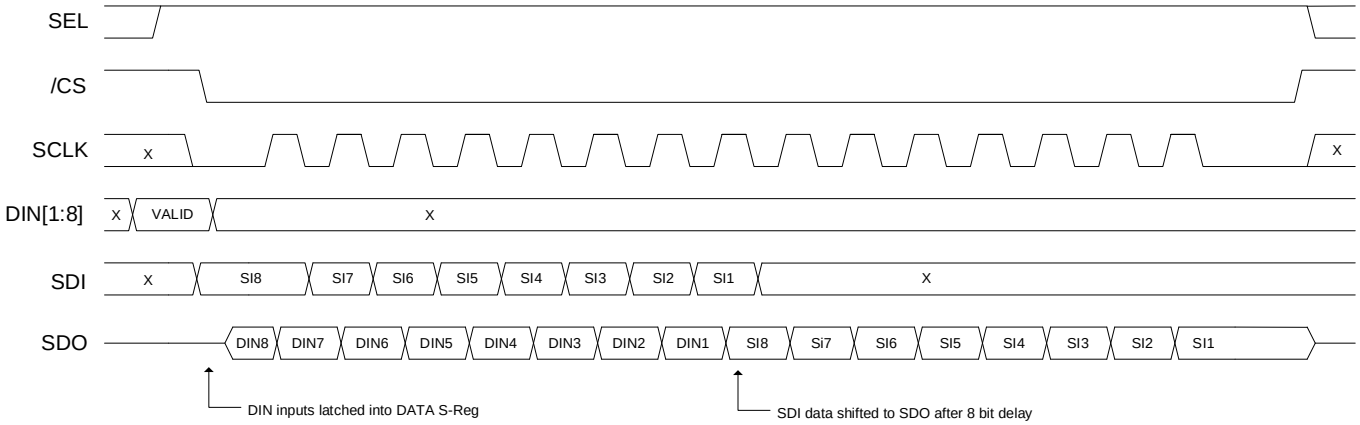


Figure 5 Read Data Register, 16 Bit Daisy Chain

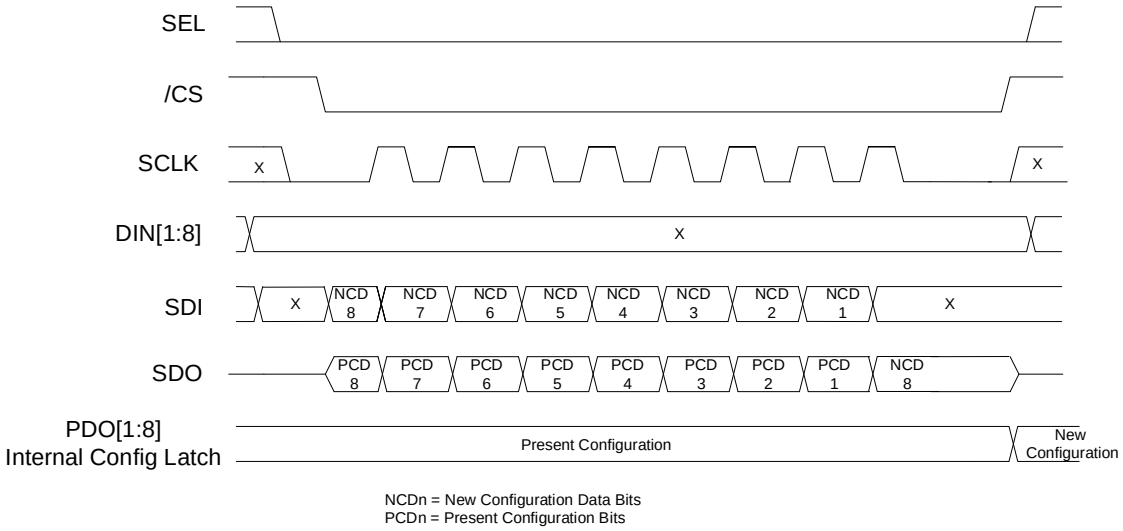


Figure 6 Write Configuration Register

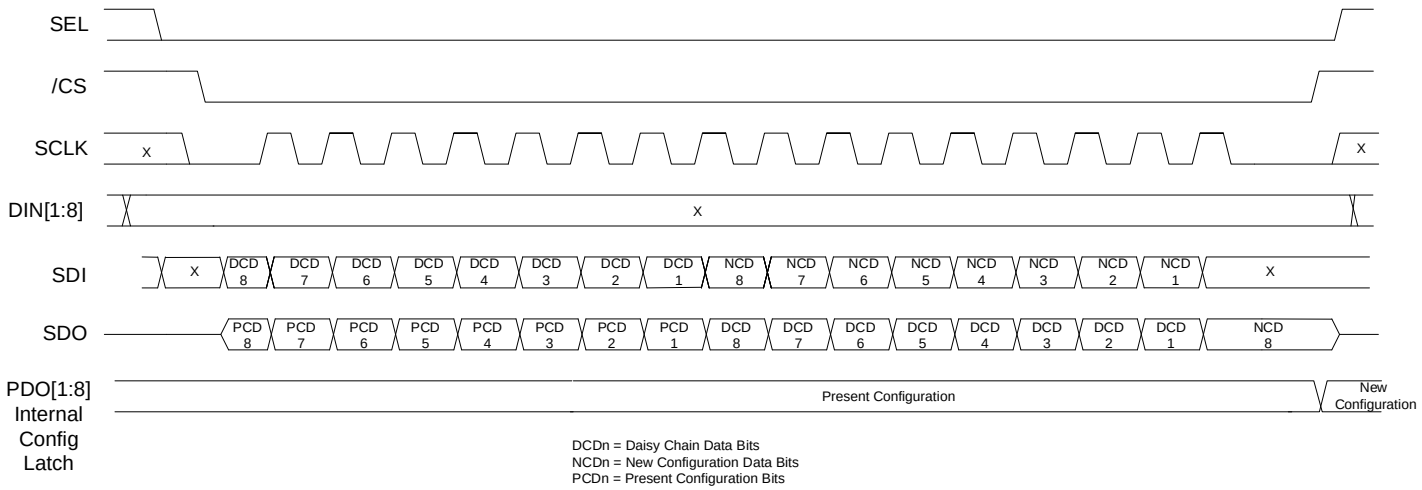


Figure 7 Write Configuration Register, 16 bit Daisy Chain

LIGHTNING PROTECTION

DINn inputs are designed to survive lightning induced transients as defined by RTCA DO160E, Section 22 Cat A3 and B3, Waveforms 3, 4, and 5A. They can withstand Level 3 stress (see waveforms below) with only the external 3 kΩ series resistor for current limiting. Protection for higher stress levels can be achieved with the addition of transient voltage suppressor (TVS) devices at the DINn pins. Select TVS clamp voltage <450 V. The 3 kΩ series resistors limit the TVS surge current.

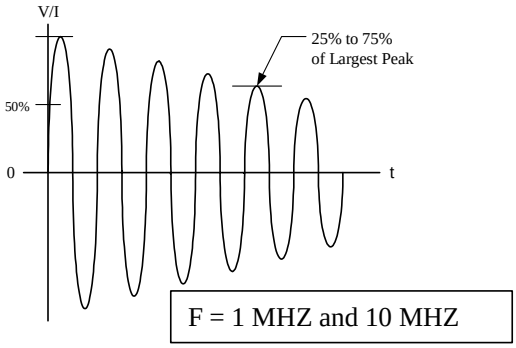


Figure 8 Voltage / Current Waveform 3

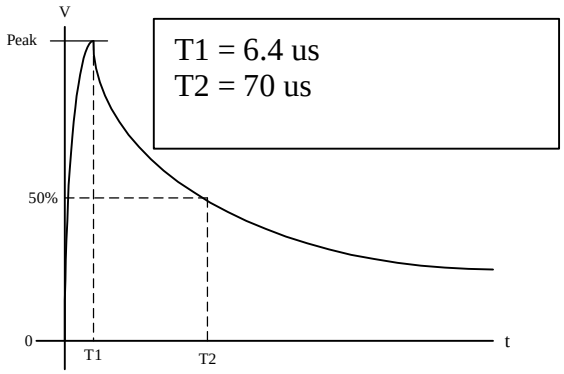


Figure 9 Voltage Waveform 4

Level 3 Waveform Source Impedance characteristics:

- Waveform 3 Voc/Isc = 600 V / 24A => 25 Ω
- Waveform 4 Voc/Isc = 300 V / 60 A => 5 Ω
- Waveform 5A Voc / Isc = 300 V / 300 A => 1 Ω
- Waveform 5A Voc / Isc = 500 V / 500 A => 1 Ω

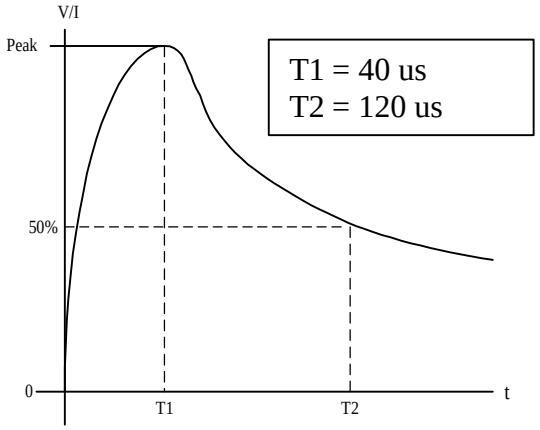


Figure 10 Current/Voltage Waveform 5A

ELECTRICAL DESCRIPTION

Table 3 Absolute Maximum Ratings

PARAMETER	MIN	MAX	UNITS
VCC Supply Voltage	-0.3	+5.0	V
VDD Supply Voltage	-0.3	18	V
Operating Temperature	-55	+125	°C
Storage Temperature	-55	+150	°C
Input Voltage (3)			
DIN[1:8] Continuous	-10	+49	V
DO160E, Waveform 3, Level 3	-600	+600	V
DO160E, Waveform 4 and 5, Level 3	-300	+300	V
DO160E, Waveform 4 and 5	-500	+500	V
DO160E, Abnormal Surge Voltage, 100 ms		80	V
Logic Inputs	-1.5	VCC + 1.5	V
DOUT	-0.5	VCC + 0.5	V
Power Dissipation @ 125 °C, steady state		0.5	W
Junction Temperature, Tjmax		145	°C
ESD per JEDEC A114-A Human Body Model			
Logic and Supply pins		2000	V
DIN pins		1000	
Peak Body Temperature (10 sec duration)		235	°C

Notes:
1. Stresses above absolute maximum ratings may cause permanent damage to the device.
2. Voltages referenced to Ground
3. Stress applied to external 3 kΩ series resistor in series with DINn pin.

Table 4 Recommended Operating Conditions

PARAMETER	SYMBOL	CONDITIONS
Supply Voltage	VCC VDD	3.3 V ±5% 15 V ±10%
Logic Inputs and Outputs		0 to VCC
Discrete Inputs	DIN[1:8]	-3 to 49 V
Operating Temperature -SMS -SES	Ta	 -55 to +125 ºC -55 to +85 ºC

Table 5 DC Electrical Characteristics

SYMBOL	PARAMETER	CONDITIONS (1)	LIMITS			UNIT
			MIN	NOM	MAX	
Logic Inputs/Outputs						
V_{IH}	HI level input voltage	VCC = 3.3 V	2.0			V
V_{IL}	LO level input voltage				0.8	V
V_{Ihst}	Input hysteresis voltage, SCLK input	(3)	50			mV
V_{OH}	HI level output voltage	IOUT = -20 uA	VCC – 0.1			V
		IOUT = -4 mA, VCC = 3 V	2.4			V
V_{OL}	LO level output voltage	IOUT = 20 uA			0.1	V
		IOUT = 4 mA, VCC = 3 V			0.4	V
I_{IN}	Input leakage, except SEL	VIN = VCC or GND	-10		10	uA
I_{IN-SEL}	Input leakage, SEL	VIN = VCC VIN = GND	-10 -50		10 10	uA
I_{OZ}	3-state leakage current	Output in Hi Impedance state. VOUT = VIHmin, VILmax	-10		10	uA
Discrete Inputs, Configured as Ground/Open (internal pull-up) (4)						
V_{IH}	HI level input voltage		10.5		49.0	V
R_{IH}	HI level Din-to-GND resistance	Resistor from Din to GND to guarantee HI input condition.	50			kΩ
I_{IH}	HI level input current	VIN = 28 V, VDD = 15 V VIN = 49 V, VDD = 15 V		0.66 0.8	1	mA mA
V_{IL}	LO level input voltage		-3.0		4.5	V
R_{IL}	LO level Din-to-GND resistance	Resistor from Din to GND to guarantee LO input condition.			500	Ω
I_{IL}	LO level input current	VIN = 0V, VDD = 15 V	-0.8	-1.3	-1.8	mA
V_{Ihst}	Input hysteresis voltage		3			V
Discrete Inputs, Configured as 28V/Open (internal pull-down) (4)						
V_{IH}	HI level input voltage		12.0		49.0	V
I_{IH}	HI level input current	VIN = 28 V, VDD = 15 V	0.8	1.3	1.8	mA
V_{IL}	LO level input voltage		-3.0		6.0	V
I_{IL}	LO level input current	VIN = 1 V, VDD = 15 V		25	50	uA
V_{Ihst}	Input hysteresis voltage		3			V
Power Supply						
ICC	Max quiescent logic supply current	VIN(logic) = VCC or GND VIN[1:8]= open		1.8	3	mA
IDD	Max quiescent analog supply current	VIN(logic) = VCC or GND VIN[1:8]= Open VIN[1:8]= GND, All configured as Ground/Open		15 22	24 33	mA

Notes:

1. Ta = -55 to +125 ºC. VDD = 15 V ±10%, VCC = 3.3 V +/-5% unless otherwise noted.
2. Current flowing into device is '+'. Current flowing out of device is '- '. Voltages are referenced to Ground.
3. Guaranteed by design. Not production tested.
4. With 3 kΩ, 2% resistor in series with DIN input pin.

Table 6 AC Electrical Characteristics (4)

SYMBOL	PARAMETER	CONDITIONS (6,7)	LIMITS		UNIT
			MIN	MAX	
f_{MAX}	SCLK frequency. (50% duty cycle) (5)		0.1	10	MHZ
t_W	SCLK pulse width. (5)		50		ns
t_{su1}	Setup time, SCLK low to /CS↓.		30		ns
t_{h1}	Hold time, /CS↓ to SCLK↑.		25		ns
t_{su2}	Setup time, DIN valid to /CS↓.		500		ns
t_{h2}	Hold time, /CS↓ to DIN not valid.		15		ns
t_{su3}	Setup time, SDIN valid to SCLK↑.		25		ns
t_{h3}	Hold time, SCLK↑ to SDIN not valid.		25		ns
t_{su4}	Setup time, SEL valid to /CS↓.		30		ns
t_{h4}	Hold time, SEL valid to /CS↑.		25		ns
t_{p1}	Propagation delay, /CS↓ to DOUT valid. (1)			105	ns
t_{p2}	Propagation delay, SCLK↑ to DOUT valid. (1)			90	ns
t_{p3}	Propagation delay, /CS↑ to DOUT HI-Z. (1) (2) (3)			80	ns
t_{p4}	Delay time between /CS active. (5)		20		ns
C_{in}	Maximum logic input pin Capacitance. (5)			10	pf
C_{out}	Maximum DOUT pin capacitance, output in HI-Z state. (5)			15	pf

Notes:
1. DOUT loaded with 50 pF to GND.
2. DOUT loaded with 1 kΩ to GND for Hi output, 1 kΩ to VCC for Low output.
3. Timing measured at 25% VCC for "0" to Hi-Z, 75% VCC for "1" to Hi-Z.
4. Sample tested on lot basis.
5. Not tested
6. Ta = -55 to +125 ºC. VCC = 3 V, VDD = 15 V, VIL = 0 V, VIH = VCC unless otherwise noted.
7. Measurements made at 50% VCC.

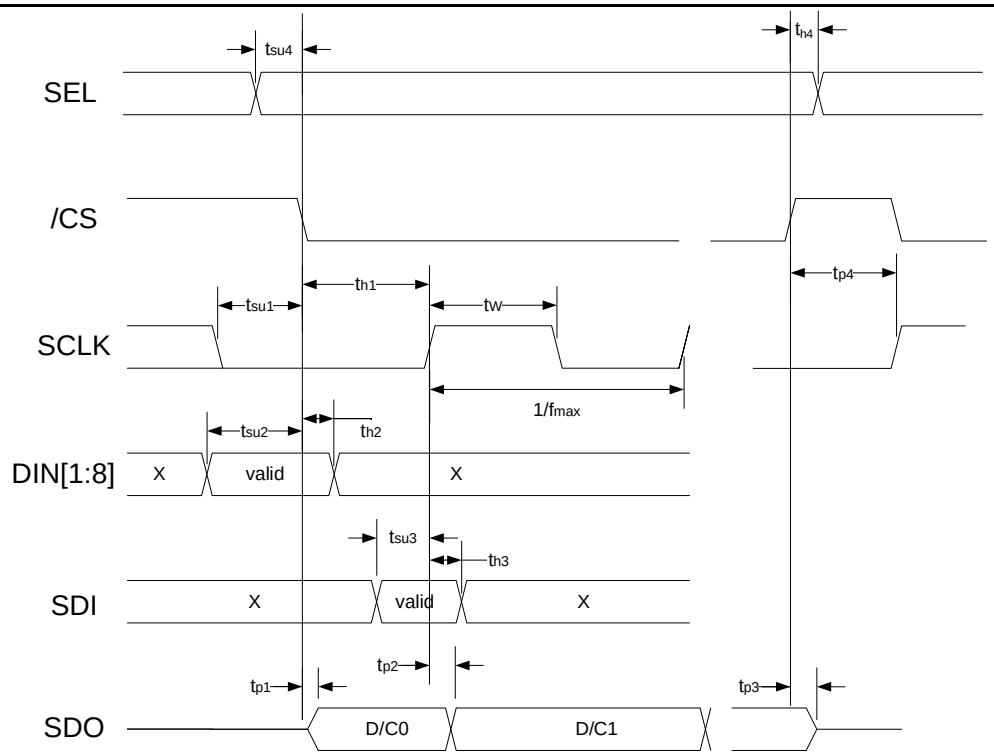


Figure 11 Switching Waveforms

APPLICATION INFORMATION

Discrete Input Filtering

The DEI1184 Analog Front End provides a moderate level of noise immunity via a combination hysteresis and limited bandwidth. The Hysteresis is 3 V minimum and the comparator bandwidth is approximately 10 MHZ.

Many applications provide additional noise immunity by means of debounce/filtering in software or in digital circuitry (i.e.: FPGA). Common input debounce techniques are readily found with a web search of the term “software debounce” and range from simple detectors of two or more sequential stable readings to FIR filters emulating RC time constants.

Input Current Characteristics

The DIN Input Current vs. Voltage characteristics for the 28V/OPEN Mode and GND/OPEN Mode are shown in Figure 12 and Figure 13.

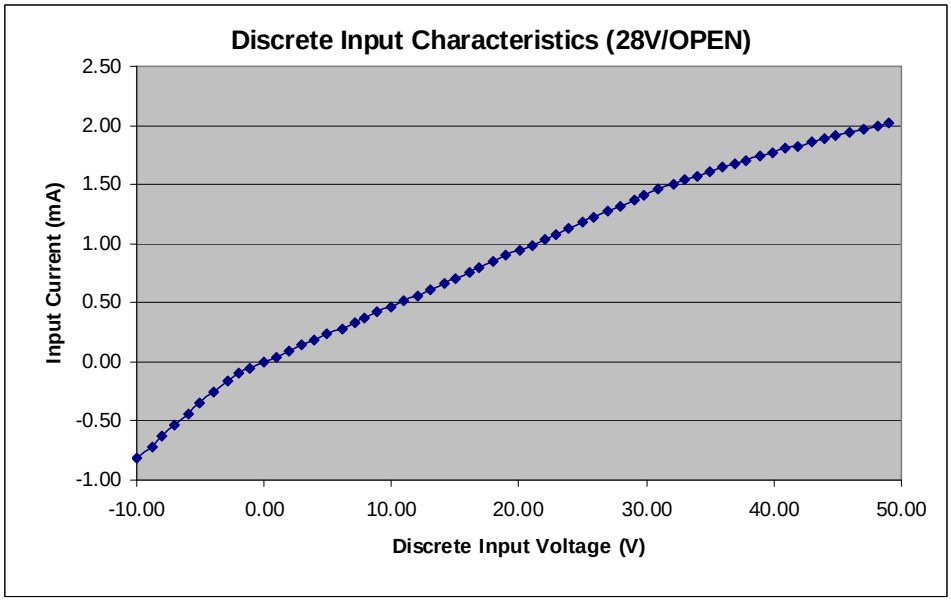


Figure 12 28V/Open Mode Input IV Characteristics (VDD=15 V)

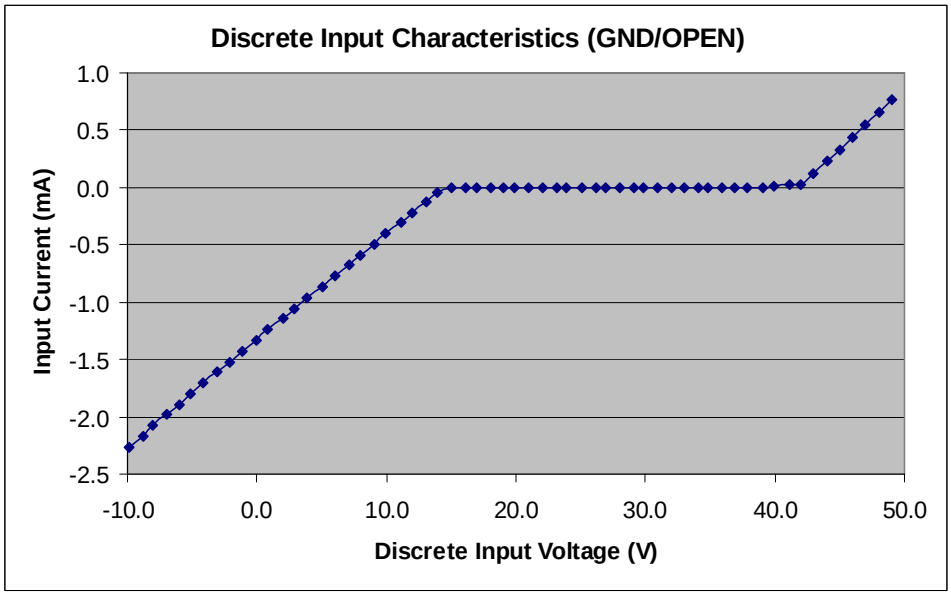


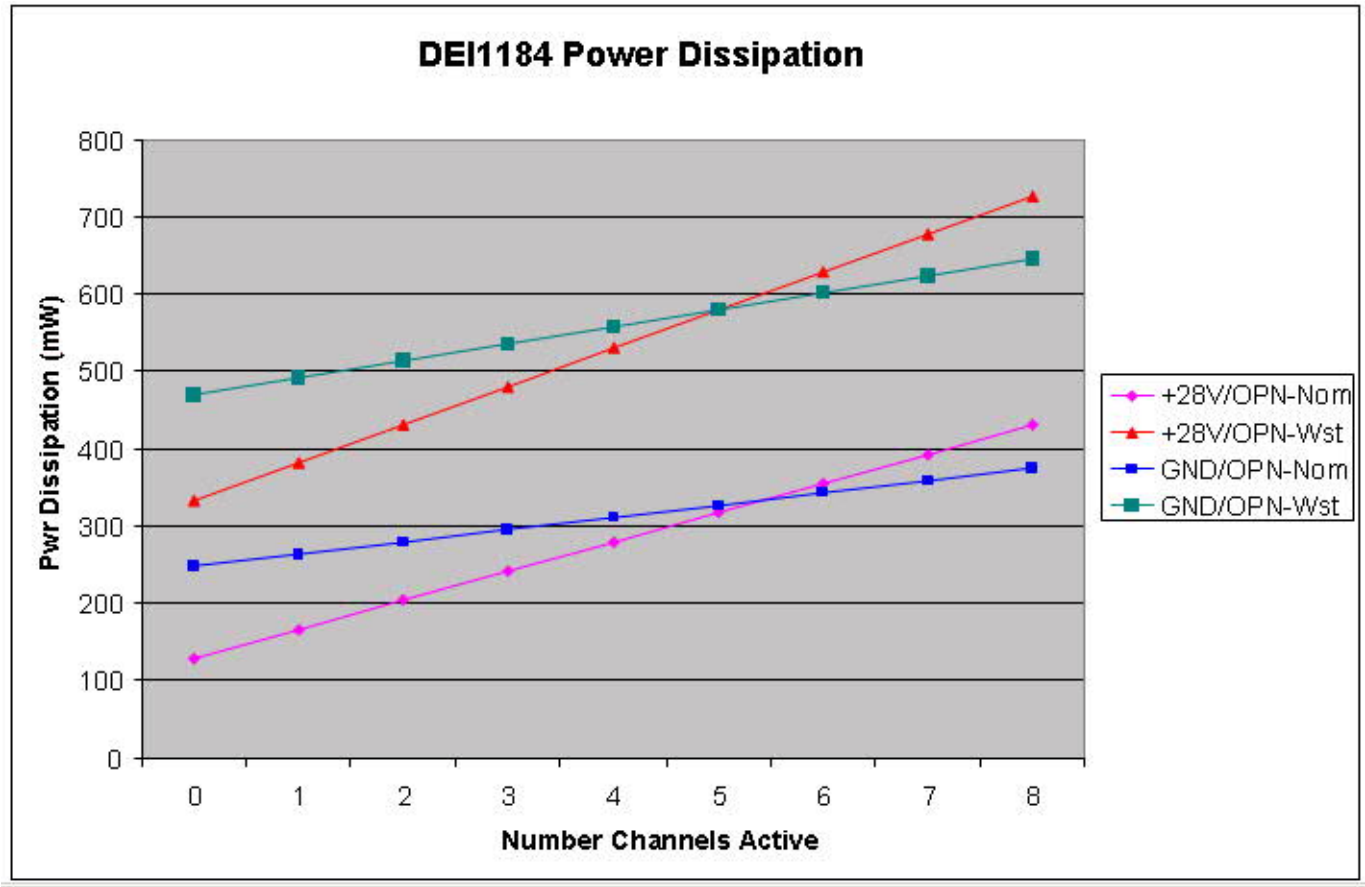
Figure 13 GND/OPEN Mode Input IV Characteristics (VDD=15 V)

Package Power Dissipation

The DEI1184 package power dissipation varies with channel configuration and operating conditions. Figure 14 shows the device package power dissipation for various conditions. This includes the contributions from Supply currents and Input currents. The four curves are as follows:

Table 7 Legend for Power Dissipation Curves

CURVE ID	SUPPLY VOLTAGE, TEMPERATURE, IC VARIATION
+28V/OPEN-Nom	3.3 V, 12 V / 27 ºC / typical IC parameters
+28V/OPEN-Wst	3.3 V, 16.5 V / 125 ºC / Worst case IC parameters
GND/OPEN-Nom	3.3 V, 12 V / 27 ºC / typical IC parameters
GND/OPEN-Wst	3.3 V, 16.5 V / 125 ºC / Worst case IC parameters



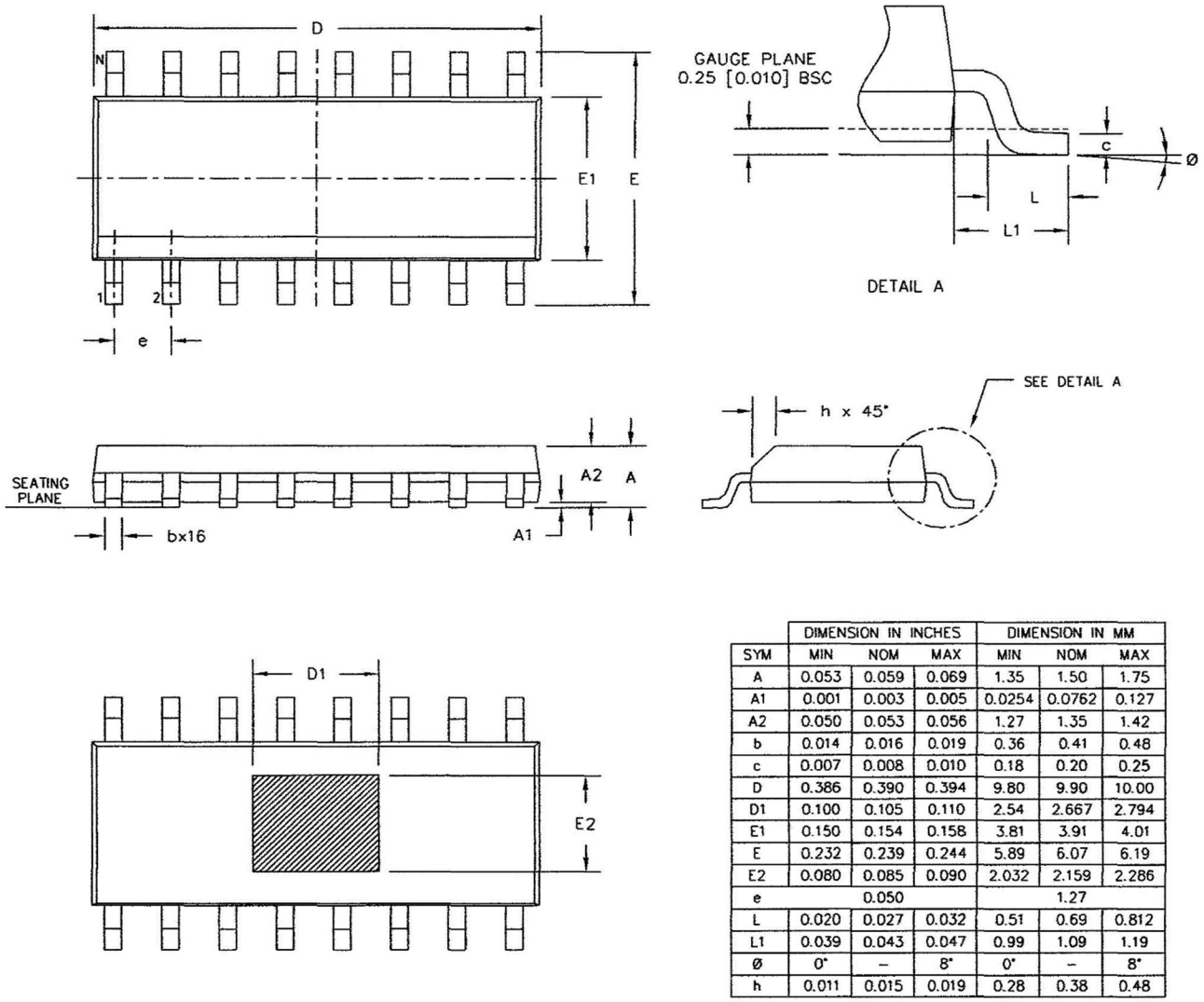
Notes: The active channels are forced to Ground for GND/OPN type and forced to 28 V for 28V/OPN type.

Figure 14 Power Dissipation for Various Conditions

PACKAGE DESCRIPTION - 16L Narrow Body EP SOIC

Moisture Sensitivity:	Level 1 / 260 ˚C per JEDEC J-STD-020
Θja:	~40 ˚C/W (Mounted on 4 layer PCB with exposed pad soldered to PCB land with thermal vias to internal GND plane)
Θjc:	~10 ˚C/W
Lead Finish:	SnPb plated
Exposed Pad:	Electrically Isolated from IC terminals.

The PCB design and layout is a significant factor in determining thermal resistance (Θja) of the IC package**.** Use maximum trace width on all power and signal connections at the IC. These traces serve as heat spreaders which improve heat flow from the IC leads**.** The exposed heat sink pad of the SOIC package should be soldered to a heat-spreader land pattern on the PCB. The IC exposed pad is electrically isolated, so the PCB land may be at any potential, typically GND, for the best heat sink. Maximize the PCB land size by extending it beyond the IC outline if possible. A grid of thermal VIAs, which drop down and connect to the buried copper plane(s), should be placed under the heat-spreader land. A typical VIA grid is 12 mil holes on a 50 mil pitch. The barrel is plated to about 1.0-ounce copper. Use as many VIAs as space allows. VIAs should be plugged to prevent voids being formed between the exposed pad and PCB heat-spreader land due to solder escaping by the capillary effect. This can be avoided by tenting the VIAs with solder mask.



	DIMENSION IN INCHES			DIMENSION IN MM		
SYM	MIN	NOM	MAX	MIN	NOM	MAX
A	0.053	0.059	0.069	1.35	1.50	1.75
A1	0.001	0.003	0.005	0.0254	0.0762	0.127
A2	0.050	0.053	0.056	1.27	1.35	1.42
b	0.014	0.016	0.019	0.36	0.41	0.48
c	0.007	0.008	0.010	0.18	0.20	0.25
D	0.386	0.390	0.394	9.80	9.90	10.00
D1	0.100	0.105	0.110	2.54	2.667	2.794
E1	0.150	0.154	0.158	3.81	3.91	4.01
E	0.232	0.239	0.244	5.89	6.07	6.19
E2	0.080	0.085	0.090	2.032	2.159	2.286
e		0.050			1.27	
L	0.020	0.027	0.032	0.51	0.69	0.812
L1	0.039	0.043	0.047	0.99	1.09	1.19
Ø	0°	–	8°	0°	–	8°
h	0.011	0.015	0.019	0.28	0.38	0.48

Figure 15 16 Lead Narrow Body EP SOIC Outline Drawing

ORDERING INFORMATION

Table 8 Ordering Information

Part Number	Marking	Package	Temperature
DEI1184-SMS	DEI1184-SMS	16 EP SOIC	-55 / +125 ºC
DEI1184-SES	DEI1184-SES	16 EP SOIC	-55 / +85 ºC